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# CD74HC390, CD54HCT390, CD74HCT390

Data sheet acquired from Harris Semiconductor
SCHS185C

September 1997 - Revised October 2003

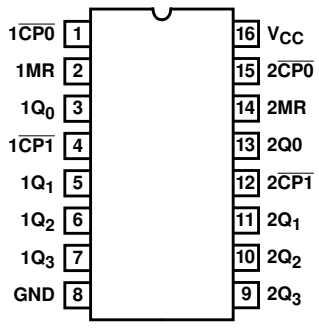
## High-Speed CMOS Logic Dual Decade Ripple Counter

### Features

- **Two BCD Decade or Bi-Quinary Counters**
- **One Package Can Be Configured to Divide-by-2, 4, 5,10, 20, 25, 50 or 100**
- **Two Master Reset Inputs to Clear Each Decade Counter Individually**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55$^{O}$C to 125$^{O}$C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, $V_{IL}$= 0.8V (Max), $V_{IH}$ = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at $V_{OL}$, $V_{OH}$**

### Pinout

**CD54HCT390**
**(CERDIP)**
**CD74HC390, CD74HCT390**
**(PDIP, SOIC)**
TOP VIEW




### Description

The CD74HC390 and 'HCT390 dual 4-bit decade ripple counters are high-speed silicon-gate CMOS devices and are pin compatible with low-power Schottky TTL (LSTTL). These devices are divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections are normally used in a BCD decade or bi-quinary configuration, since they share a common master reset (nMR). If the two master reset inputs (1MR and 2MR) are used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clock inputs (n$\overline{CP0}$ and n$\overline{CP1}$) of each section allow ripple counter or frequency division applications of divide-by-2, 4. 5, 10, 20, 25, 50 or 100. Each section is triggered by the High-to-Low transition of the input pulses (n$\overline{CP0}$ and n$\overline{CP1}$).

For BCD decade operation, the nQ0 output is connected to the n$\overline{CP1}$ input of the divide-by-5 section. For bi-quinary decade operation, the nO3 output is connected to the n$\overline{CP0}$ input and n$Q_0$ becomes the decade output.

The master reset inputs (1MR and 2MR) are active-High asynchronous inputs to each decade counter which operates on the portion of the counter identified by the "1" and "2" prefixes in the pin configuration. A High level on the nMR input overrides the clock and sets the four outputs Low.

### Ordering Information

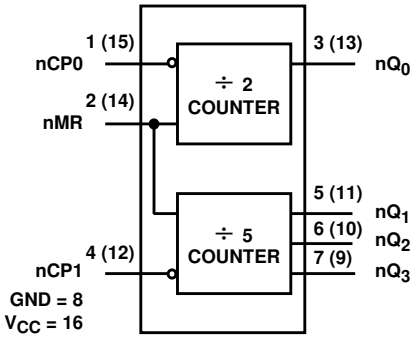
| PART NUMBER | TEMP. RANGE ($^{O}$C) | PACKAGE |
|---|---|---|
| CD54HCT390F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC390E | -55 to 125 | 16 Ld PDIP |
| CD74HC390M | -55 to 125 | 16 Ld SOIC |
| CD74HC390MT | -55 to 125 | 16 Ld SOIC |
| CD74HC390M96 | -55 to 125 | 16 Ld SOIC |
| CD74HCT390E | -55 to 125 | 16 Ld PDIP |
| CD74HCT390M | -55 to 125 | 16 Ld SOIC |
| CD74HCT390MT | -55 to 125 | 16 Ld SOIC |
| CD74HCT390M96 | -55 to 125 | 16 Ld SOIC |

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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## Functional Diagram




**TRUTH TABLE**

| INPUTS | | ACTION |
|---|---|---|
| CP | MR | |
| ↑ | L | No Change |
| ↓ | L | Count |
| X | H | All Qs Low |

H = High Voltage Level, L = Low Voltage Level, X = Don't Care,
↑ = Transition from Low to High Level, ↓ = Transition from High to Low.

**BCD COUNT SEQUENCE FOR 1/2 THE 390**

| COUNT | OUTPUTS | | | |
|---|---|---|---|---|
| | Q0 | Q1 | Q2 | Q3 |
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | H | L | H | L |
| 6 | L | H | H | L |
| 7 | H | H | H | L |
| 8 | L | L | L | H |
| 9 | H | L | L | H |

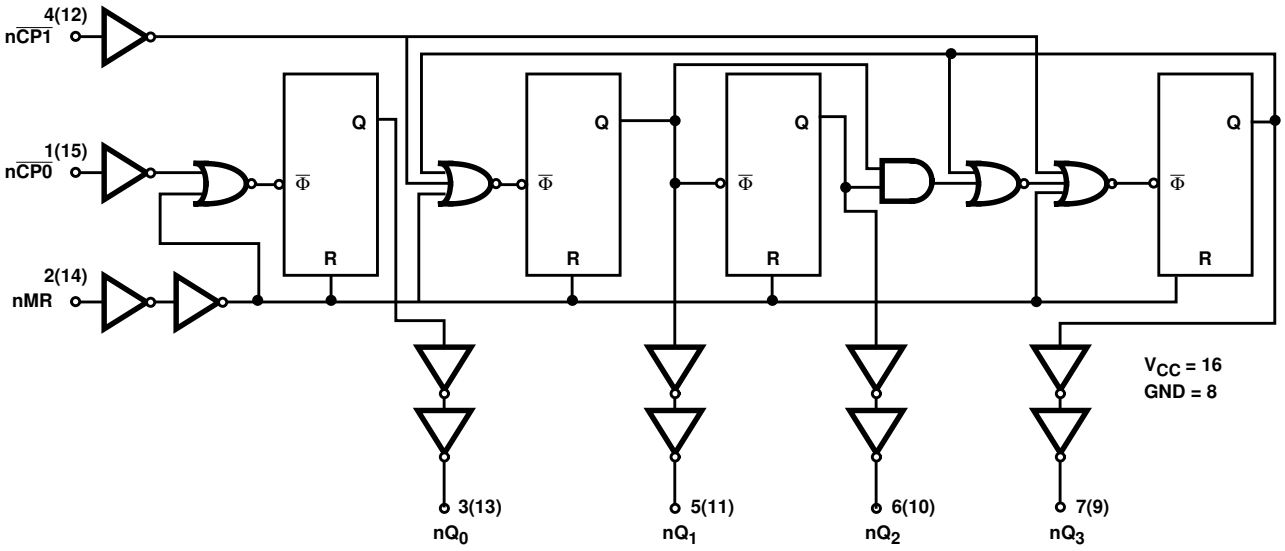
Output nQ0 connected to $n\overline{CP1}$ with counter input on $n\overline{CP0}$.

**B-QUINARY COUNT SEQUENCE FOR 1/2 THE 390**

| COUNT | OUTPUTS | | | |
|---|---|---|---|---|
| | Q0 | Q1 | Q2 | Q3 |
| 0 | L | L | L | L |
| 1 | L | H | L | L |
| 2 | L | L | H | L |
| 3 | L | H | H | L |
| 4 | L | L | L | H |
| 5 | H | L | L | L |
| 6 | H | H | H | L |
| 7 | H | L | H | L |
| 8 | H | H | H | L |
| 9 | H | L | L | H |

Output nQ3 connected to $n\overline{CP0}$ with counter input on $n\overline{CP1}$.

## *Logic Diagram*



## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . -0.5V to 7V
DC Input Diode Current, $I_{IK}$
For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, $I_O$
For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ . . . . . ±50mA

## Operating Conditions

Temperature Range ($T_A$) . . . . . -55°C to 125°C
Supply Voltage Range, $V_{CC}$
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . 0V to $V_{CC}$
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ (°C/W) |
|---|---|
| E (PDIP) Package | 67 |
| M (SOIC) Package | 73 |

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS $V_I$ (V) | TEST CONDITIONS $I_O$ (mA) | $V_{CC}$ (V) | 25°C MIN | 25°C TYP | 25°C MAX | -40°C TO 85°C MIN | -40°C TO 85°C MAX | -55°C TO 125°C MIN | -55°C TO 125°C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **HC TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | | | - | - | - | - | - | - | - | - | - | V |
| | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | - | - | - | - | - | - | - | - | - | V |
| | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | µA |

## DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HCT TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ and GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | µA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note 2) | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | µA |

NOTE:

2. For dual-supply systems theoretical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| n$\overline{CP0}$ | 0.45 |
| n$\overline{CP1}$, MR | 0.6 |

NOTE: Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

## Prerequisite for Switching Specifications

| CHARACTERISTIC | SYMBOL | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | |
| Maximum Clock Frequency | $f_{MAX}$ | 2 | 6 | - | - | 5 | - | 4 | - | MHz |
| | | 4.5 | 30 | - | - | 24 | - | 20 | - | MHz |
| | | 6 | 35 | - | - | 28 | - | 24 | - | MHz |
| Clock Pulse Width, n$\overline{CP0}$, n$\overline{CP1}$ | $t_W$ | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | - | 17 | - | 20 | - | ns |

## Prerequisite for Switching Specifications (Continued)

| CHARACTERISTIC | SYMBOL | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Reset Removal Time | $t_{REM}$ | 2 | 70 | - | - | 90 | - | 105 | - | ns |
| | | 4.5 | 14 | - | - | 18 | - | 21 | - | ns |
| | | 6 | 12 | - | - | 15 | - | 18 | - | ns |
| Reset Pulse Width | $t_W$ | 2 | 50 | - | - | 65 | - | 75 | - | ns |
| | | 4.5 | 10 | - | - | 13 | - | 15 | - | ns |
| | | 6 | 9 | - | - | 11 | - | 13 | - | ns |
| **HCT TYPES** | | | | | | | | | | |
| Maximum Clock Frequency | $f_{MAX}$ | 4.5 | 27 | - | - | 22 | - | 18 | - | MHz |
| Clock Pulse Width, $n\overline{CP0}$, $n\overline{CP1}$ | $t_W$ | 4.5 | 19 | - | - | 24 | - | 29 | - | ns |
| Reset Removal Time | $t_{REM}$ | 4.5 | 15 | - | - | 19 | - | 22 | - | ns |
| Reset Pulse Width | $t_W$ | 4.5 | 13 | - | - | 16 | - | 20 | - | ns |

## Switching Specifications Input $t_r$, $t_f$ = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | |
| Propagation Delay (Figure 1) $n\overline{CP0}$ to $nQ_0$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 175 | - | 220 | - | 265 | ns |
| | | | 4.5 | - | - | 35 | - | 44 | - | 53 | ns |
| | | $C_L$ =15pF | 5 | - | 14 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 30 | - | 37 | - | 45 | ns |
| $n\overline{CP1}$ to $nQ_1$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 185 | - | 230 | - | 280 | ns |
| | | | 4.5 | - | - | 37 | - | 46 | - | 56 | ns |
| | | | 6 | - | - | 31 | - | 39 | - | 48 | ns |
| $n\overline{CP1}$ to $nQ_2$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 245 | - | 305 | - | 370 | ns |
| | | | 4.5 | - | - | 49 | - | 61 | - | 74 | ns |
| | | | 6 | - | - | 42 | - | 52 | - | 63 | ns |
| $n\overline{CP1}$ to $nQ_3$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 180 | - | 225 | - | 270 | ns |
| | | | 4.5 | - | - | 36 | - | 45 | - | 54 | ns |
| | | | 5 | - | 15 | - | - | - | - | - | ns |
| | | | 6 | - | - | 31 | - | 38 | - | 46 | ns |
| $n\overline{CP0}$ to nQ3 ($nQ_0$ connected to $n\overline{CP1}$) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 365 | - | 455 | - | 550 | ns |
| | | | 4.5 | - | - | 73 | - | 91 | - | 110 | ns |
| | | | 6 | - | - | 62 | - | 77 | - | 94 | ns |
| MR to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 190 | - | 240 | - | 285 | ns |
| | | | 4.5 | - | - | 38 | - | 48 | - | 57 | ns |
| | | $C_L$ =15pF | 5 | - | 16 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 32 | - | 41 | - | 48 | ns |

**Switching Specifications** Input $t_r$, $t_f$ = 6ns **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Output Transition Time (Figure 1) | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Input Capacitance | $C_{IN}$ | $C_L$ = 50pF | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$ | $C_L$ =15pF | 5 | - | 28 | - | - | - | - | - | pF |
| **HCT TYPES** | | | | | | | | | | | |
| Propagation Delay (Figure 1) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 40 | - | 50 | - | 60 | ns |
| $n\overline{CP0}$ to $nQ_0$ | | $C_L$ =15pF | 5 | - | 17 | - | - | - | - | - | ns |
| $n\overline{CP1}$ to $nQ_1$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 43 | - | 51 | - | 65 | ns |
| $n\overline{CP}1$ to $nQ_2$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 55 | - | 69 | - | 83 | ns |
| $n\overline{CP1}$ to $nQ_3$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 42 | - | 53 | - | 63 | ns |
| | | $C_L$ =15pF | 5 | - | 18 | - | - | - | - | - | ns |
| $n\overline{CP0}$ to nQ2 ($nQ_0$ connected to $n\overline{CP1}$) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 84 | - | 105 | - | 126 | ns |
| MR to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 42 | - | 53 | - | 63 | ns |
| | | $C_L$ =15pF | 5 | - | 18 | - | - | - | - | - | ns |
| Output Transition | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| Input Capacitance | $C_{IN}$ | $C_L$ =15pF | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$ | $C_L$ =15pF | 5 | - | 32 | - | - | - | - | - | pF |

NOTES:

3. $C_{PD}$ is used to determine the dynamic power consumption, per multiplexer.
4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where $f_i$ = Input Frequency, $C_L$ = Output Load Capacitance, $V_{CC}$ = Supply Voltage.

## Test Circuits and Waveforms

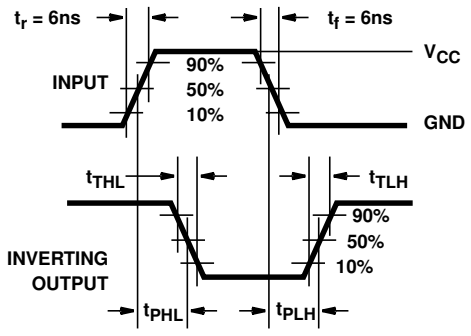



**FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

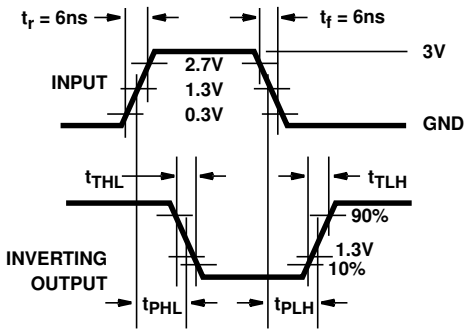



**FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9098401MEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9098401ME A CD54HCT390F3A | Samples |
| CD54HCT390F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9098401ME A CD54HCT390F3A | Samples |
| CD74HC390E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC390E | Samples |
| CD74HC390EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC390E | Samples |
| CD74HC390M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC390M | Samples |
| CD74HC390M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC390M | Samples |
| CD74HC390M96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC390M | Samples |
| CD74HC390M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC390M | Samples |
| CD74HC390MT | ACTIVE | SOIC | D | 16 | | TBD | Call TI | Call TI | -55 to 125 | HC390M | Samples |
| CD74HCT390E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT390E | Samples |
| CD74HCT390EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT390E | Samples |
| CD74HCT390M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT390M | Samples |
| CD74HCT390M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT390M | Samples |
| CD74HCT390M96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT390M | Samples |
| CD74HCT390MG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT390M | Samples |
| CD74HCT390MT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT390M | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54HCT390, CD74HCT390 :**

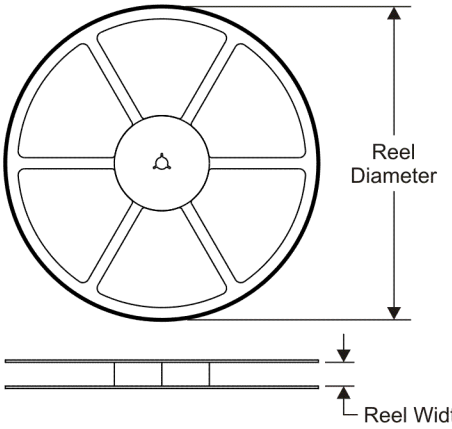
- Catalog: CD74HCT390
- Military: CD54HCT390

NOTE: Qualified Version Definitions:

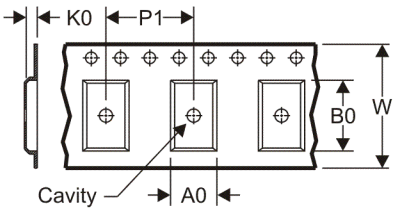
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

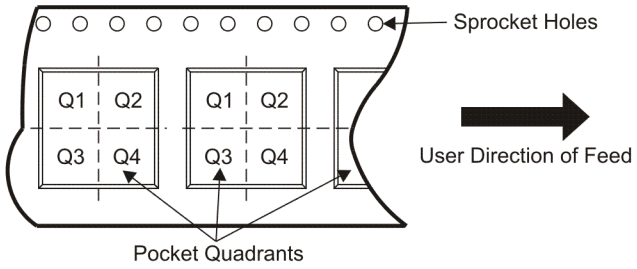



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

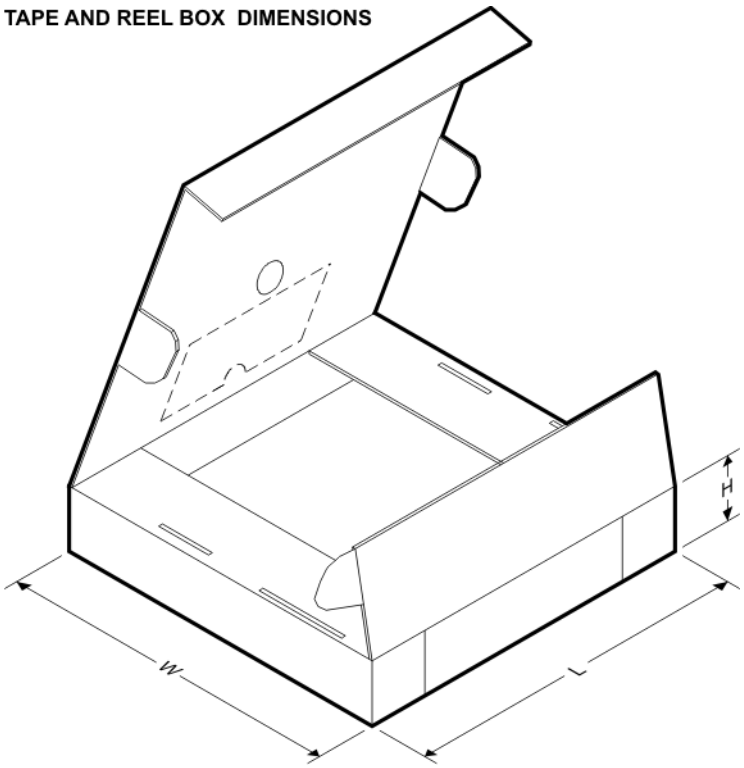
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HC390M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT390M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



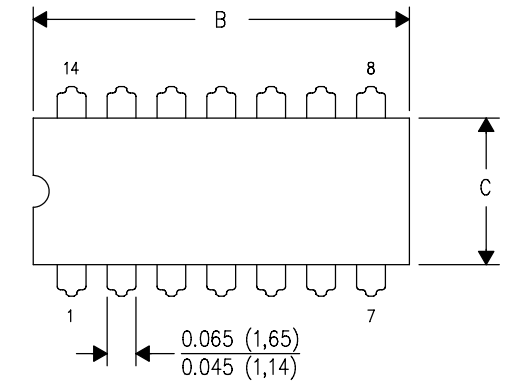

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HC390M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74HCT390M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

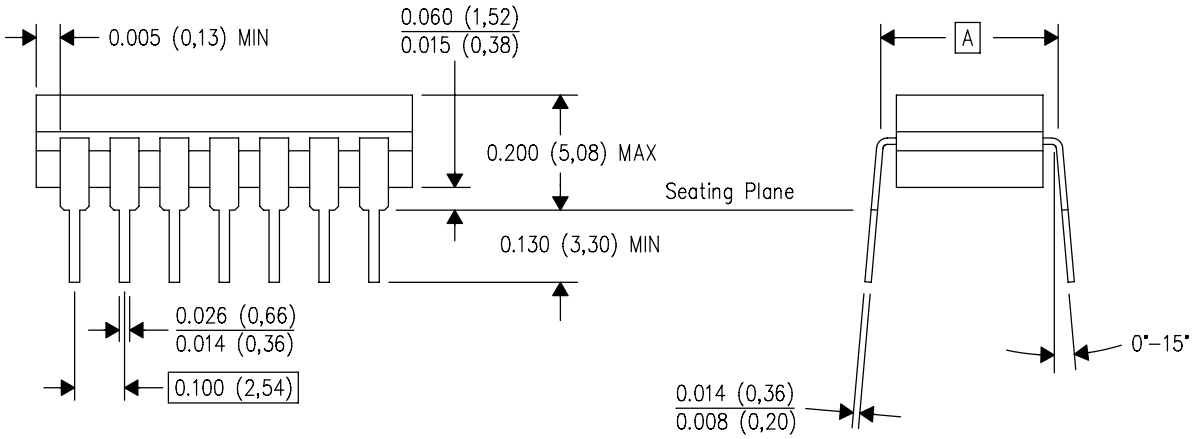
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



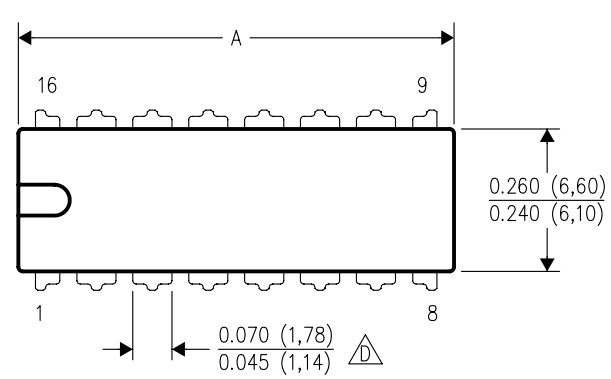

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

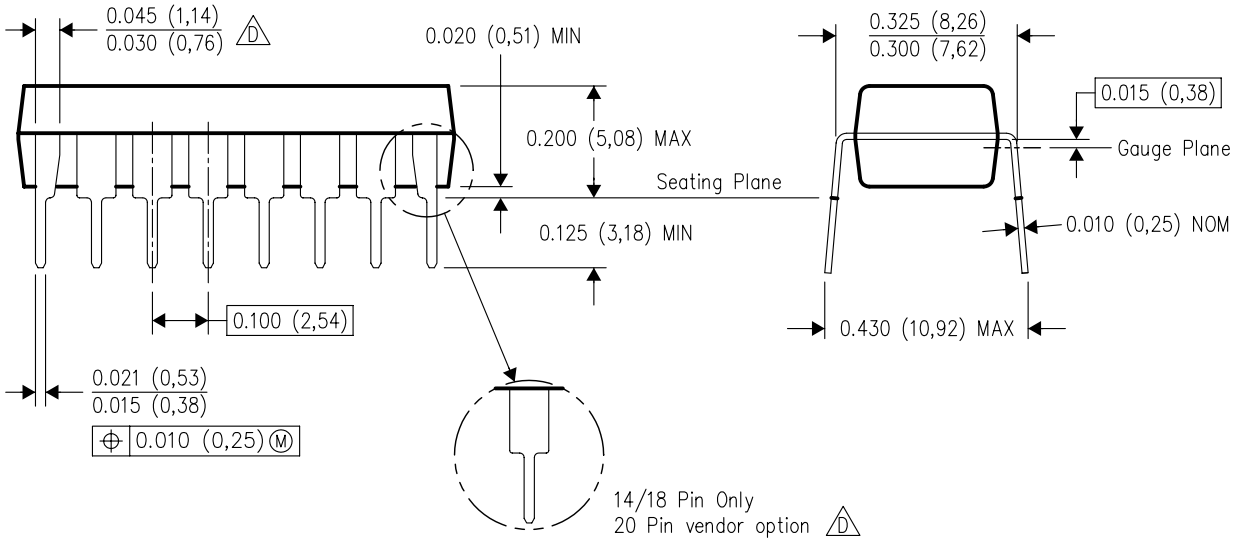
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



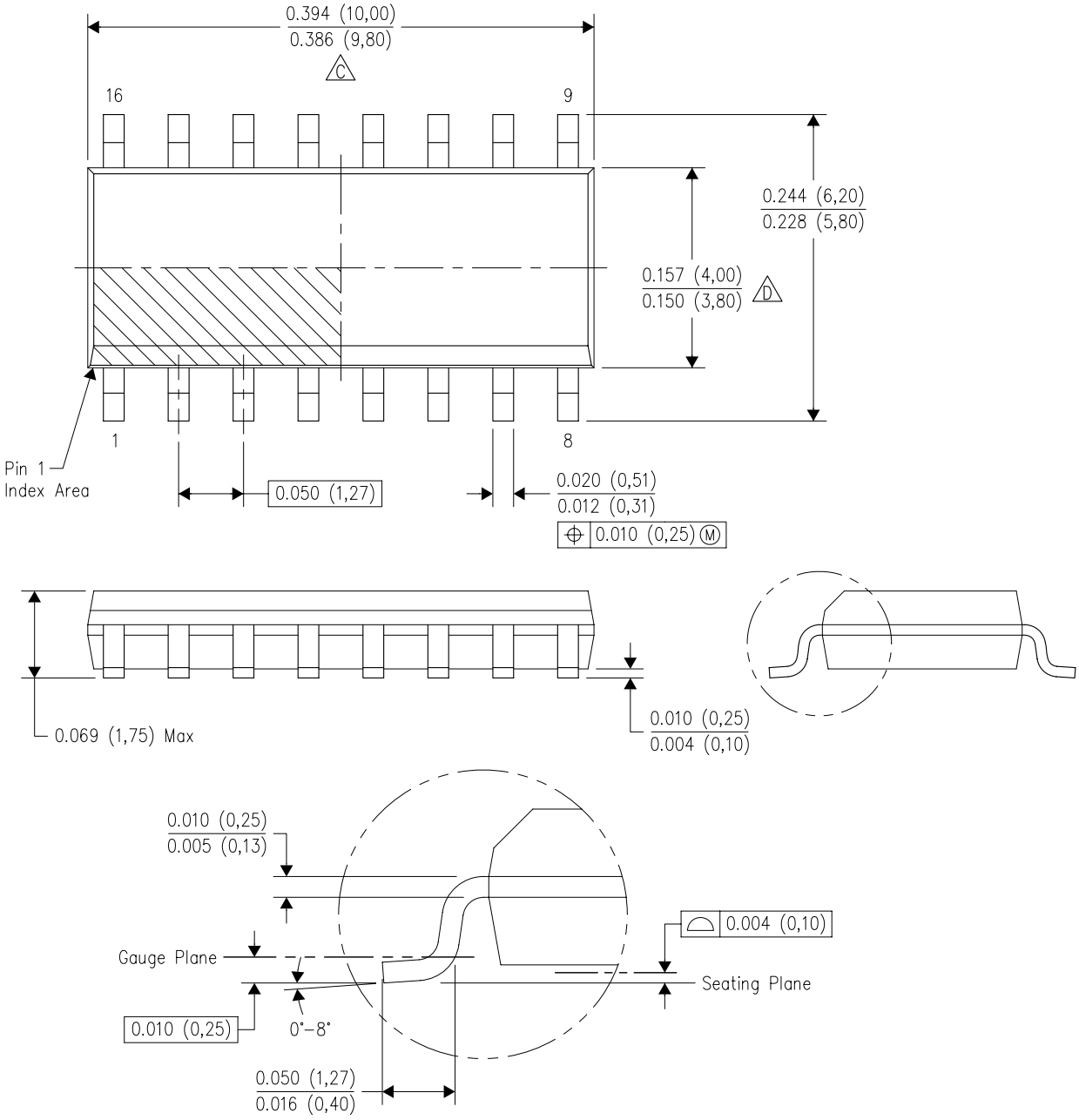

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

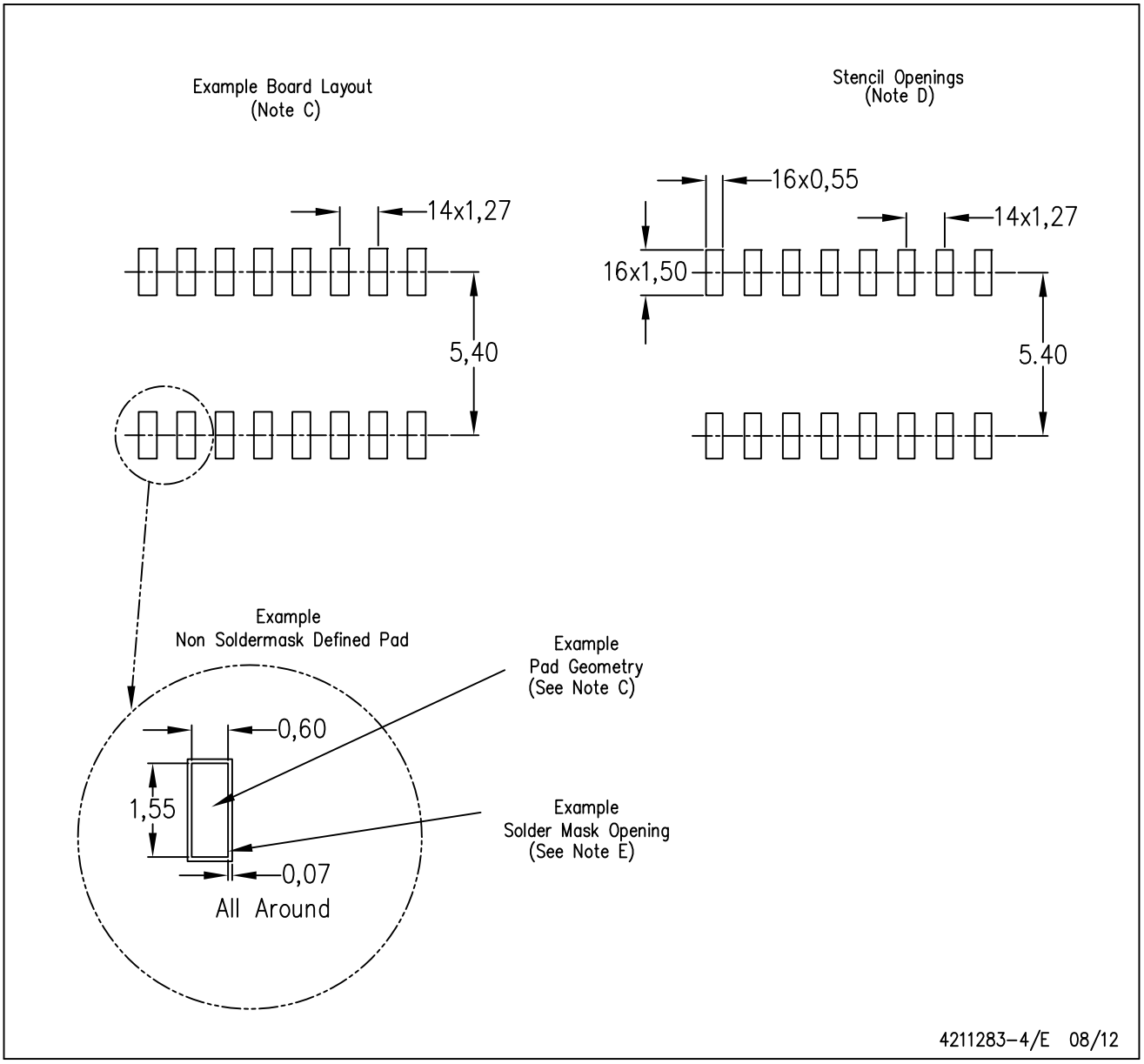
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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