



EN: This Datasheet is presented by the manufacturer.

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RC4136, RM4136, RV4136 QUAD GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

The RM4136 and RV4136 are obsolete and are no longer supplied.

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- Continuous Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-Up
- Unity-Gain Bandwidth . . . 3 MHz Typ
- Gain and Phase Match Between Amplifiers
- Designed To Be Interchangeable With Raytheon RC4136, RM4136, and RV4136
- Low Noise . . . $8 \text{ nV}/\sqrt{\text{Hz}}$ Typ at 1 kHz

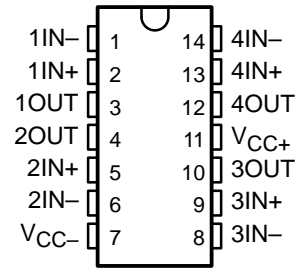
description

The RC4136, RM4136, and RV4136 are quad general-purpose operational amplifiers, with each amplifier electrically similar to the $\mu\text{A}741$, except that offset null capability is not provided.

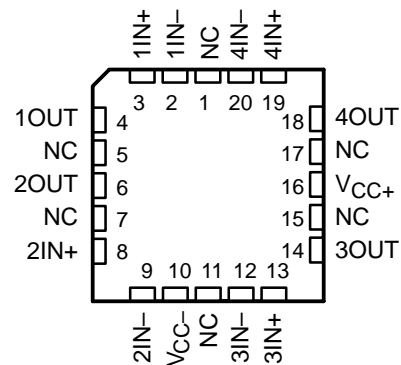
The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The RC4136 is characterized for operation from 0°C to 70°C , the RM4136 is characterized for operation over the full military temperature range of -55°C to 125°C , and the RV4136 is characterized for operation from -40°C to 85°C .

RM4136 . . . J OR W PACKAGE
ALL OTHERS . . . D OR N PACKAGE
(TOP VIEW)

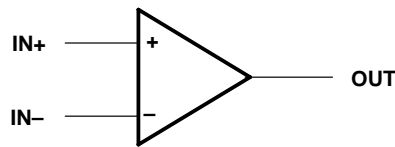


RM4136 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

symbol (each amplifier)



AVAILABLE OPTIONS

T_A	$V_{IO\text{MAX}}$ AT 25°C	PACKAGE				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	FLAT (W)
0°C to 70°C	6 mV	RC4136D	—	—	RC4136N	—
-40°C to 85°C	6 mV	RV4136D	—	—	RV4136N	—
-55°C to 125°C	4 mV	—	RM4136FK	RM4136J	—	RM4136W

The D packages are available taped and reeled. Add the suffix R to the device type (e.g., RC4136DR).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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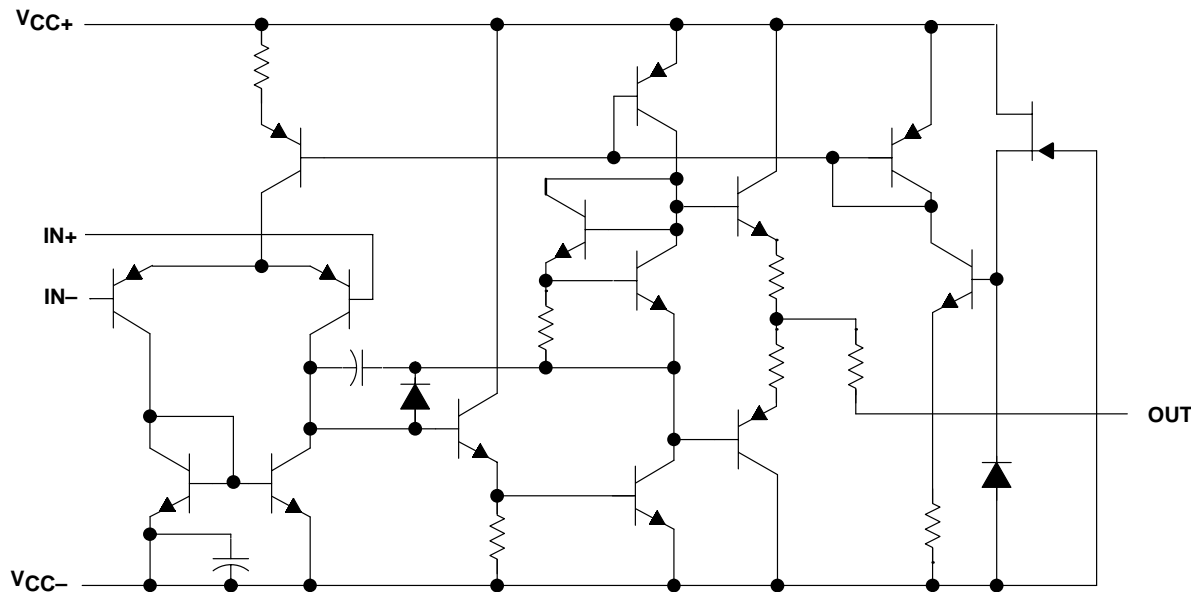
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

RC4136, RM4136, RV4136
QUAD GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

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schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): V_{CC+} , RC4136 and RV4136	18 V
V_{CC+} , RM4136	22 V
V_{CC-} , RC4136 and RV4136	-18 V
V_{CC-} , RM4136	-22 V
Differential input voltage, V_{ID} (see Note 2)	± 30 V
Input voltage, V_I (any input) (see Notes 1 and 3)	± 15 V
Duration of output short circuit to ground, one amplifier at a time (see Note 4)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Package thermal impedance, θ_{JA} (see Note 5): D package	86°C/W
N package	80°C/W
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Differential voltages are at IN+ with respect to IN-.
 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
 4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK	800 mW	11.0 mW/°C	77°C	800 mW	715 mW	275 mW
J	800 mW	11.0 mW/°C	77°C	800 mW	715 mW	275 mW
W	800 mW	8.0 mW/°C	50°C	640 mW	520 mW	200 mW



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recommended operating conditions

		MIN	MAX	UNIT
V_{CC+}	Supply voltage	5	15	V
V_{CC-}	Supply voltage	-5	-15	V

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER	TEST CONDITIONS†		RC4136			RM4136			RV4136			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL} Input offset voltage	$V_O = 0$	25°C		0.5	6		0.5	4		0.5	6	mV
		Full range			7.5			6			7.5	
I_{IO} Input offset current	$V_O = 0$	25°C		5	200		5	150		5	200	nA
		Full range			300			500			500	
I_{IB} Input bias current	$V_O = 0$	25°C		140	500		140	400		140	500	nA
		Full range			800			1500			1500	
V_i Input voltage range		25°C	±12	±14		±12	±14		±12	±14		V
V_{OM} Maximum peak output voltage swing	$R_L = 10$ kΩ	25°C	±12	±14		±12	±14		±12	±14		V
	$R_L = 2$ kΩ	25°C	±10	±13		±10	±13		±10	±13		
	$R_L \geq 2$ kΩ	Full range	±10			±10			±10			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2$ kΩ	25°C	20	300		50	350		20	300		V/mV
		Full range	15			25			15			
B_1 Unity-gain bandwidth		25°C		3			3.5			3		MHz
r_i Input resistance		25°C	0.3*	5		0.3*	5		0.3*	5		MΩ
CMRR Common-mode rejection ratio	$V_O = 0$, $R_S = 50$ Ω	25°C	70	90		70	90		70	90		dB
k_{SVS} Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ± 15 V, $V_O = 0$	25°C		30	150		30	150		30	150	μV/V
V_n Equivalent input noise voltage (closed loop)	$A_{VD} = 100$, BW = 1 Hz, f = 1 kHz, $R_S = 100$ Ω	25°C		8			8			8		nV/√Hz
I_{CC} Supply current (all four amplifiers)	$V_O = 0$, No load	25°C		5	11.3		5	11.3		5	11.3	mA
		MIN T_A		6	13.7		6	13.3		6	13.7	
		MAX T_A		4.5	10		4.5	10		4.5	10	
P_D Total power dissipation (all four amplifiers)	$V_O = 0$, No load	25°C		150	340		150	340		150	340	mW
		MIN T_A		180	400		180	400		180	400	
		MAX T_A		135	300		135	300		135	300	
Crosstalk attenuation (V_{O1}/V_{O2})	$A_{VD} = 100$, f = 10 kHz, $R_S = 1$ kΩ	25°C		105			105			105		dB

* This parameter is not production tested.

† All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range is 0°C to 70°C for RC4136, -55°C to 125°C for RM4136, and -40°C to 85°C for RV4136. Minimum T_A is 0°C for RC4136, -55°C for RM4136, and -40°C for RV4136. Maximum T_A is 70°C for RC4136, 125°C for RM4136, and 85°C for RV4136.



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operating characteristics, $V_{CC+} = 15\text{ V}$, $V_{CC-} = -15\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
t_r	Rise time	$V_I = 20\text{ mV}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$	0.13	μs
	Overshoot factor	$V_I = 20\text{ mV}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$	5	%
SR	Slew rate at unity gain	$V_I = 10\text{ V}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$	1.7	$\text{V}/\mu\text{s}$



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
RC4136D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70		
RC4136DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70		
RC4136N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	RC4136N	Samples
RC4136NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	RC4136N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

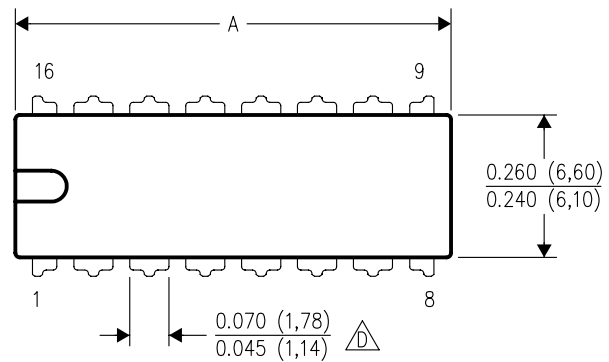
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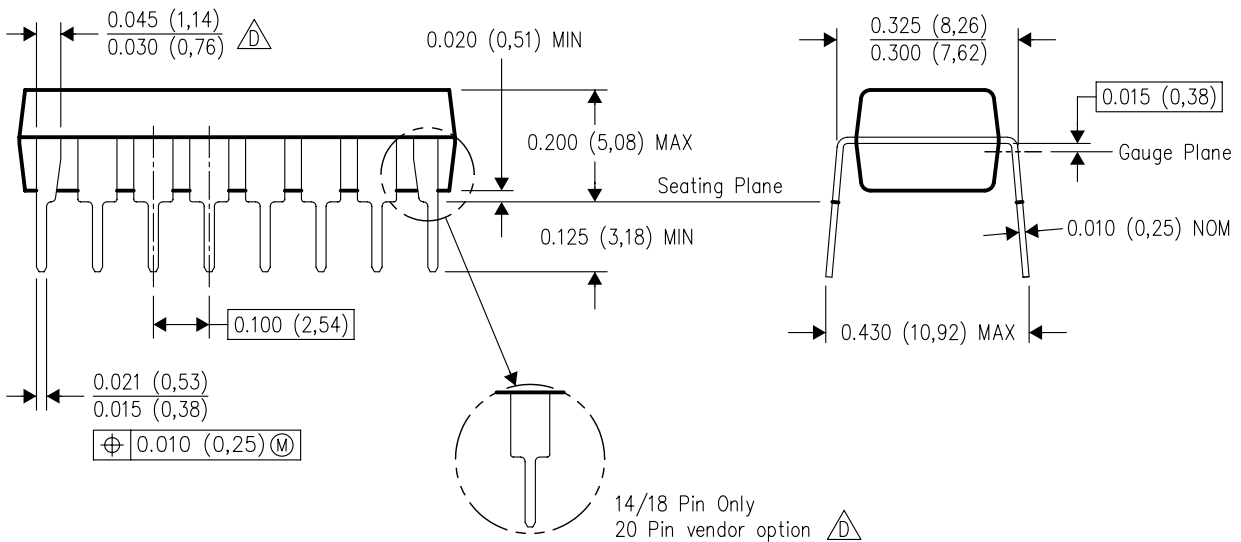
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



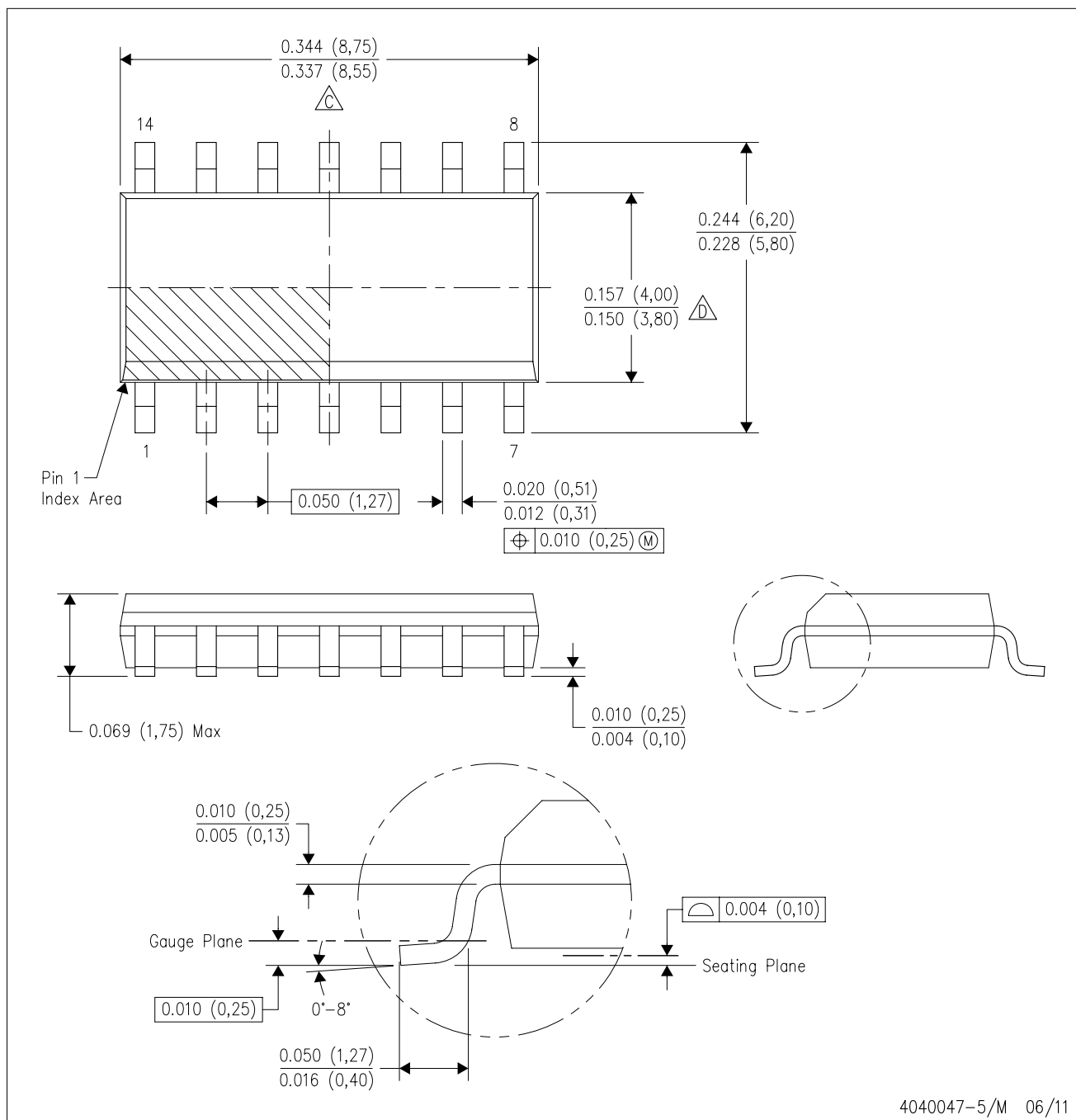
14/18 Pin Only
20 Pin vendor option

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- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

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