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Application example for RFM69CW replacing RFM12B

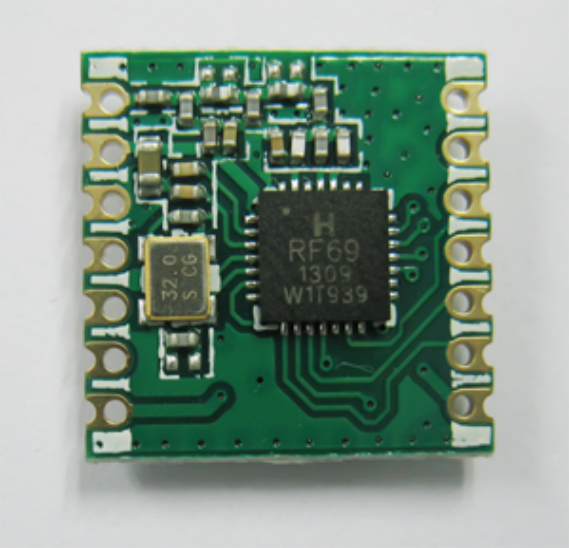
1. Introduction：

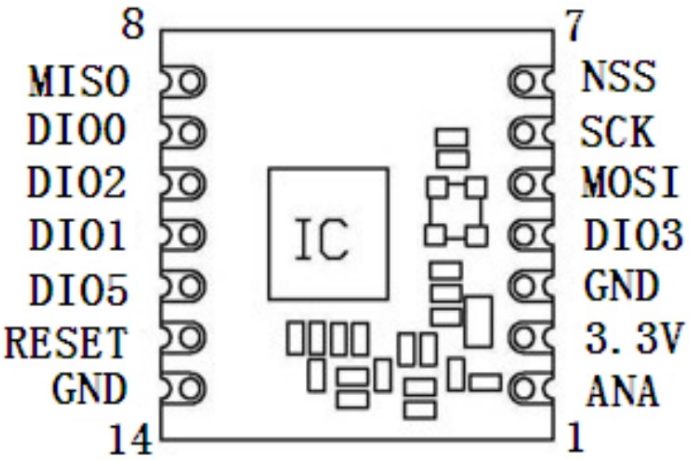
RFM69CW is a transceiver module based on our new generation RF IC, which is fully hardware compatible with RFM12B. This document detailed compare hardware and comprehensive application between RFM69CW and RFM12B, which will make it easier for customers to use RFM69CW instead in project based on RFM12B design.

2. module hardware compatible:

PCB size and pins position of RFM69CW and RFM12B are same. Customers can replace RFM12B with RFM69CW by changing the drive application software accordingly, no hardware change is needed.

Below is the physically and pin diagram of RFM69CW





RFM69CW Pinouts

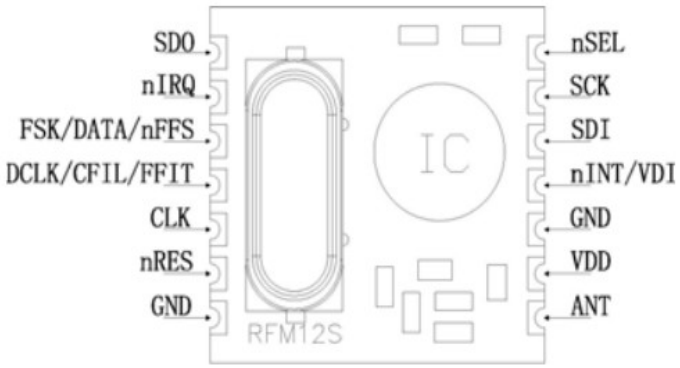
Number	Name	Type	Description
1	ANA	O	Transmitter RF Output
2	3.3V	I	Supply voltage
4	DIO3	I/O	Digital I/O, software configured
5	MOSI	I	SPI Data input
6	SCK	I	SPI Clock input
7	NSS	I	SPI Chip select input
8	MISO	O	SPI Data output
9	DIO0	I/O	Digital I/O, software configured

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10	DIO2	I/O	Digital I/O, software configured
11	DIO1	I/O	Digital I/O, software configured
12	DIO5	I/O	Digital I/O, software configured
13	NRESET	I/O	Reset trigger input

Below is the physically and pin diagrams of RFM12B



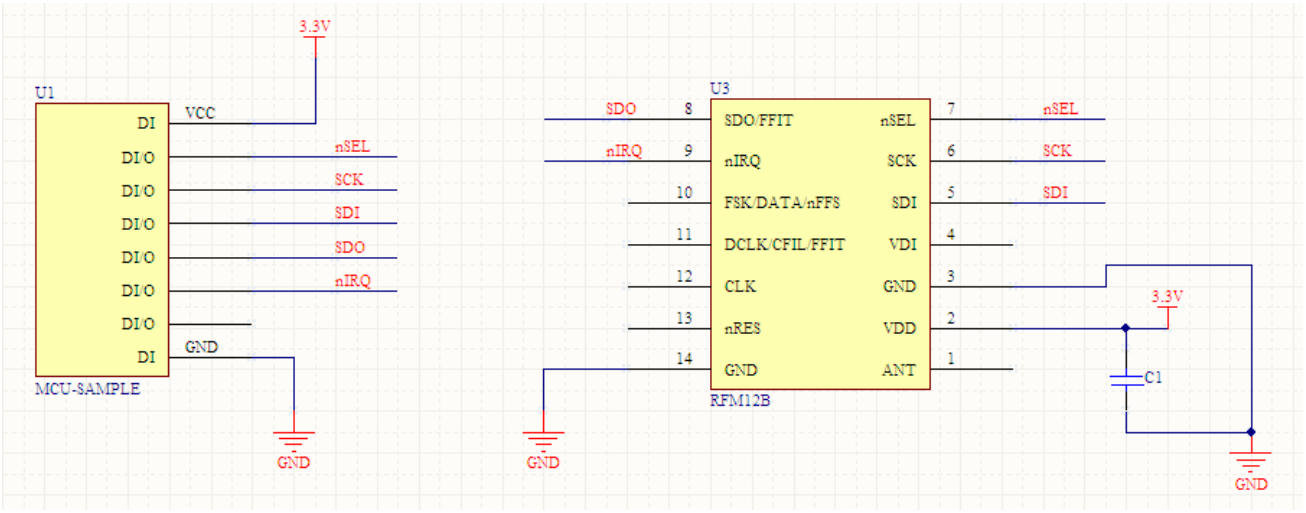


RFM12B Pinouts

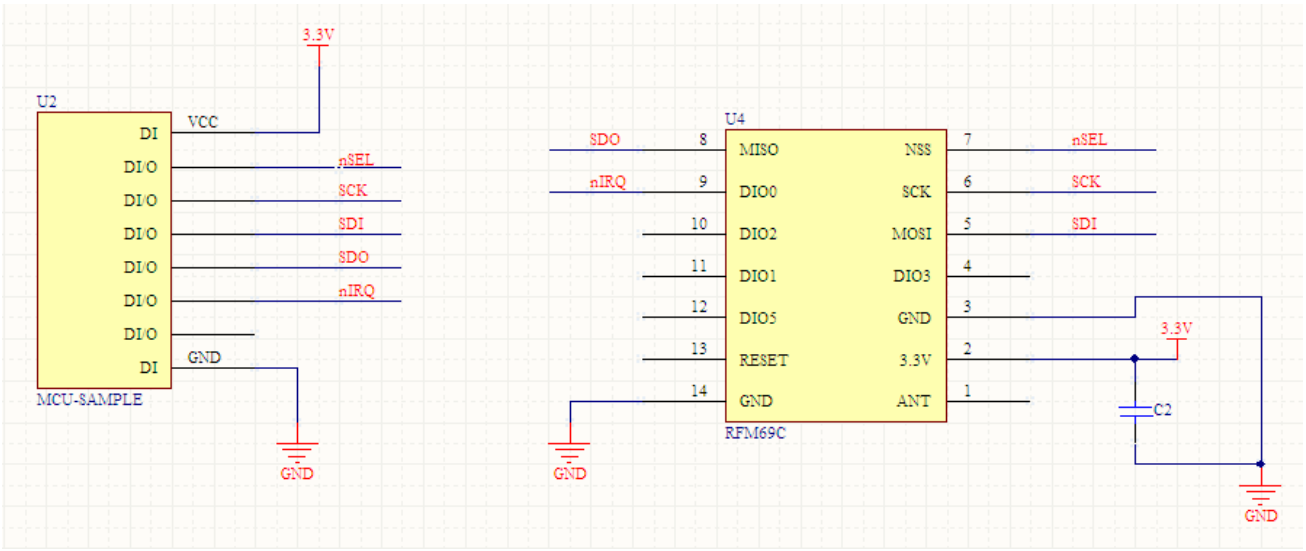
Nimber	Name	TYPE	Description
1	ANT	O	Transmitter RF Output
2	VDD	I	Positive power supply
4	nINT	I/O	Interrupt input (active low)/Valid data indicator
5	SDI	I	SPI data input
6	SCK	I	SPI clock input
7	nSEL	I	Chip select (active low)
8	SDO	O	SPI data output
9	nIRQ	O	Interrupts request output（active low）
10	FSK/DATA/nFFS	I/O/I	Transmit FSK data input/ Received data output (FIFO not used)/ FIFO select
11	DCLK/CFIL/FFIT	O/(AI/O)	Clock output (no FIFO)/ external filter capacitor (analog mode) / FIFO interrupts(active high) when FIFO level set to 1, FIFO empty interruption can be achieved
12	CLK	O	clock out for MCU (1 MHz-10 MHz)
13	nRES	I/O	Reset output（active low）

Customers can directly use RFM69CW as replacement in the project designed with RFM12B. No hardware changes needed. Hardware connection diagram of RFM69CW and RFM12B is as follows:

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RFM12B hardware connection diagram



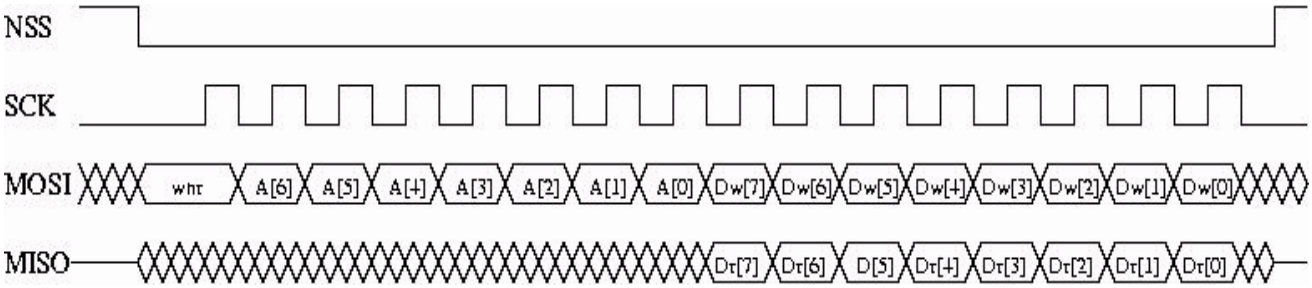
RFM69CW hardware connection diagram

3. Summary of module software application:

RFM69CW can fully replace RFM12B in hardware. Each module can be replaced with another by changing drive application software accordingly. Below is the modules software application instruction:

The configure pout of RFM69CW is standard SPI interface, MCU write and read the configuration of module register from SPI port. Time sequence is as below:

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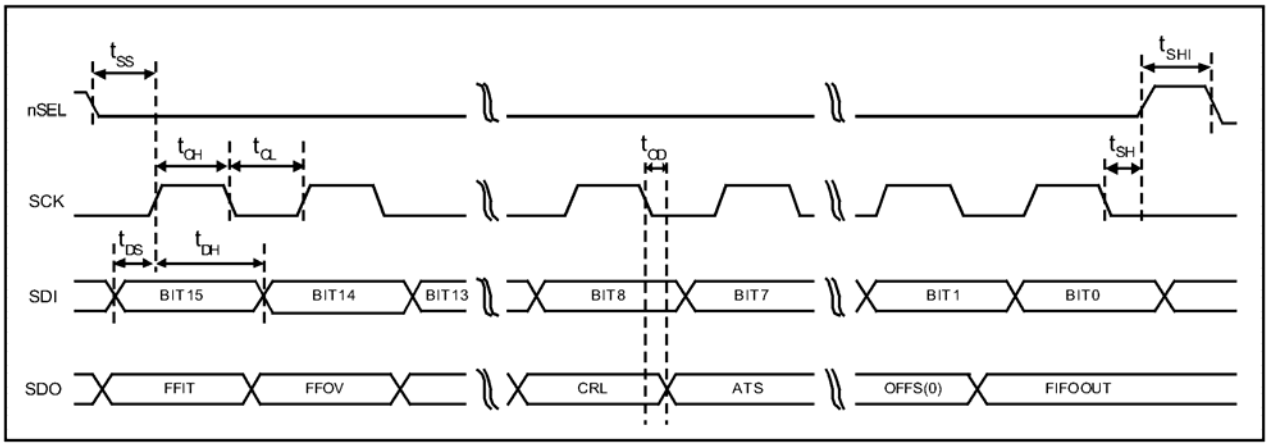
SPI time sequence

After RFM69CW initialized and configured, DIO0~4 as state mapping output pins, can be configured as state mapping output via configuring Reg DioMapping register, the function will be equal to NIRQ of RFM12B.

When the module in TX state, after writing transmitting data into data buffer FIFO, the data will be sent according the packet format and parameter already set.

When the module in RX state, after receiving valid data packet successfully, the data will be loaded into data buffer FIFO automatically and read via SPI. FIFO need be reset after valid data handled.

The configuration port of RFM12B is standard SPI interface. Module command is configured via SPI time sequence. SPI time sequence is as follows:



SPI time sequence

When RFM12B in TX state, it send data after hand packed via configuration data transmitting command.

When RFM12B in RX state, after receiving valid data, nIRQ will output low level interrupt signal and store the data into FIFO, then read the data via SPI interface.

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4. Demo Code：

Please click below link to find FM69CW and RFM12B application demo code for your reference.

http://www.hoperf.com/rf/fsk_module/RFM69.htm

http://www.hoperf.com/rf/fsk_module/RFM12B.htm

5. Please visit www.hoperf.com to learn more info.

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