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74HC40103

8-bit synchronous binary down counter

Rev. 03 — 12 November 2004 Product data sheet

1. General description

The 74HC40103 is a high-speed Si-gate CMOS device and are pin compatible with the 40103 of the 4000B series. The 74HC40103 is specified in compliance with JEDEC standard no. 7A.

The 74HC40103 consists of an 8-bit synchronous down counter with a single output which is active when the internal count is zero. The 74HC40103 contains a single 8-bit binary counter and has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count output ($\overline{TC}$) are active-LOW logic.

In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input ($\overline{TE}$) is HIGH. The terminal count output ($\overline{TC}$) goes LOW when the count reaches zero if $\overline{TE}$ is LOW, and remains LOW for one full clock period.

When the synchronous preset enable input ($\overline{PE}$) is LOW, data at the jam input (P0 to P7) is clocked into the counter on the next positive-going clock transition regardless of the state of $\overline{TE}$. When the asynchronous preset enable input ($\overline{PL}$) is LOW, data at the jam input (P0 to P7) is asynchronously forced into the counter regardless of the state of $\overline{PE}$, $\overline{TE}$, or CP. The jam inputs (P0 to P7) represent a single 8-bit binary word.

When the master reset input ($\overline{MR}$) is LOW, the counter is asynchronously cleared to its maximum count (decimal 255) regardless of the state of any other input.

If all control inputs except $\overline{TE}$ are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 256 clock pulses long.

The 74HC40103 may be cascaded using the $\overline{TE}$ input and the $\overline{TC}$ output, in either a synchronous or ripple mode.

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2. Features

- Cascadable
- Synchronous or asynchronous preset
- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C.

3. Applications

- Divide-by-n counters
- Programmable timers
- Interrupt timers
- Cycle/program counters.

4. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay CP to $\overline{TC}$	C_L = 15 pF; V_{CC} = 5 V		-	30	-	ns
f_{max}	maximum clock frequency	C_L = 15 pF; V_{CC} = 5 V		-	32	-	MHz
C_I	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	[1]	-	24	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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5. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC40103N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC40103D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC40103DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC40103PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

6. Functional diagram

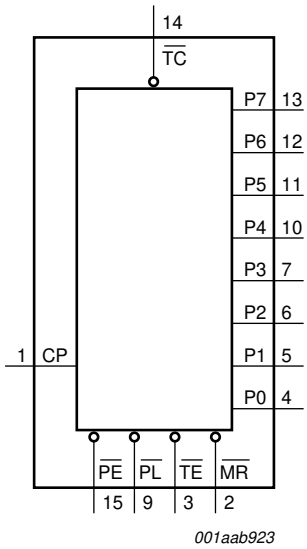


Fig 1. Functional diagram

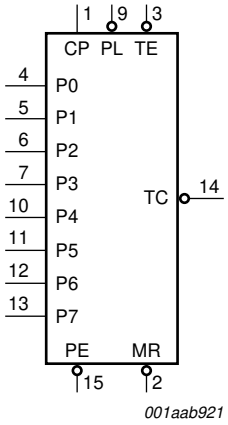


Fig 2. Logic symbol

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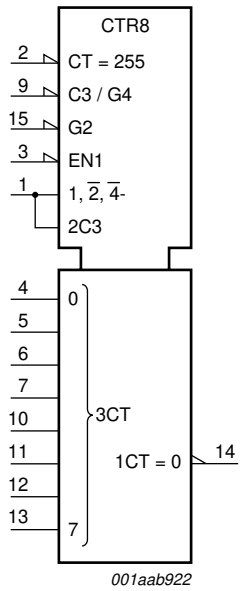


Fig 3. IEC logic symbol

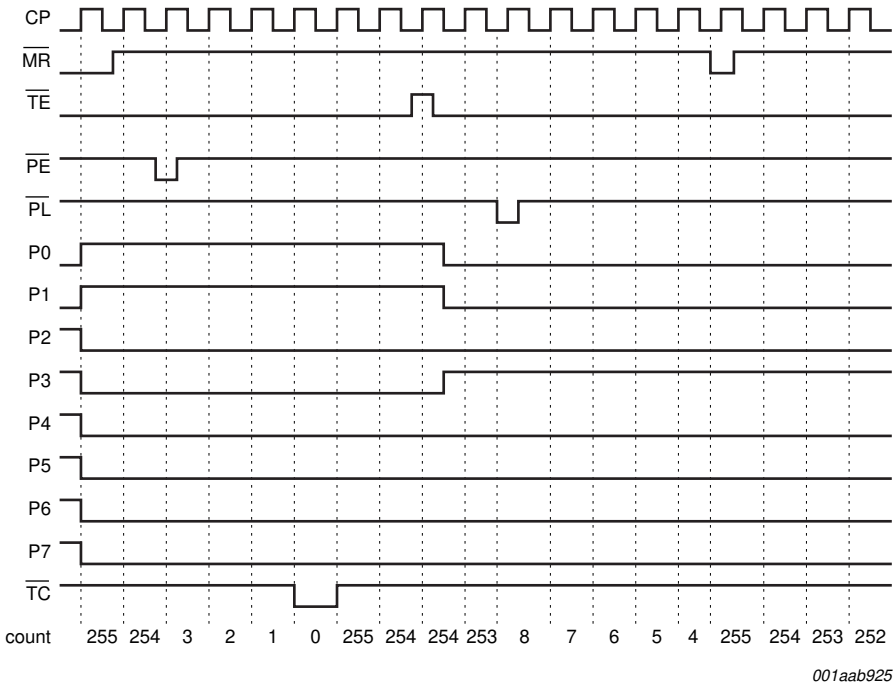


Fig 4. Timing diagram

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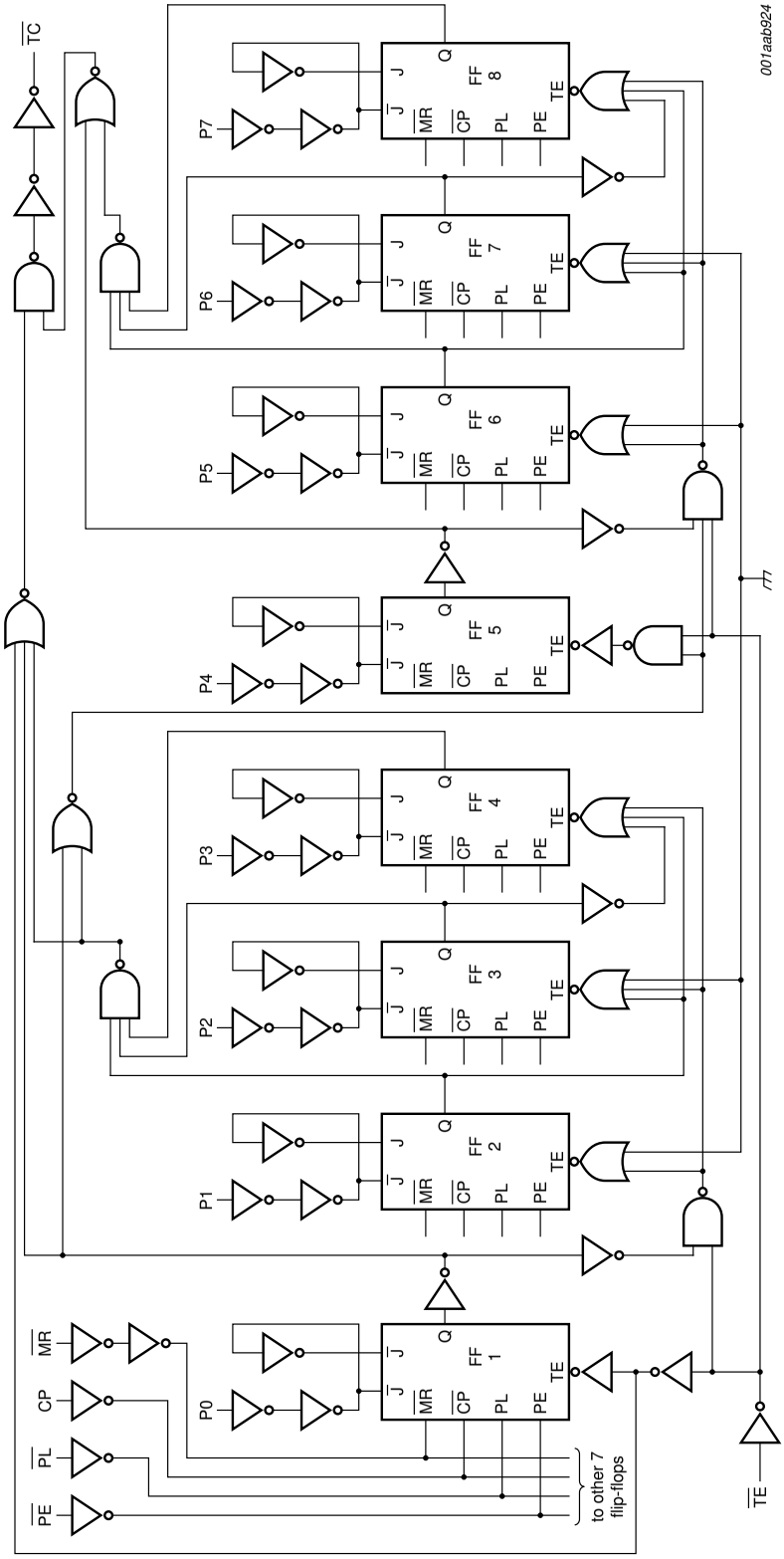


Fig 5. Logic diagram

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7. Pinning information

7.1 Pinning

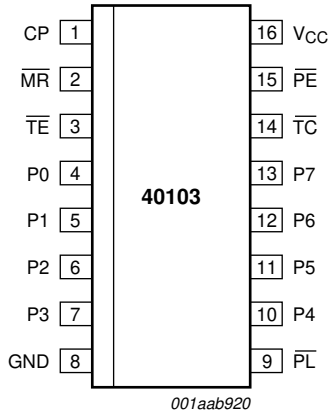


Fig 6. Pin configuration

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
CP	1	clock input (LOW-to-HIGH, edge-triggered)
$\overline{MR}$	2	asynchronous master reset input (active LOW)
$\overline{TE}$	3	terminal enable input (active LOW)
P0	4	jam input 0
P1	5	jam input 1
P2	6	jam input 2
P3	7	jam input 3
GND	8	ground (0 V)
$\overline{PL}$	9	asynchronous preset enable input (active LOW)
P4	10	jam input 4
P5	11	jam input 5
P5	12	jam input 6
P7	13	jam input 7
$\overline{TC}$	14	terminal count output (active LOW)
$\overline{PE}$	15	synchronous preset enable input (active LOW)
V_{CC}	16	positive supply voltage

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8. Functional description

8.1 Function table

Table 4: Function table [1]

Control inputs				Preset mode	Action [2]
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
L	X	X	X	asynchronous	clear to maximum count
H	L	X	X	asynchronous	preset asynchronously
	H	L	X	synchronous	preset on next LOW-to HIGH clock transition
		H	L	synchronous	count down
			H	synchronous	inhibit counter

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

[2] Clock connected to CP.
Synchronous operation: changes occur on the LOW-to-HIGH CP transition.
Jam inputs: MSD = P7, LSD = P0.

9. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input diode current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±20	mA
I_O	output source or sink current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V		-	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation					
	DIP16 package		[1]	-	750	mW
	SO16, SSOP16 and TSSOP16 packages		[2]	-	500	mW

[1] Above 70 °C: P_{tot} derates linearly with 12 mW/K.

[2] Above 70 °C: P_{tot} derates linearly with 8 mW/K.

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10. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall times	V_{CC} = 2.0 V	-	-	1000	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	-	400	ns
T_{amb}	ambient temperature		–40	-	+125	°C

11. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	µA
C_I	input capacitance		-	3.5	-	pF

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Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = −4 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	µA
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = −4 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.2	-	-	V

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Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	160	µA

12. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 13.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
t_{PHL}, t_{PLH}	propagation delay CP to $\overline{TC}$	see Figure 7				
		V_{CC} = 2.0 V	-	96	300	ns
		V_{CC} = 4.5 V	-	35	60	ns
		V_{CC} = 6.0 V	-	28	51	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	30	-	ns
	propagation delay $\overline{TE}$ to $\overline{TC}$	see Figure 8				
		V_{CC} = 2.0 V	-	50	175	ns
		V_{CC} = 4.5 V	-	18	35	ns
		V_{CC} = 6.0 V	-	14	30	ns
	propagation delay $\overline{PL}$ to $\overline{TC}$	see Figure 9				
		V_{CC} = 2.0 V	-	102	315	ns
		V_{CC} = 4.5 V	-	37	63	ns
		V_{CC} = 6.0 V	-	30	53	ns
t_{PHL}	propagation delay $\overline{MR}$ to $\overline{TC}$	see Figure 9				
		V_{CC} = 2.0 V	-	83	275	ns
		V_{CC} = 4.5 V	-	30	55	ns
		V_{CC} = 6.0 V	-	24	47	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 2.0 V	-	19	75	ns
		V_{CC} = 4.5 V	-	7	15	ns
		V_{CC} = 6.0 V	-	6	13	ns

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Table 8: Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 13.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_W	CP clock pulse width HIGH or LOW	see Figure 7				
		V_{CC} = 2.0 V	165	22	-	ns
		V_{CC} = 4.5 V	33	8	-	ns
		V_{CC} = 6.0 V	28	6	-	ns
	$\overline{MR}$ master reset pulse width LOW	see Figure 9				
		V_{CC} = 2.0 V	125	39	-	ns
		V_{CC} = 4.5 V	25	14	-	ns
		V_{CC} = 6.0 V	21	11	-	ns
	$\overline{PL}$ preset enable pulse width LOW	see Figure 9				
		V_{CC} = 2.0 V	125	33	-	ns
		V_{CC} = 4.5 V	25	12	-	ns
		V_{CC} = 6.0 V	21	10	-	ns
t_{rem}	removal time $\overline{MR}$ to CP, $\overline{PL}$ to CP	see Figure 10				
		V_{CC} = 2.0 V	50	14	-	ns
		V_{CC} = 4.5 V	10	5	-	ns
		V_{CC} = 6.0 V	9	4	-	ns
t_{su}	set-up time $\overline{PE}$ to CP	see Figure 11				
		V_{CC} = 2.0 V	75	22	-	ns
		V_{CC} = 4.5 V	15	8	-	ns
		V_{CC} = 6.0 V	13	6	-	ns
	set-up time $\overline{TE}$ to CP	see Figure 12				
		V_{CC} = 2.0 V	150	44	-	ns
		V_{CC} = 4.5 V	30	16	-	ns
		V_{CC} = 6.0 V	26	13	-	ns
	set-up time Pn to CP	see Figure 11				
		V_{CC} = 2.0 V	75	22	-	ns
		V_{CC} = 4.5 V	15	8	-	ns
		V_{CC} = 6.0 V	13	6	-	ns
t_h	hold time $\overline{PE}$ to CP	see Figure 11				
		V_{CC} = 2.0 V	0	–14	-	ns
		V_{CC} = 4.5 V	0	–5	-	ns
		V_{CC} = 6.0 V	0	–4	-	ns
	hold time $\overline{TE}$ to CP	see Figure 12				
		V_{CC} = 2.0 V	0	–30	-	ns
		V_{CC} = 4.5 V	0	–11	-	ns
		V_{CC} = 6.0 V	0	–9	-	ns
	hold time Pn to CP	see Figure 11				
		V_{CC} = 2.0 V	0	–17	-	ns
		V_{CC} = 4.5 V	0	–6	-	ns
		V_{CC} = 6.0 V	0	–5	-	ns

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Table 8: Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 13.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{max}	maximum clock frequency	see Figure 7					
		V_{CC} = 2.0 V		3.0	10	-	MHz
		V_{CC} = 4.5 V		15	29	-	MHz
		V_{CC} = 6.0 V		18	35	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF		-	32	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	[1]	-	24	-	pF
T_{amb} = −40 °C to +85 °C							
t_{PHL}, t_{PLH}	propagation delay CP to $\overline{TC}$	see Figure 7					
		V_{CC} = 2.0 V		-	-	375	ns
		V_{CC} = 4.5 V		-	-	75	ns
		V_{CC} = 6.0 V		-	-	64	ns
	propagation delay $\overline{TE}$ to $\overline{TC}$	see Figure 8					
		V_{CC} = 2.0 V		-	-	220	ns
		V_{CC} = 4.5 V		-	-	44	ns
		V_{CC} = 6.0 V		-	-	37	ns
	propagation delay $\overline{PL}$ to $\overline{TC}$	see Figure 9					
		V_{CC} = 2.0 V		-	-	395	ns
		V_{CC} = 4.5 V		-	-	79	ns
		V_{CC} = 6.0 V		-	-	40	ns
t_{PHL}	propagation delay $\overline{MR}$ to $\overline{TC}$	see Figure 9					
		V_{CC} = 2.0 V		-	-	345	ns
		V_{CC} = 4.5 V		-	-	69	ns
		V_{CC} = 6.0 V		-	-	59	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8					
		V_{CC} = 2.0 V		-	-	95	ns
		V_{CC} = 4.5 V		-	-	19	ns
		V_{CC} = 6.0 V		-	-	16	ns
t_W	CP clock pulse width HIGH or LOW	see Figure 7					
		V_{CC} = 2.0 V		205	-	-	ns
		V_{CC} = 4.5 V		41	-	-	ns
		V_{CC} = 6.0 V		35	-	-	ns
	$\overline{MR}$ master reset pulse width LOW	see Figure 9					
		V_{CC} = 2.0 V		155	-	-	ns
		V_{CC} = 4.5 V		31	-	-	ns
		V_{CC} = 6.0 V		26	-	-	ns
	$\overline{PL}$ preset enable pulse width LOW	see Figure 9					
		V_{CC} = 2.0 V		155	-	-	ns
		V_{CC} = 4.5 V		31	-	-	ns
		V_{CC} = 6.0 V		26	-	-	ns

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Table 8: Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 13.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rem}	removal time $\overline{MR}$ to CP, $\overline{PL}$ to CP	see Figure 10				
		V_{CC} = 2.0 V	65	-	-	ns
		V_{CC} = 4.5 V	13	-	-	ns
		V_{CC} = 6.0 V	11	-	-	ns
t_{su}	set-up time $\overline{PE}$ to CP	see Figure 11				
		V_{CC} = 2.0 V	95	-	-	ns
		V_{CC} = 4.5 V	19	-	-	ns
		V_{CC} = 6.0 V	16	-	-	ns
	set-up time $\overline{TE}$ to CP	see Figure 12				
		V_{CC} = 2.0 V	190	-	-	ns
		V_{CC} = 4.5 V	38	-	-	ns
		V_{CC} = 6.0 V	33	-	-	ns
	set-up time Pn to CP	see Figure 11				
		V_{CC} = 2.0 V	95	-	-	ns
		V_{CC} = 4.5 V	19	-	-	ns
		V_{CC} = 6.0 V	16	-	-	ns
t_h	hold time $\overline{PE}$ to CP	see Figure 11				
		V_{CC} = 2.0 V	0	-	-	ns
		V_{CC} = 4.5 V	0	-	-	ns
		V_{CC} = 6.0 V	0	-	-	ns
	hold time $\overline{TE}$ to CP	see Figure 12				
		V_{CC} = 2.0 V	0	-	-	ns
		V_{CC} = 4.5 V	0	-	-	ns
		V_{CC} = 6.0 V	0	-	-	ns
	hold time Pn to CP	see Figure 11				
		V_{CC} = 2.0 V	0	-	-	ns
		V_{CC} = 4.5 V	0	-	-	ns
		V_{CC} = 6.0 V	0	-	-	ns
f_{max}	maximum clock frequency	see Figure 7				
		V_{CC} = 2.0 V	2.4	-	-	MHz
		V_{CC} = 4.5 V	12	-	-	MHz
		V_{CC} = 6.0 V	14	-	-	MHz

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Table 8: Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 13.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$	see Figure 7				
		V_{CC} = 2.0 V	-	-	450	ns
		V_{CC} = 4.5 V	-	-	90	ns
		V_{CC} = 6.0 V	-	-	77	ns
	propagation delay $\overline{TE}$ to $\overline{TC}$	see Figure 8				
		V_{CC} = 2.0 V	-	-	265	ns
		V_{CC} = 4.5 V	-	-	53	ns
		V_{CC} = 6.0 V	-	-	45	ns
	propagation delay $\overline{PL}$ to $\overline{TC}$	see Figure 9				
		V_{CC} = 2.0 V	-	-	475	ns
		V_{CC} = 4.5 V	-	-	95	ns
		V_{CC} = 6.0 V	-	-	81	ns
t_{PHL}	propagation delay $\overline{MR}$ to $\overline{TC}$	see Figure 9				
		V_{CC} = 2.0 V	-	-	415	ns
		V_{CC} = 4.5 V	-	-	83	ns
		V_{CC} = 6.0 V	-	-	71	ns
t_{THL}/t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 2.0 V	-	-	110	ns
		V_{CC} = 4.5 V	-	-	22	ns
		V_{CC} = 6.0 V	-	-	19	ns
t_W	CP clock pulse width HIGH or LOW	see Figure 7				
		V_{CC} = 2.0 V	250	-	-	ns
		V_{CC} = 4.5 V	50	-	-	ns
		V_{CC} = 6.0 V	43	-	-	ns
	$\overline{MR}$ master reset pulse width LOW	see Figure 9				
		V_{CC} = 2.0 V	190	-	-	ns
		V_{CC} = 4.5 V	38	-	-	ns
		V_{CC} = 6.0 V	32	-	-	ns
	$\overline{PL}$ preset enable pulse width LOW	see Figure 9				
		V_{CC} = 2.0 V	190	-	-	ns
		V_{CC} = 4.5 V	38	-	-	ns
		V_{CC} = 6.0 V	32	-	-	ns
t_{rem}	removal time $\overline{MR}$ to CP, $\overline{PL}$ to CP	see Figure 10				
		V_{CC} = 2.0 V	75	-	-	ns
		V_{CC} = 4.5 V	15	-	-	ns
		V_{CC} = 6.0 V	13	-	-	ns

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Table 8: Dynamic characteristics *...continued*

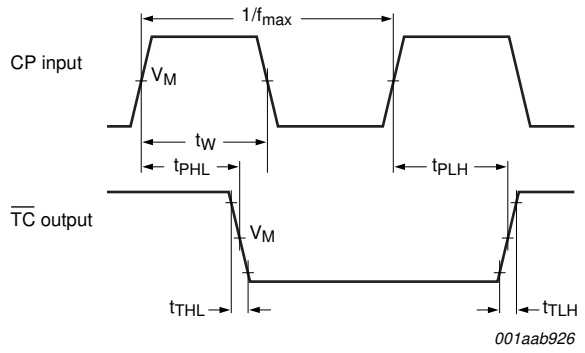
GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 13.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{su}	set-up time $\overline{PE}$ to CP	see Figure 11				
		V_{CC} = 2.0 V	110	-	-	ns
		V_{CC} = 4.5 V	22	-	-	ns
		V_{CC} = 6.0 V	19	-	-	ns
	set-up time $\overline{TE}$ to CP	see Figure 12				
		V_{CC} = 2.0 V	225	-	-	ns
		V_{CC} = 4.5 V	45	-	-	ns
		V_{CC} = 6.0 V	38	-	-	ns
	set-up time Pn to CP	see Figure 11				
		V_{CC} = 2.0 V	110	-	-	ns
		V_{CC} = 4.5 V	22	-	-	ns
		V_{CC} = 6.0 V	19	-	-	ns
t_h	hold time $\overline{PE}$ to CP	see Figure 11				
		V_{CC} = 2.0 V	0	-	-	ns
		V_{CC} = 4.5 V	0	-	-	ns
		V_{CC} = 6.0 V	0	-	-	ns
	hold time $\overline{TE}$ to CP	see Figure 12				
		V_{CC} = 2.0 V	0	-	-	ns
		V_{CC} = 4.5 V	0	-	-	ns
		V_{CC} = 6.0 V	0	-	-	ns
	hold time Pn to CP	see Figure 11				
		V_{CC} = 2.0 V	0	-	-	ns
		V_{CC} = 4.5 V	0	-	-	ns
		V_{CC} = 6.0 V	0	-	-	ns
f_{max}	maximum clock frequency	see Figure 7				
		V_{CC} = 2.0 V	2.0	-	-	MHz
		V_{CC} = 4.5 V	10	-	-	MHz
		V_{CC} = 6.0 V	12	-	-	MHz

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

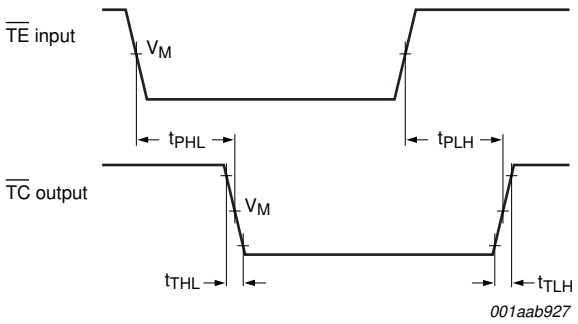
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13. Waveforms



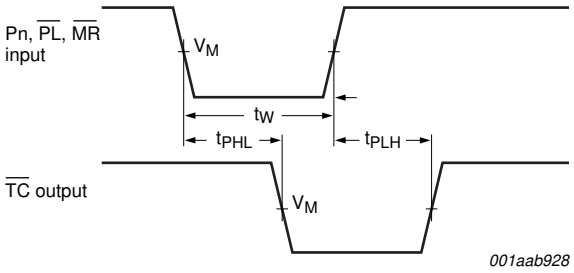
$V_M = 0.5 \times V_I$.

Fig 7. Waveforms showing the clock input (CP) to $\overline{TC}$ propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency



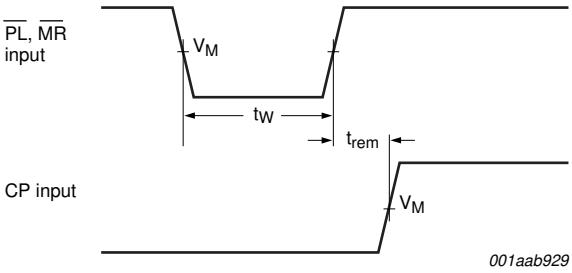
$V_M = 0.5 \times V_I$.

Fig 8. Waveforms showing the $\overline{TE}$ to $\overline{TC}$ propagation delays



$V_M = 0.5 \times V_I$.

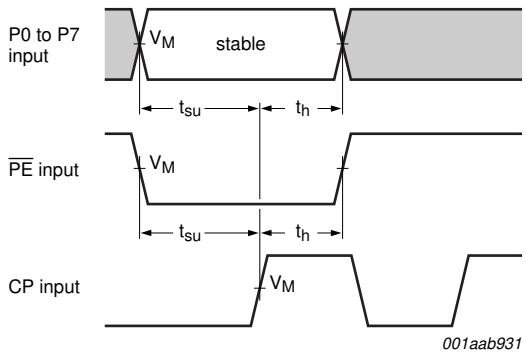
Fig 9. Waveforms showing $\overline{PL}$, $\overline{MR}$, Pn to $\overline{TC}$ propagation delays



$V_M = 0.5 \times V_I$.

Fig 10. Waveforms showing removal time for $\overline{MR}$ and $\overline{PL}$

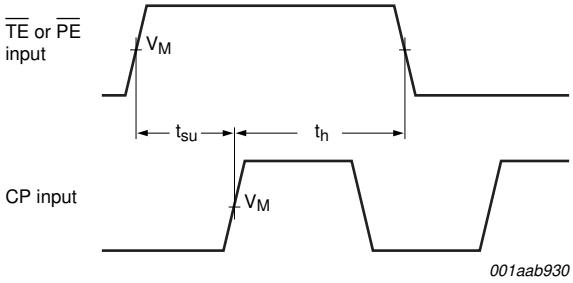
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The shaded areas indicate when the input is permitted to change for predictable output performance.

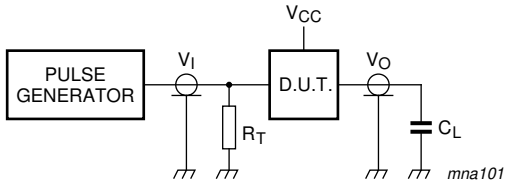
$V_M = 0.5 \times V_I$.

Fig 11. Waveforms showing hold and set-up times for Pn, $\overline{PE}$ to CP



$V_M = 0.5 \times V_I$.

Fig 12. Waveforms showing hold and set-up times for $\overline{MR}$ or $\overline{PE}$ to CP



Test data is given in Table 9.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 13. Load circuitry for switching times

Table 9: Test data

Supply	Input		Load
V_{CC}	V_I	t_r, t_f	C_L
2.0 V	V_{CC}	6 ns	50 pF
4.5 V	V_{CC}	6 ns	50 pF
6.0 V	V_{CC}	6 ns	50 pF
5.0 V	V_{CC}	6 ns	15 pF

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14. Application information

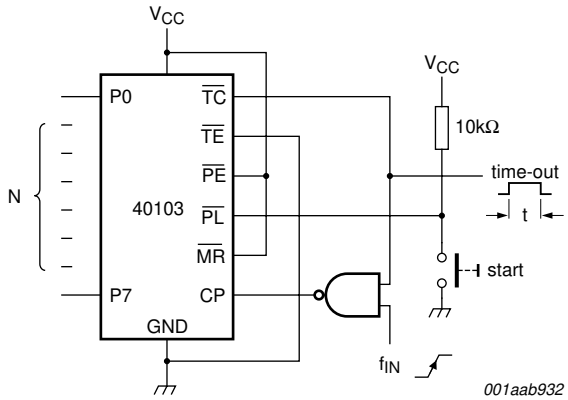


Fig 14. Programmable timer

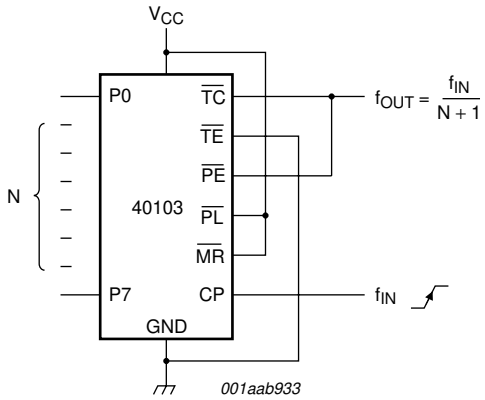
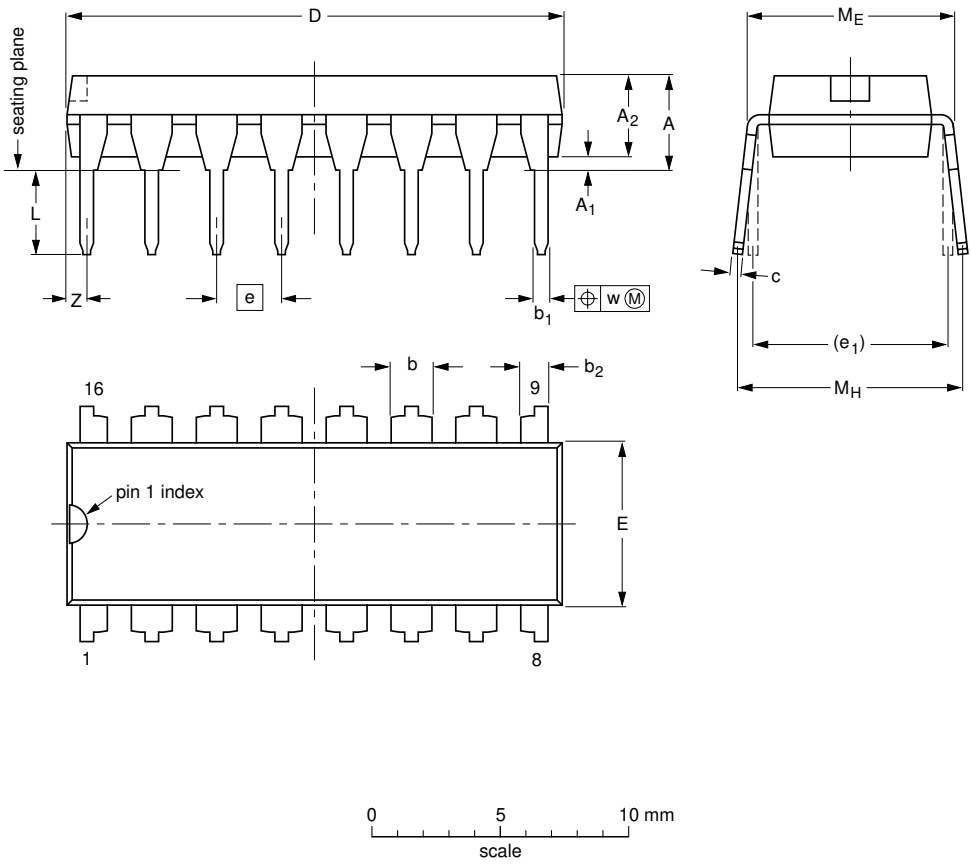


Fig 15. Divide-by-N counter

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15. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

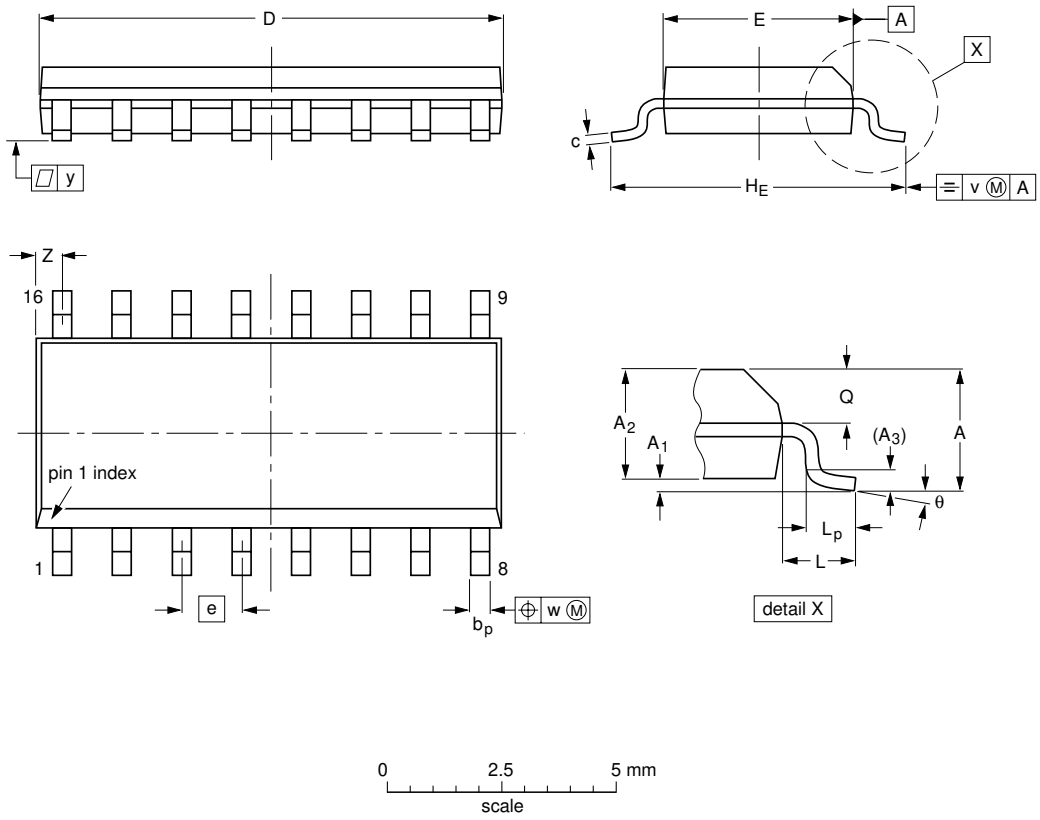
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 16. Package outline SOT38-4 (DIP16)

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SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

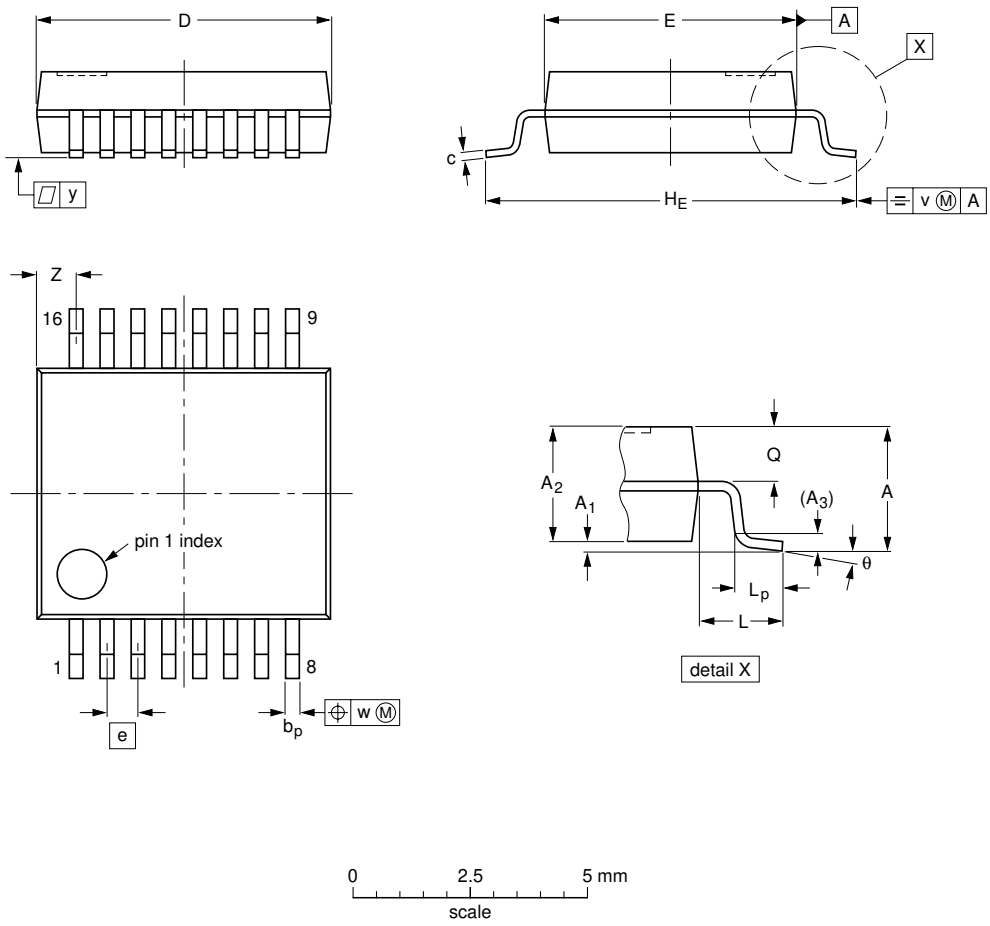
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 17. Package outline SOT109-1 (SO16)

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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

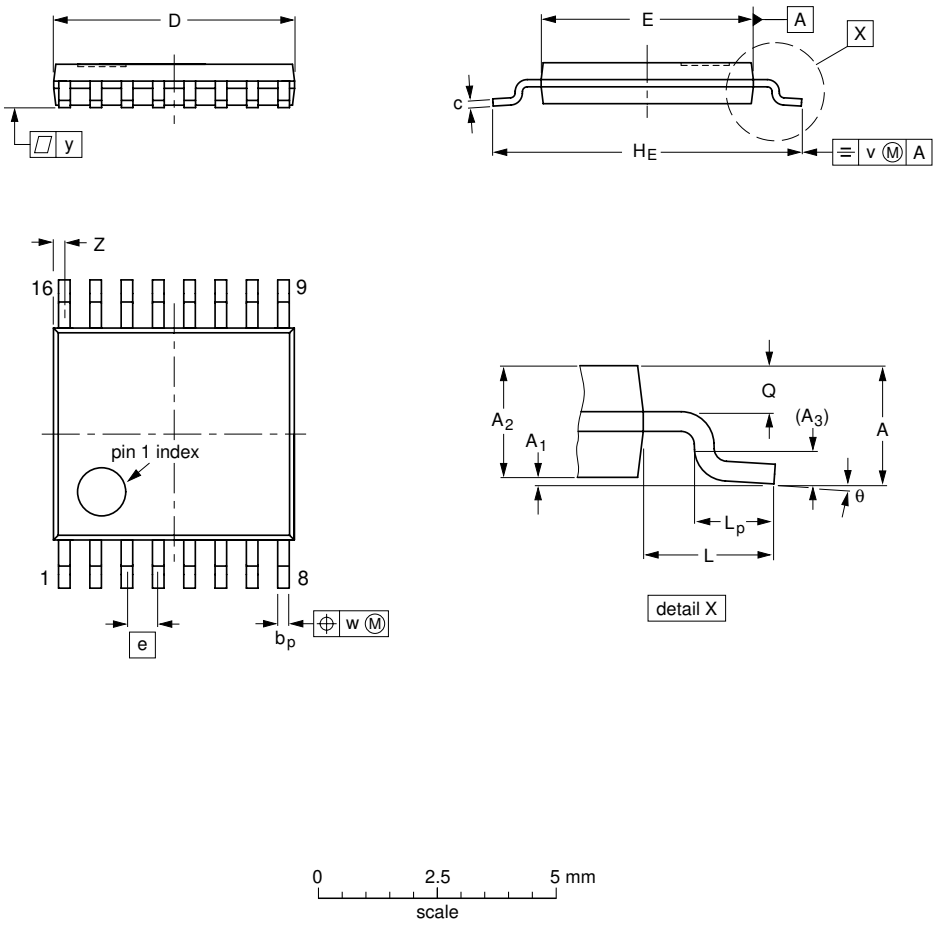
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 18. Package outline SOT338-1 (SSOP16)

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 19. Package outline SOT403-1 (TSSOP16)

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16. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC40103_3	20041112	Product data sheet	-	9397 750 13812	74HC_HCT40103_CNV_2
Modifications:	• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Removed type number 74HCT40103. • Inserted family specification.				
74HC_HCT40103_CNV_2	19970918	Product specification	-	-	74HC_HCT40103_1
74HC_HCT40103_1	19901201	Product specification	-	-	-

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17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 12 November 2004
Document number: 9397 750 13812

Published in The Netherlands