EN: This Datasheet/Document is presented by the manufacturer.

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MCP4706/4716/4726

8-/10-/12-Bit Voltage Output Digital-to-Analog Converter with EEPROM and I²C Interface

Features

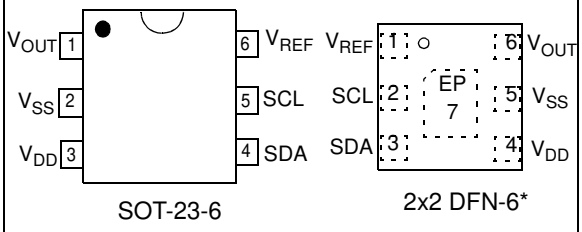
- Output Voltage Resolutions
  - 12-bit: MCP4726
  - 10-bit: MCP4716
  - 8-bit: MCP4706
- Rail-to-Rail Output
- Fast Settling Time of 6 µs (typical)
- DAC Voltage Reference Options
  - V_{DD}
  - V_{REF} Pin
- Output Gain Options
  - Unity (1x)
  - 2x, only when V_{REF} pin is used as voltage source
- Nonvolatile Memory (EEPROM)
  - Auto Recall of Saved DAC register setting
  - Auto Recall of Saved Device Configuration (Voltage Reference, Gain, Power Down)
- Power-Down Modes
  - Disconnects output buffer
  - Selection of V_{OUT} pull-down resistors (640 kΩ, 125 kΩ, or 1 kΩ)
- Low Power Consumption
  - Normal Operation: 210 µA typ.
  - Power Down Operation: 60 nA typ. (PD1:PD0 = "11")
- Single-Supply Operation: 2.7V to 5.5V
- I²C™ Interface:
  - Eight Available Addresses
  - Standard (100 kbps), Fast (400 kbps), and High-Speed (3.4 Mbps) Modes
- Small 6-lead SOT-23 and DFN (2x2) Packages
- Extended Temperature Range: -40°C to +125°C

Applications

- Set Point or Offset Trimming
- Sensor Calibration
- Low Power Portable Instrumentation
- PC Peripherals
- Data AcquisitionSystems
- Motor Control

Package Types

MCP4706 / 16 / 26



SOT-23-6 2x2 DFN-6*

* Includes Exposed Thermal Pad (EP); see Table 3-1.

Description

The MCP4706/4716/4726 are single channel 8-bit, 10-bit, and 12-bit buffered voltage output Digital-to-Analog Converters (DAC) with nonvolatile memory and an I²C Serial Interface. This family will also be referred to as MCP47X6.

The V_{REF} pin or the device V_{DD} can be selected as the DAC's reference voltage. When V_{DD} is selected, V_{DD} is connected internally to the DAC reference circuit. When the V_{REF} pin is used, the user can select the output buffer's gain to 1 or 2. When the gain is 2, the V_{REF} pin voltage should be limited to a maximum of $V_{DD}/2$.

The DAC Register value and configuration bits can be programmed to nonvolatile memory (EEPROM). The nonvolatile memory holds the DAC Register and configuration bit values when the device is powered off. A device reset (such as a Power On Reset) latches these stored values into the volatile memory.

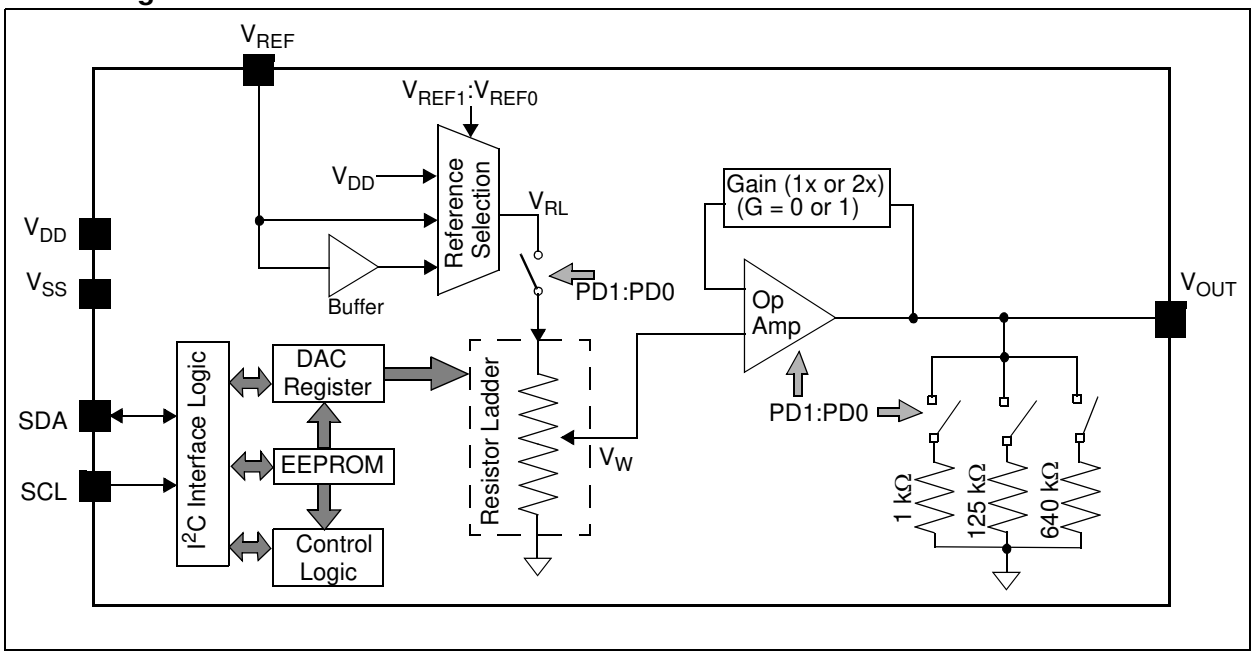
Power-down modes enable system current reduction when the DAC output voltage is not required. The V_{OUT} pin can be configured to present a low, medium, or high resistance load.

These devices have a two-wire I²C™ compatible serial interface for standard (100 kHz), fast (400 kHz), or high speed (3.4 MHz) mode.

These devices are available in small 6-pin SOT-23 and DFN 2x2 mm packages.

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Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V_{DD} with respect to V_{SS} ..... -0.6V to +6.5V
Voltage on all pins with respect to V_{SS}
..... -0.3V to V_{DD} + 0.3V
Input clamp current, I_{IK} ($V_I < 0$, $V_I > V_{DD}$, V_I)
.....±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)
.....±20 mA
Maximum input current source/sunk by SDA, SCL pins
.....2 mA
Maximum output current sunk by SDA Output pin
.....25 mA
Maximum current out of V_{SS} pin .....50 mA
Maximum current into V_{DD} pin .....50 mA
Maximum current sourced by the V_{OUT} pin .....40 mA
Maximum current sunk by the V_{OUT} pin.....40 mA
Maximum current sunk by the V_{REF} pin.....40 µA
Package power dissipation (T_A = +50°C, T_J = +150°C)
SOT-23-6 .....452 mW
DFN-6 .....1098 mW
Storage temperature .....-65°C to +150°C
Ambient temperature with power applied
.....-55°C to +125°C
ESD protection on all pins .....≥ 6 kV (HBM)
.....≥ 400V (MM)
Maximum Junction Temperature (T_J) .....+150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = 2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF, T_A = -40°C to +125°C. Typical values at +25°C.

Parameters	Symbol	Min	Typical	Max	Units	Conditions
Power Requirements						
Input Voltage	V_{DD}	2.7	—	5.5	V	
Input Current	I_{DD}	—	210	400	µA	V_{REF1}:V_{REF0} = '00', SCL = SDA = V_{SS}, V_{OUT} is unloaded, volatile DAC Register = 0x000
		—	210	400	µA	V_{REF1}:V_{REF0} = '11', V_{REF} = V_{DD}, SCL = SDA = V_{SS}, V_{OUT} is unloaded, volatile DAC Register = 0x000
Power-Down Current	I_{DDP}	—	0.09	2	µA	PD1:PD0 = '01' (**Note 6**), V_{OUT} not connected
Power-On Reset Threshold	V_{POR}	—	2.2	—	V	RAM retention voltage, (V_{RAM}) < V_{POR}
Power-Up Ramp Rate	V_{RAMP}	1	—	—	V/S	**(Note 1, Note 4)**

Note 1: This parameter is ensured by design and is not 100% tested.

2: This gain error does not include offset error. See Section 2 for more details in plots.

3: Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12- bit device).

4: The power-up ramp rate affects on uploading the EEPROM contents to the DAC register. It measures the rise of V_{DD} over time.

5: This parameter is ensured by characterization, and not 100% tested.

6: The PD1:PD0 = '10', and '11' configurations should have the same current.

7: V_{DD} = 5.5V.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF, T_A = -40°C to +125°C. Typical values at +25°C.

Parameters	Symbol	Min	Typical	Max	Units	Conditions
DC Accuracy						
Offset Error	V_{OS}		±0.02	0.75	% of FSR	Code = 0x000h V_{REF1}:V_{REF0} = '00', G = '0'
Offset Error Temperature Coefficient	V_{OS}/°C	—	±1	—	ppm/°C	-40°C to +25°C
		—	±2	—	ppm/°C	+25°C to +85°C
Zero Scale Error	E_{ZS}	—	0.13	2.0	LSb	MCP4706, Code = 0x00h
		—	0.52	7.7	LSb	MCP4716, Code = 0x000h
		—	2.05	30.8	LSb	MCP4726, Code = 0x000h
Full Scale Error	E_{FS}	—	0.3	5.2	LSb	MCP4706, Code = 0xFFh
		—	1.1	20.5	LSb	MCP4716, Code = 0x3FFh
		—	4.1	82.0	LSb	MCP4726, Code = 0xFFFh
Gain Error (Note 2)	g_E	-2	-0.10	2	% of FSR	MCP4706, Code = 0xFFh V_{REF1}:V_{REF0} = '00', G = '0'
		-2	-0.10	2	% of FSR	MCP4716, Code = 0x3FFh V_{REF1}:V_{REF0} = '00', G = '0'
		-2	-0.10	2	% of FSR	MCP4726, Code = 0xFFFh V_{REF1}:V_{REF0} = '00', G = '0'
Gain Error Drift	ΔG/°C	—	-3	—	ppm/°C	
Resolution	n		8		bits	MCP4706
			10		bits	MCP4716
			12		bits	MCP4726
INL Error (Note 7)	INL	-0.907	±0.125	+0.907	LSb	MCP4706 (codes: 6 to 250)
		-3.625	±0.5	+3.625	LSb	MCP4716 (codes: 25 to 1000)
		-14.5	±2	+14.5	LSb	MCP4726 (codes: 100 to 4000)
DNL Error (Note 7)	DNL	-0.05	±0.0125	+0.05	LSb	MCP4706 (codes: 6 to 250)
		-0.188	±0.05	+0.188	LSb	MCP4716 (codes: 25 to 1000)
		-0.75	±0.2	+0.75	LSb	MCP4726 (codes: 100 to 4000)

Note 1: This parameter is ensured by design and is not 100% tested.

2: This gain error does not include offset error. See Section 2 for more details in plots.

3: Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12- bit device).

4: The power-up ramp rate affects on uploading the EEPROM contents to the DAC register. It measures the rise of V_{DD} over time.

5: This parameter is ensured by characterization, and not 100% tested.

6: The PD1:PD0 = '10', and '11' configurations should have the same current.

7: V_{DD} = 5.5V.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF, T_A = -40°C to +125°C. Typical values at +25°C.

Parameters	Symbol	Min	Typical	Max	Units	Conditions
Output Amplifier						
Minimum Output Voltage	$V_{OUT(MIN)}$	—	0.01	—	V	Output Amplifier's minimum drive
Maximum Output Voltage	$V_{OUT(MAX)}$	—	V_{DD} – 0.04	—	V	Output Amplifier's maximum drive
Phase Margin	PM	—	66	—	Degree (°)	C_L = 400 pF, R_L = ∞
Slew Rate	SR	—	0.55	—	V/µs	
Short Circuit Current	I_{SC}	7	15	24	mA	
Settling Time	$t_{SETTLING}$	—	6	—	µs	**Note 3**
Power Down Output Disable Time Delay	T_{PDD}	—	1	—	µs	PD1:PD0 = "00" -> '11', '10', or '01' started from falling edge SCL at end of ACK bit. V_{OUT} = V_{OUT} - 10 mV. V_{OUT} not connected.
Power Down Output Enable Time Delay	T_{PDE}	—	10.5	—	µs	PD1:PD0 = '11', '10', or '01' -> "00" started from falling edge SCL at end of ACK bit. Volatile DAC Register = FFh, V_{OUT} = 10 mV. V_{OUT} not connected.
External Reference (V_{REF}) (Note 1)						
Input Range	V_{REF}	0.04	—	V_{DD} - 0.04	V	Buffered Mode
		0	—	V_{DD}	V	Unbuffered Mode
Input Impedance	R_{VREF}	—	210	—	kΩ	Unbuffered Mode
Input Capacitance	C_REF	—	29	—	pF	Unbuffered Mode
-3 dB Bandwidth		—	86.5	—	kHz	V_{REF} = 2.048V ± 0.1V, V_{REF1}:V_{REF0} = '10', G = '0'
		—	67.7	—	kHz	V_{REF} = 2.048V ± 0.1V, V_{REF1}:V_{REF0} = '10', G = '1'
Total Harmonic Distortion	THD	—	-73	—	dB	V_{REF} = 2.048V ± 0.1V, V_{REF1}:V_{REF0} = '10', G = '0', Frequency = 1 kHz
Dynamic Performance (Note 1)						
Major Code Transition Glitch		—	45	—	nV-s	1 LSb change around major carry (800h to 7FFh)
Digital Feedthrough		—	<10	—	nV-s	

Note 1: This parameter is ensured by design and is not 100% tested.

2: This gain error does not include offset error. See Section 2 for more details in plots.

3: Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12- bit device).

4: The power-up ramp rate affects on uploading the EEPROM contents to the DAC register. It measures the rise of V_{DD} over time.

5: This parameter is ensured by characterization, and not 100% tested.

6: The PD1:PD0 = '10', and '11' configurations should have the same current.

7: V_{DD} = 5.5V.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF, T_A = -40°C to +125°C. Typical values at +25°C.

Parameters	Symbol	Min	Typical	Max	Units	Conditions
Digital Interface						
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA
Input High Voltage (SDA and SCL Pins)	V_{IH}	$0.7V_{DD}$	—	—	V	
Input Low Voltage (SDA and SCL Pins)	V_{IL}	—	—	$0.3V_{DD}$	V	
Input Leakage	I_{LI}	—	—	±1	µA	SCL = SDA = V_{SS} or SCL = SDA = V_{DD}
Pin Capacitance	C_{PIN}	—	—	3	pF	**(Note 5)**
EEPROM						
EEPROM Write Time	T_{WRITE}	—	25	50	ms	
Data Retention		—	200	—	Years	At +25°C, **(Note 1)**
Endurance		1	—	—	Million Cycles	At +25°C, **(Note 1)**

Note 1: This parameter is ensured by design and is not 100% tested.

2: This gain error does not include offset error. See Section 2 for more details in plots.

3: Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12- bit device).

4: The power-up ramp rate affects on uploading the EEPROM contents to the DAC register. It measures the rise of V_{DD} over time.

5: This parameter is ensured by characterization, and not 100% tested.

6: The PD1:PD0 = '10', and '11' configurations should have the same current.

7: V_{DD} = 5.5V.

1.1 I²C Mode Timing Waveforms and Requirements

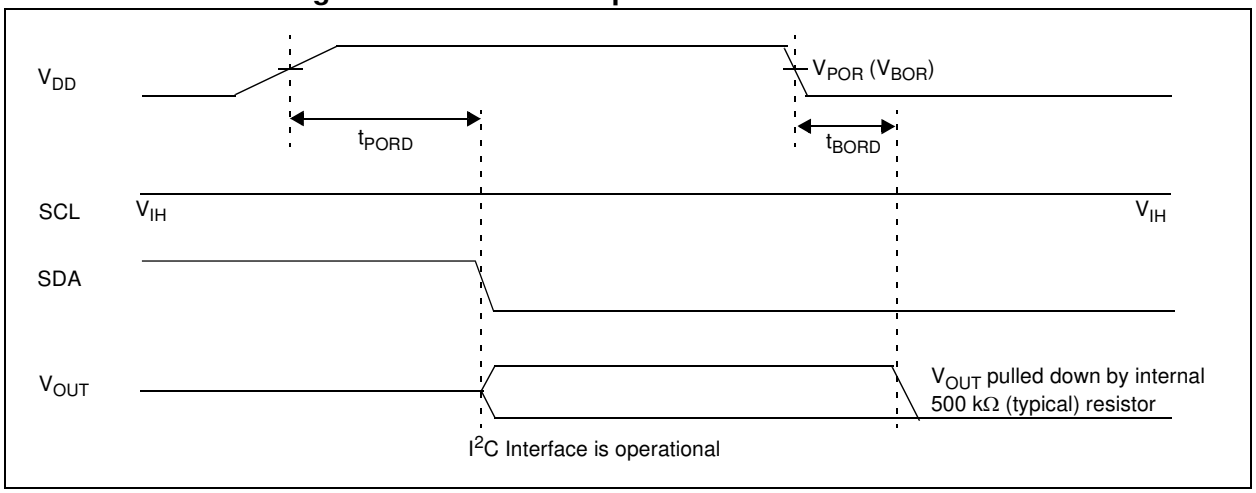


FIGURE 1-1: *Power-On and Brown-Out Reset Waveforms.*

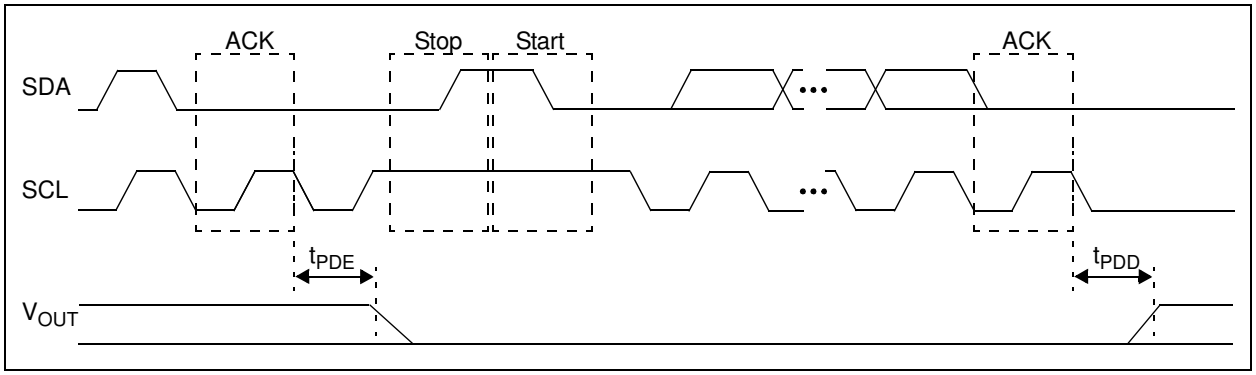


FIGURE 1-2: *I²C Power-Down Command Timing.*

TABLE 1-1: RESET TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Power Up Reset Delay	t_{PORD}	—	60	—	µs	Monitor ACK bit response to ensure device responds to command.
Brown Out Reset Delay	t_{BORD}	—	1	—	µs	V_{DD} transitions from $V_{DD(MIN)}$ → > V_{POR} V_{OUT} driven to V_{OUT} disabled
Power Down Disable Time Delay	T_{PDD}	—	2.5	—	µs	V_{DD} = 5V PD1:PD0 → '00' (from '01', '10', or '11'), from falling edge SCL at end of ACK bit.
		—	5	—	µs	V_{DD} = 3V PD1:PD0 → '00' (from '01', '10', or '11'), from falling edge SCL at end of ACK bit.
Power Down Enable Time Delay	T_{PDE}	—	10.5	—	µs	PD1:PD0 → '01', '10', or '11' (from '00'), from falling edge SCL at end of ACK bit.

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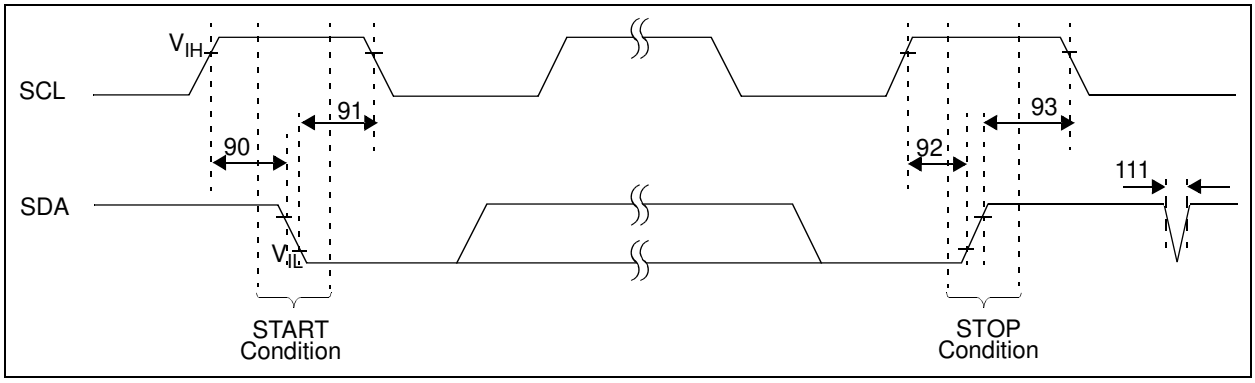


FIGURE 1-3: *I²C Bus Start/Stop Bits Timing Waveforms.*

TABLE 1-2: I²C BUS START/STOP BITS REQUIREMENTS

I²C AC Characteristics				**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage VDD range is described in **Electrical characteristics**			
Param. No.	**Symbol**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
	F_{SCL}	SCL pin Frequency	Standard Mode	0	100	kHz	C_b = 400 pF, 2.7V - 5.5V
			Fast Mode	0	400	kHz	C_b = 400 pF, 2.7V - 5.5V
			High-Speed 1.7	0	1.7	MHz	C_b = 400 pF, 4.5V - 5.5V
			High-Speed 3.4	0	3.4	MHz	C_b = 100 pF, 4.5V - 5.5V
D102	C_b	Bus capacitive loading	100 kHz mode	—	400	pF	
			400 kHz mode	—	400	pF	
			1.7 MHz mode	—	400	pF	
			3.4 MHz mode	—	100	pF	
90	TSU:STA	START condition Setup time	100 kHz mode	4700	—	ns	Only relevant for repeated START condition
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
91	THD:STA	START condition Hold time	100 kHz mode	4000	—	ns	After this period the first clock pulse is generated
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
92	TSU:STO	STOP condition Setup time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
93	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
94	T_{HVCSU}	HVC to SCL Setup time		25	—	uS	High Voltage Commands
95	T_{HVCHD}	SCL to HVC Hold time		25	—	uS	High Voltage Commands

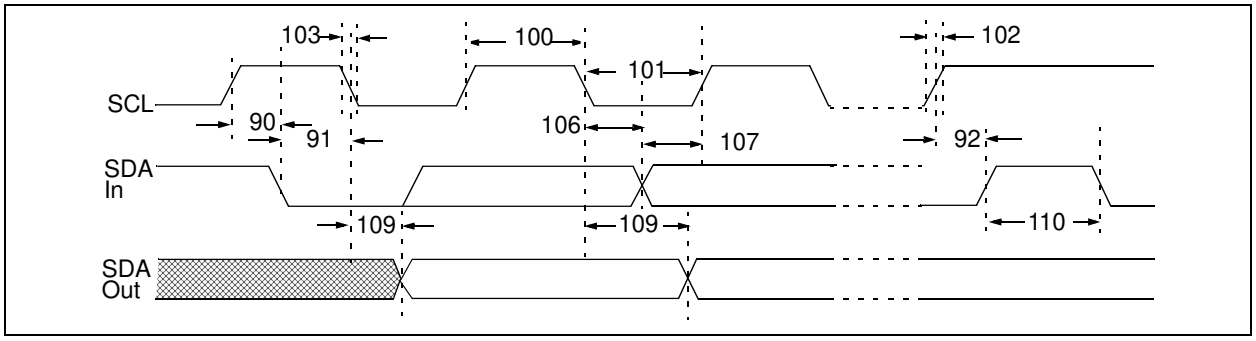


FIGURE 1-4: *I^2C Bus Data Timing.*

TABLE 1-3: I^2C BUS DATA REQUIREMENTS (SLAVE MODE)

I^2C AC Characteristics				**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage V_{DD} range is described in **Electrical characteristics**			
Param. No.	**Sym**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
100	THIGH	Clock high time	100 kHz mode	4000	—	ns	2.7V-5.5V
			400 kHz mode	600	—	ns	2.7V-5.5V
			1.7 MHz mode	120		ns	4.5V-5.5V
			3.4 MHz mode	60	—	ns	4.5V-5.5V
101	TLOW	Clock low time	100 kHz mode	4700	—	ns	2.7V-5.5V
			400 kHz mode	1300	—	ns	2.7V-5.5V
			1.7 MHz mode	320		ns	4.5V-5.5V
			3.4 MHz mode	160	—	ns	4.5V-5.5V

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I^2C-bus device can be used in a standard-mode (100 kHz) I^2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line.
T_R max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I^2C bus specification) before the SCL line is released.

3: The MCP47X6 device must provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCL signal. This specification is not a part of the I^2C specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

4: Use C_b in pF for the calculations.

5: Not Tested. This parameter ensured by characterization.

6: A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.
If this parameter is too short, it can create an unintentional Start or Stop condition to other devices on the I^2C bus line. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.
Data Input: This parameter must be longer than t_{SP}.
Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

7: Ensured by the T_{AA} 3.4 MHz specification test.

8: The specification is not part of the I^2C specification. $T_{AA} = T_{HD:DAT} + T_{FSDA}$ (or T_{RSDA}).

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TABLE 1-3: I²C BUS DATA REQUIREMENTS (SLAVE MODE) (CONTINUED)

I²C AC Characteristics				Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage V_{DD} range is described in **Electrical characteristics**			
Param. No.	**Sym**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
102A(5)	T_{RSCL}	SCL rise time	100 kHz mode	—	1000	ns	C_b is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb	300	ns	
			1.7 MHz mode	20	80	ns	
			1.7 MHz mode	20	160	ns	After a Repeated Start condition or an Acknowledge bit
			3.4 MHz mode	10	40	ns	
			3.4 MHz mode	10	80	ns	After a Repeated Start condition or an Acknowledge bit
102B(5)	T_{RSDA}	SDA rise time	100 kHz mode	—	1000	ns	C_b is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	
103A(5)	T_{FSCL}	SCL fall time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb	300	ns	
			1.7 MHz mode	20	80	ns	
			3.4 MHz mode	10	40	ns	
103B(5)	T_{FSDA}	SDA fall time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb(4)	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line.
T_R max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

3: The MCP47X6 device must provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCL signal. This specification is not a part of the I²C specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

4: Use C_b in pF for the calculations.

5: Not Tested. This parameter ensured by characterization.

6: A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.
If this parameter is too short, it can create an unintentional Start or Stop condition to other devices on the I²C bus line. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.

Data Input: This parameter must be longer than t_{SP}.
Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

7: Ensured by the T_{AA} 3.4 MHz specification test.

8: The specification is not part of the I²C specification. $T_{AA} = T_{HD:DAT} + T_{FSDA}$ (or T_{RSDA}).

TABLE 1-3: I²C BUS DATA REQUIREMENTS (SLAVE MODE) (CONTINUED)

I²C AC Characteristics				Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage V_{DD} range is described in **Electrical characteristics**			
Param. No.	**Sym**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
106	$T_{HD:DAT}$	Data input hold time	100 kHz mode	0	—	ns	2.7V-5.5V, **Note 6**
			400 kHz mode	0	—	ns	2.7V-5.5V, **Note 6**
			1.7 MHz mode	0	—	ns	4.5V-5.5V, **Note 6**
			3.4 MHz mode	0	—	ns	4.5V-5.5V, **Note 6**
107	$T_{SU:DAT}$	Data input setup time	100 kHz mode	250	—	ns	**Note 2**
			400 kHz mode	100	—	ns	
			1.7 MHz mode	10	—	ns	
			3.4 MHz mode	10	—	ns	
109	T_{AA}	Output valid from clock	100 kHz mode	—	3750	ns	**Note 1**, **Note 8**
			400 kHz mode	—	1200	ns	
			1.7 MHz mode	—	150	ns	Cb = 100 pF, **Note 1**, **Note 7**, **Note 8**
				—	310	ns	Cb = 400 pF, **Note 1**, **Note 5**, **Note 8**
			3.4 MHz mode	—	150	ns	Cb = 100 pF, **Note 1**, **Note 8**
110	T_{BUF}	Bus free time	100 kHz mode	4700	—	ns	Time the bus must be free before a new transmission can start
			400 kHz mode	1300	—	ns	
			1.7 MHz mode	N.A.	—	ns	
			3.4 MHz mode	N.A.	—	ns	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement $t_{SU:DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line.
T_R max.+$t_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

3: The MCP47X6 device must provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCL signal. This specification is not a part of the I²C specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

4: Use C_b in pF for the calculations.

5: Not Tested. This parameter ensured by characterization.

6: A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.
If this parameter is too short, it can create an unintentional Start or Stop condition to other devices on the I²C bus line. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.

Data Input: This parameter must be longer than t_{SP}.

Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

7: Ensured by the T_{AA} 3.4 MHz specification test.

8: The specification is not part of the I²C specification. $T_{AA} = T_{HD:DAT} + T_{FSDA}$ (or T_{RSDA}).

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TABLE 1-3: I²C BUS DATA REQUIREMENTS (SLAVE MODE) (CONTINUED)

I²C AC Characteristics				Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage V_{DD} range is described in **Electrical characteristics**			
Param. No.	**Sym**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
111	T_{SP}	Input filter spike suppression (SDA and SCL)	100 kHz mode	—	50	ns	NXP Spec states N.A.
			400 kHz mode	—	50	ns	
			1.7 MHz mode	—	10	ns	Spike suppression
			3.4 MHz mode	—	10	ns	Spike suppression
			—	—	—	ns	Standard Mode, (Not Applicable)
			50 (typ)	—	—	ns	Fast Mode
			10 (typ)	—	—	ns	High Speed Mode 1.7
			10 (typ)	—	—	ns	High Speed Mode 3.4

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line.
T_R max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

3: The MCP47X6 device must provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCL signal. This specification is not a part of the I²C specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

4: Use C_b in pF for the calculations.

5: Not Tested. This parameter ensured by characterization.

6: A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.
If this parameter is too short, it can create an unintentional Start or Stop condition to other devices on the I²C bus line. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.

Data Input: This parameter must be longer than t_{SP}.
Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

7: Ensured by the T_{AA} 3.4 MHz specification test.

8: The specification is not part of the I²C specification. $T_{AA} = T_{HD:DAT} + T_{FSDA}$ (or T_{RSDA}).

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Symbol**	**Min**	**Typical**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 6L-SOT-23	θ_{JA}	—	190	—	°C/W	
Thermal Resistance, 6L-DFN (2 x 2)	θ_{JA}	—	91	—	°C/W	

Note 1: The MCP47X6 devices operate over this extended temperature range, but with reduced performance. Operation in this range must not cause T_J to exceed the Maximum Junction Temperature of +150°C.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

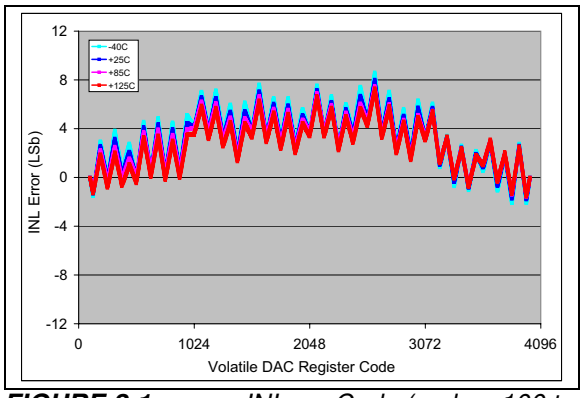


FIGURE 2-1: *INL vs. Code (code = 100 to 4000) and Temperature (**MCP4726**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '00'.*

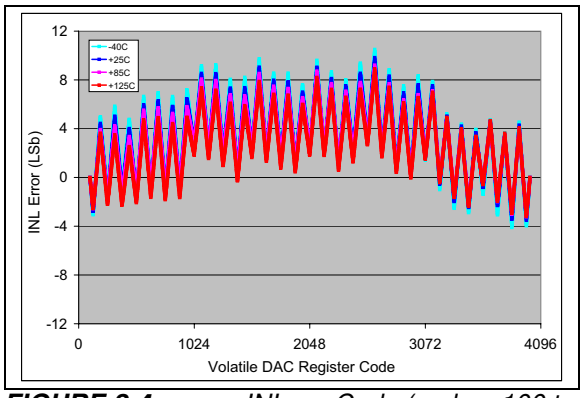


FIGURE 2-4: *INL vs. Code (code = 100 to 4000) and Temperature (**MCP4726**). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '00'.*

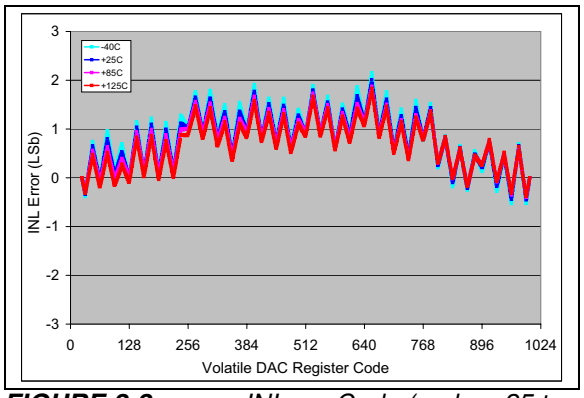


FIGURE 2-2: *INL vs. Code (code = 25 to 1000) and Temperature (MCP4716). V_{DD} = 5V, V_{REF1}:V_{REF0} = '00'.*

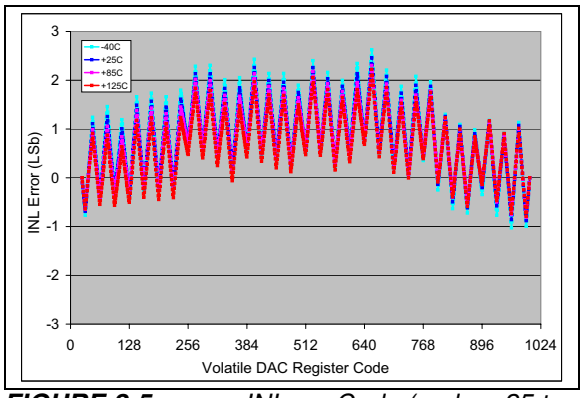


FIGURE 2-5: *INL vs. Code (code = 25 to 1000) and Temperature (MCP4716). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '00'.*

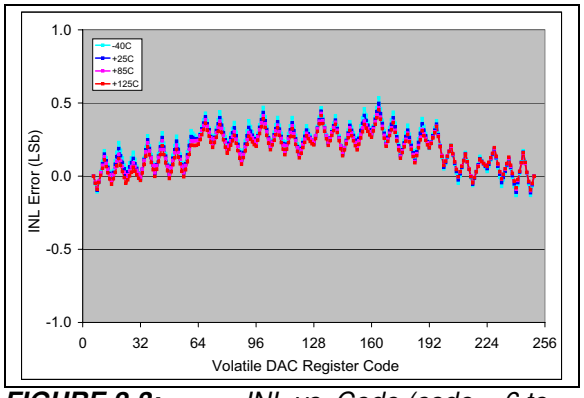


FIGURE 2-3: *INL vs. Code (code = 6 to 250) and Temperature (MCP4706). V_{DD} = 5V, V_{REF1}:V_{REF0} = '00'.*

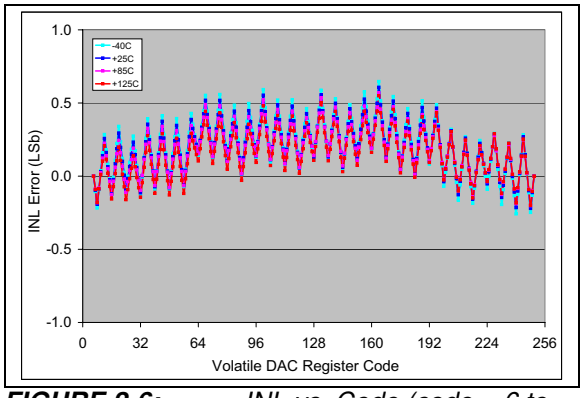


FIGURE 2-6: *INL vs. Code (code = 6 to 250) and Temperature (MCP4706). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '00'.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

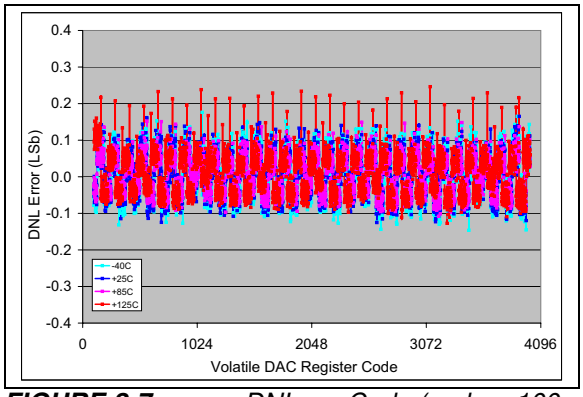


FIGURE 2-7: *DNL vs. Code (code = 100 to 4000) and Temperature (**MCP4726**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '00'.*

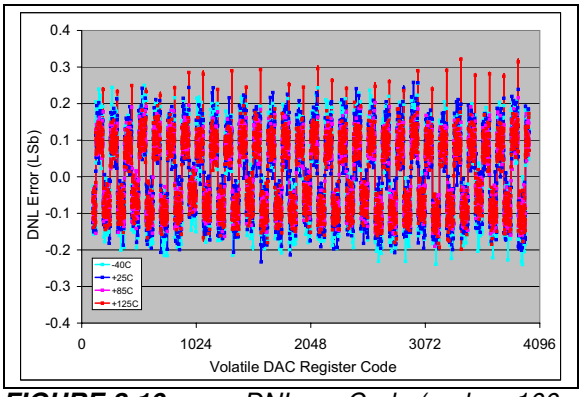


FIGURE 2-10: *DNL vs. Code (code = 100 to 4000) and Temperature (**MCP4726**). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '00'.*

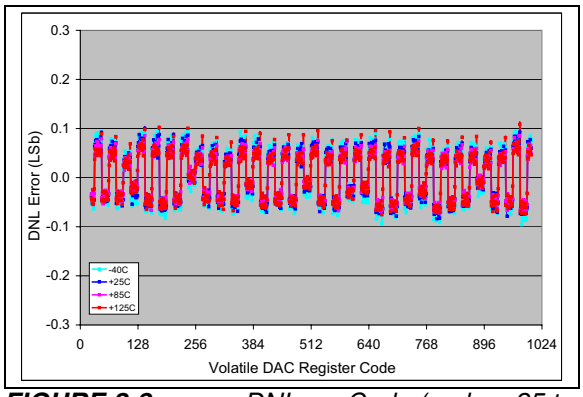


FIGURE 2-8: *DNL vs. Code (code = 25 to 1000) and Temperature (**MCP4716**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '00'.*

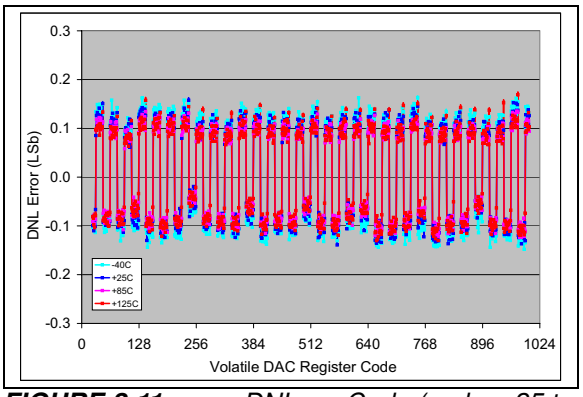


FIGURE 2-11: *DNL vs. Code (code = 25 to 1000) and Temperature (**MCP4716**). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '00'.*

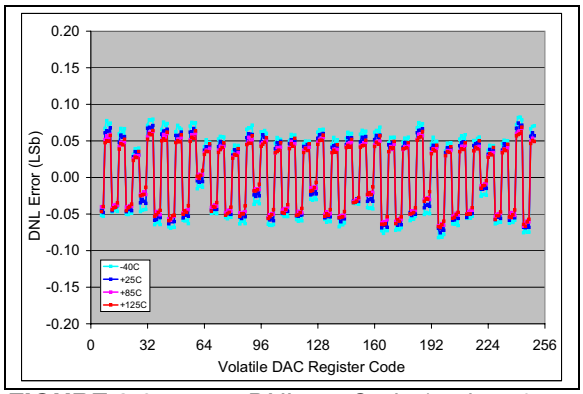


FIGURE 2-9: *DNL vs. Code (code = 6 to 250) and Temperature (**MCP4706**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '00'.*

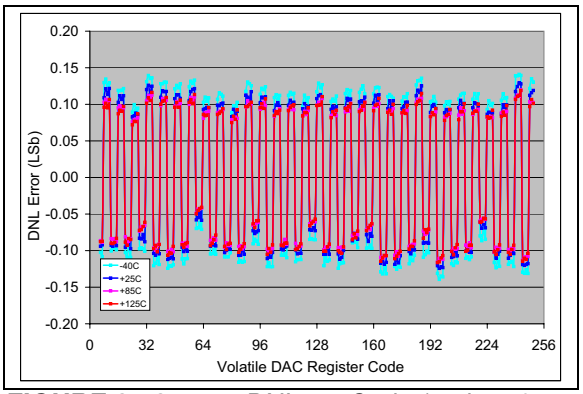


FIGURE 2-12: *DNL vs. Code (code = 6 to 250) and Temperature (**MCP4706**). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '00'.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

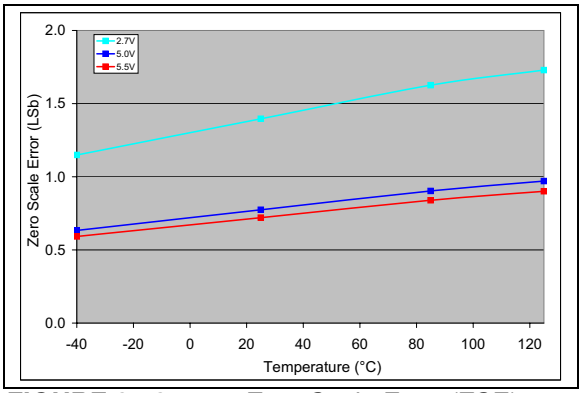


FIGURE 2-13: *Zero Scale Error (ZSE) vs. Temperature (**MCP4726**).*
V_{DD} = 5V, V_{REF1}:V_{REF0} = '00'.

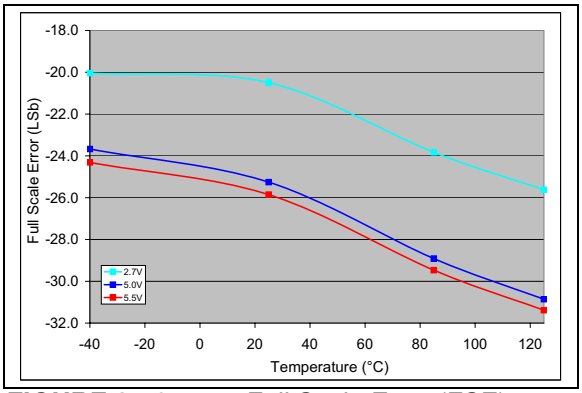


FIGURE 2-16: *Full Scale Error (FSE) vs. Temperature (**MCP4726**).*
V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '00'.

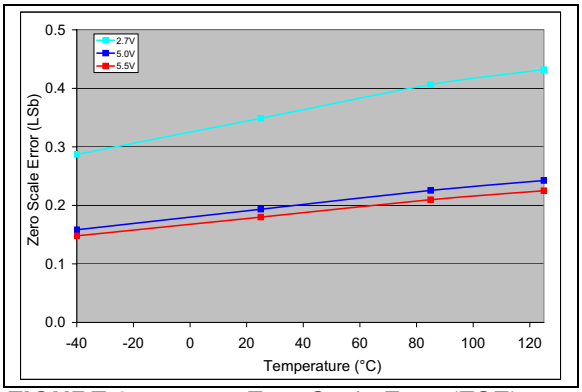


FIGURE 2-14: *Zero Scale Error (ZSE) vs. Temperature (**MCP4716**).*
V_{DD} = 5V, V_{REF1}:V_{REF0} = '00'.

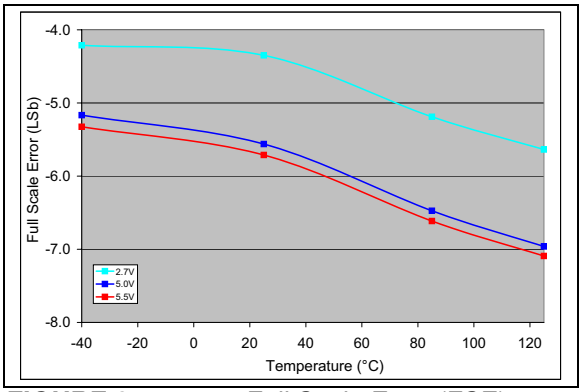


FIGURE 2-17: *Full Scale Error (FSE) vs. Temperature (**MCP4716**).*
V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '00'.

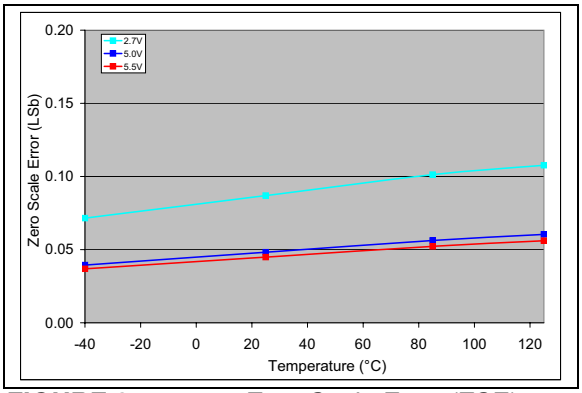


FIGURE 2-15: *Zero Scale Error (ZSE) vs. Temperature (**MCP4706**).*
V_{DD} = 5V, V_{REF1}:V_{REF0} = '00'.

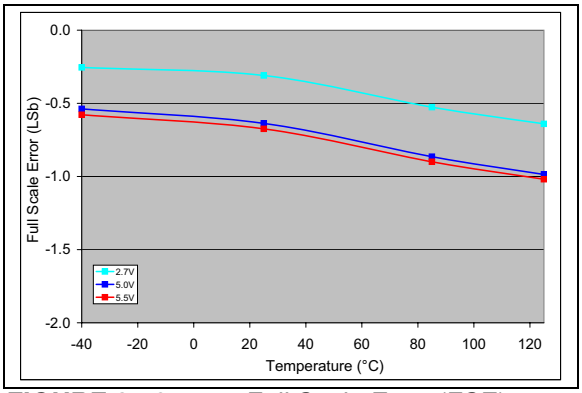


FIGURE 2-18: *Full Scale Error (FSE) vs. Temperature (**MCP4706**).*
V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '00'.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

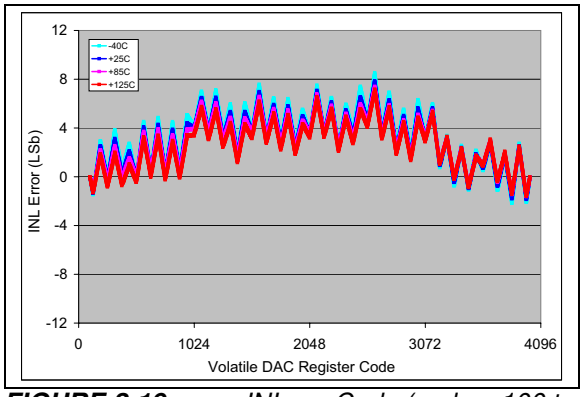


FIGURE 2-19: *INL vs. Code (code = 100 to 4000) and Temperature (**MCP4726**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.*

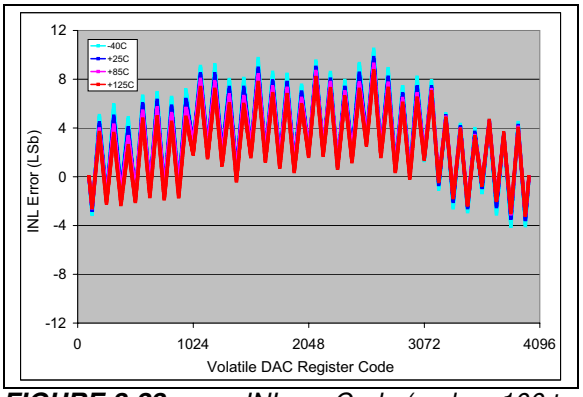


FIGURE 2-22: *INL vs. Code (code = 100 to 4000) and Temperature (**MCP4726**). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.*

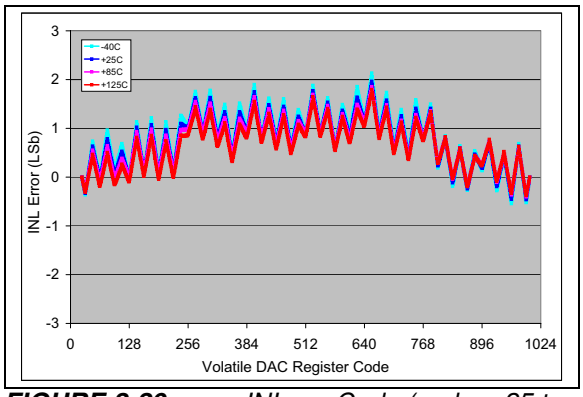


FIGURE 2-20: *INL vs. Code (code = 25 to 1000) and Temperature (**MCP4716**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.*

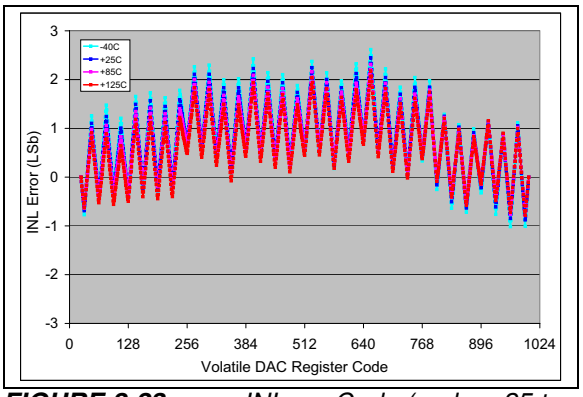


FIGURE 2-23: *INL vs. Code (code = 25 to 1000) and Temperature (**MCP4716**). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.*

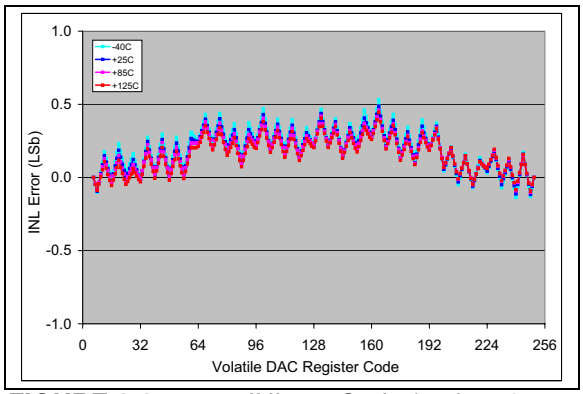


FIGURE 2-21: *INL vs. Code (code = 6 to 250) and Temperature (**MCP4706**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.*

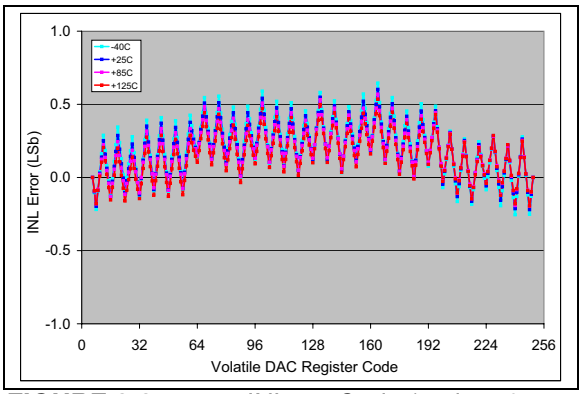


FIGURE 2-24: *INL vs. Code (code = 6 to 250) and Temperature (**MCP4706**). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

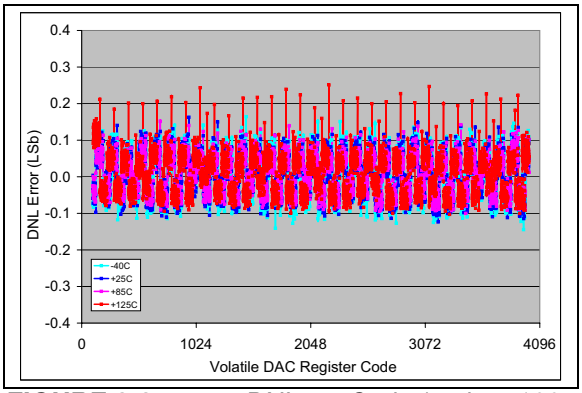


FIGURE 2-25: *DNL vs. Code (code = 100 to 4000) and Temperature (**MCP4726**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.*

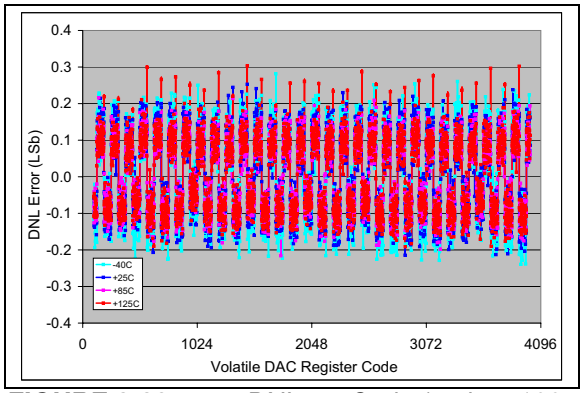


FIGURE 2-28: *DNL vs. Code (code = 100 to 4000) and Temperature (**MCP4726**). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.*

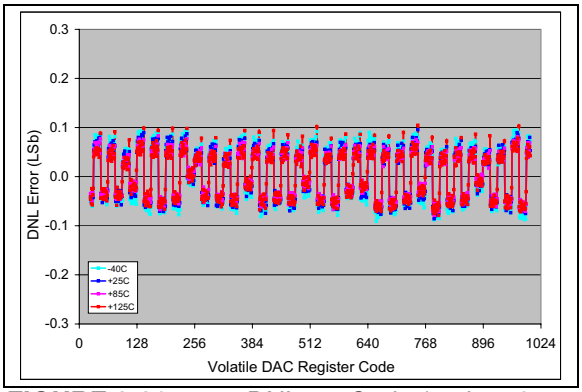


FIGURE 2-26: *DNL vs. Code (code = 25 to 1000) and Temperature (**MCP4716**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.*

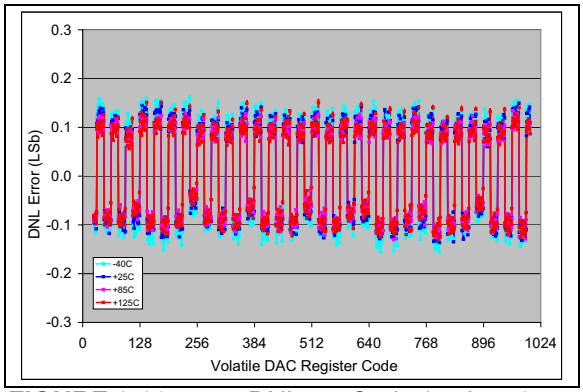


FIGURE 2-29: *DNL vs. Code (code = 25 to 1000) and Temperature (**MCP4716**). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.*

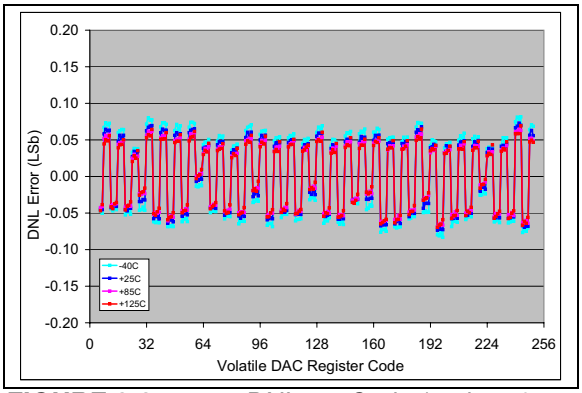


FIGURE 2-27: *DNL vs. Code (code = 6 to 250) and Temperature (**MCP4706**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.*

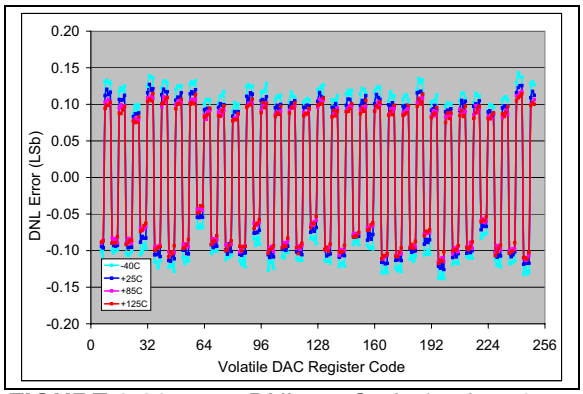


FIGURE 2-30: *DNL vs. Code (code = 6 to 250) and Temperature (**MCP4706**). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

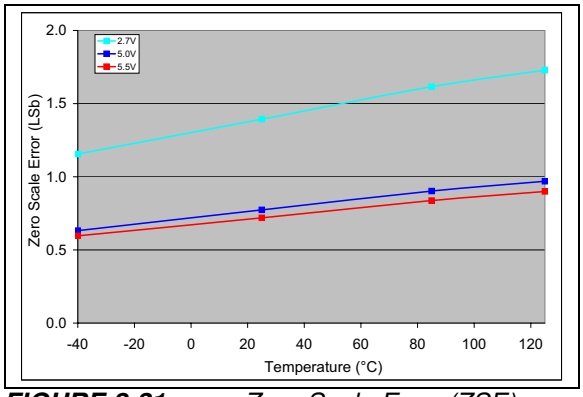


FIGURE 2-31: *Zero Scale Error (ZSE) vs. Temperature (**MCP4726**).*
V_{DD} = 5V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.

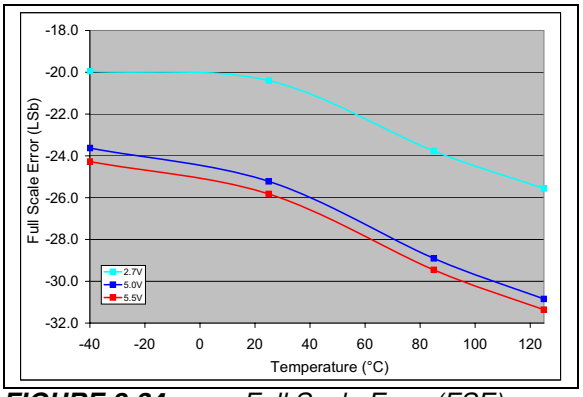


FIGURE 2-34: *Full Scale Error (FSE) vs. Temperature (**MCP4726**).*
V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.

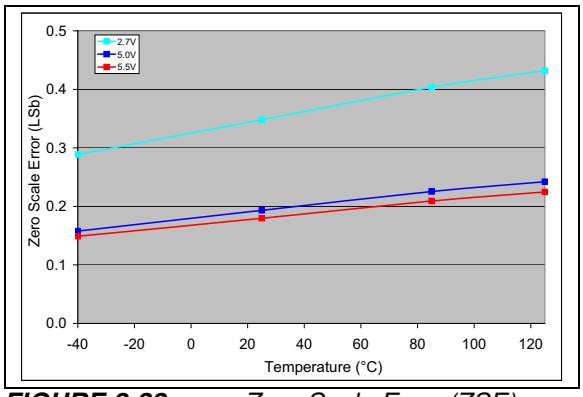


FIGURE 2-32: *Zero Scale Error (ZSE) vs. Temperature (**MCP4716**).*
V_{DD} = 5V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.

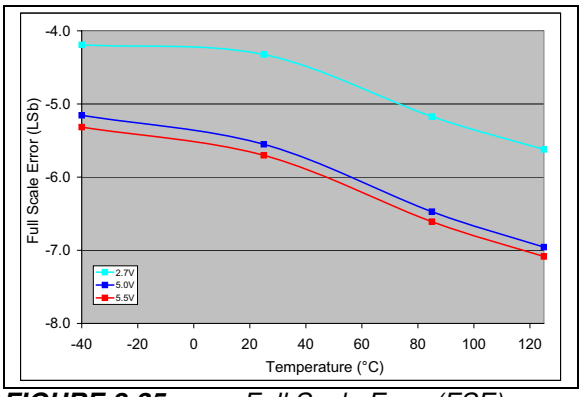


FIGURE 2-35: *Full Scale Error (FSE) vs. Temperature (**MCP4716**).*
V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.

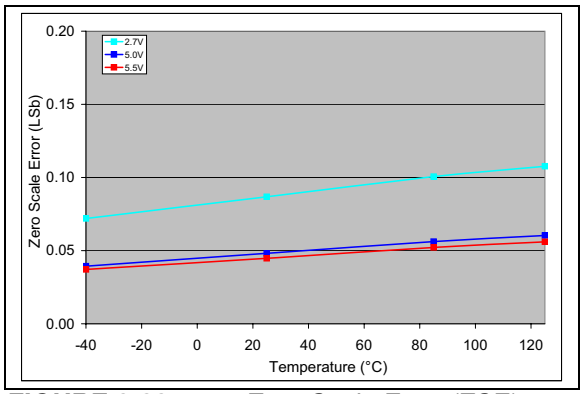


FIGURE 2-33: *Zero Scale Error (ZSE) vs. Temperature (**MCP4706**).*
V_{DD} = 5V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.

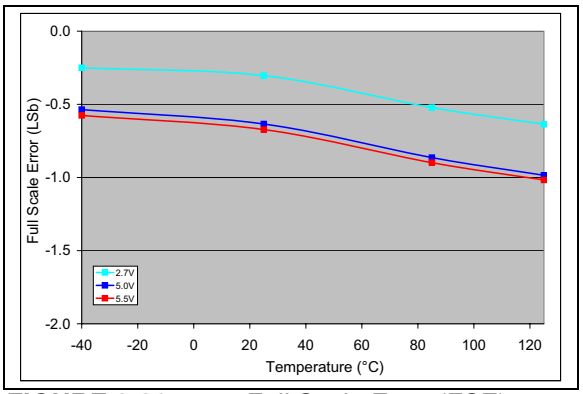


FIGURE 2-36: *Full Scale Error (FSE) vs. Temperature (**MCP4706**).*
V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

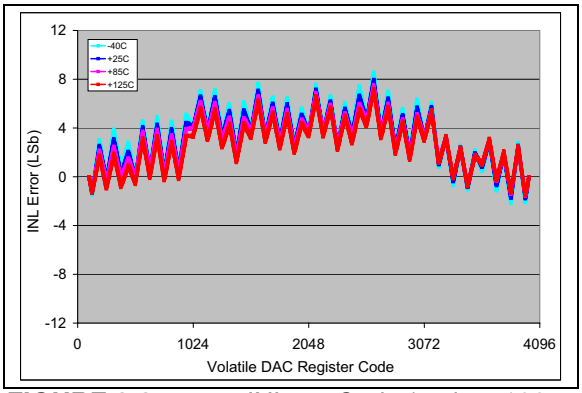


FIGURE 2-37: *INL vs. Code (code = 100 to 4000) and Temperature (**MCP4726**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.*

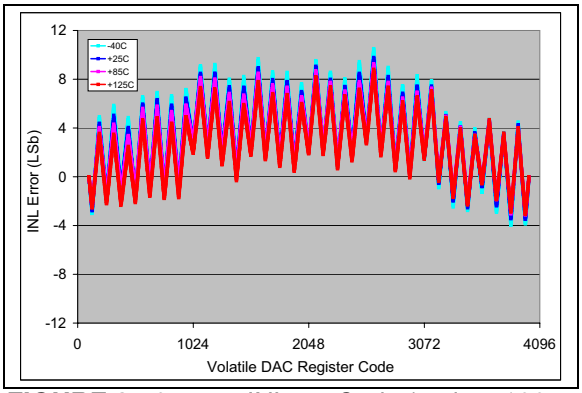


FIGURE 2-40: *INL vs. Code (code = 100 to 4000) and Temperature (**MCP4726**). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.*

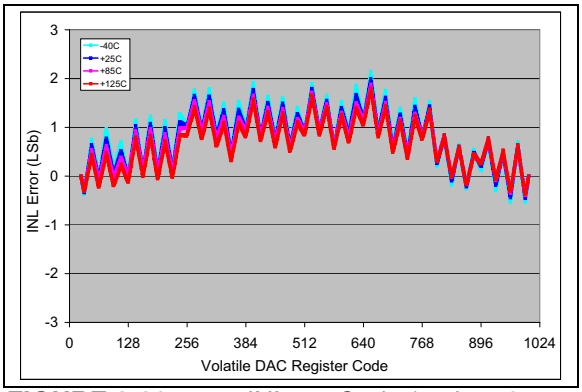


FIGURE 2-38: *INL vs. Code (code = 25 to 1000) and Temperature (**MCP4716**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.*

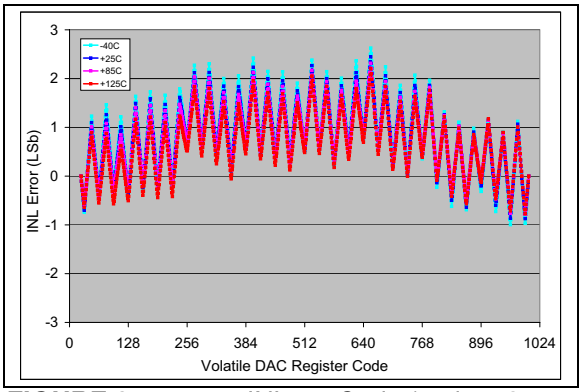


FIGURE 2-41: *INL vs. Code (code = 25 to 1000) and Temperature (**MCP4716**). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.*

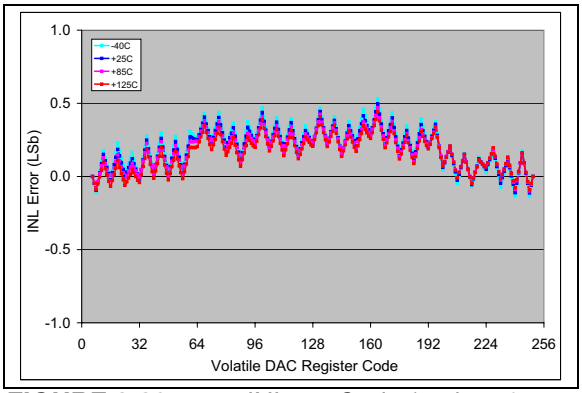


FIGURE 2-39: *INL vs. Code (code = 6 to 250) and Temperature (**MCP4706**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.*

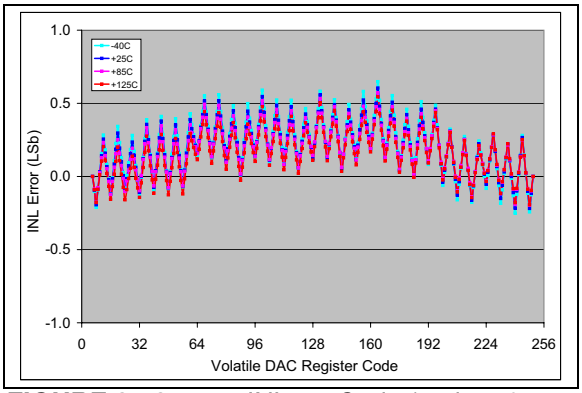


FIGURE 2-42: *INL vs. Code (code = 6 to 250) and Temperature (**MCP4706**). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

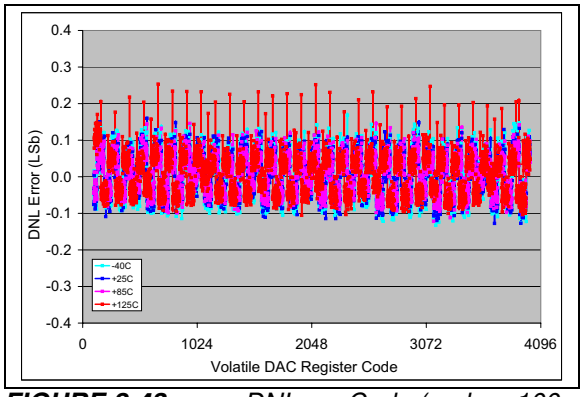


FIGURE 2-43: *DNL vs. Code (code = 100 to 4000) and Temperature (**MCP4726**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.*

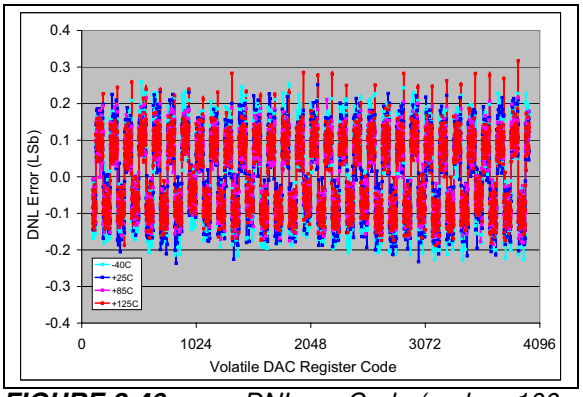


FIGURE 2-46: *DNL vs. Code (code = 100 to 4000) and Temperature (**MCP4726**). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.*

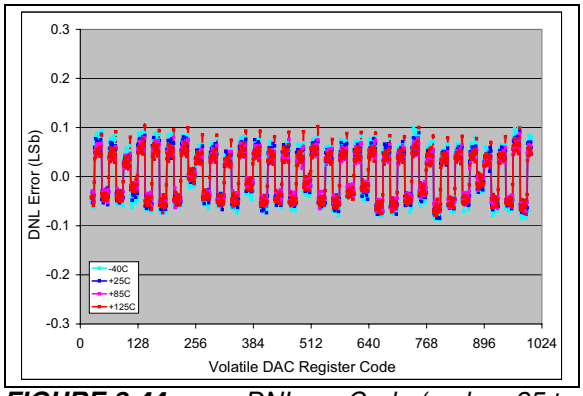


FIGURE 2-44: *DNL vs. Code (code = 25 to 1000) and Temperature (**MCP4716**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.*

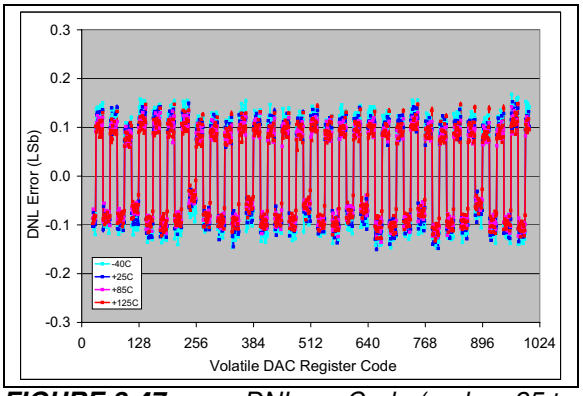


FIGURE 2-47: *DNL vs. Code (code = 25 to 1000) and Temperature (**MCP4716**). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.*

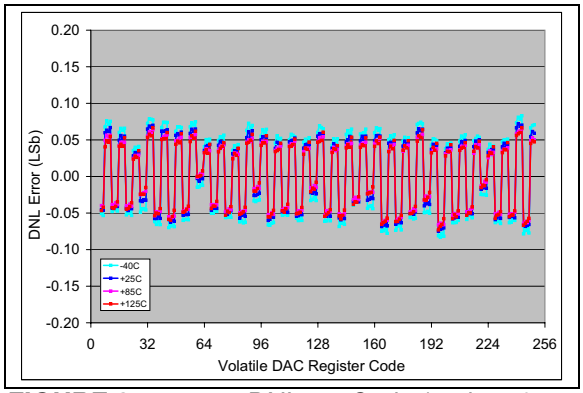


FIGURE 2-45: *DNL vs. Code (code = 6 to 250) and Temperature (**MCP4706**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.*

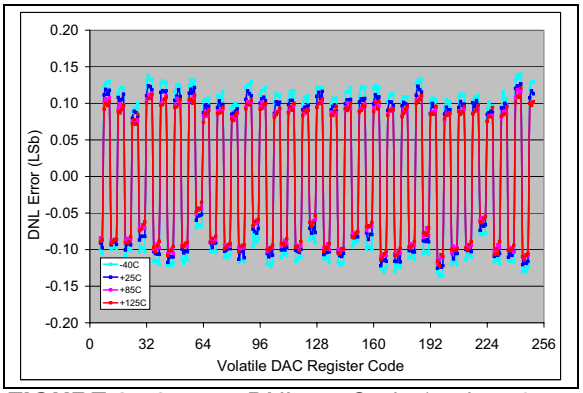


FIGURE 2-48: *DNL vs. Code (code = 6 to 250) and Temperature (**MCP4706**). V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

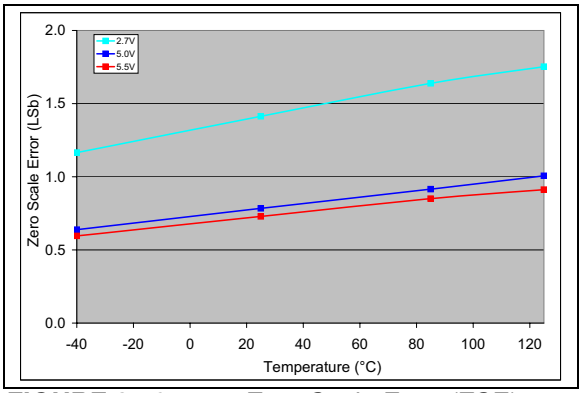


FIGURE 2-49: *Zero Scale Error (ZSE) vs. Temperature (**MCP4726**).*
V_{DD} = 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.

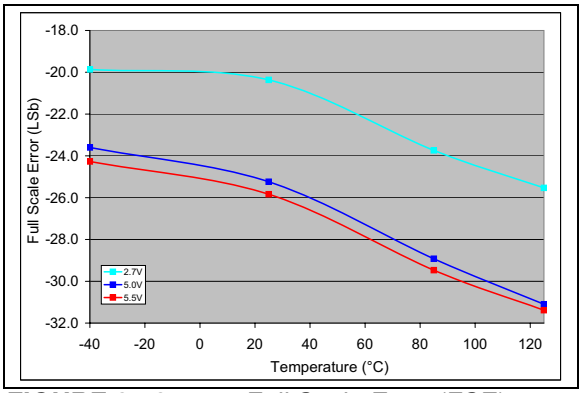


FIGURE 2-52: *Full Scale Error (FSE) vs. Temperature (**MCP4726**).*
V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.

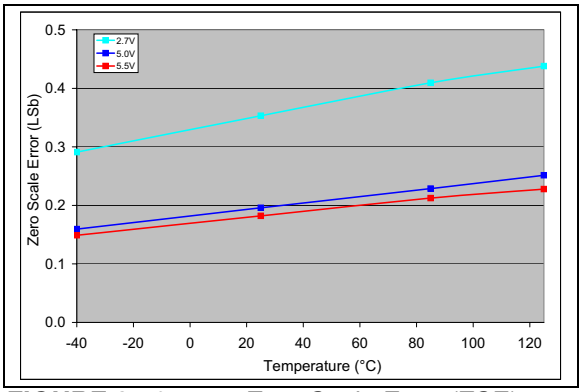


FIGURE 2-50: *Zero Scale Error (ZSE) vs. Temperature (**MCP4716**).*
V_{DD} = 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.

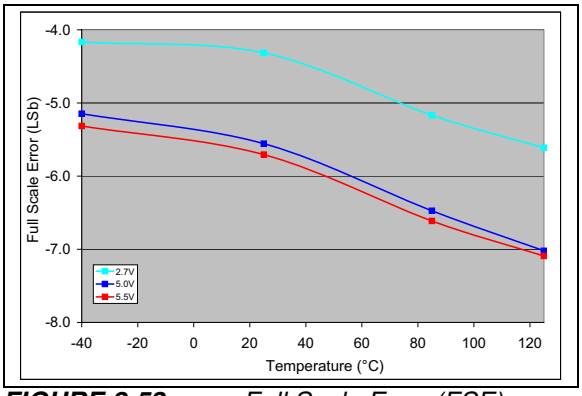


FIGURE 2-53: *Full Scale Error (FSE) vs. Temperature (**MCP4716**).*
V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.

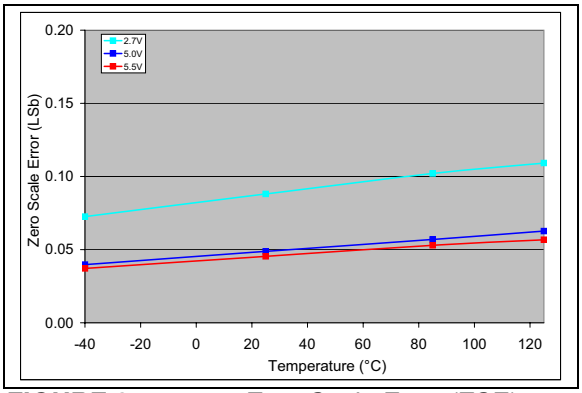


FIGURE 2-51: *Zero Scale Error (ZSE) vs. Temperature (**MCP4706**).*
V_{DD} = 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.

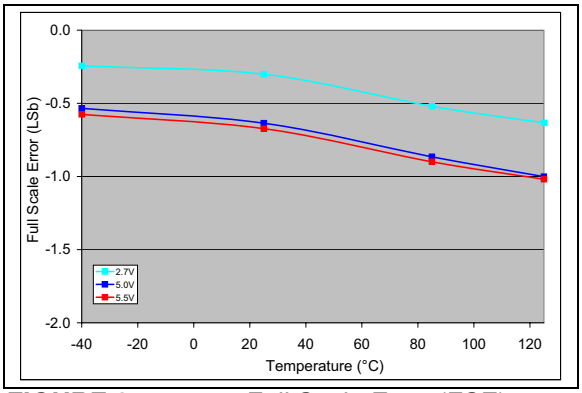


FIGURE 2-54: *Full Scale Error (FSE) vs. Temperature (**MCP4706**).*
V_{DD} = 2.7V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

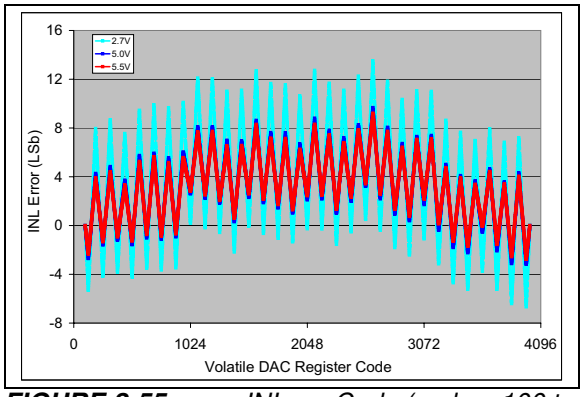


FIGURE 2-55: *INL vs. Code (code = 100 to 4000) and V_{DD} (2.7V, 5V, 5.5V) (**MCP4726**). V_{REF1}:V_{REF0} = '10', G = '1', V_{REF} = V_{DD}/2, Temp = +25°C.*

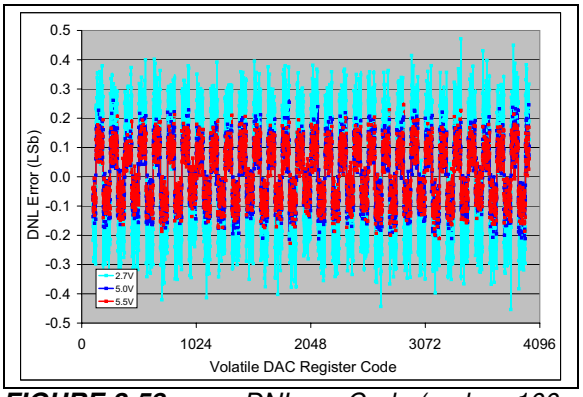


FIGURE 2-58: *DNL vs. Code (code = 100 to 4000) and V_{DD} (2.7V, 5V, 5.5V) (**MCP4726**). V_{REF1}:V_{REF0} = '10', G = '1', V_{REF} = V_{DD}/2, Temp = +25°C.*

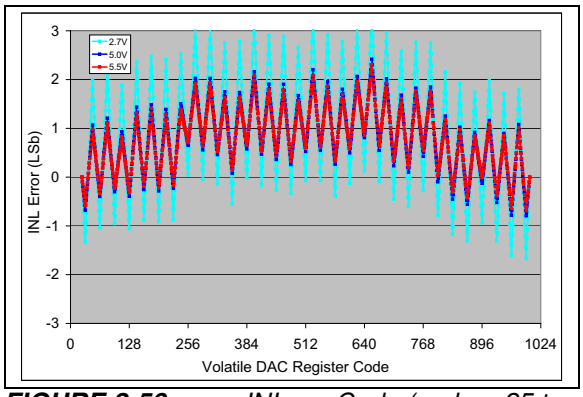


FIGURE 2-56: *INL vs. Code (code = 25 to 1000) and V_{DD} (2.7V, 5V, 5.5V) (**MCP4716**). V_{REF1}:V_{REF0} = '10', G = '1', V_{REF} = V_{DD}/2, Temp = +25°C.*

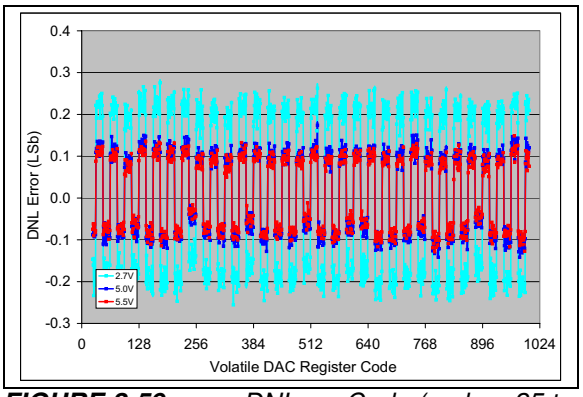


FIGURE 2-59: *DNL vs. Code (code = 25 to 1000) and V_{DD} (2.7V, 5V, 5.5V) (**MCP4716**). V_{REF1}:V_{REF0} = '10', G = '1', V_{REF} = V_{DD}/2, Temp = +25°C.*

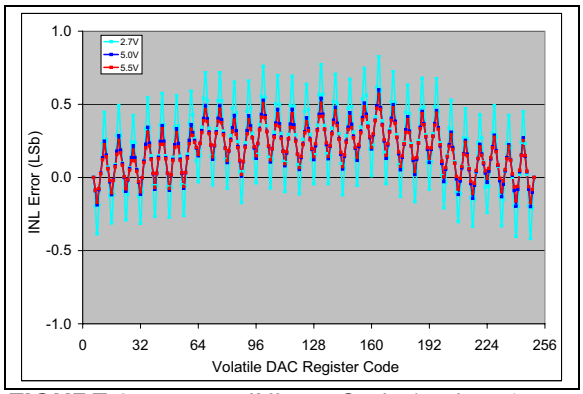


FIGURE 2-57: *INL vs. Code (code = 6 to 250) and V_{DD} (2.7V, 5V, 5.5V) (**MCP4706**). V_{REF1}:V_{REF0} = '10', G = '1', V_{REF} = V_{DD}/2, Temp = +25°C.*

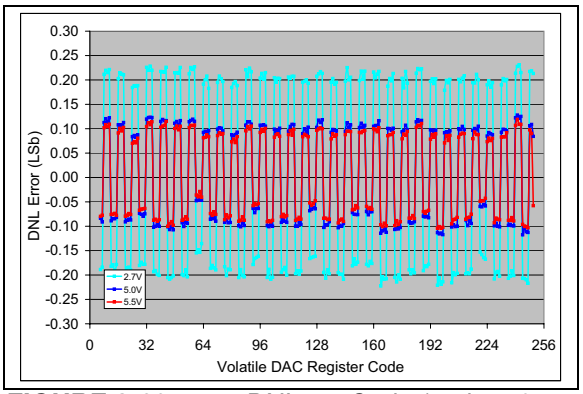


FIGURE 2-60: *DNL vs. Code (code = 6 to 250) and V_{DD} (2.7V, 5V, 5.5V) (**MCP4706**). V_{REF1}:V_{REF0} = '10', G = '1', V_{REF} = V_{DD}/2, Temp = +25°C.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

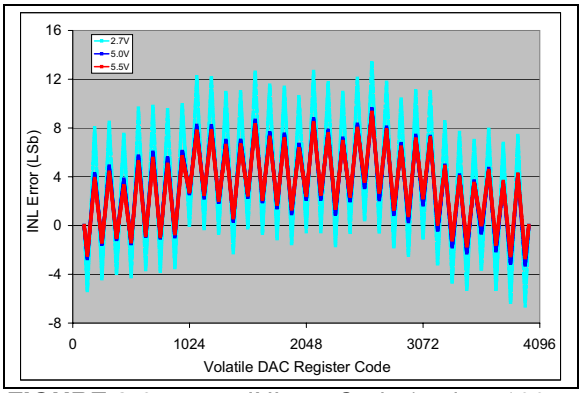


FIGURE 2-61: *INL vs. Code (code = 100 to 4000) and V_{DD} (2.7V, 5V, 5.5V) (**MCP4726**). V_{REF1}:V_{REF0} = '11', G = '1', V_{REF} = V_{DD}/2, Temp = +25°C.*

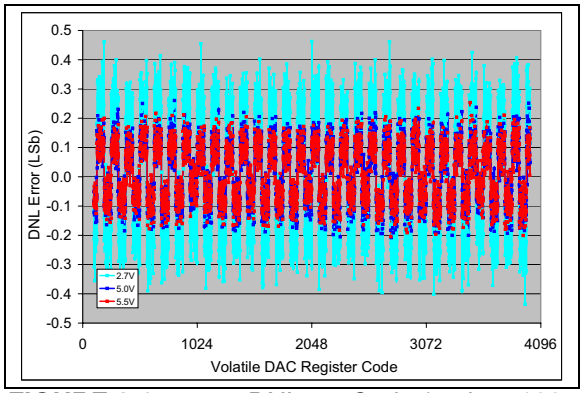


FIGURE 2-64: *DNL vs. Code (code = 100 to 4000) and V_{DD} (2.7V, 5V, 5.5V) (**MCP4726**). V_{REF1}:V_{REF0} = '11', G = '1', V_{REF} = V_{DD}/2, Temp = +25°C.*

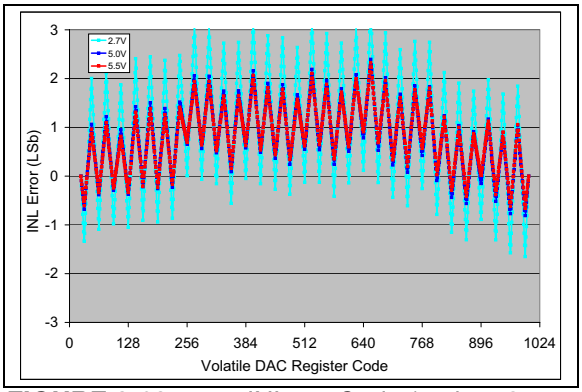


FIGURE 2-62: *INL vs. Code (code = 25 to 1000) and V_{DD} (2.7V, 5V, 5.5V) (MCP4716). V_{REF1}:V_{REF0} = '11', G = '1', V_{REF} = V_{DD}/2, Temp = +25°C.*

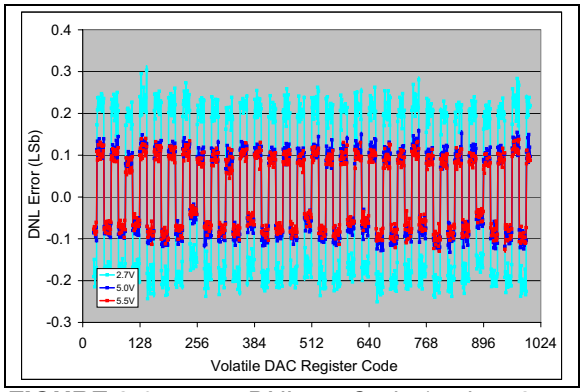


FIGURE 2-65: *DNL vs. Code (code = 25 to 1000) and V_{DD} (2.7V, 5V, 5.5V) (MCP4716). V_{REF1}:V_{REF0} = '11', G = '1', V_{REF} = V_{DD}/2, Temp = +25°C.*

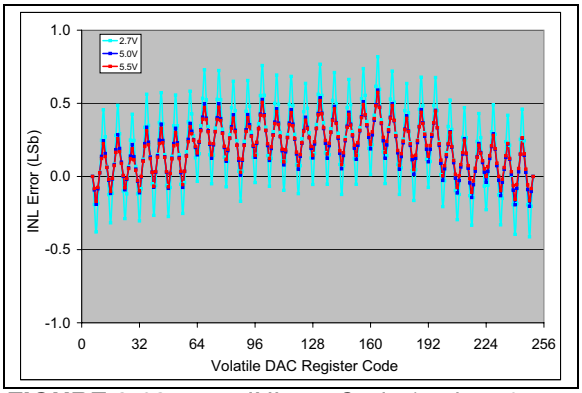


FIGURE 2-63: *INL vs. Code (code = 6 to 250) and V_{DD} (2.7V, 5V, 5.5V) (MCP4706). V_{REF1}:V_{REF0} = '11', G = '1', V_{REF} = V_{DD}/2, Temp = +25°C.*

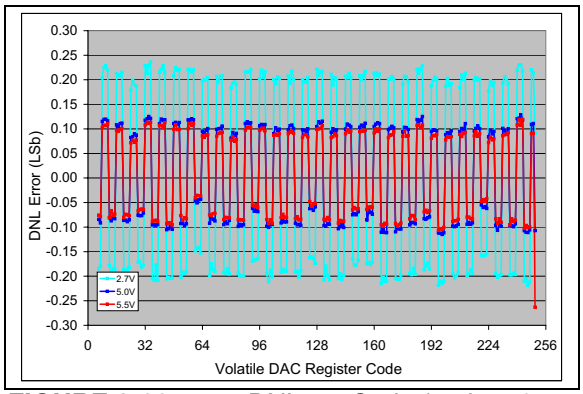


FIGURE 2-66: *DNL vs. Code (code = 6 to 250) and V_{DD} (2.7V, 5V, 5.5V) (MCP4706). V_{REF1}:V_{REF0} = '11', G = '1', V_{REF} = V_{DD}/2, Temp = +25°C.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

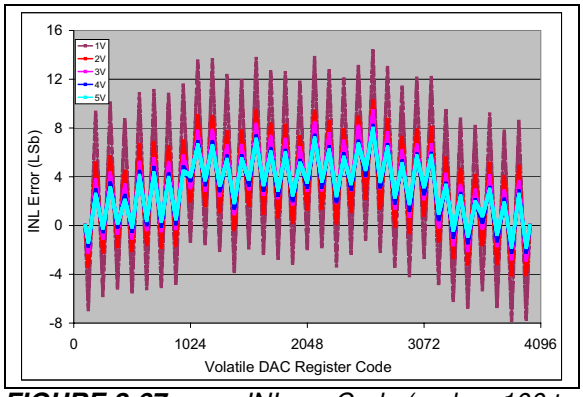


FIGURE 2-67: *INL vs. Code (code = 100 to 4000) and V_{REF} (**MCP4726**).*
V_{DD} = 5V, V_{REF1}:V_{REF0} = '10', G = '0',
V_{REF} = 1V, 2V, 3V, 4V, and 5V, Temp = +25°C.

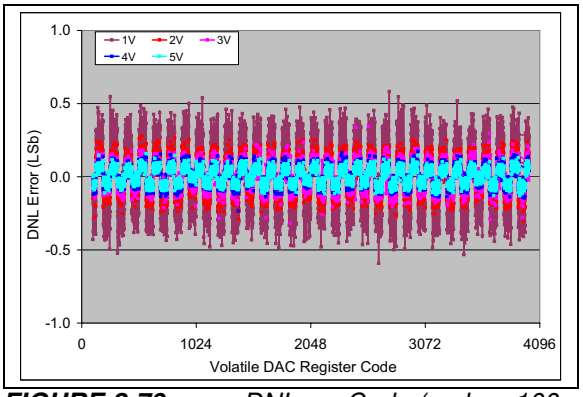


FIGURE 2-70: *DNL vs. Code (code = 100 to 4000) and V_{REF} (**MCP4726**).*
V_{DD} = 5V, V_{REF1}:V_{REF0} = '10', G = '0',
V_{REF} = 1V, 2V, 3V, 4V, and 5V, Temp = +25°C.

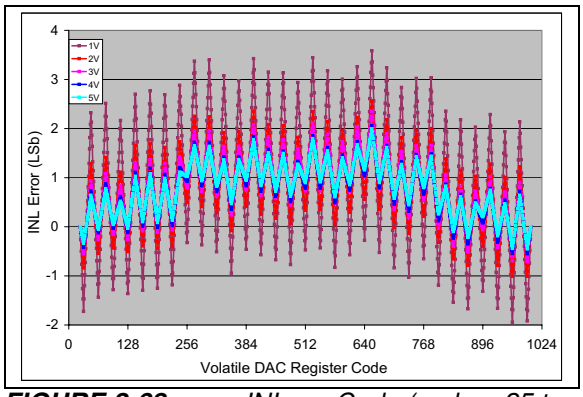


FIGURE 2-68: *INL vs. Code (code = 25 to 1000) and V_{REF} (**MCP4716**).*
V_{DD} = 5V, V_{REF1}:V_{REF0} = '10', G = '0',
V_{REF} = 1V, 2V, 3V, 4V, and 5V, Temp = +25°C.

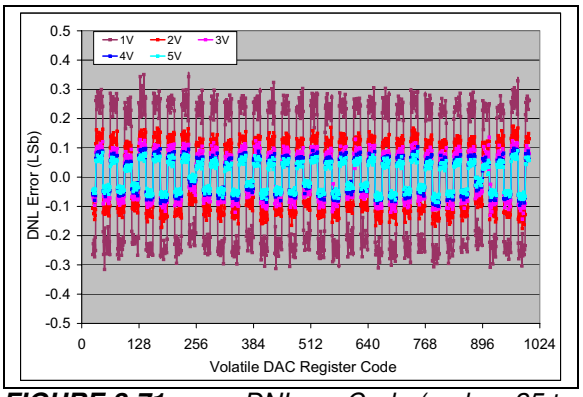


FIGURE 2-71: *DNL vs. Code (code = 25 to 1000) and V_{REF} (**MCP4716**).*
V_{DD} = 5V, V_{REF1}:V_{REF0} = '10', G = '0',
V_{REF} = 1V, 2V, 3V, 4V, and 5V, Temp = +25°C.

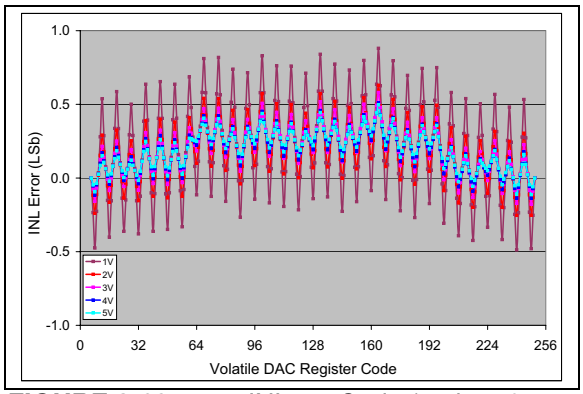


FIGURE 2-69: *INL vs. Code (code = 6 to 250) and V_{REF} (**MCP4706**).*
V_{DD} = 5V, V_{REF1}:V_{REF0} = '10', G = '0',
V_{REF} = 1V, 2V, 3V, 4V, and 5V, Temp = +25°C.

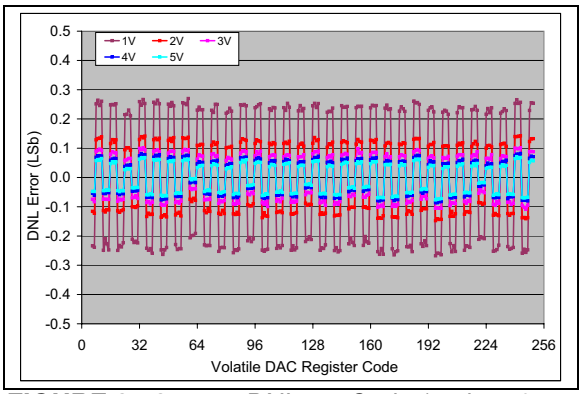


FIGURE 2-72: *DNL vs. Code (code = 6 to 250) and V_{REF} (**MCP4706**).*
V_{DD} = 5V, V_{REF1}:V_{REF0} = '10', G = '0',
V_{REF} = 1V, 2V, 3V, 4V, and 5V, Temp = +25°C.

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

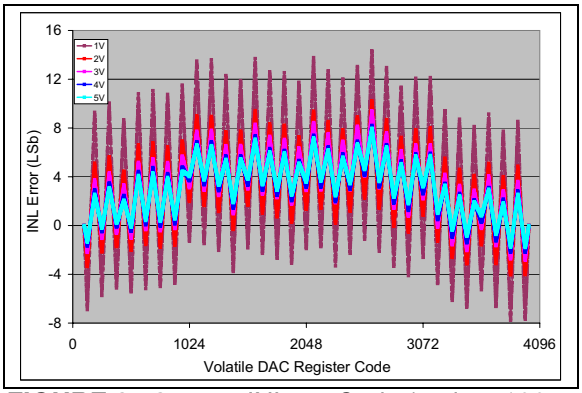


FIGURE 2-73: *INL vs. Code (code = 100 to 4000) and V_{REF} (**MCP4726**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = 1V, 2V, 3V, 4V, and 5V, Temp = +25°C.*

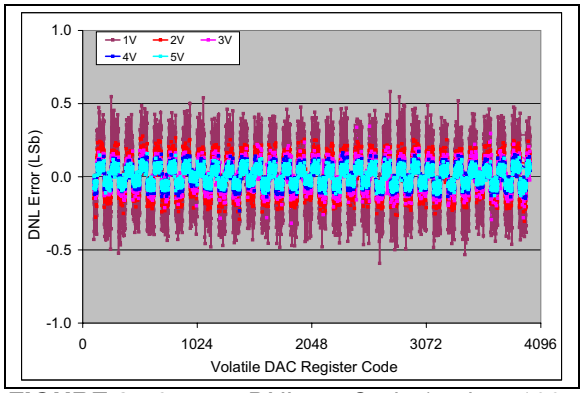


FIGURE 2-76: *DNL vs. Code (code = 100 to 4000) and V_{REF} (**MCP4726**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = 1V, 2V, 3V, 4V, and 5V, Temp = +25°C.*

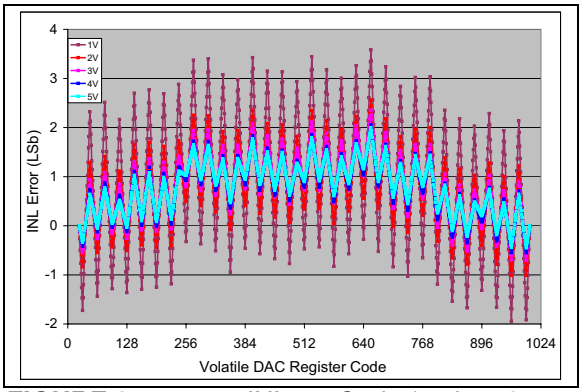


FIGURE 2-74: *INL vs. Code (code = 25 to 1000) and V_{REF} (**MCP4716**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = 1V, 2V, 3V, 4V, and 5V, Temp = +25°C.*

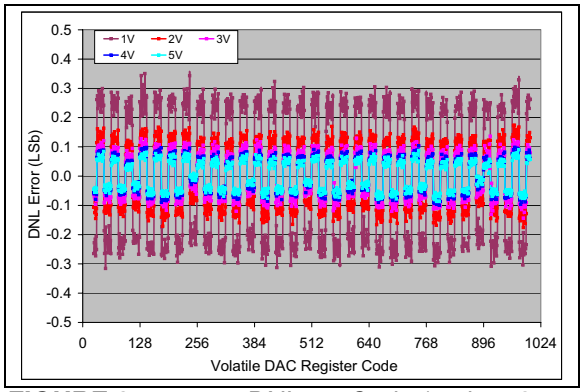


FIGURE 2-77: *DNL vs. Code (code = 25 to 1000) and V_{REF} (**MCP4716**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = 1V, 2V, 3V, 4V, and 5V, Temp = +25°C.*

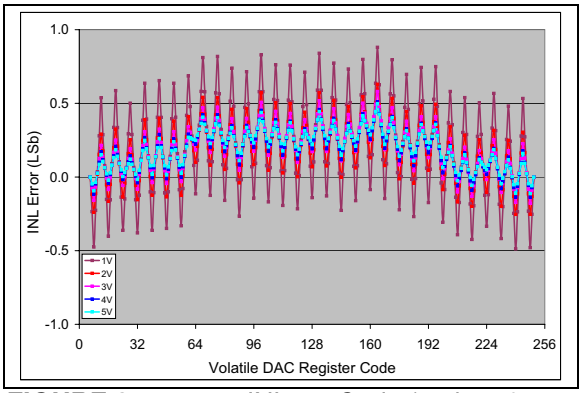


FIGURE 2-75: *INL vs. Code (code = 6 to 250) and V_{REF} (**MCP4706**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = 1V, 2V, 3V, 4V, and 5V, Temp = +25°C.*

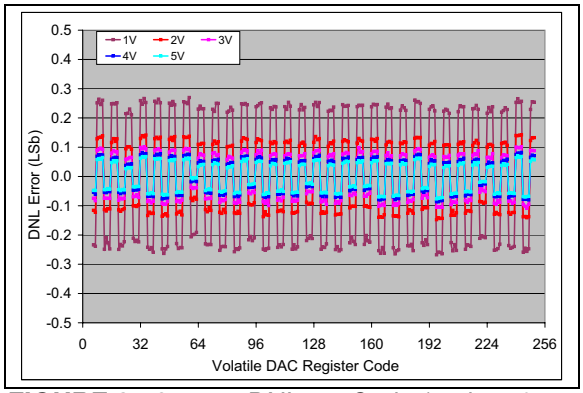


FIGURE 2-78: *DNL vs. Code (code = 6 to 250) and V_{REF} (**MCP4706**). V_{DD} = 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = 1V, 2V, 3V, 4V, and 5V, Temp = +25°C.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

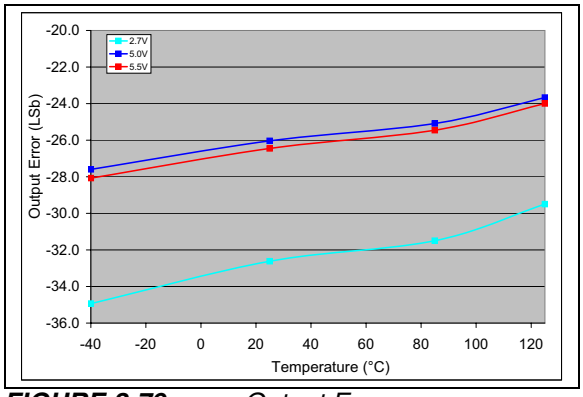


FIGURE 2-79: *Output Error vs. Temperature (**MCP4726**). V_{DD} = 2.7V and 5V, V_{REF1}:V_{REF0} = '00', Code = 4000.*

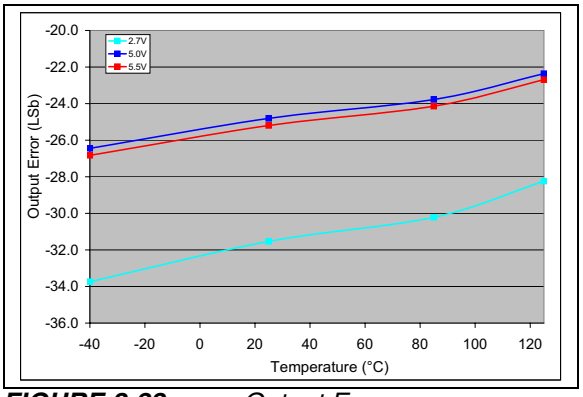


FIGURE 2-82: *Output Error vs. Temperature (**MCP4726**). V_{DD} = 2.7V and 5V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}, Code = 4000.*

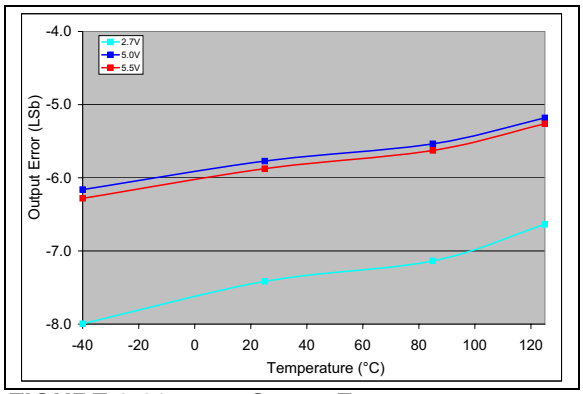


FIGURE 2-80: *Output Error vs. Temperature (MCP4716). V_{DD} = 2.7V and 5V, V_{REF1}:V_{REF0} = '00', Code = 1000.*

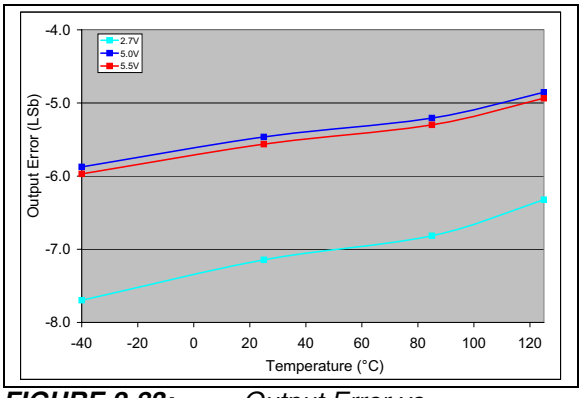


FIGURE 2-83: *Output Error vs. Temperature (MCP4716). V_{DD} = 2.7V and 5V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}, Code = 1000.*

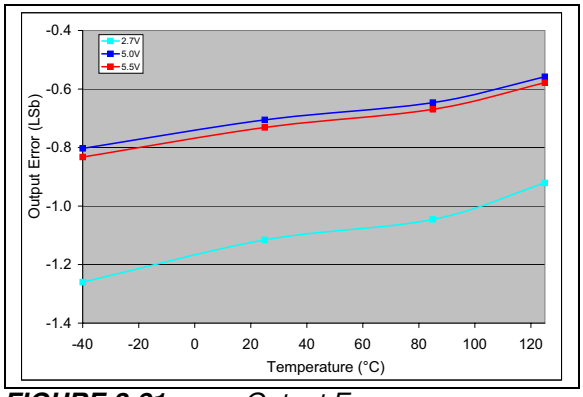


FIGURE 2-81: *Output Error vs. Temperature (MCP4706). V_{DD} = 2.7V and 5V, V_{REF1}:V_{REF0} = '00', Code = 250.*

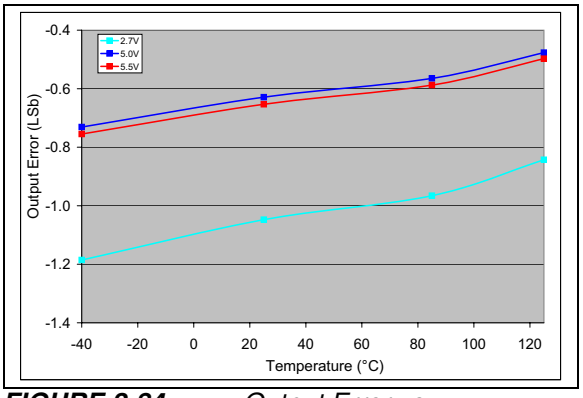


FIGURE 2-84: *Output Error vs. Temperature (MCP4706). V_{DD} = 2.7V and 5V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}, Code = 250.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

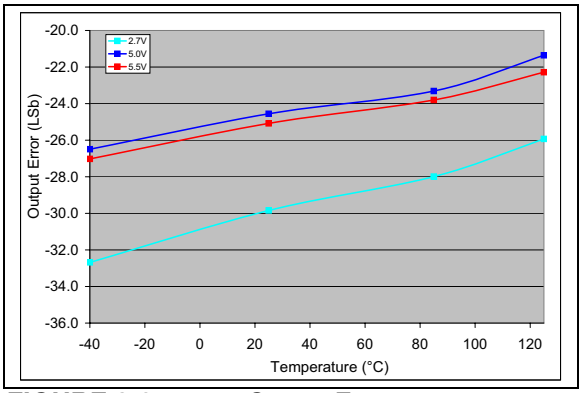


FIGURE 2-85: *Output Error vs. Temperature (**MCP4726**). V_{DD} = 2.7V and 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}, Code = 4000.*

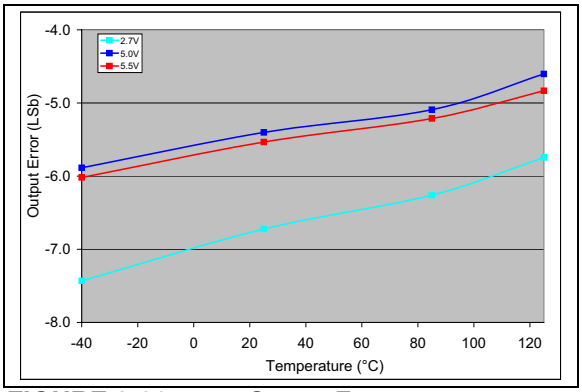


FIGURE 2-86: *Output Error vs. Temperature (**MCP4716**). V_{DD} = 2.7V and 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}, Code = 1000.*

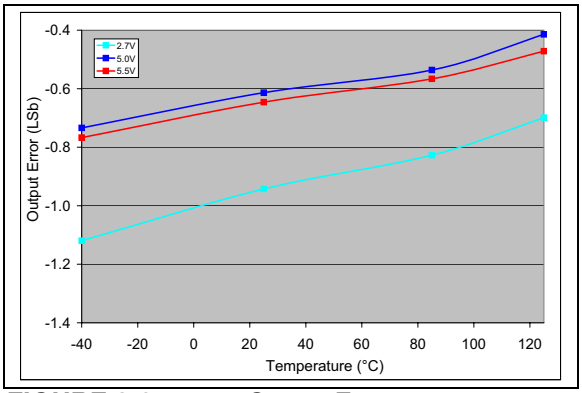


FIGURE 2-87: *Output Error vs. Temperature (**MCP4706**). V_{DD} = 2.7V and 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}, Code = 250.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

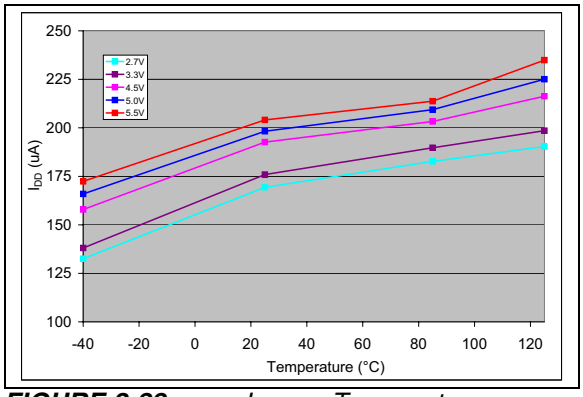


FIGURE 2-88: *I_{DD} vs. Temperature. V_{DD} = 2.7V and 5V, V_{REF1}:V_{REF0} = '00'.*

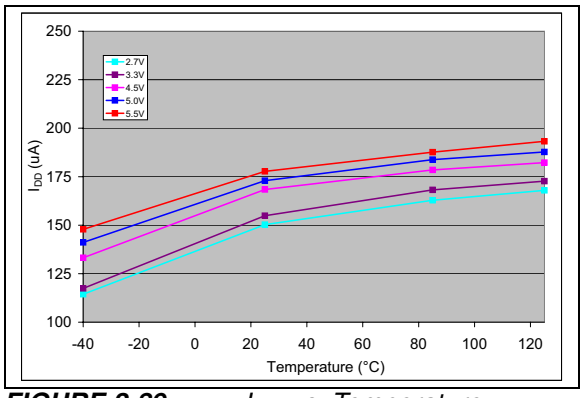


FIGURE 2-89: *I_{DD} vs. Temperature. V_{DD} = 2.7V and 5V, V_{REF1}:V_{REF0} = '10', G = '0', V_{REF} = V_{DD}.*

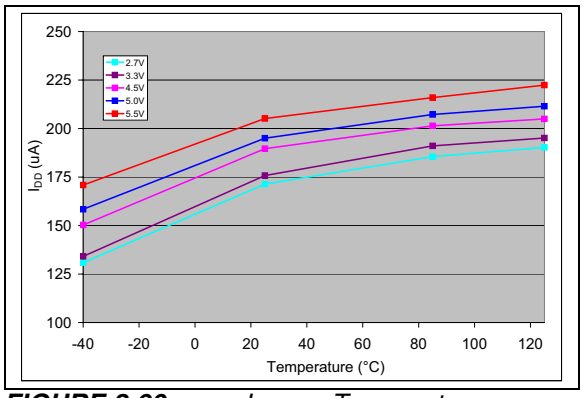


FIGURE 2-90: *I_{DD} vs. Temperature. V_{DD} = 2.7V and 5V, V_{REF1}:V_{REF0} = '11', G = '0', V_{REF} = V_{DD}.*

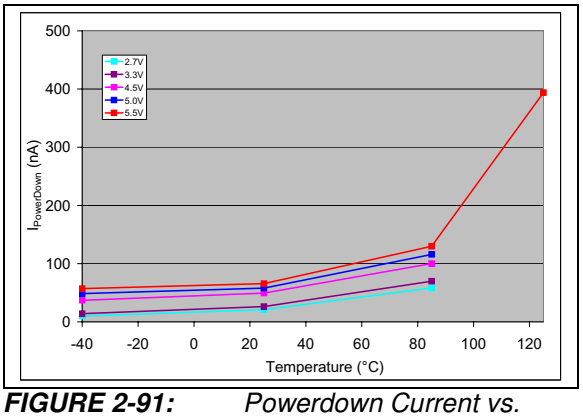


FIGURE 2-91: *Powerdown Current vs. Temperature. V_{DD} = 2.7V, 3.3V, 4.5V, 5.0V and 5.5V, PD1:PD0 = '11'.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{RL} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.

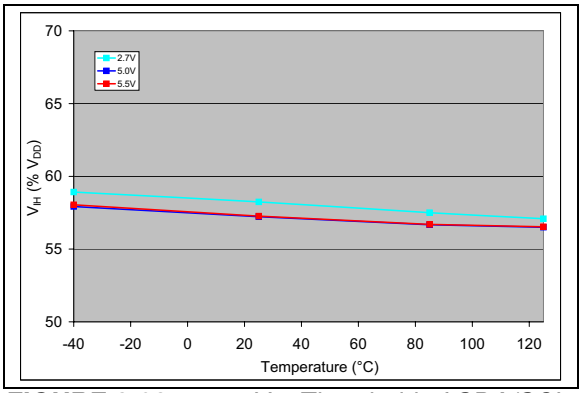


FIGURE 2-92: *V_{IH} Threshold of SDA/SCL Inputs vs. Temperature and V_{DD}.*

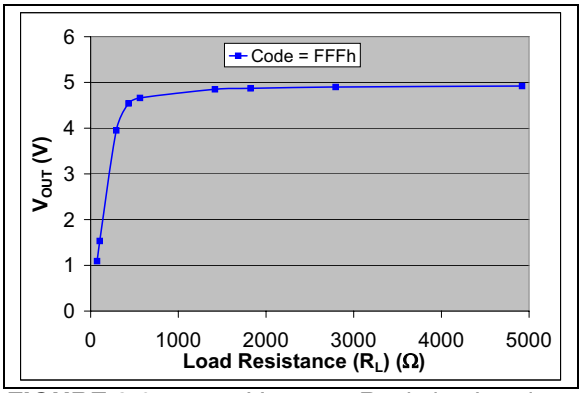


FIGURE 2-94: *V_{OUT} vs. Resistive Load. V_{DD} = 5.0V.*

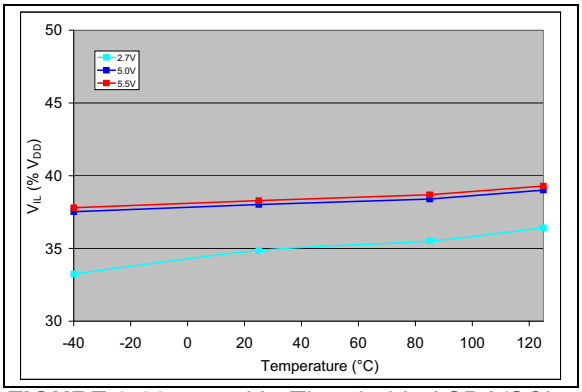


FIGURE 2-93: *V_{IL} Threshold of SDA/SCL Inputs vs. Temperature and V_{DD}.*

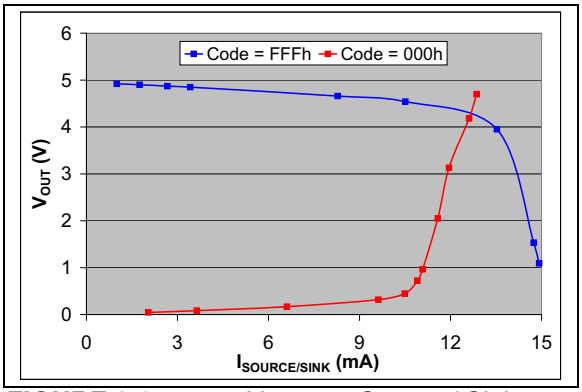


FIGURE 2-95: *V_{OUT} vs. Source / Sink Current. V_{DD} = 5.0V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = Internal, Gain = x1, R_L = 5 kΩ, C_L = 100 pF.



FIGURE 2-96: *Full-Scale Settling Time (000h to FFFh) (**MCP4726**).*

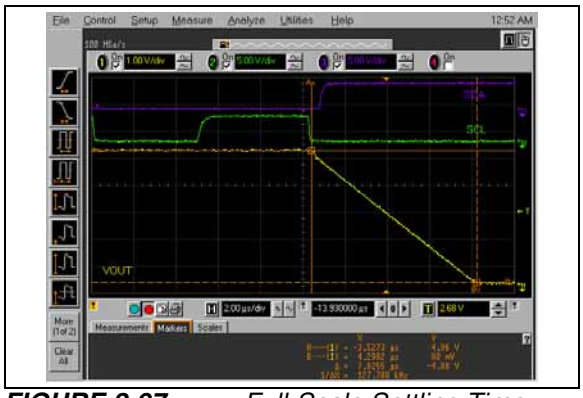


FIGURE 2-97: *Full-Scale Settling Time (FFFh to 000h) (**MCP4726**).*

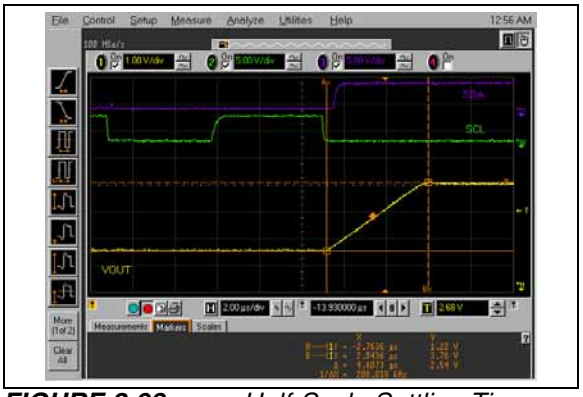


FIGURE 2-98: *Half-Scale Settling Time (400h to C00h) (**MCP4726**).*



FIGURE 2-99: *Half-Scale Settling Time (C00h to 400h) (**MCP4726**).*



FIGURE 2-100: *Exiting Power Down Mode (MCP4726, Volatile DAC Register = FFFh).*

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3.0 PIN DESCRIPTIONS

An overview of the pin functions are described in **Section 3.1** through **Section 3.7**. The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: MCP47X6 PINOUT DESCRIPTION

Pin		Symbol	I/O	Buffer Type	Standard Function
SOT-23 6L	DFN 6L				
1	6	V_{OUT}	A	Analog	Buffered analog voltage output pin
2	5	V_{SS}	—	P	Ground reference pin for all circuitries on the device
3	4	V_{DD}	—	P	Supply Voltage Pin
4	3	SDA	I/O	ST	I^2C Serial Data Pin
5	2	SCL	I	ST	I^2C Serial Clock Pin
6	1	V_{REF}	A	Analog	Voltage Reference Input Pin
—	7	EP	—	—	Exposed Pad Note 1

Legend: A = Analog pins
O = Digital output
P = Power
I = Digital input (high Z)
I/O = Input / Output

Note 1: The DFN package has a contact on the bottom of the package. This contact is conductively connected to the die substrate, and therefore should be unconnected or connected to the same ground as the device's V_{SS} pin.

3.1 Analog Output Voltage Pin (V_{OUT})

V_{OUT} is the DAC analog output pin. The DAC output has an output amplifier. V_{OUT} can swing from approximately 0V to approximately V_{DD}. The full-scale range of the DAC output is from V_{SS} to G * V_{RL}, where G is the gain selection option (1x or 2x).

In normal mode, the DC impedance of the output pin is about 1Ω. In Power-Down mode, the output pin is internally connected to a known pull-down resistor of 1 kΩ, 125 kΩ, or 640 kΩ. The Power-Down selection bits settings are shown Table 4-2.

3.2 Positive Power Supply Input (V_{DD})

V_{DD} is the positive supply voltage input pin. The input supply voltage is relative to V_{SS}.

The power supply at the V_{DD} pin should be as clean as possible for a good DAC performance. It is recommended to use an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate high-frequency noise present in application boards.

3.3 Ground (V_{SS})

The V_{SS} pin is the device ground reference.

The user must connect the V_{SS} pin to a ground plane through a low-impedance connection. If an analog ground path is available in the application PCB (printed circuit board), it is highly recommended that the V_{SS} pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.4 Serial Data Pin (SDA)

SDA is the serial data pin of the I^2C interface. The SDA pin is used to write or read the DAC registers and configuration bits. The SDA pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V_{DD} line to the SDA pin. Except for start and stop conditions, the data on the SDA pin must be stable during the high period of the clock. The high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. Refer to **Section 5.0 "I^2C Serial Interface"** for more details of I^2C Serial Interface communication.

3.5 Serial Clock Pin (SCL)

SCL is the serial clock pin of the I^2C interface. The MCP47X6 devices act only as a slave and the SCL pin accepts only external serial clocks. The input data from the Master device is shifted into the SDA pin on the rising edges of the SCL clock and output from the device occurs at the falling edges of the SCL clock. The SCL pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V_{DD} line to the SCL pin. Refer to **Section 5.0 "I^2C Serial Interface"** for more details of I^2C Serial Interface communication.

3.6 Voltage Reference Pin (V_{REF})

This pin is used for the external voltage reference input. The user can select V_{DD} voltage or the V_{REF} pin voltage as the reference resistor ladder's voltage reference.

When the V_{REF} pin signal is selected, there is an option for this voltage to be buffered or unbuffered. This is offered in cases where the reference voltage does not have the current capability not to drop its voltage when connected to the internal resistor ladder circuit.

When the V_{DD} is selected as reference voltage, this pin is disconnected from the internal circuit.

See **Section 4.2 "DAC's (Resistor Ladder) Reference Voltage"** and Table 4-4 for more details on the configuration bits.

3.7 Exposed Pad (EP)

This pad is conductively connected to the device's substrate. This pad should be tied to the same potential as the V_{SS} pin (or left unconnected). This pad could be used to assist as a heat sink for the device when connected to a PCB heat sink.

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4.0 GENERAL DESCRIPTION

The MCP4706, MCP4716, and MCP4726 devices are single channel voltage output 8-bit, 10-bit, and 12-bit DAC devices with nonvolatile memory (EEPROM) and an I^2C serial interface. This family will be referred to as MCP47X6.

The devices use a resistor ladder architecture. The resistor ladder DAC is driven from a software selectable voltage reference source. The source can be either the device's internal V_{DD} or the external V_{REF} pin voltage.

The DAC output is buffered with a low power and precision output amplifier (op amp). This output amplifier provides a rail-to-rail output with low offset voltage and low noise. The gain of the output buffer is software configurable.

This device also has user programmable nonvolatile memory (EEPROM), which allows the user to save the desired POR/BOR value of the DAC register and device configuration bits.

The devices use a two-wire I^2C serial communication interface and operate with a single supply voltage from 2.7V to 5.5V.

4.1 Power-On-Reset / Brown Out Reset (POR/BOR)

The internal Power-On-Reset (POR) / Brown-Out Reset (BOR) circuit monitors the power supply voltage (V_{DD}) during operation. This circuit ensures correct device start-up at system power-up and power-down events. V_{RAM} is the RAM retention voltage and is always lower than the POR trip point voltage.

POR occurs as the voltage is rising (typically from 0V), while BOR occurs as the voltage is falling (typically from $V_{DD(MIN)}$ or higher).

When the rising V_{DD} voltage crosses the V_{POR} trip point, the following occurs:

- Nonvolatile DAC Register value latched into volatile DAC Register
- Nonvolatile configuration bit values latched into volatile configuration bits
- POR status bit is set ("1")
- The reset delay timer starts; when timer times out (t_{PORD}), the I^2C interface is operational.

The analog output (V_{OUT}) state will be determined by the state of the volatile configuration bits and the DAC Register. This is called a POR reset (event).

When the falling V_{DD} voltage crosses the V_{POR} trip point, the following occurs:

- Device is forced into a power down state (PD1:PD0 = '11'). Analog circuitry is turned off.
- Volatile DAC Register is forced to 000h
- Volatile configuration bits V_{REF1}, V_{REF0} and G are forced to '0'

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

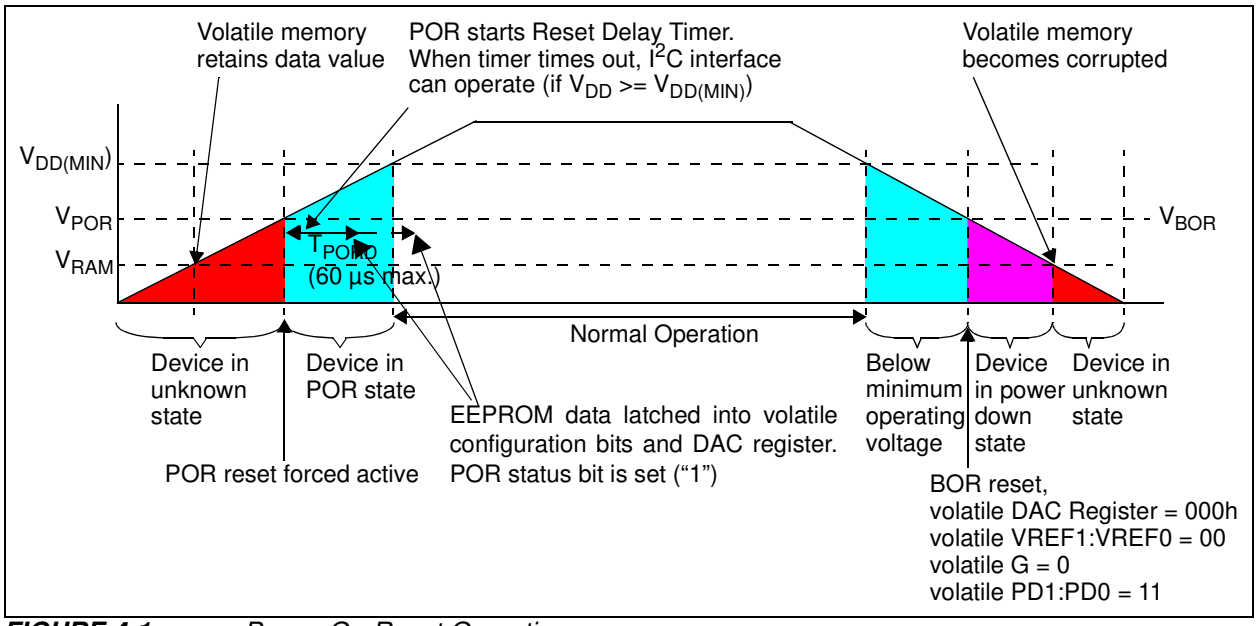


FIGURE 4-1: *Power-On-Reset Operation.*

4.2 DAC's (Resistor Ladder) Reference Voltage

The device can be configured to use one of three voltage sources for the resistor ladder's reference voltage (V_{RL}) (see Figure 4-2). These are:

1. V_{DD} pin voltage
2. V_{REF} pin voltage internally buffered
3. V_{REF} pin voltage unbuffered

The selection of the voltage is specified with the volatile V_{REF1}:V_{REF0} configuration bits (see Table 4-4). There are nonvolatile and volatile V_{REF1}:V_{REF0} configuration bits. On a POR/BOR event, the state of the nonvolatile V_{REF1}:V_{REF0} configuration bits are latched into the volatile V_{REF1}:V_{REF0} configuration bits.

When the user selects the V_{DD} as reference, the V_{REF} pin voltage is not connected to the resistor ladder.

If the V_{REF} pin is selected, then one needs to select between the buffered or unbuffered mode.

In unbuffered mode, the V_{REF} pin voltage may be from V_{SS} to V_{DD}.

Note:	In unbuffered mode, the voltage source should have a low output impedance. If the voltage source has a high output impedance, then the voltage on the V_{REF}'s pin would be lower than expected. The resistor ladder has a typical impedance of 210 kΩ and a typical capacitance of 29 pF.

In buffered mode, the V_{REF} pin voltage may be from 0.01V to V_{DD}-0.04V. The input buffer (amplifier) provides low offset voltage, low noise, and a very high input impedance, with only minor limitations on the input range and frequency response.

Note:	Any variation or noises on the reference source can directly affect the DAC output. The reference voltage needs to be as clean as possible for accurate DAC performance.

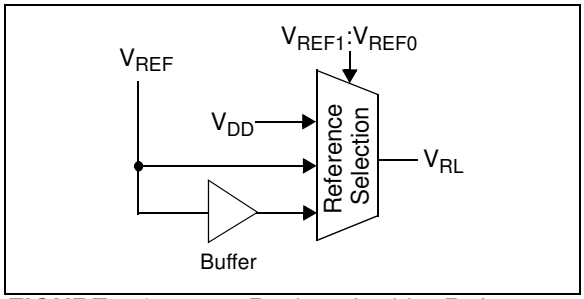


FIGURE 4-2: *Resistor Ladder Reference Voltage Selection Block Diagram.*

4.3 Resistor Ladder

The resistor ladder is a digital potentiometer with the B Terminal internally grounded and the A terminal connected to the selected reference voltage (see Figure 4-3). The volatile DAC register controls the wiper position. The wiper voltage (V_W) is proportional to the DAC register value divided by the number of resistor elements (R_S) in the ladder (256, 1024, or 4096) related to the V_{RL} voltage.

Note:	The maximum wiper position is 2^n - 1, while the number of resistors in the resistor ladder is 2^n. This means that when the DAC register is at full scale, there is one resistor element (R_S) between the wiper and the V_{RL} voltage.

The resistor ladder (R_{RL}) has a typical impedance of approximately 210 kΩ. This resistor ladder resistance (R_{RL}) may vary from device to device up to ±20%. Since this is a voltage divider configuration, the actual R_{RL} resistance does not effect the output given a fixed voltage at V_{RL}.

If the unbuffered V_{REF} pin is used as the V_{RL} voltage source, this voltage source should have a low output impedance.

When the DAC is powered down, the resistor ladder is disconnected from the selected reference voltage.

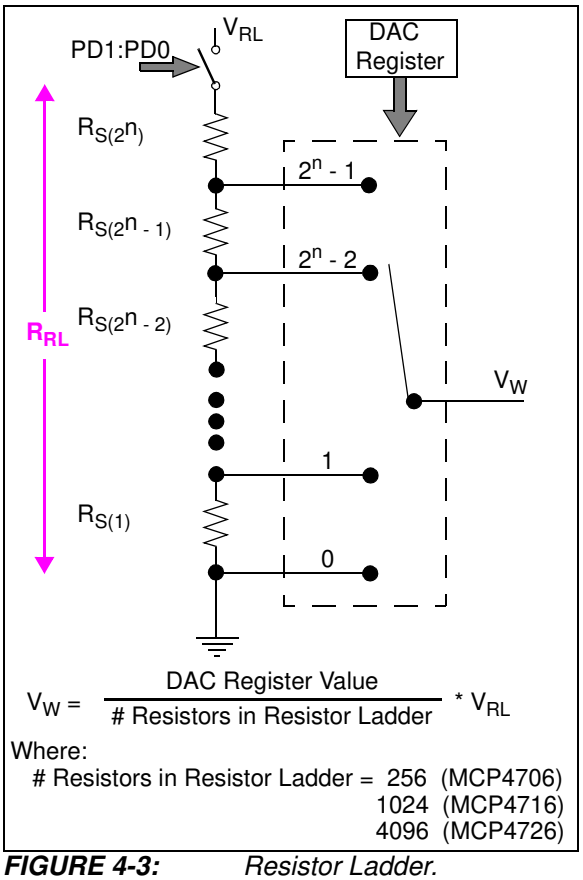


FIGURE 4-3: *Resistor Ladder.*

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4.4 Output Buffer / V_{OUT} Operation

The DAC output is buffered with a low power and precision output amplifier (op amp). Figure 4-4 shows a block diagram.

This amplifier provides a rail-to-rail output with low offset voltage and low noise. The user can select the output gain of the output amplifier. Gain options are:

a) Gain of 1, with either V_{DD} or V_{REF} pin used as reference voltage

b) Gain of 2, only when V_{REF} pin is used as reference voltage. The V_{REF} pin voltage should be limited to $V_{DD}/2$.

The amplifier's output can drive the resistive and high capacitive loads without oscillation. The amplifier provides a maximum load current which is enough for most programmable voltage reference applications. Refer to **Section 1.0 "Electrical Characteristics"** for the specifications of the output amplifier.

Note:	The load resistance must keep higher than 5 kΩ for the stable and expected analog output (to meet electrical specifications).

In any of the three Power-Down modes, the op amp is powered down and it's output becomes a high impedance to the V_{OUT} pin.

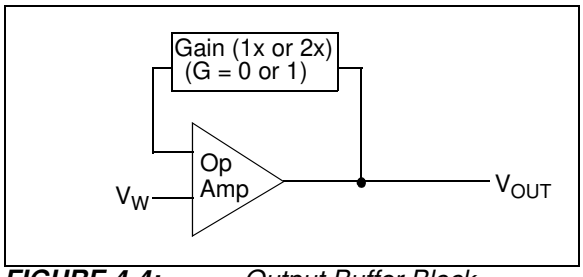


FIGURE 4-4: *Output Buffer Block Diagram.*

4.4.1 PROGRAMMABLE GAIN

The amplifier's gain is controlled by the Gain (G) configuration bit (See **Table 4-4**) and the V_{RL} reference selection. When the V_{RL} reference selection is the device's V_{DD} voltage, the G bit is ignored and a gain of 1 is used. The volatile G bit value can be modified by:

- POR event
- BOR event
- I^2C write commands
- I^2C General Call Reset command

4.4.2 OUTPUT VOLTAGE

The volatile DAC Register's value controls the analog V_{OUT} voltage, along with the device's five configuration bits. The volatile DAC Register's value is unsigned binary.

The formula for the output voltage is given in Equation 4-1. Table 4-1 shows examples of volatile DAC Register values and the corresponding theoretical V_{OUT} voltage for the MCP47X6 devices.

Note:	When Gain = 2 ($V_{RL} = V_{REF}$), if $V_{REF} > V_{DD} / 2$, the V_{OUT} voltage will be limited to V_{DD}. So if $V_{REF} = V_{DD}$, then the V_{OUT} voltage will not change for volatile DAC Register values mid-scale and greater, since the op amp at full scale output.

EQUATION 4-1: CALCULATING OUTPUT VOLTAGE (V_{OUT})

$$V_{OUT} = \frac{V_{RL} * \text{DAC Register Value}}{\text{\# Resistors in Resistor Ladder}} * \text{Gain}$$

\# Resistors in Resistor Ladder = 4096 (MCP4726)
1024 (MCP4716)
256 (MCP4706)

The DAC register value will be latched on the falling edge of the acknowledge pulse of the write command's last byte. Then the V_{OUT} voltage will start driving to the new value.

The following events update the analog voltage output (V_{OUT}):

- Power-On-Reset or General Call Reset command: Output is updated with EEPROM data.
- Falling edge of the acknowledge pulse of the last write command byte.

4.4.2.1 Resolution / Step Voltage

The Step voltage is dependent on the device resolution and the output voltage range. One LSb is defined as the ideal voltage difference between two successive codes. The step voltage can easily be calculated by using Equation 4-1 where the DAC Register Value is equal to 1.

4.4.3 DRIVING RESISTIVE AND CAPACITIVE LOADS

The V_{OUT} pin can drive up to 100 pF of capacitive load in parallel with a 5 kΩ resistive load (to meet electrical specifications). **Figure 2-57** shows the V_{OUT} vs. Resistive Load.

V_{OUT} drops slowly as the load resistance decreases after about 3.5 kΩ. It is recommended to use a load with R_L greater than 5 kΩ.

TABLE 4-1: DAC INPUT CODE VS. ANALOG OUTPUT (V_{OUT}) (V_{DD} = 5.0V)

Device	Volatile DAC Register Value	V_{RL} (1)	LSb		Gain Selection (2)	V_{OUT} (4)	
			Equation	uV		Equation	V
MCP4726 (12-bit)	1111 1111 1111	5.0V	5.0V/4096	1,220.7	1x	V_{RL} * (4095/4096) * 1	4.998779
		2.5V	2.5V/4096	610.4	1x	V_{RL} * (4095/4096) * 1	2.499390
					2x(3)	V_{RL} * (4095/4096) * 2)	4.998779
	0111 1111 1111	5.0V	5.0V/4096	1,220.7	1x	V_{RL} * (2047/4096) * 1)	2.498779
		2.5V	2.5V/4096	610.4	1x	V_{RL} * (2047/4096) * 1)	1.249390
					2x(3)	V_{RL} * (2047/4096) * 2)	2.498779
	0011 1111 1111	5.0V	5.0V/4096	1,220.7	1x	V_{RL} * (1023/4096) * 1)	1.248779
		2.5V	2.5V/4096	610.4	1x	V_{RL} * (1023/4096) * 1)	0.624390
					2x(3)	V_{RL} * (1023/4096) * 2)	1.248779
	0000 0000 0000	5.0V	5.0V/4096	1,220.7	1x	V_{RL} * (0/4096) * 1)	0
		2.5V	2.5V/4096	610.4	1x	V_{RL} * (0/4096) * 1)	0
					2x(3)	V_{RL} * (0/4096) * 2)	0
MCP4716 (10-bit)	11 1111 1111	5.0V	5.0V/1024	4,882.8	1x	V_{RL} * (1023/1024) * 1	4.995117
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} * (1023/1024) * 1	2.497559
					2x(3)	V_{RL} * (1023/1024) * 2	4.995117
	01 1111 1111	5.0V	5.0V/1024	4,882.8	1x	V_{RL} * (511/1024) * 1	2.495117
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} * (511/1024) * 1	1.247559
					2x(3)	V_{RL} * (511/1024) * 2	2.495117
	00 1111 1111	5.0V	5.0V/1024	4,882.8	1x	V_{RL} * (255/1024) * 1	1.245117
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} * (255/1024) * 1	0.622559
					2x(3)	V_{RL} * (255/1024) * 2	1.245117
	00 0000 0000	5.0V	5.0V/1024	4,882.8	1x	V_{RL} * (0/1024) * 1	0
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} * (0/1024) * 1	0
					2x(3)	V_{RL} * (0/1024) * 1	0
MCP4706 (8-bit)	1111 1111	5.0V	5.0V/256	19,531.3	1x	V_{RL} * (255/256) * 1	4.980469
		2.5V	2.5V/256	9,765.6	1x	V_{RL} * (255/256) * 1	2.490234
					2x(3)	V_{RL} * (255/256) * 2	4.980469
	0111 1111	5.0V	5.0V/256	19,531.3	1x	V_{RL} * (127/256) * 1	2.480469
		2.5V	2.5V/256	9,765.6	1x	V_{RL} * (127/256) * 1	1.240234
					2x(3)	V_{RL} * (127/256) * 2	2.480469
	0011 1111	5.0V	5.0V/256	19,531.3	1x	V_{RL} * (63/256) * 1	1.230469
		2.5V	2.5V/256	9,765.6	1x	V_{RL} * (63/256) * 1	0.615234
					2x(3)	V_{RL} * (63/256) * 2	1.230469
	0000 0000	5.0V	5.0V/256	19,531.3	1x	V_{RL} * (0/256) * 1	0
		2.5V	2.5V/256	9,765.6	1x	V_{RL} * (0/256) * 1	0
					2x(3)	V_{RL} * (0/256) * 2	0

Note 1: V_{RL} is the resistor ladder's reference voltage. It is independent of V_{REF1}:V_{REF0} selection.

2: Gain selection of 2x requires voltage reference source to come from V_{REF} pin and requires V_{REF} pin voltage ≤ V_{DD} / 2.

3: Requires G = '1', V_{REF1}:V_{REF0} = '10' or '11', and V_{RL} ≤ V_{DD} / 2.

4: These theoretical calculations do not take into account the offset and gain errors.

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4.5 Power-Down Operation

To allow the application to conserve power when the DAC operation is not required, three power down modes are available. The Power-Down configuration bits (PD1:PD0) control the power down operation (Figure 4-5). All power down modes do the following:

- Turning off most of its internal circuits (op amp, resistor ladder, ...)
- Op amp output becomes high impedance to the V_{OUT} pin
- Disconnects resistor ladder from reference voltage (V_{RL})
- Retains the value of the volatile DAC register and configuration bits, and the nonvolatile (EEPROM) DAC register and configuration bits

Depending on the selected power down mode, the following will occur:

- V_{OUT} pin is switched to one of three resistive pull downs (See Table 4-2)
  - 640kΩ (typical)
  - 125kΩ (typical)
  - 1kΩ (typical)

There is a delay (T_{PDE}) between the PD1:PD0 bits changing from '00' to either '01', '10', or '11' and the op amp no longer driving the V_{OUT} output and the pull down resistors are sinking current.

In any of the power down modes, where the V_{OUT} pin is not externally connected (sinking or sourcing current), the power down current will typical be 60 nA (see **Section 1.0 "Electrical Characteristics"**).

Section 6.0 "MCP47X6 I2C Commands" describes the I^2C commands for writing the power-down bits. The commands that can update the volatile PD1:PD0 bits are:

- Write Volatile DAC Register
- Write Volatile Memory
- Write All Memory
- Write Volatile Configuration bits
- General Call Reset
- General Call Wake-up

Note:	The I^2C serial interface circuit is not affected by the Power-Down mode. This circuit remains active in order to receive any command that might come from the I^2C master device.

TABLE 4-2: POWER-DOWN BITS AND OUTPUT RESISTIVE LOAD

PD1	PD0	Function
0	0	Normal operation
0	1	1 kΩ resistor to ground
1	0	125 kΩ resistor to ground
1	1	640 kΩ resistor to ground

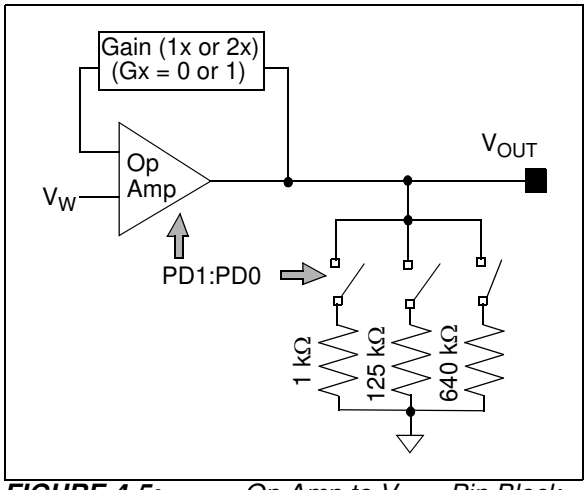


FIGURE 4-5: *Op Amp to V_{OUT} Pin Block Diagram.*

4.5.1 EXITING POWER-DOWN

When the device exits the power down mode the following occurs:

- Disabled circuits (op amp, resistor ladder, ...) are turned on
- Resistor ladder is connected to selected reference voltage (V_{RL})
- Selected pull down resistor is disconnected
- The V_{OUT} output will be driven to the voltage represented by the volatile DAC Register's value and configuration bits

The V_{OUT} output signal will require time as these circuits are powered up and the output voltage is driven to the specified value as determined by the volatile DAC register and configuration bits.

Note:	Since the op amp and resistor ladder were powered off (0V), the op amp's input voltage (V_W) can be considered 0V. There is a delay (T_{PDD}) between the PD1:PD0 bits updated to '00' and the op amp driving the V_{OUT} output. The op amp's settling time (from 0V) needs to be taken into account to ensure the V_{OUT} voltage reflects the selected value.

The following events will change the PD1:PD0 bits to '00' and therefore exit the Power-Down mode. These are:

- Any I^2C write command for where the PD1:PD0 bits are '00'.
- I^2C General Call Wake-up Command.
- I^2C General Call Reset Command. (if nonvolatile PD1:PD0 bits are '00').

4.6 Device Resets

Device Resets can be grouped into two types. Resets due to change in voltage (POR/BOR Reset), and resets caused by the system master (such as a microcontroller).

After a device reset, and when $V_{DD} \geq V_{DD(MIN)}$, the device memory may be written or read.

4.6.1 POR/BOR RESET OPERATION

The POR and BOR trip points are at the same voltage, and is determined if the V_{DD} voltage is rising or falling (see Figure 4-1). What occurs is different depending if the reset is a POR or BOR reset.

POR Reset (V_{DD} Rising)

On a POR Reset, the nonvolatile memory values (DAC Register and Configuration bits) are latched into the volatile memory. This configures the analog output (V_{OUT}) circuitry. Also a reset delay timer starts. During this delay time, the I^2C interface will not accept commands.

BOR Reset (V_{DD} Falling)

On a BOR Reset, the device is forced into a power down state. The volatile PD1:PD0 bits forced to '11' and all other volatile memory forced to '0'. The I^2C interface will not accept commands.

4.6.2 RESET COMMANDS

When the MCP47X6 is in the valid operating voltage, the I^2C General Call Reset command will force a reset event. This is similar to the POR reset, except that the reset delay timer is not started.

In the case where the I^2C Interface bus does not seem to be responsive, the technique shown in **Section 8.9, Software I2C Interface Reset Sequence** can be used to force the I^2C interface to be reset.

4.7 DAC Registers, Configuration Bits, and Status Bits

The MCP47X6 devices have both volatile and nonvolatile (EEPROM) memory. Figure 4-6 shows the volatile and nonvolatile memory and their interaction due to a POR event.

There are five configuration bits in both the volatile and nonvolatile memory, the DAC registers in both the volatile and nonvolatile memory, and two volatile status bits. The DAC registers (volatile and nonvolatile) will be either 12-bits (MCP4726), 10-bits (MCP4716), or 8-bits (MCP4706) wide.

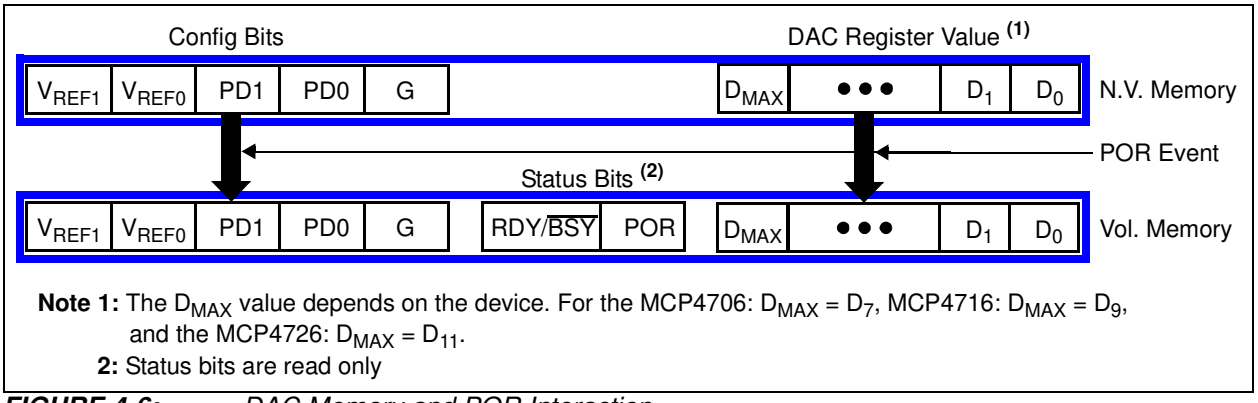
When the device is first powered up, it automatically uploads the EEPROM memory values to the volatile memory. The volatile memory determines the analog output (V_{OUT}) pin voltage. After the device is powered up, the user can update the device memory.

The I^2C interface is how this memory is read and written. Refer to **Section 5.0 "I^2C Serial Interface"** and **Section 6.0 "MCP47X6 I2C Commands"** for more details on the reading and writing the device's memory.

When the nonvolatile memory is written (using the I^2C Write All Memory command), the volatile memory is written with the same values. The device starts writing the EEPROM cell at the acknowledge pulse of the EEPROM write command.

Table 4-3 shows the operation of the device status bits, Table 4-4 shows the operation of the device configuration bits, and Table 4-5 shows the factory default value of a POR/BOR event for the device configuration bits.

There are two Status bits. These are only in volatile memory and give indication on the status of the device. The POR bit indicates if the device V_{DD} is above or below the POR trip point. During normal operation, this bit should be '1'. The RDY/$\overline{BSY}$ bit indicates if an EEPROM write cycle is in progress. While the RDY/$\overline{BSY}$ bit is low (during the EEPROM writing), all commands are ignored, except for the Read Command command.



Note 1: The D_{MAX} value depends on the device. For the MCP4706: $D_{MAX} = D_7$, MCP4716: $D_{MAX} = D_9$, and the MCP4726: $D_{MAX} = D_{11}$.
2: Status bits are read only

FIGURE 4-6: *DAC Memory and POR Interaction.*

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TABLE 4-3: STATUS BITS OPERATION

Name	Function
RDY/$\overline{BSY}$	This bit indicates the state of the EEPROM program memory 1 = EEPROM is not in a programming cycle 0 = EEPROM is in a programming cycle
POR	Power-On-Reset status indicator (flag) 1 = Device is powered on with $V_{DD} > V_{POR}$. Ensure that V_{DD} is above $V_{DD(MIN)}$ to ensure proper operation. 0 = Device is in powered off state. If this value is read, $V_{DD} < V_{DD(MIN)} < V_{POR}$. Unreliable device operation should be expected.

TABLE 4-4: CONFIGURATION BITS

Name	Function
VREF1:VREF0	Resistor Ladder Voltage Reference (V_{RL}) selection bits 0x = V_{DD} (Unbuffered) 10 = V_{REF} pin (Unbuffered) 11 = V_{REF} pin (Buffered)
PD1:PD0	Power-Down selection bits When the DAC is powered down, most of the internal circuits are powered off and the op amp is disconnected from the V_{OUT} pin. 00 = Not Powered Down (Normal operation) 01 = Powered Down - V_{OUT} is loaded with 1 kΩ resistor to ground. 10 = Powered Down - V_{OUT} is loaded with 100 kΩ resistor to ground. 11 = Powered Down - V_{OUT} is loaded with 500 kΩ resistor to ground.
	Note: See Table 4-2 and Figure 4-5 for more details.
G	Gain selection bit 0 = 1x (gain of 1) 1 = 2x (gain of 2). Not applicable when V_{DD} is used as V_{RL}
	Note: If $V_{REF} = V_{DD}$, the device uses a gain of 1 only, regardless of the gain selection bit (G) setting.

TABLE 4-5: CONFIGURATION BIT VALUES AFTER POR/BOR EVENT

	R/W	R/W	R/W	R/W	R/W	Comment
Bit Name	VREF1	VREF0	PD1	PD0	G	
POR Event	0(1)	0(1)	0(1)	0(1)	0(1)	When V_{DD} transitions from $V_{DD} < V_{POR}$ to $V_{DD} > V_{POR}$
BOR Event	0	0	1	1	0	When V_{DD} transitions from $V_{DD} > V_{BOR}$ to $V_{DD} < V_{BOR}$

Note 1: Default configuration when the device is shipped to customer. The POR/BOR value may be modified by writing the corresponding nonvolatile configuration bit.

REGISTER 4-1: DAC REGISTER BITS

	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Comment
Bit Name	—(2)	—(2)	—(2)	—(2)	D7	D6	D5	D4	D3	D2	D1	D0	MCP4706
	—(2)	—(2)	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	MCP4716
	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	MCP4726
POR/BOR Event	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	

Note 1: Default configuration when the device is shipped to customer. The POR/BOR value may be modified by writing the corresponding nonvolatile configuration bit.

2: This device does not implement this bit, so there is no corresponding POR/BOR value.

NOTES:

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5.0 I²C SERIAL INTERFACE

The MCP47X6 devices support the I²C serial protocol. The MCP47X6 I²C's module operates in Slave mode (does not generate the serial clock).

5.1 Overview

This I²C interface is a two-wire interface. Figure 5-1 shows a typical I²C Interface connection.

The I²C interface specifies different communication bit rates. These are referred to as standard, fast or high speed modes. The MCP47X6 supports these three modes. The bit rates of these modes are:

- Standard Mode: bit rates up to 100 kbit/s
- Fast Mode: bit rates up to 400 kbit/s
- High Speed Mode (HS mode): bit rates up to 3.4 Mbit/s

A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the START and STOP conditions. The MCP47X6 device works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. Communication is initiated by the master (microcontroller) which sends the START bit, followed by the slave address byte. The first byte transmitted is always the slave address byte, which contains the device code, the address bits, and the R/$\overline{W}$ bit.

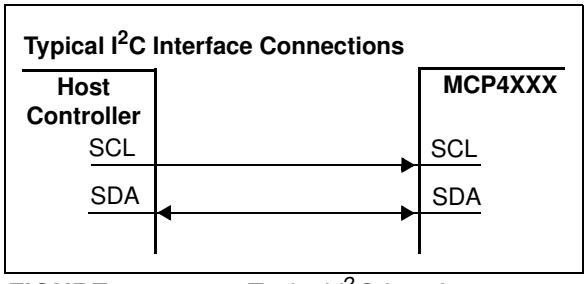


FIGURE 5-1: *Typical I²C Interface.*

The I²C serial protocol only defines the field types, field lengths, timings, etc. of a frame. The frame content defines the behavior of the device. For details on the frame content (commands/data) refer to **Section 6.0**.

Refer to the NXP I²C document for more details on the I²C specifications.

5.2 Signal Descriptions

The I²C interface uses up to two pins (signals). These are:

- SDA (Serial Data)
- SCL (Serial Clock)

5.2.1 SERIAL DATA (SDA)

The Serial Data (SDA) signal is the data signal of the device. The value on this pin is latched on the rising edge of the SCL signal when the signal is an input.

With the exception of the START and STOP conditions, the high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. During the high period of the clock, the SDA pin's value (high or low) must be stable. Changes in the SDA pin's value while the SCL pin is HIGH will be interpreted as a START or a STOP condition.

5.2.2 SERIAL CLOCK (SCL)

The Serial Clock (SCL) signal is the clock signal of the device. The rising edge of the SCL signal latches the value on the SDA pin.

The MCP47X6 will not stretch the clock signal (SCL) since memory read access occurs fast enough.

Depending on the clock rate mode, the interface will display different characteristics.

5.3 I²C Operation

The MCP47X6's I²C module is compatible with the NXP I²C specification. The following lists some of the module's features:

- 7-bit slave addressing
- Supports three clock rate modes:
  - Standard mode, clock rates up to 100 kHz
  - Fast mode, clock rates up to 400 kHz
  - High-speed mode (HS mode), clock rates up to 3.4 MHz
- Support Multi-Master Applications
- General call addressing (Reset and Wake-Up commands)

The I²C 10-bit addressing mode is not supported.

The NXP I²C specification only defines the field types, field lengths, timings, etc. of a frame. The frame content defines the behavior of the device. The frame content for the MCP47X6 is defined in **Section 6.0**.

5.3.1 I²C BIT STATES AND SEQUENCE

Figure 5-8 shows the I²C transfer sequence. The serial clock is generated by the master. The following definitions are used for the bit states:

- Start bit (S)
- Data bit
- Acknowledge (A) bit (driven low) / No Acknowledge ($\overline{A}$) bit (not driven low)
- Repeated Start bit (Sr)
- Stop bit (P)

5.3.1.1 Start Bit

The Start bit (see Figure 5-2) indicates the beginning of a data transfer sequence. The Start bit is defined as the SDA signal falling when the SCL signal is "High".

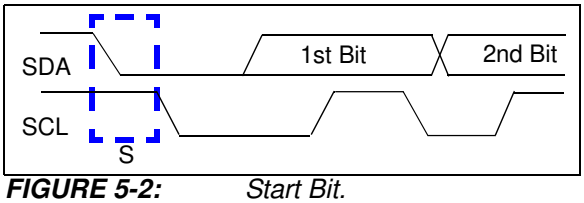


FIGURE 5-2: *Start Bit.*

5.3.1.2 Data Bit

The SDA signal may change state while the SCL signal is Low. While the SCL signal is High, the SDA signal MUST be stable (see Figure 5-5).

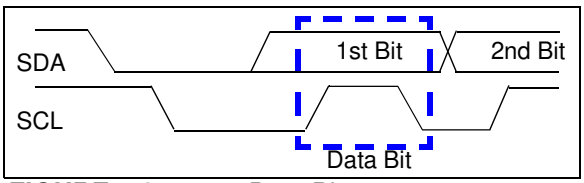


FIGURE 5-3: *Data Bit.*

5.3.1.3 Acknowledge (A) Bit

The A bit (see Figure 5-4) is typically a response from the receiving device to the transmitting device. Depending on the context of the transfer sequence, the A bit may indicate different things. Typically the Slave device will supply an A response after the Start bit and 8 "data" bits have been received. An A bit has the SDA signal low.

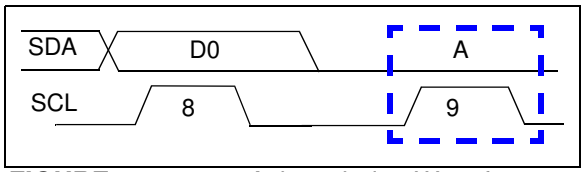


FIGURE 5-4: *Acknowledge Waveform.*

Not A ($\overline{A}$) Response

The $\overline{A}$ bit has the SDA signal high. Table 5-1 shows some of the conditions where the Slave Device will issue a Not A ($\overline{A}$).

If an error condition occurs (such as an $\overline{A}$ instead of A), then a START bit must be issued to reset the command state machine.

TABLE 5-1: MCP47X6 A / $\overline{A}$ RESPONSES

Event	Acknowledge Bit Response	Comment
General Call	A	
Slave Address valid	A	
Slave Address not valid	$\overline{A}$	
Communication during EEPROM write cycle	A	After device has received address and command, and valid conditions for EEPROM write
Bus Collision	N.A.	I²C Module Resets, or a "Don't Care" if the collision occurs on the Master's "Start bit"

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5.3.1.4 Repeated Start Bit

The Repeated Start bit (see Figure 5-5) indicates the current Master Device wishes to continue communicating with the current Slave Device without releasing the I^2C bus. The Repeated Start condition is the same as the Start condition, except that the Repeated Start bit follows a Start bit (with the Data bits + A bit) and not a Stop bit.

The Start bit is the beginning of a data transfer sequence and is defined as the SDA signal falling when the SCL signal is “High”.

Note 1: A bus collision during the Repeated Start condition occurs if:

- SDA is sampled low when SCL goes from low to high.
- SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data "1".

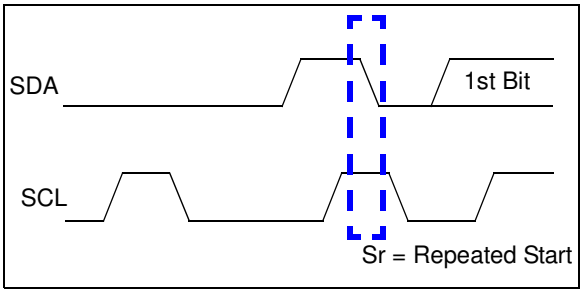


FIGURE 5-5: *Repeat Start Condition Waveform.*

5.3.1.5 Stop Bit

The Stop bit (see Figure 5-6) Indicates the end of the I^2C Data Transfer Sequence. The Stop bit is defined as the SDA signal rising when the SCL signal is “High”.

A Stop bit resets the I^2C interface of all MCP47X6 devices.

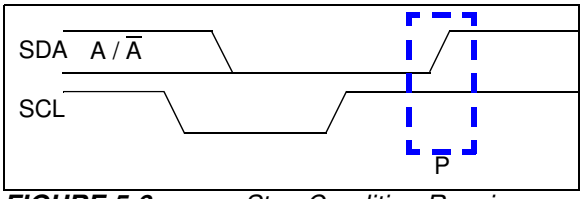


FIGURE 5-6: *Stop Condition Receive or Transmit Mode.*

5.3.2 CLOCK STRETCHING

“Clock Stretching” is something that the receiving Device can do, to allow additional time to “respond” to the “data” that has been received.

The MCP47X6 will not stretch the clock signal (SCL) since memory read access occurs fast enough.

5.3.3 ABORTING A TRANSMISSION

If any part of the I^2C transmission does not meet the command format, it is aborted. This can be intentionally accomplished with a START or STOP condition. This is done so that noisy transmissions (usually an extra START or STOP condition) are aborted before they corrupt the device.

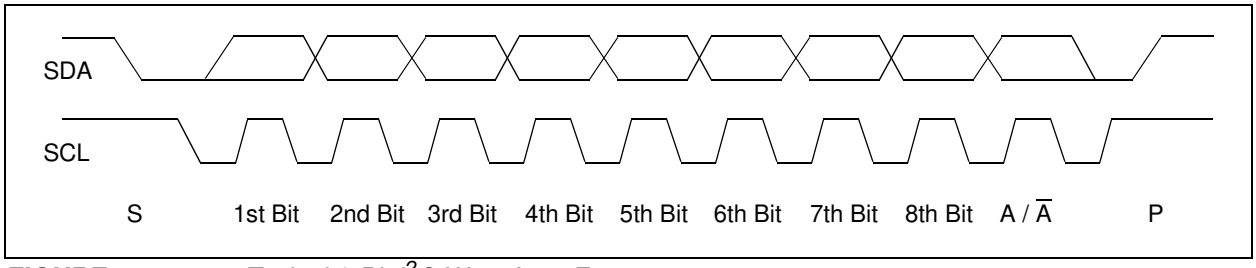


FIGURE 5-7: *Typical 8-Bit I^2C Waveform Format.*

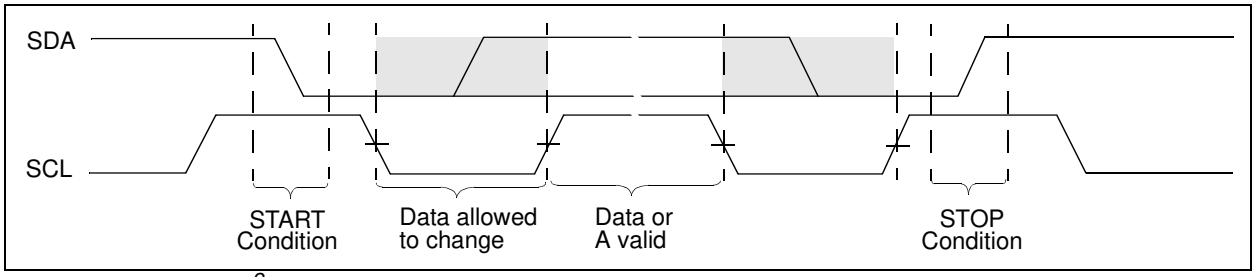


FIGURE 5-8: *I^2C Data States and Bit Sequence.*

5.3.4 SLOPE CONTROL

The MCP47X6 implements slope control on the SDA output.

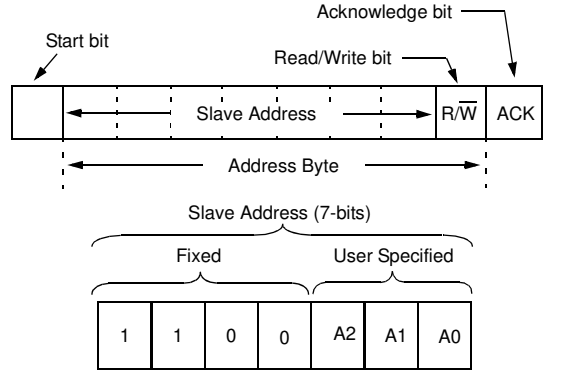
As the device transitions from HS mode to FS mode, the slope control parameter will change from the HS specification to the FS specification.

For Fast (FS) and High-Speed (HS) modes, the device has a spike suppression and a Schmidt trigger at SDA and SCL inputs.

5.3.5 DEVICE ADDRESSING

The address byte is the first byte received following the START condition from the master device. The MCP47X6's slave address consists of a 4-bit fixed code ('1100') and a 3-bit code that is user specified when the device is ordered. This allows up to eight MCP47X6 devices on a single I^2C bus.

Figure 5-9 shows the I^2C slave address byte format, which contains the seven address bits and a read/write ($R/\overline{W}$) bit. Table 5-2 shows the eight I^2C Slave address options and their respective device order code.



Note: Address Bits (A2:A0) specified at time of device order, see Table 5-2.

FIGURE 5-9: *Slave Address Bits in the I^2C Control Byte.*

TABLE 5-2: I^2C ADDRESS / ORDER CODE

7-bit I^2C Address	Device Order Code	Comment
'1100000'	MCP47x6A0-E/xx	
	MCP47x6A0T-E/xx	Tape and Reel
'1100001'	MCP47x6A1-E/xx	
	MCP47x6A1T-E/xx	Tape and Reel
'1100010'	MCP47x6A2-E/xx	
	MCP47x6A2T-E/xx	Tape and Reel
'1100011'	MCP47x6A3-E/xx	
	MCP47x6A3T-E/xx	Tape and Reel
'1100100'	MCP47x6A4-E/xx	
	MCP47x6A4T-E/xx	Tape and Reel
'1100101'	MCP47x6A5-E/xx	
	MCP47x6A5T-E/xx	Tape and Reel
'1100110'	MCP47x6A6-E/xx	
	MCP47x6A6T-E/xx	Tape and Reel
'1100111'	MCP47x6A7-E/xx	
	MCP47x6A7T-E/xx	Tape and Reel

Note 1: The sample center will generally stock I^2C address '1100000', other addresses may be available.

2: 'xx' in the order code is the device package code (CH for SOT-23 and MA for DFN)

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5.3.6 HS MODE

The I^2C specification requires that a high-speed mode device must be 'activated' to operate in high-speed (3.4 Mbit/s) mode. This is done by the Master sending a special address byte following the START bit. This byte is referred to as the high-speed Master Mode Code (HSMMC).

The MCP47X6 device does not acknowledge this byte. However, upon receiving this command, the device switches to HS mode. The device can now communicate at up to 3.4 Mbit/s on SDA and SCL lines. The device will switch out of the HS mode on the next STOP condition.

The master code is sent as follows:

1. START condition (S)
2. High-Speed Master Mode Code (0000 1XXX), The XXX bits are unique to the high-speed (HS) mode Master.
3. No Acknowledge ($\overline{A}$)

After switching to the High-Speed mode, the next transferred byte is the I^2C control byte, which specifies the device to communicate with, and any number of data bytes plus acknowledgements. The Master Device can then either issue a Repeated Start bit to address a different device (at High-Speed) or a Stop bit to return to Fast/Standard bus speed. After the Stop bit, any other Master Device (in a Multi-Master system) can arbitrate for the I^2C bus.

See Figure 5-10 for illustration of HS mode command sequence.

For more information on the HS mode, or other I^2C modes, please refer to the NXP I^2C specification.

5.3.6.1 Slope Control

The slope control on the SDA output is different between the Fast/Standard Speed and the High-Speed clock modes of the interface.

5.3.6.2 Pulse Gobbler

The pulse gobbler on the SCL pin is automatically adjusted to suppress spikes < 10 ns during HS mode.

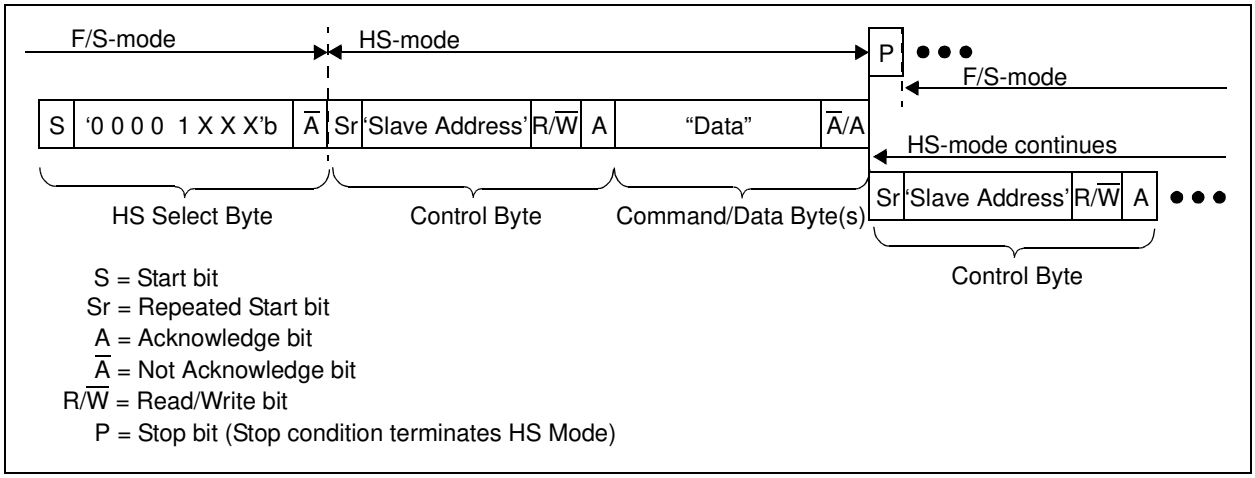


FIGURE 5-10: *HS Mode Sequence.*

5.3.7 GENERAL CALL

The General Call is a method that the “Master” device can communicate with all other “Slave” devices. In a Multi-Master application, the other Master devices are operating in Slave mode. The General Call address has two documented formats. These are shown in Figure 5-11.

The MCP47X6 has two General Call Commands. The function of these commands are:

- Reset the device(s) (Software Reset)
- Wake-Up the device(s)

For details on the operation of the MCP47X6’s General Call Commands, see **Section 6.6**.

Note:	Only one General Call command per issue of the General Call control byte. Any additional General Call commands are ignored and Not Acknowledged.

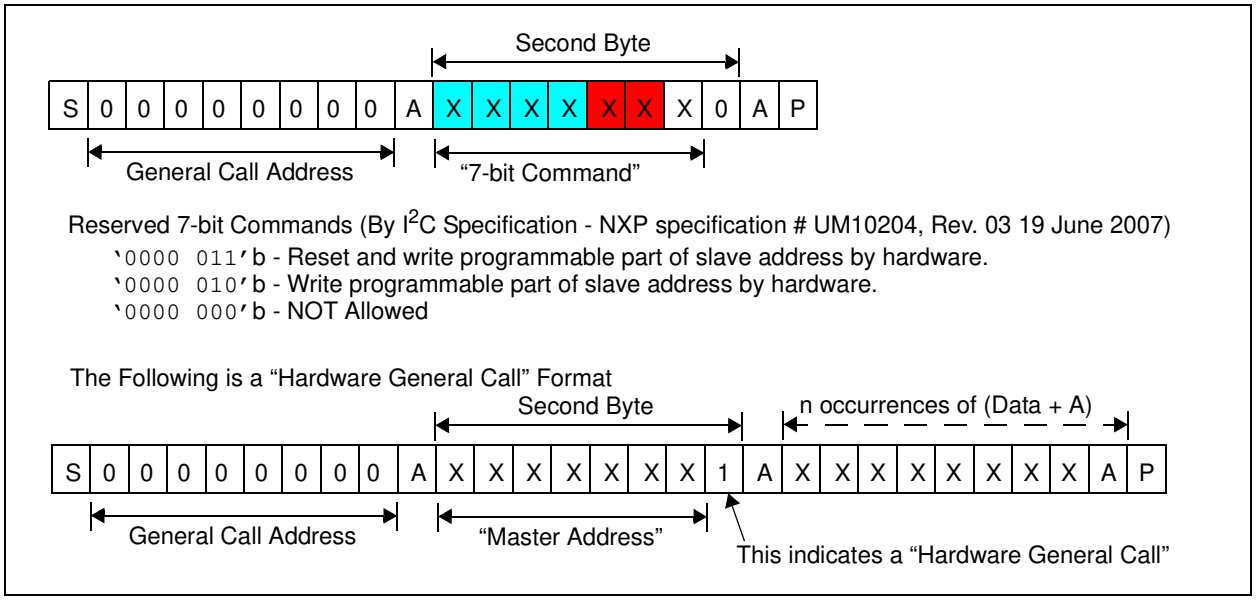


FIGURE 5-11: *General Call Formats.*

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6.0 MCP47X6 I²C COMMANDS

The I²C protocol does not specify how commands are formatted, so this section specifies the MCP47X6's I²C command formats and operation.

The commands can be grouped into the following categories:

- Write memory
- Read memory
- General Call commands

The supported commands are shown in Table 6-2. Many of these commands allow for continuous operation. This means that the I²C Master does not generate a Stop bit but repeats the required data/clocks. This allows faster updates since the overhead of the I²C control byte is removed. Table 6-1 shows the supported commands and the required number of bit clocks for both single and continuous commands.

Write commands, determined by the R/W bit = '0', use up to three command codes bits (C2:C0) to determine the write's operation.

The Read command is strictly determined by the R/W bit = '1'. There are two formats of the command. One for 12-bit and 10-bit devices and a second for 8-bit devices.

The General Call commands utilize the I²C specification reserved General Call command address and command codes.

TABLE 6-1: I²C COMMANDS - NUMBER OF CLOCKS

Command		# of Bit Clocks (1)
Operation	Mode	
Write Volatile DAC Register Command (2)	Single	29
	Continuous	18n + 11
Write Volatile Memory Command	Single	38
	Continuous	27n + 11
Write All Memory Command	Single	38
	Continuous	27n + 11
Write Volatile Configuration bits Command	Single	20
	Continuous	9n + 11
Read Command (12 and 10-bit DAC register) (2)	Single	65
	Continuous	54n + 11
Read Command (8-bit DAC register) (2)	Single	47
	Continuous	36n + 11

Note 1: "n" indicates the number of times the command operation is to be repeated.

2: This command is useful to determine when an EEPROM programming cycle has completed (RDY/$\overline{BSY}$ status bit)

6.0.1 ABORTING A TRANSMISSION

A Restart or Stop condition in an expected data bit position will abort the current command sequence and data will not be written to the MCP47X6.

TABLE 6-2: MCP47X6 SUPPORTED COMMANDS

Command Code (Note 1)			Command Name	Writes Volatile Memory?		Writes EEPROM Memory?		Command during EEPROM Write Cycle?	Comment
C2	C1	C0		Config.	DAC	Config.	DAC		
0	0	X	Write Volatile DAC Register Command (Note 2)	PD1:PD0 only	Yes	No	No	No	Writes volatile Power Down bits so can also be used to exit a power down state.
0	1	0	Write Volatile Memory Command	Yes	Yes	No	No	No	
0	1	1	Write All Memory Command	Yes	Yes	Yes	Yes	No	
1	0	0	Write Volatile Configuration bits Command	Yes	No	No	No	No	
1	0	1	Reserved	N.A.	N.A.	N.A.	N.A.	N.A.	Reserved (Note 3)
1	1	0							
1	1	1		N.A.	N.A.	N.A.	N.A.		Reserved (Note 3)
N.A.			Read Command	N.A.	N.A.	N.A.	N.A.	Yes	Determined by R/W bit in I²C Control byte
			General Call Reset	N.A.	N.A.	N.A.	N.A.	No	Determined by General Call command byte after the I²C General Call address.
			General Call Wake-up	N.A.	N.A.	N.A.	N.A.	No	

Note 1: These bits are the MSb of the 2nd byte in the I²C write command. See Figure 6-1 to Figure 6-4.

2: X = Don't Care bit. This command format does not use C0 bit.

3: Device operation is not specified.

6.1 Write Volatile DAC Register (C2:C0 = '00x')

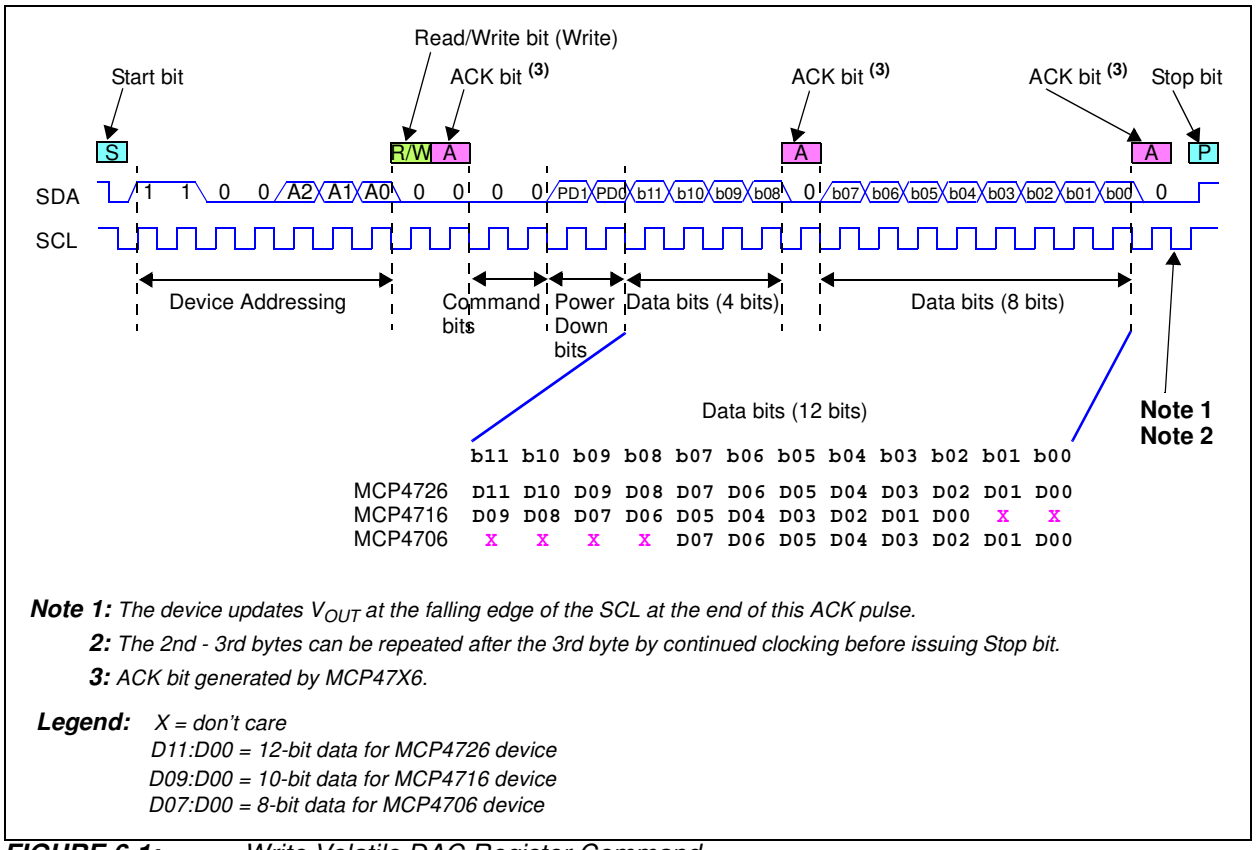
This command is used to update the volatile DAC Register value and the two Power-down configuration bits (PD1:PD0). This command is typically used for a quick update of the analog output by modifying the minimum parameters. The EEPROM values are not affected by this command.

Figure 6-1 shows an example of the command format, where a stop bit completes the command.

The volatile DAC register and Power-down configuration bits are updated with the written date at the completion of the ACK bit (falling edge of SCL).

After this ACK bit, the I^2C Master should generate a Stop bit or the I^2C Master can repeat the 2nd (2 command bits + 2 power down bits + 4 data bits (b11:b08)) and the 3rd byte (8 data bits (b07:b00)). Repeating the 2nd and 3rd bytes allows a continuous command where the volatile DAC register can be updated without the communication overhead of the device addressing byte (1st byte).

The device updates the V_{OUT} at the falling edge of the Acknowledge pulse of the 3rd byte.



Note 1: *The device updates V_{OUT} at the falling edge of the SCL at the end of this ACK pulse.*

2: *The 2nd - 3rd bytes can be repeated after the 3rd byte by continued clocking before issuing Stop bit.*

3: *ACK bit generated by MCP47X6.*

Legend: *X = don't care*
D11:D00 = 12-bit data for MCP4726 device
D09:D00 = 10-bit data for MCP4716 device
D07:D00 = 8-bit data for MCP4706 device

FIGURE 6-1: *Write Volatile DAC Register Command.*

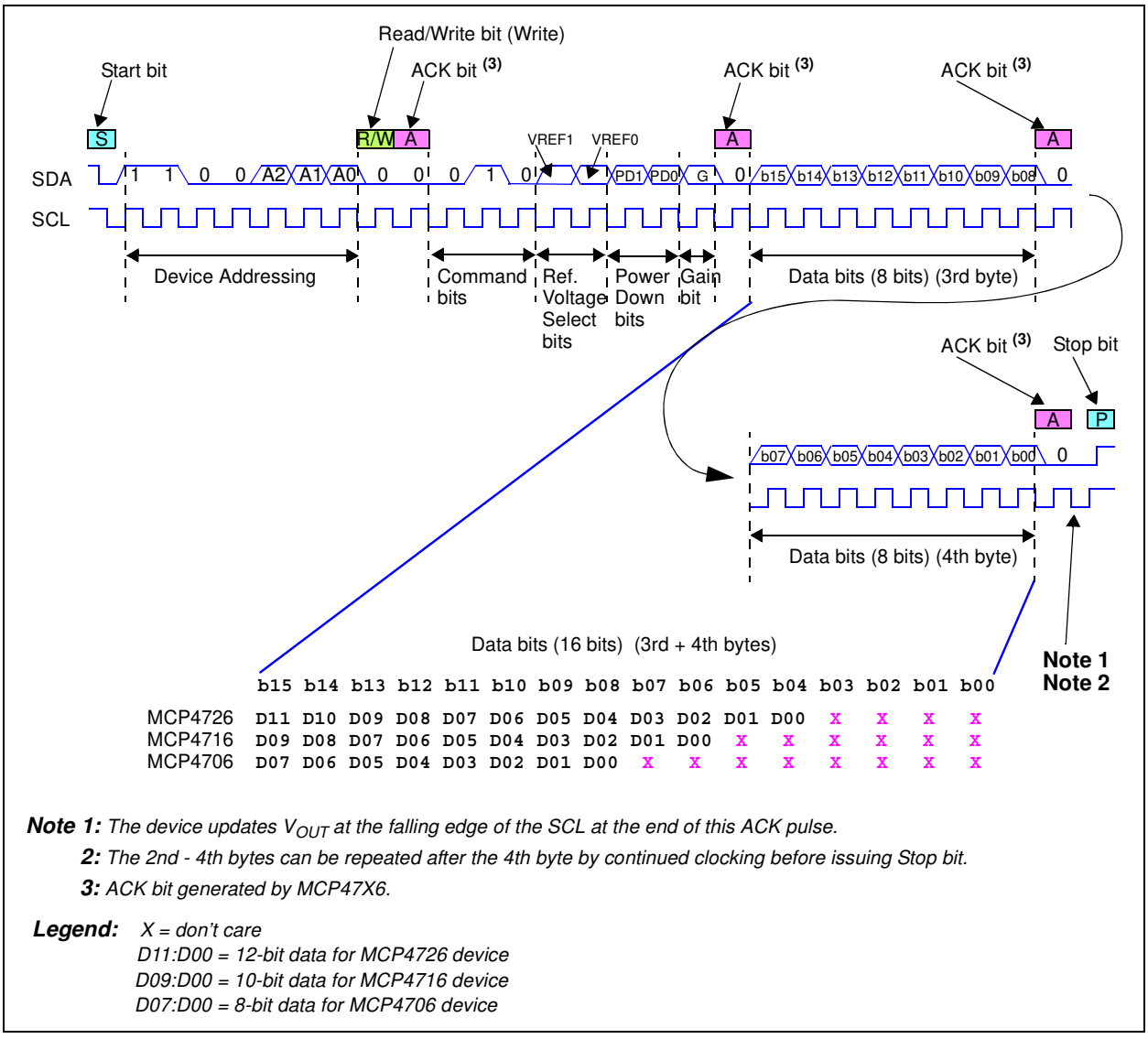
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6.2 Write Volatile Memory (C2:C0 = '010')

This write command is used to update the volatile DAC Register value and configuration bits. The EEPROM is not affected by this command. Figure 6-2 shows an example of this write command.

The volatile DAC register and configuration bits are updated with the written date at the completion of the ACK bit (falling edge of SCL).

After this ACK bit, the I^2C Master should generate a Stop bit or the I^2C Master can repeat the 2nd (3 command bits + 5 configuration bits), and the 3rd byte (8 data bits (b15:b08)), and the 4th byte (8 data bits (b07:b00)). Repeating the 2nd through 4th bytes allows a continuous command where the volatile DAC register and configuration bits can be updated without the communication overhead of the device addressing byte (1st byte).



Note 1: *The device updates V_{OUT} at the falling edge of the SCL at the end of this ACK pulse.*

2: *The 2nd - 4th bytes can be repeated after the 4th byte by continued clocking before issuing Stop bit.*

3: *ACK bit generated by MCP47X6.*

Legend: *X = don't care*
D11:D00 = 12-bit data for MCP4726 device
D09:D00 = 10-bit data for MCP4716 device
D07:D00 = 8-bit data for MCP4706 device

FIGURE 6-2: *Write Volatile Memory Command.*

6.3 Write All Memory (C2:C0 = '011')

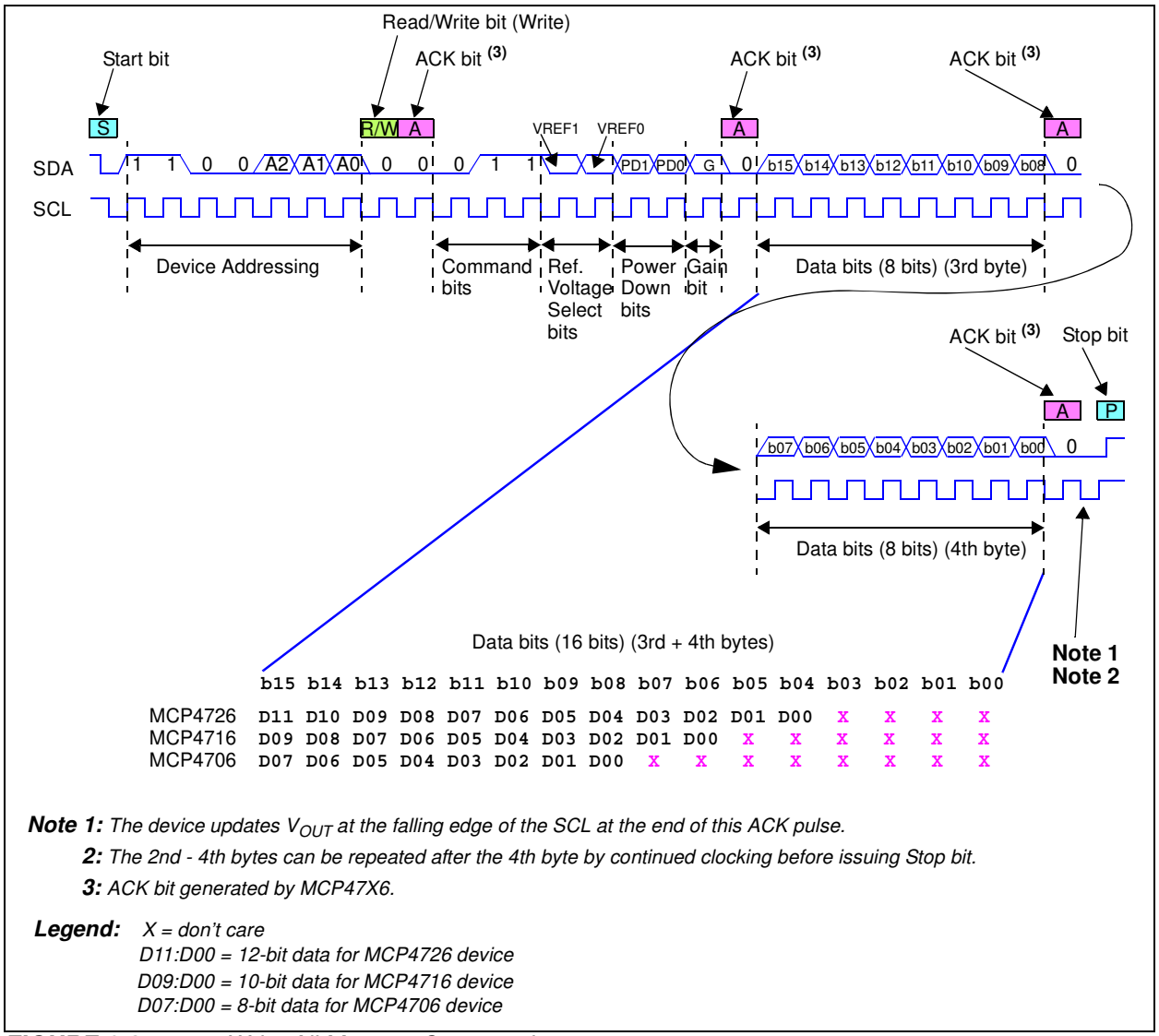
This write command is used to update the volatile and nonvolatile (EEPROM) DAC Register value and configuration bits. Figure 6-3 shows an example of this write command.

- V_{OUT} update: At the falling edge of the Acknowledge pulse of the 4th byte.
- EEPROM update: At the falling edge of the Acknowledge pulse of the 4th byte.

The DAC register and Power-down configuration bits (volatile and EEPROM) are updated with the written date at the completion of the ACK bit (falling edge of SCL). The EEPROM memory requires time (T_{WC}) for the values to be written. Another Write All memory command should not be issued until the EEPROM write is complete.

Note: RDY/$\overline{BSY}$ bit toggles to "low" and back to "high" after the EEPROM write is completed. The state of the RDY/$\overline{BSY}$ bit can be monitored by a read command.

Write commands which only update volatile memory (C2:C0 = '00x' or '010') can be issued. Read commands and the General Call commands may not be issued.



Note 1: *The device updates V_{OUT} at the falling edge of the SCL at the end of this ACK pulse.*

2: *The 2nd - 4th bytes can be repeated after the 4th byte by continued clocking before issuing Stop bit.*

3: *ACK bit generated by MCP47X6.*

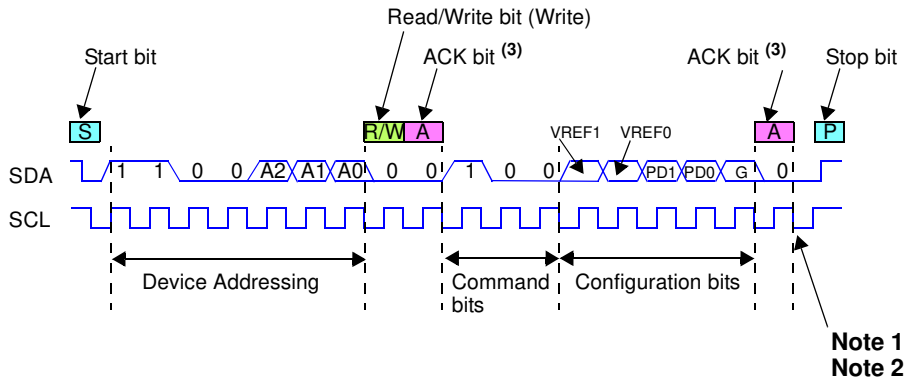
Legend: *X = don't care*
D11:D00 = 12-bit data for MCP4726 device
D09:D00 = 10-bit data for MCP4716 device
D07:D00 = 8-bit data for MCP4706 device

FIGURE 6-3: *Write All Memory Command.*

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6.4 Write Volatile Configuration bits (C2:C0 = '100')

This write command is used to update the volatile configuration register bits only. This command is a quick method to modify the configuration of the DAC, such as the selection of the resistor ladder reference voltage, the op amp gain, and the Power Down state. Figure 6-4 shows an example of this write command.



Note 1: *The device updates V_{OUT} at the falling edge of the SCL at the end of this ACK pulse.*

2: *The 2nd byte can be repeated after the 2nd by continued clocking before issuing Stop bit.*

3: *ACK bit generated by MCP47X6.*

FIGURE 6-4: *Write Volatile Configuration Bits Command.*

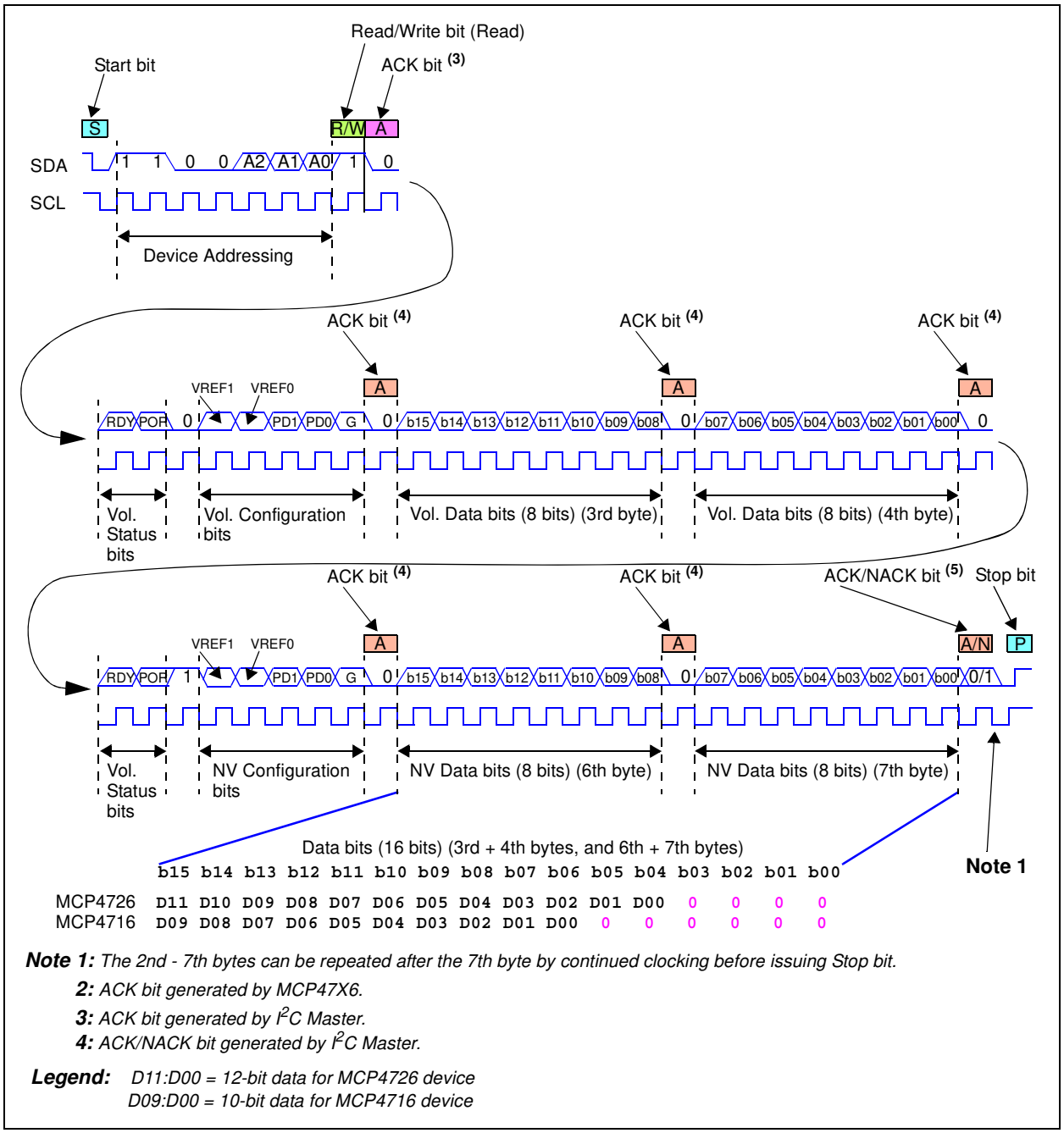
6.5 READ COMMAND

This command reads all the device memory. This includes the volatile and nonvolatile (EEPROM) DAC Register values and configuration bits, and the volatile status bits.

This command is executed when the I^2C control byte's Read/Write bit is a '1' (read).

This command has two different formats based on the resolution of the device. The 12-bit and 10-bit devices use the format in Figure 6-5, while the 8-bit device uses the format in Figure 6-6.

The 2nd byte (configuration bits) indicates the current condition of the device operation. The RDY/$\overline{BSY}$ bit indicates EEPROM writing status.



Note 1: *The 2nd - 7th bytes can be repeated after the 7th byte by continued clocking before issuing Stop bit.*

2: *ACK bit generated by MCP47X6.*

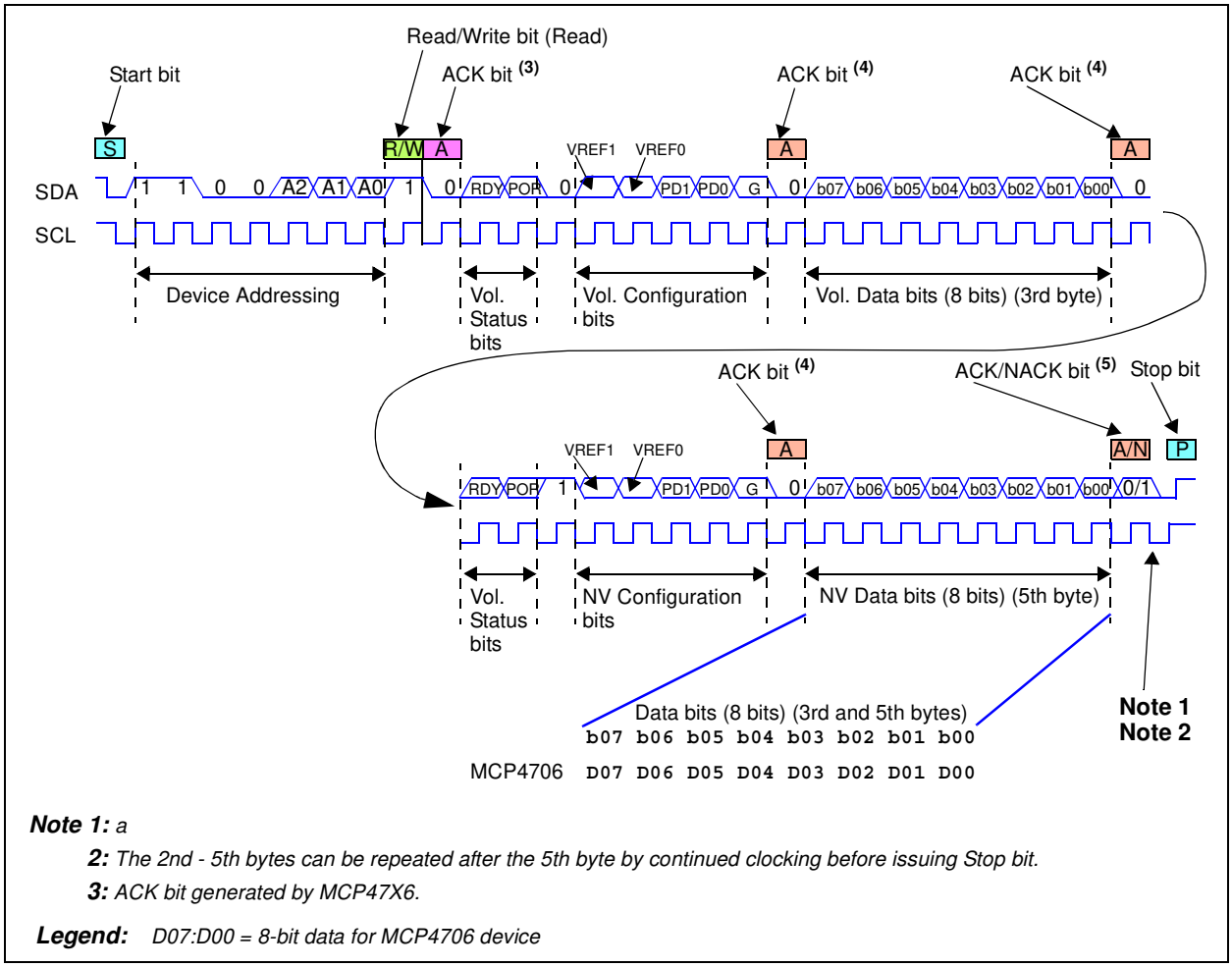
3: *ACK bit generated by I^2C Master.*

4: *ACK/NACK bit generated by I^2C Master.*

Legend: *D11:D00 = 12-bit data for MCP4726 device*
D09:D00 = 10-bit data for MCP4716 device

FIGURE 6-5: *Read Command Format for 12-bit DAC (MCP4726) and 10-bit DAC (MCP4716).*

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Note 1: *a*

2: *The 2nd - 5th bytes can be repeated after the 5th byte by continued clocking before issuing Stop bit.*

3: *ACK bit generated by MCP47X6.*

Legend: *D07:D00 = 8-bit data for MCP4706 device*

FIGURE 6-6: *Read Command Format for 8-bit DAC (MCP4706).*

6.6 I²C General Call Commands

The device acknowledges the general call address command (0x00 in the first byte). The meaning of the general call address is always specified in the second byte. The I²C specification does not allow "00000000" (00h) in the second byte. Please refer to the Phillips I²C document for more details on the General Call specifications.

The MCP47X6 devices support the following I²C general calls:

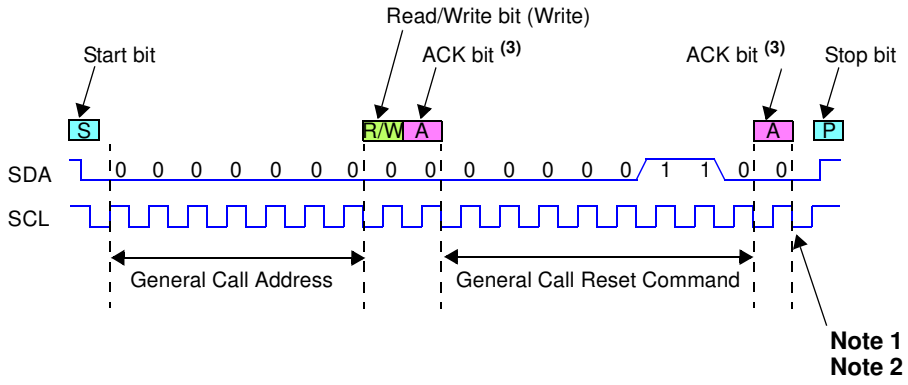
- General Call Reset
- General Call Wake-Up

6.6.1 GENERAL CALL RESET

The device performs General Call Reset if the second byte is "00000110" (06h). At the acknowledgement of this byte, the device will abort the current conversion and perform the following tasks:

- Internal reset similar to a Power-On-Reset (POR). The contents of the EEPROM are loaded into the DAC registers and analog output is available immediately.
- This is a similar event to the POR. The V_{OUT} will be available immediately, but after a short time delay following the Acknowledgement pulse. The V_{OUT} value is determined by the EEPROM contents.

This command allows multiple MCP47X6 devices to be reset synchronously.



Note 1: *At the falling edge of the SCL at the end of this ACK pulse a reset occurs (startup timer starts and DAC register latched).*

2: *The 2nd byte can be repeated after the 2nd by continued clocking before issuing Stop bit.*

3: *ACK bit generated by MCP47X6.*

FIGURE 6-7: *General Call Reset Command.*

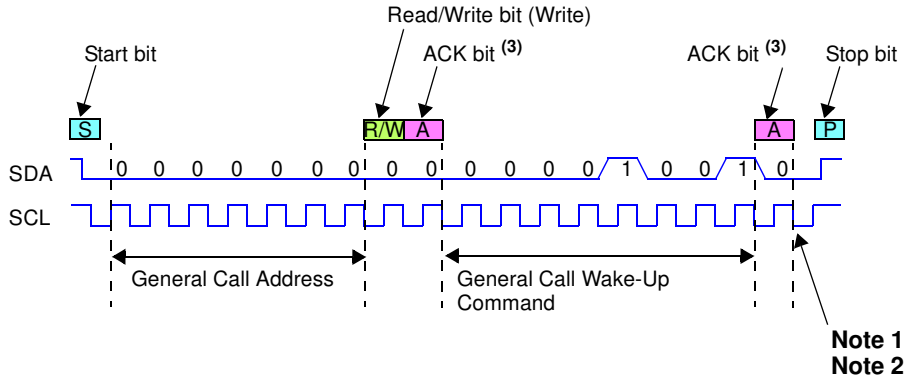
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6.6.2 GENERAL CALL WAKE-UP

If the second byte is "00001001" (09h), the device forces the volatile power-down bits to '00'. The nonvolatile (EEPROM) power-down bit values are not affected by this command.

This command allows multiple MCP47X6 devices to wake-up synchronously.

Note:	This command does not adhere to the I^2C specification where if the LSb of the 2nd byte is a '1', it is a 'Hardware General Call' (see the NXP I2C Specification).



Note 1: *At the falling edge of the SCL, at the end of this ACK pulse, the volatile PD1:PD0 bits are forced to '00'.*

2: *The 2nd byte can be repeated after the 2nd by continued clocking before issuing Stop bit.*

3: *ACK bit generated by MCP47X6.*

FIGURE 6-8: *General Call Wake-Up Command.*

NOTES:

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7.0 TERMINOLOGY

7.1 Resolution

The resolution is the number of DAC output states that divide the full-scale range. For the 12-bit DAC, the resolution is 2^{12}, meaning the DAC code ranges from 0 to 4095.

7.2 Least Significant bit (LSb)

Normally this is thought of as the ideal voltage difference between two successive codes. This bit has the smallest value or weight of all bits in the register.

For a given output voltage range, which is typically the voltage between the Full-Scale voltage and the Zero-Scale voltage ($V_{OUT(FS)}$ - $V_{OUT(ZS)}$), it is divided by the resolution of the device (Equation 7-1).

EQUATION 7-1: LSb VOLTAGE CALCULATION

$$V_{LSb} = \frac{V_{OUT(FS)} - V_{OUT(ZS)}}{2^N - 1}$$

2^N = 4096 (MCP4726)
1024 (MCP4716)
256 (MCP4706)

7.3 Monotonicity

Normally this is thought of as the V_{OUT} voltage never decreasing, as the DAC Register code is continuously incremented by 1 code step (LSb).

7.4 Full-Scale Error (FSE)

The Full-scale error (see Figure 7-4) is the sum of offset error plus gain error. It is the difference between the ideal and measured DAC output voltage with all bits set to one (DAC input code = FFFh for 12-bit DAC).

EQUATION 7-2: FULL SCALE ERROR

$$FSE = \frac{V_{OUT(@FS)} - V_{IDEAL(@FS)}}{V_{LSb}}$$

Where:
FSE is expressed in LSb
$V_{OUT(@FS)}$ is the V_{OUT} voltage when the DAC register code is at Full-scale.
$V_{IDEAL(@FS)}$ is the ideal output voltage when the DAC register code is at Full-scale.
V_{LSb} is the delta voltage of one DAC register code step (such as code 000h to code 001h).

7.5 Zero-Scale Error (ZSE)

The Zero-Scale Error (see Figure 7-4) is the difference between the ideal and measured V_{OUT} voltage with the volatile DAC Register equal to 000h. The Zero-Scale Error is the same as the Offset Error for this case (volatile DAC Register = 000h).

EQUATION 7-3: ZERO SCALE ERROR

$$ZSE = \frac{V_{OUT(@ZS)}}{V_{LSb}}$$

Where:
FSE is expressed in LSb
$V_{OUT(@ZS)}$ is the V_{OUT} voltage when the DAC register code is at Zero-scale.
V_{LSb} is the delta voltage of one DAC register code step (such as code 000h to code 001h).

7.6 Offset Error

The Offset error (see Figure 7-1) is the deviation from zero voltage output when the volatile DAC Register value = 000h (zero scale voltage). This error affects all codes by the same amount. The offset error can be calibrated by software in application circuits.

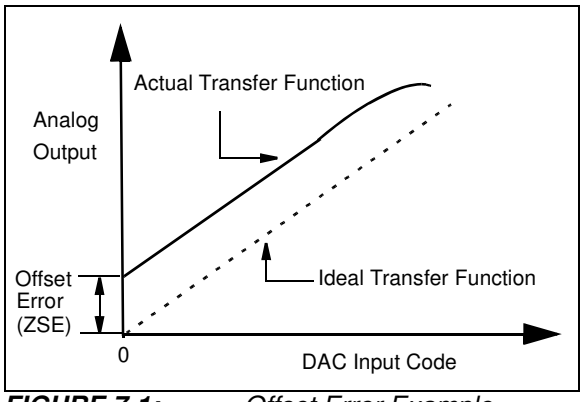


FIGURE 7-1: *Offset Error Example.*

7.7 Integral Nonlinearity (INL)

The Integral nonlinearity (INL) error is the maximum deviation of an actual transfer function from an ideal transfer function (straight line).

In the MCP47X6, INL is calculated using two end points (zero and full scale). INL can be expressed as a percentage of full scale range (FSR) or in a fraction of an LSb. INL is also called relative accuracy. Equation 7-4 shows how to calculate the INL error in LSb and Figure 7-2 shows an example of INL accuracy.

EQUATION 7-4: INL ERROR

$$INL = \frac{(V_{OUT} - V_{Ideal})}{LSb}$$

Where:

INL is expressed in LSb.

V_{Ideal} = Code*LSb

V_{OUT} = The output voltage measured with a given DAC input code

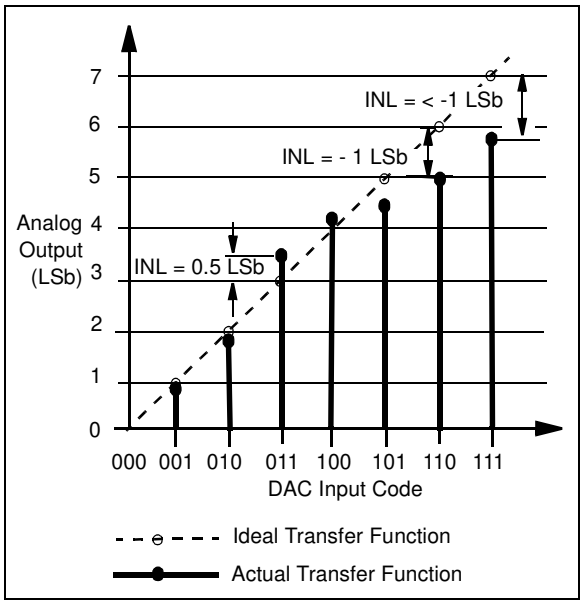


FIGURE 7-2: *INL Accuracy Example.*

7.8 Differential Nonlinearity (DNL)

The Differential nonlinearity (DNL) error (see Figure 7-3) is the measure of step size between codes in actual transfer function. The ideal step size between codes is 1 LSb. A DNL error of zero would imply that every code is exactly 1 LSb wide. If the DNL error is less than 1 LSb, the DAC guarantees monotonic output and no missing codes. The DNL error between any two adjacent codes is calculated as follows:

EQUATION 7-5: DNL ERROR

$$DNL = \frac{\Delta V_{OUT} - LSb}{LSb}$$

Where:

DNL is expressed in LSb.

ΔV_{OUT} = The measured DAC output voltage difference between two adjacent input codes.

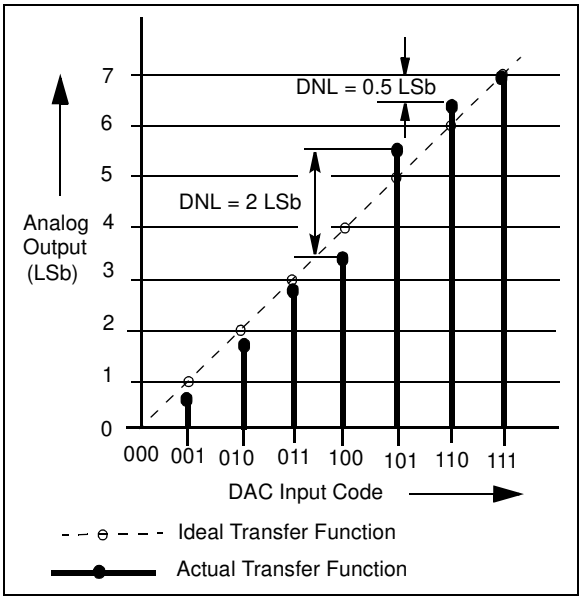


FIGURE 7-3: *DNL Accuracy Example.*

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7.9 Gain Error

The Gain error (see Figure 7-4) is the difference between the actual full-scale output voltage from the ideal output voltage of the DAC transfer curve. The gain error is calculated after nullifying the offset error, or full scale error minus the offset error.

The gain error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The gain error is usually expressed as percent of full-scale range (% of FSR) or in LSb.

In the MCP4706/4716/4726, the gain error is not calibrated at the factory and most of the gain error is contributed by the output buffer (op amp) saturation near the code range beyond 4000d. For the applications that need the gain error specification less than 1% maximum, the user may consider using the DAC code range between 100d and 4000d instead of using full code range (code 0 to 4095d). The DAC output of the code range between 100d and 4000d is much more linear than full-scale range (0 to 4095d). The gain error can be calibrated out by software in the application.

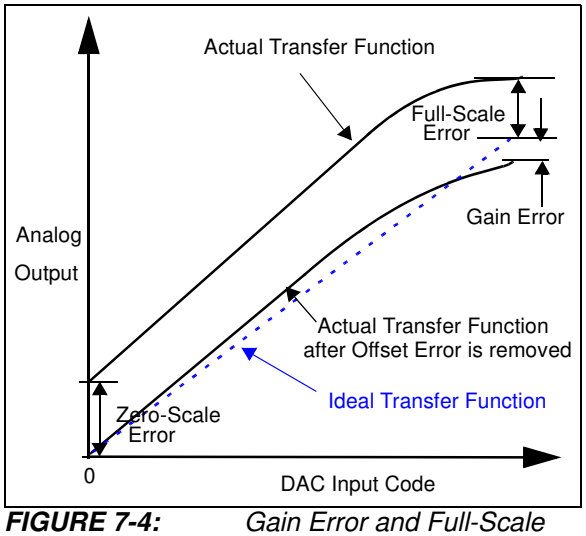


FIGURE 7-4: *Gain Error and Full-Scale Error Example.*

7.10 Gain Error Drift

The Gain error drift is the variation in gain error due to a change in ambient temperature. The gain error drift is typically expressed in ppm/^{o}C.

7.11 Offset Error Drift

The Offset error drift is the variation in offset error due to a change in ambient temperature. The offset error drift is typically expressed in ppm/^{o}C.

7.12 Settling Time

The Settling time is the time delay required for the V_{OUT} voltage to settle into its new output value. This time is measured from the start of code transition, to when the V_{OUT} voltage is within the specified accuracy.

In the MCP47X6, the settling time is a measure of the time delay until the V_{OUT} voltage reaches within 0.5 LSb of its final value, when the volatile DAC Register changes from 400h to C00h.

7.13 Major-Code Transition Glitch

Major-code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-Sec, and is measured when the digital code is changed by 1 LSb at the major carry transition (Example: `011...111` to `100...000`, or `100... 000` to `011 ... 111`).

7.14 Digital Feedthrough

The Digital feedthrough is the glitch that appears at the analog output caused by coupling from the digital input pins of the device. The area of the glitch is expressed in nV-Sec, and is measured with a full scale change (Example: all `0`s to all `1`s and vice versa) on the digital input pins. The digital feedthrough is measured when the DAC is not being written to the output register.

7.15 Power-Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. The V_{OUT} is measured while the V_{DD} is varied +/- 10%, and expressed in dB or µV/V.

NOTES:

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8.0 TYPICAL APPLICATIONS

The MCP47X6 family of devices are general purpose, single channel voltage output DACs for various applications where a precision operation with low-power and nonvolatile EEPROM memory is needed.

Since the devices include a nonvolatile EEPROM memory, the user can utilize these devices for applications that require the output to return to the previous set-up value on subsequent power-ups.

Applications generally suited for the devices are:

- Set Point or Offset Trimming
- Sensor Calibration
- Portable Instrumentation (Battery Powered)
- Motor Control

8.1 Connecting to I²C BUS using Pull-Up Resistors

The SCL and SDA pins of the MCP47X6 devices are open-drain configurations. These pins require a pull-up resistor as shown in Figure 8-2.

The pull-up resistor values (R1 and R2) for SCL and SDA pins depend on the operating speed (standard, fast, and high speed) and loading capacitance of the I²C bus line. A higher value of the pull-up resistor consumes less power, but increases the signal transition time (higher RC time constant) on the bus line. Therefore, it can limit the bus operating speed. The lower resistor value, on the other hand, consumes higher power, but allows higher operating speed. If the bus line has higher capacitance due to long metal traces or multiple device connections to the bus line, a smaller pull-up resistor is needed to compensate the long RC time constant. The pull-up resistor is typically chosen between 1 kΩ and 10 kΩ ranges for standard and fast modes, and less than 1 kΩ for high speed mode.

8.1.1 DEVICE CONNECTION TEST

The user can test the presence of the device on the I²C bus line using a simple I²C command. This test can be achieved by checking an acknowledge response from the device after sending a read or write command. Figure 8-1 shows an example with a read command. The steps are:

a) Set the R/$\overline{W}$ bit “High” in the device’s address byte.

b) Check the ACK bit of the address byte.
If the device acknowledges (ACK = 0) the command, then the device is connected, otherwise it is not connected.

c) Send Stop bit.

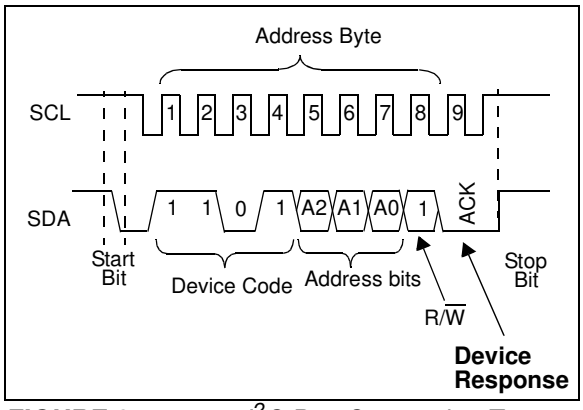
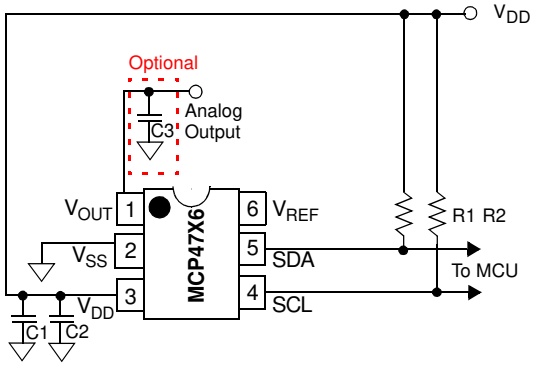


FIGURE 8-1: *I²C Bus Connection Test.*

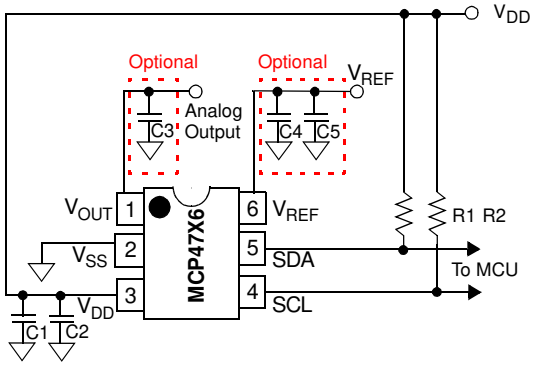
8.2 Power Supply Considerations

The power source should be as clean as possible. The power supply to the device is also used for the DAC voltage reference internally if the internal V_{DD} is selected as the resistor ladders reference voltage (VREF1:VREF0 = 00 or 01).

Any noise induced on the V_{DD} line can affect the DAC performance. Typical applications will require a bypass capacitor in order to filter out high frequency noise on the V_{DD} line. The noise can be induced onto the power supply's traces or as a result of changes on the DAC output. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-2 shows an example of using two bypass capacitors (a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor) in parallel on the V_{DD} line. These capacitors should be placed as close to the V_{DD} pin as possible (within 4 mm). If the application circuit has separate digital and analog power supplies, the V_{DD} and V_{SS} pins of the device should reside on the analog plane.



(a) Circuit when V_{DD} is selected as reference
(**Note:** V_{DD} is connected to the reference circuit internally.)



(b) Circuit when external reference is used.

R1 and R2 are I^2C pull-up resistors:

R1 and R2:

5 kΩ - 10 kΩ for f_{SCL}	=	100 kHz to 400 kHz
~700Ω for f_{SCL}	=	3.4 MHz
C1: 0.1 µF capacitor		Ceramic
C2: 10 µF capacitor		Tantalum
C3: ~ 0.1 µF		Optional to reduce noise in VOUT pin.
C4: 0.1 µF capacitor		Ceramic
C5: 10 µF capacitor		Tantalum

Note: *Pin assignment is opposite in DFN-6 package.*

FIGURE 8-2: *Example MCP47X6 Circuit with SOT-23 package.*

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8.3 Application Examples

The MCP47X6 devices are rail-to-rail output DACs designed to operate with a V_{DD} range of 2.7V to 5.5V. The internal output op amplifier is robust enough to drive common, small-signal loads directly, thus eliminating the cost and size of external buffers for most applications. The user can use gain of 1 or 2 of the output op amplifier by setting the configuration register bits. Also, the user can use internal V_{DD} as the reference or use external reference. Various user options and easy-to-use features make the devices suitable for various modern DAC applications.

Application examples include:

- Decreasing Output Step Size
- Building a “Window” DAC
- Bipolar Operation
- Selectable Gain and Offset Bipolar Voltage Output
- Designing a Double-Precision DAC
- Building Programmable Current Source
- Serial Interface Communication Times
- Software I2C Interface Reset Sequence
- Power Supply Considerations
- Layout Considerations

8.3.1 DC SET POINT OR CALIBRATION

A common application for the devices is a digitally-controlled set point and/or calibration of variable parameters, such as sensor offset or slope. For example, the MCP4726 provides 4096 output steps. If voltage reference is 4.096V, the LSb size is 1 mV. If a smaller output step size is desired, a lower external voltage reference is needed.

8.3.1.1 Decreasing Output Step Size

If the application is calibrating the bias voltage of a diode or transistor, a bias voltage range of 0.8V may be desired with about 200 µV resolution per step. Two common methods to achieve small step size are using lower V_{REF} pin voltage or using a voltage divider on the DAC’s output.

Using an external voltage reference (V_{REF}) is an option, if the external reference is available with the desired output voltage range. However, occasionally, when using a low-voltage reference voltage, the noise floor causes a SNR error that is intolerable. Using a voltage divider method is another option, and provides some advantages when external voltage reference needs to be very low, or when the desired output voltage is not available. In this case, a larger value reference voltage is used, while two resistors scale the output range down to the precise desired level.

Figure 8-3 illustrates this concept. A bypass capacitor on the output of the voltage divider plays a critical function in attenuating the output noise of the DAC and the induced noise from the environment.

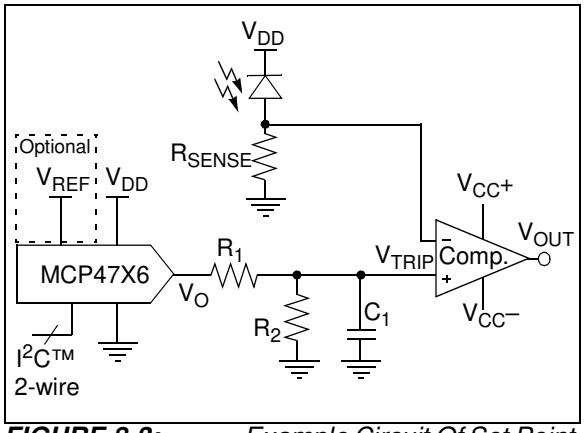


FIGURE 8-3: *Example Circuit Of Set Point or Threshold Calibration.*

EQUATION 8-1: V_{OUT} AND V_{TRIP} CALCULATIONS

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{\text{DAC Register Value}}{2^N}$$

$$V_{trip} = V_{OUT}\left(\frac{R_2}{R_1 + R_2}\right)$$

8.3.1.2 Building a “Window” DAC

When calibrating a set point or threshold of a sensor, typically only a small portion of the DAC output range is utilized. If the LSb size is adequate enough to meet the application’s accuracy needs, the unused range is sacrificed without consequences. If greater accuracy is needed, then the output range will need to be reduced to increase the resolution around the desired threshold.

If the threshold is not near V_{REF}, 2 • V_{REF}, or V_{SS} then creating a “window” around the threshold has several advantages. One simple method to create this “window” is to use a voltage divider network with a pull-up and pull-down resistor. Figure 8-4 and Figure 8-6 illustrate this concept.

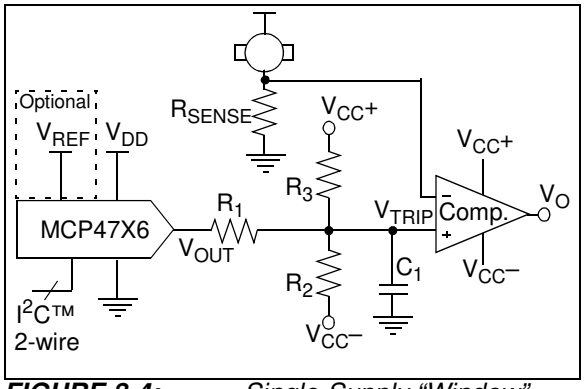


FIGURE 8-4: *Single-Supply “Window” DAC.*

EQUATION 8-2: V_{OUT} AND V_{TRIP} CALCULATIONS

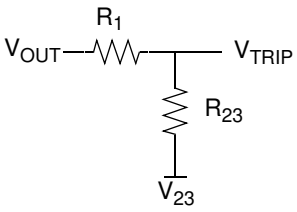
$$V_{OUT} = V_{REF} \bullet G \bullet \frac{\text{DAC Register Value}}{2^N}$$

$$V_{TRIP} = \frac{V_{OUT}R_{23} + V_{23}R_1}{R_1 + R_{23}}$$

Thevenin Equivalent:

$$R_{23} = \frac{R_2R_3}{R_2 + R_3}$$

$$V_{23} = \frac{(V_{CC+}R_2) + (V_{CC-}R_3)}{R_2 + R_3}$$



8.4 Bipolar Operation

Bipolar operation is achievable by utilizing an external operational amplifier. This configuration is desirable due to the wide variety and availability of op amps. This allows a general purpose DAC, with its cost and availability advantages, to meet almost any desired output voltage range, power and noise performance.

Figure 8-5 illustrates a simple bipolar voltage source configuration. R_1 and R_2 allow the gain to be selected, while R_3 and R_4 shift the DAC's output to a selected offset. Note that R4 can be tied to V_{DD}, instead of V_{SS}, if a higher offset is desired.

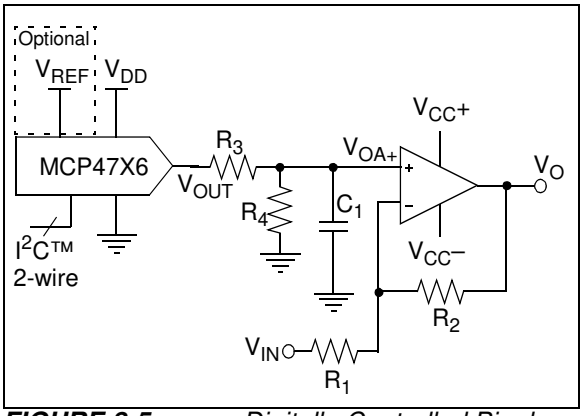


FIGURE 8-5: *Digitally-Controlled Bipolar Voltage Source Example Circuit.*

EQUATION 8-3: V_{OUT}, V_{OA+}, AND V_O CALCULATIONS

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{\text{DAC Register Value}}{2^N}$$

$$V_{OA+} = \frac{V_{OUT} \bullet R_4}{R_3 + R_4}$$

$$V_O = V_{OA+} \bullet \left(1 + \frac{R_2}{R_1}\right) - V_{DD} \bullet \left(\frac{R_2}{R_1}\right)$$

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8.5 Selectable Gain and Offset Bipolar Voltage Output

In some applications, precision digital control of the output range is desirable. Example 8-6 illustrates how to use the DAC devices to achieve this in a bipolar or single-supply application.

This circuit is typically used for linearizing a sensor whose slope and offset varies.

The equation to design a bipolar "window" DAC would be utilized if R_3, R_4 and R_5 are populated.

8.5.1 BIPOLAR DAC EXAMPLE USING MCP4726

An output step size of 1 mV, with an output range of ±2.05V, is desired for a particular application.

Step 1: Calculate the range: +2.05V – (-2.05V) = 4.1V.

Step 2: Calculate the resolution needed:

4.1V/1 mV = 4100

Since 2^{12} = 4096, 12-bit resolution is desired.

Step 3: The amplifier gain (R_2/R_1), multiplied by full-scale V_{OUT} (4.096V), must be equal to the desired minimum output to achieve bipolar operation. Since any gain can be realized by choosing resistor values (R_1+R_2), the V_{REF} value must be selected first. If a V_{REF} of 4.096V is used, solve for the amplifier's gain by setting the DAC to 0, knowing that the output needs to be -2.05V.

The equation can be simplified to:

$$\frac{-R_2}{R_1} = \frac{-2.05}{4.096V} \qquad \frac{R_2}{R_1} = \frac{1}{2}$$

If R_1 = 20 kΩ and R_2 = 10 kΩ, the gain will be 0.5.

Step 4: Next, solve for R_3 and R_4 by setting the DAC to 4096, knowing that the output needs to be +2.05V.

$$\frac{R_4}{(R_3 + R_4)} = \frac{2.05V + (0.5 \cdot 4.096V)}{1.5 \cdot 4.096V} = \frac{2}{3}$$

If R_4 = 20 kΩ, then R_3 = 10 kΩ

Figure 8-6 (C1 = 0.1uF)

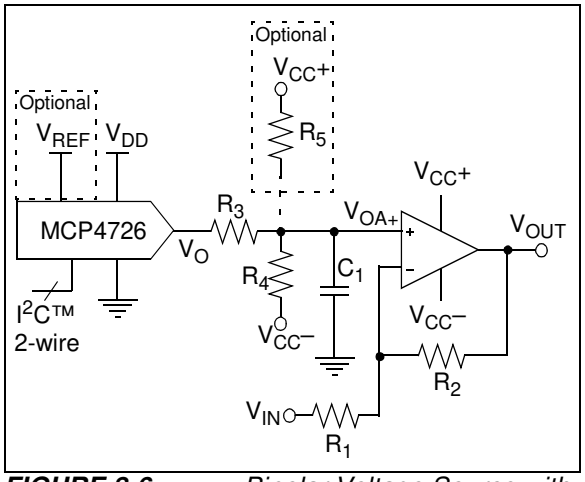


FIGURE 8-6: *Bipolar Voltage Source with Selectable Gain and Offset.*

EQUATION 8-4: V_{OUT}, V_{OA+}, AND V_O CALCULATIONS

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{\text{DAC Register Value}}{2^N}$$

$$V_{OA+} = \frac{V_{OUT} \bullet R_4 + V_{CC-} \bullet R_5}{R_3 + R_4}$$

$$V_O = \underbrace{V_{OA+} \bullet \left(1 + \frac{R_2}{R_1}\right)}_{\text{Offset Adjust}} \underbrace{- V_{IN} \bullet \left(\frac{R_2}{R_1}\right)}_{\text{Gain Adjust}}$$

EQUATION 8-5: BIPOLAR "WINDOW" DAC USING R_4 AND R_5

Thevenin Equivalent

$$V_{45} = \frac{V_{CC+}R_4 + V_{CC-}R_5}{R_4 + R_5}$$

$$V_{IN+} = \frac{V_{OUT}R_{45} + V_{45}R_3}{R_3 + R_{45}}$$

$$R_{45} = \frac{R_4R_5}{R_4 + R_5}$$

$$V_O = \underbrace{V_{IN+}\left(1 + \frac{R_2}{R_1}\right)}_{\text{Offset Adjust}} \underbrace{- V_A\left(\frac{R_2}{R_1}\right)}_{\text{Gain Adjust}}$$

8.6 Designing a Double-Precision DAC

Figure 8-7 shows an example design of a single-supply voltage output capable of up to 24-bit resolution. This requires two 12-bit DACs. This design is simply a voltage divider with a buffered output.

As an example, if a similar application to the one developed in **Section 8.5.1 "Bipolar DAC Example Using MCP4726"** required a resolution of 1 µV instead of 1 mV, and a range of 0V to 4.1V, then 12-bit resolution would not be adequate.

Step 1: Calculate the resolution needed:

4.1V/1 µV = 4.1 x 10^6. Since 2^{22} = 4.2 x 10^6, 22-bit resolution is desired. Since DNL = ±0.75 LSb, this design can be attempted with the 12-bit DAC.

Step 2: Since DAC_B's V_{OUTB} has a resolution of 1 mV, its output only needs to be "pulled" 1/1000 to meet the 1 µV target. Dividing V_{OUTA} by 1000 would allow the application to compensate for DAC_B's DNL error.

Step 3: If R_2 is 100Ω, then R_1 needs to be 100 kΩ.

Step 4: The resulting transfer function is shown in the equation of Example 8-6.

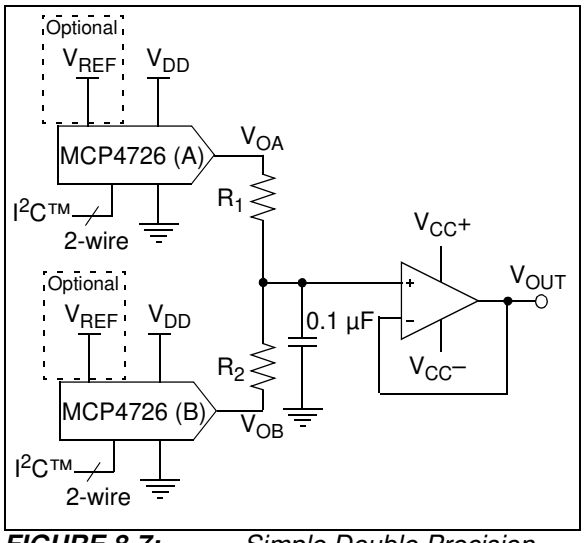


FIGURE 8-7: *Simple Double Precision DAC using MCP4726.*

EQUATION 8-6: V_{OUT} CALCULATION

$$V_{OUT} = \frac{V_{OA} * R_2 + V_{OB} * R_1}{R_1 + R_2}$$

Where:

V_{OA} = (V_{REF} * G * DAC A Register Value)/4096

V_{OB} = (V_{REF} * G * DAC B Register Value)/4096

G = Selected Op Amp Gain

8.7 Building Programmable Current Source

Example 8-8 shows an example of building programmable current source using a voltage follower. The current sensor resistor is used to convert the DAC voltage output into a digitally-selectable current source.

The smaller R_{SENSE} is, the less power dissipated across it. However, this also reduces the resolution that the current can be controlled.

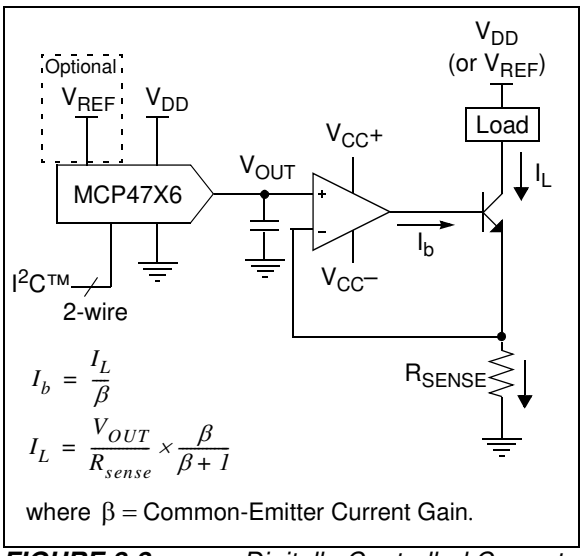


FIGURE 8-8: *Digitally-Controlled Current Source.*

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8.8 Serial Interface Communication Times

Table 8-1 shows time/frequency of the supported operations of the I^2C serial interface for the different serial interface operational frequencies. This, along with the V_{OUT} output performance (such as slew rate), would be used to determine your applications volatile DAC register update rate.

TABLE 8-1: SERIAL INTERFACE TIMES / FREQUENCIES

Command				Writes Volatile Memory?		Writes EEPROM Memory?		# of Serial Interface bits (2)	Command Time (uS)			Command Frequency (kHz)		
Code			Function	Config.	DAC	Config.	DAC		100kHz	400kHz	3.4MHz	100kHz	400kHz	3.4MHz
C2	C1	C0												
0	0	x	Write Volatile DAC	Yes(1)	Yes	No	No	29	290	72.5	8.5	3.4	13.8	117.2
0	1	0	Write Volatile Memory	Yes	Yes	No	No	38	380	95	11.2	2.6	10.5	89.5
0	1	1	Write All Memory	Yes	Yes	Yes	Yes	38	380	95	11.2	2.6	10.5	89.5
1	0	0	Write NV Configuration Bits	Yes	No	No	No	20	200	50	5.9	5.0	20.0	170.0
N.A.			Read	N.A.	N.A.	N.A.	N.A.	77	750	187.5	22.1	1.3	5.3	45.3

Note 1: Only the volatile PD1:PD0 bits of the Configuration bits are written.

2: Includes the Start or Stop bits.

8.9 Software I²C Interface Reset Sequence

Note: This technique is documented in AN1028.

At times, it may become necessary to perform a Software Reset Sequence to ensure the MCP47X6 device is in a correct and known I²C Interface state. This technique only resets the I²C state machine.

This is useful if the MCP47X6 device powers up in an incorrect state (due to excessive bus noise, etc), or if the Master Device is reset during communication. Figure 8-9 shows the communication sequence to software reset the device.

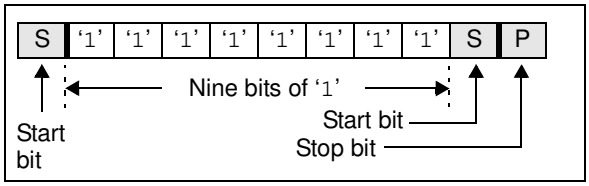


FIGURE 8-9: *Software Reset Sequence Format.*

The 1st Start bit will cause the device to reset from a state in which it is expecting to receive data from the Master Device. In this mode, the device is monitoring the data bus in Receive mode and can detect if the Start bit forces an internal Reset.

The nine bits of '1' are used to force a Reset of those devices that could not be reset by the previous Start bit. This occurs only if the MCP47X6 is driving an A bit on the I²C bus, or is in output mode (from a Read command) and is driving a data bit of '0' onto the I²C bus. In both of these cases, the previous Start bit could not be generated due to the MCP47X6 holding the bus low. By sending out nine '1' bits, it is ensured that the device will see an $\overline{A}$ bit (the Master Device does not drive the I²C bus low to acknowledge the data sent by the MCP47X6), which also forces the MCP47X6 to reset.

The 2nd Start bit is sent to address the rare possibility of an erroneous write. This could occur if the Master Device was reset while sending a Write command to the MCP47X6, AND then as the Master Device returns to normal operation and issues a Start condition, while the MCP47X6 is issuing an Acknowledge. In this case, if the 2nd Start bit is not sent (and the Stop bit was sent) the MCP47X6 could initiate a write cycle.

Note: The potential for this erroneous write ONLY occurs if the Master Device is reset while sending a Write command to the MCP47X6.

The Stop bit terminates the current I²C bus activity. The MCP47X6 waits to detect the next Start condition.

This sequence does not effect any other I²C devices which may be on the bus, as they should disregard this as an invalid command.

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8.10 Design Considerations

In the design of a system with the MCP4706/4716/4726 devices, the following considerations should be taken into account:

- **Power Supply Considerations**
- **Layout Considerations**

8.10.1 POWER SUPPLY CONSIDERATIONS

The typical application will require a bypass capacitor in order to filter high-frequency noise, which can be induced onto the power supply's traces. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-10 illustrates an appropriate bypass strategy.

In this example, the recommended bypass capacitor value is 0.1 µF. This capacitor should be placed as close (within 4 mm) to the device power pin (V_{DD}) as possible.

The power source supplying these devices should be as clean as possible. If the application circuit has separate digital and analog power supplies, V_{DD} and V_{SS} should reside on the analog plane.

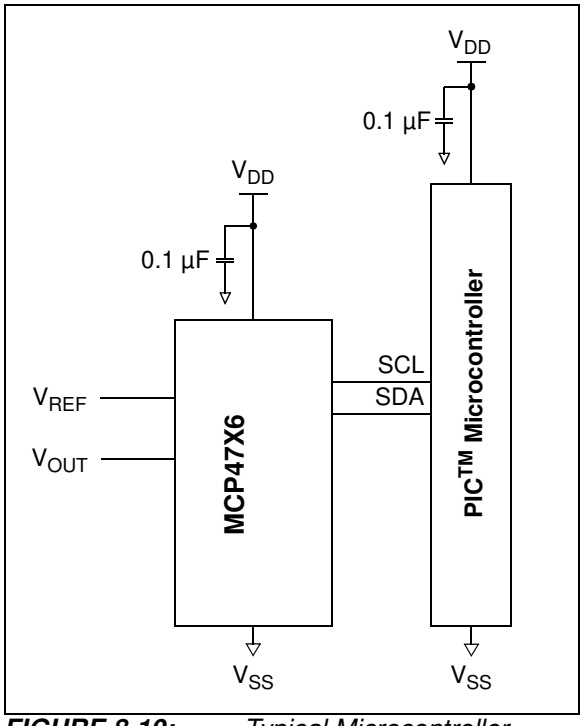


FIGURE 8-10: *Typical Microcontroller Connections.*

8.10.2 LAYOUT CONSIDERATIONS

Several layout considerations may be applicable to your application. These may include:

- **Noise**
- **PCB Area Requirements**

8.10.2.1 Noise

Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP47X6's performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR). Multi-layer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing. Particularly harsh environments may require shielding of critical signals.

Separate digital and analog ground planes are recommended. In this case, the V_{SS} pin and the ground pins of the V_{DD} capacitors should be terminated to the analog ground plane.

Note:	Breadboards and wire-wrapped boards are not recommended.

8.10.2.2 PCB Area Requirements

In some applications, PCB area is a criteria for device selection. Table 8-2 shows the typical package dimensions and area for the different package options. The table also shows the relative area factor compared to the smallest area. For space critical applications, the DFN package would be the suggested package.

TABLE 8-2: PACKAGE FOOTPRINT (1)

Package			Package Footprint			
Pins	Type	Code	Dimensions (mm)		Area (mm^2)	Relative Area
			Length	Width		
6	SOT-23	CH	2.90	2.70	7.83	1.96
6	DFN	MA	2.00	2.00	4.00	1

Note 1: Does not include recommended land pattern dimensions. Dimensions are typical values.

NOTES:

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9.0 DEVELOPMENT SUPPORT

Development support can be classified into two groups. These are:

- Development Tools
- Technical Documentation

9.1 Development Tools

Several development tools are available to assist in your design and evaluation of the MCP47X6 devices. The currently available tools are shown in Table 9-1.

These boards may be purchased directly from the Microchip web site at www.microchip.com.

9.1.1 MCP47X6 PICTAIL PLUS DAUGHTER BOARD

The MCP47X6 PICtail Plus Daughter Board (Order Number: ADM00317) is available from Microchip Technology Inc. This board works with Microchip's PICkit™ Serial Analyzer and PIC Explorer 16 Development Board. The firmware example is also available for the Explore 16 Development Board with PIC24FJ128.

Figure 9-1 shows the MCP47X6 PICtail Plus Daughter Board being used with a PIC Explorer 16 Development Board (order #: ADM00317), while Figure 9-2 shows the MCP47X6 PICtail Plus Daughter Board being used with a PICkit™ Serial Analyzer. The PICkit™ Serial Analyzer allows the user to quickly evaluate the DAC operation. Refer to the MCP47X6 PICtail Plus Daughter Board User's Guide for detailed descriptions on operating the daughter board.

Refer to www.microchip.com for further information on this product and related material for the users.

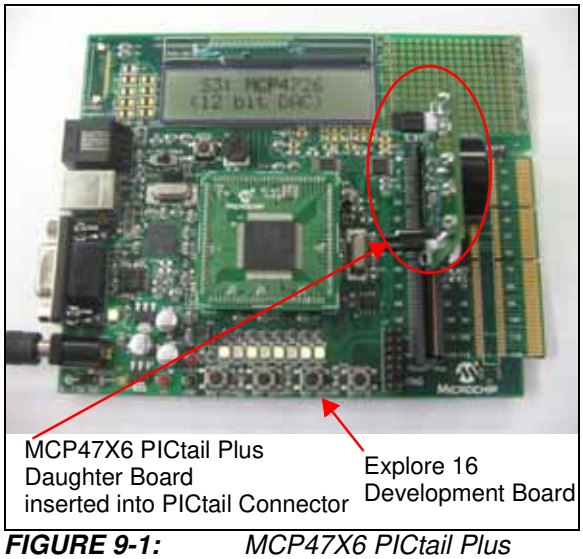


FIGURE 9-1: *MCP47X6 PICtail Plus Daughter Board with PIC Explorer 16 Development Board.*

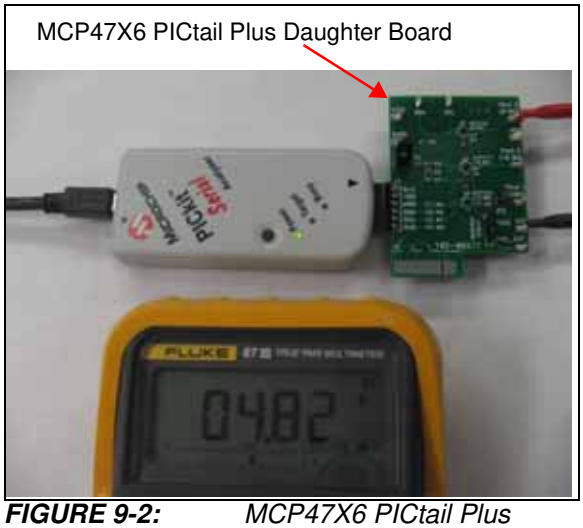


FIGURE 9-2: *MCP47X6 PICtail Plus Daughter Board with PICkit™ Serial Analyzer.*

TABLE 9-1: DEVELOPMENT TOOLS

Board Name	Part #	Supported Devices
6-pin SC70 Evaluation Board	SC70EV	MCP4706, MCP4716, MCP4726
MCP4706/4716/4726 Evaluation Board(1, 2)	ADM00317(3)	MCP4726

Note 1: Requires a PICDEM Demo board. See the User's Guide for additional information and requirements.

2: Requires a PICkit Serial Analyzer. See the User's Guide for additional information and requirements.

3: This board is currently in the manufacturing cycle, and should be available by end of March 2011.

9.2 Technical Documentation

Several additional technical documents are available to assist you in your design and development. These technical documents include Application Notes, Technical Briefs, and Design Guides. Table 9-2 shows some of these documents.

TABLE 9-2: TECHNICAL DOCUMENTATION

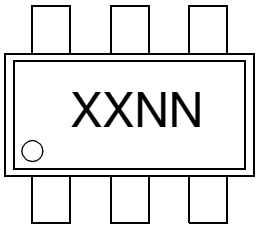
Application Note Number	Title	Literature #
AN1326	Using DAC for LDMOS Amplifier Bias Control Applications	DS01326
—	Signal Chain Design Guide	DS21825
—	Analog Solutions for Automotive Applications Design Guide	DS01005

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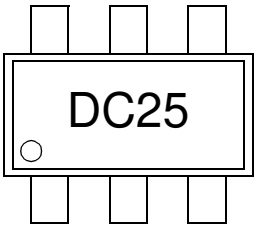
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

6-Lead SOT-23

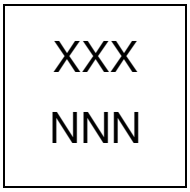


Example

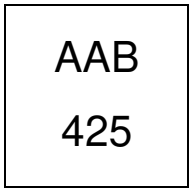


Address Option	Code		
	MCP4706A0T-E/CH	MCP4716A0T-E/CH	MCP4726A0T-E/CH
A0 (00)	DBNN	DFNN	DKNN
A1 (01)	DCNN	DGNN	DLNN
A2 (10)	DDNN	DHNN	DMNN
A3 (11)	DENN	DJNN	DPNN

6-Lead DFN (2x2)



Example



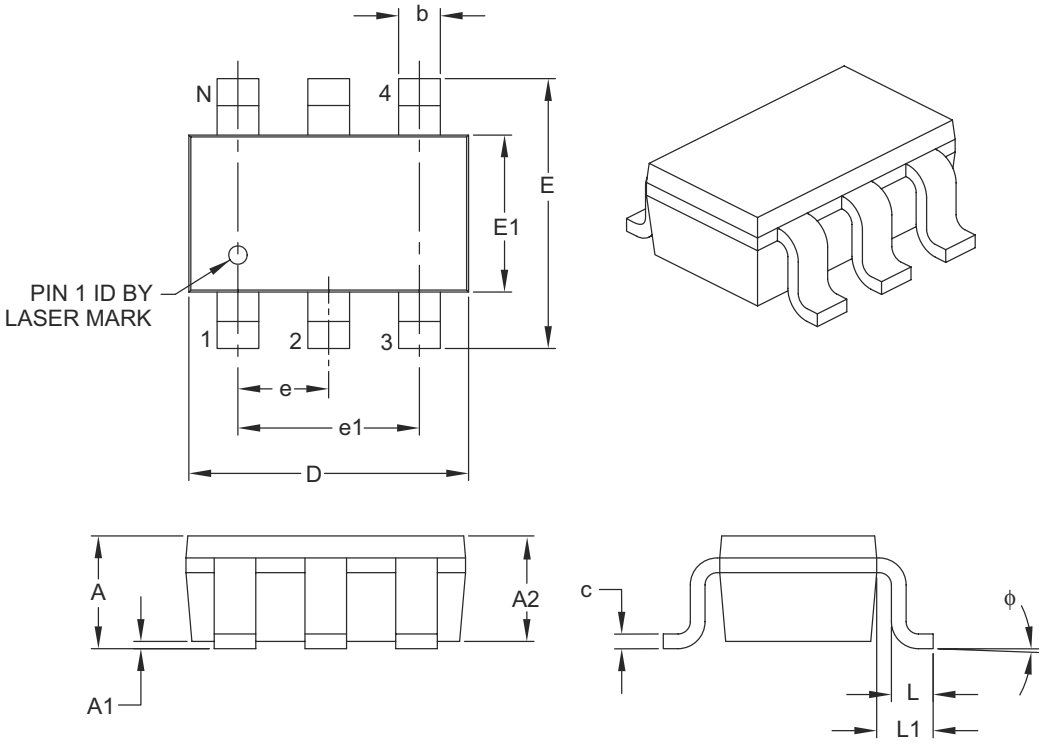
Address Option	Code		
	MCP4706A0T-E/MA	MCP4716A0T-E/MA	MCP4726A0T-E/MA
A0 (00)	AAA	AAE	AAP
A1 (01)	AAB	AAF	AAQ
A2 (10)	AAC	AAG	AAR
A3 (11)	AAD	AAH	AAS

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

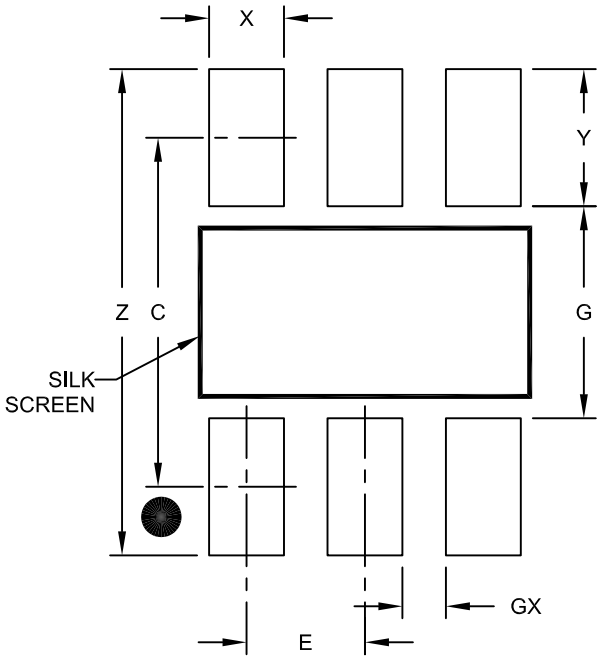
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

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6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

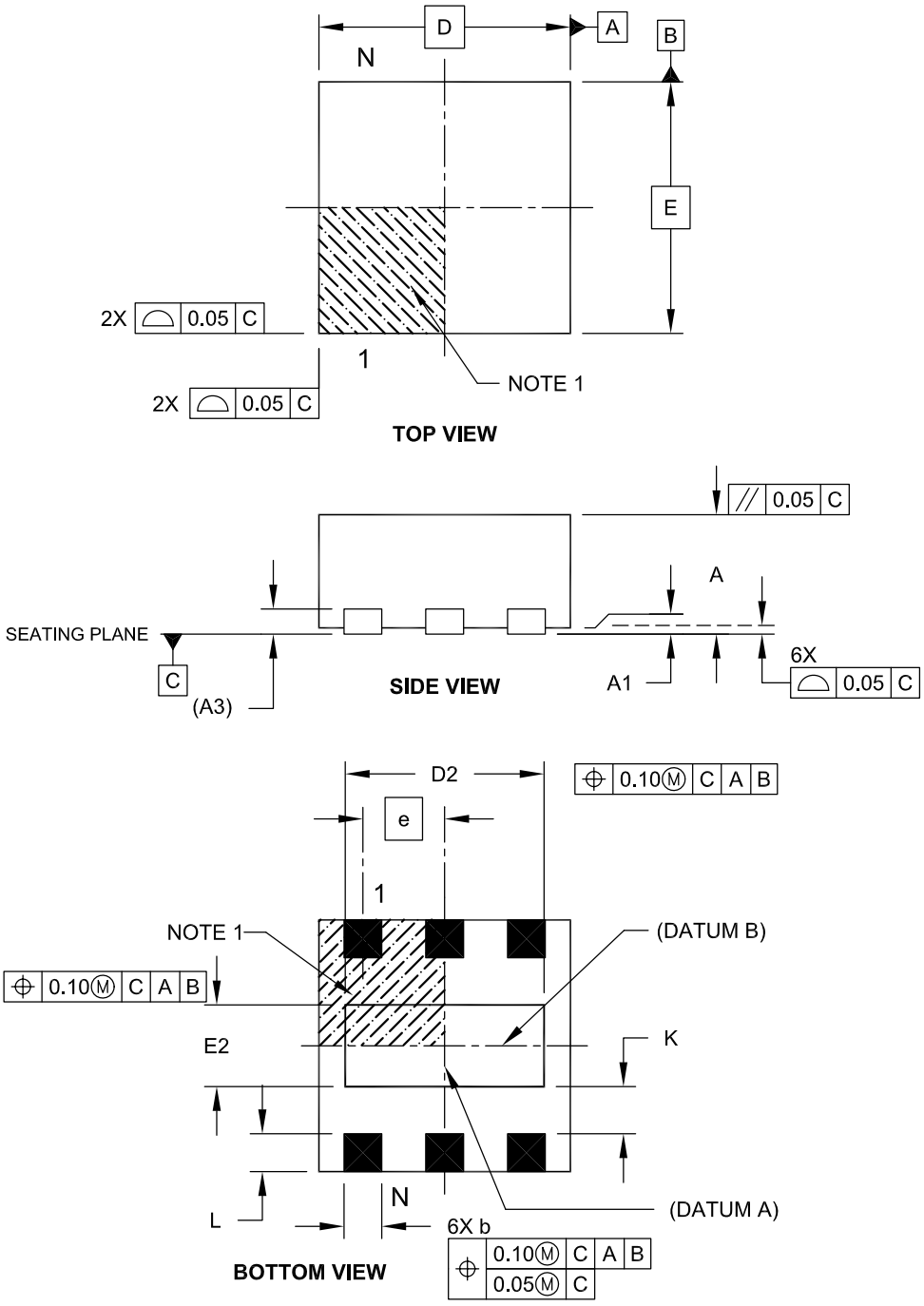
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A

6-Lead Plastic Dual Flat, No Lead Package (MA) - 2x2x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

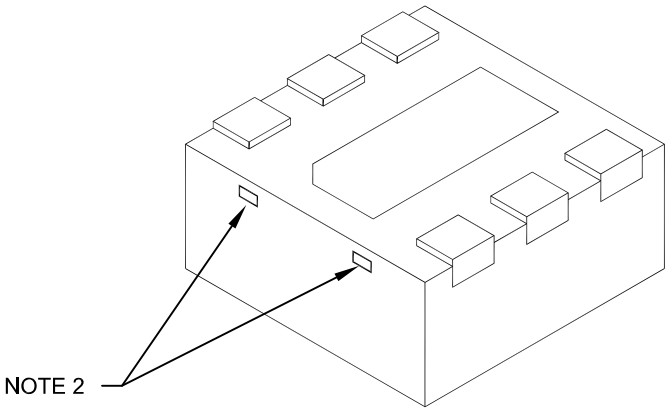


Microchip Technology Drawing C04-120B Sheet 1 of 2

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6-Lead Plastic Dual Flat, No Lead Package (MA) - 2x2x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		2.00 BSC	
Exposed Pad Length	D2	1.50	1.60	1.70
Exposed Pad Width	E2	0.90	1.00	1.10
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

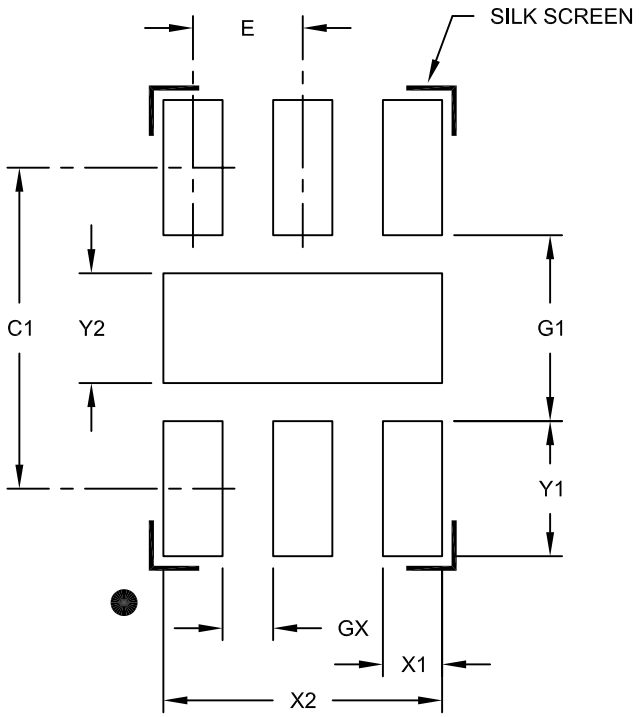
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-120B Sheet 2 of 2

6-Lead Plastic Dual Flat, No Lead Package (MA) - 2x2x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	Y2			1.00
Optional Center Pad Length	X2			1.70
Contact Pad Spacing	C1		2.10	
Contact Pad Width (X6)	X1			0.35
Contact Pad Length (X6)	Y1			0.65
Distance Between Pads	GX	0.20		
Distance Between Pads	G1	1.10		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2120A

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APPENDIX A: REVISION HISTORY

Revision A (February 2011)

- Original Release of this Document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	X	—	X	/XX
Device	Address Options	Tape and Reel		Temperature Range	Package

Device:	MCP4706:	Single Channel 8-Bit DAC with EEPROM Memory	
	MCP4716:	Single Channel 10-Bit DAC with EEPROM Memory	
	MCP4726:	Single Channel 12-Bit DAC with EEPROM Memory	
Address Options:	A0 =	"1100000" I^2C Address. Devices ordered from the Microchip Sample center will have this address.	
	A1 =	"1100001" I^2C Address.	
	A2 =	"1100010" I^2C Address.	
	A3 =	"1100011" I^2C Address.	
	A4 =	"1100100" I^2C Address.	
	A5 =	"1100101" I^2C Address.	
	A6 =	"1100110" I^2C Address.	
	A7 =	"1100111" I^2C Address.	
Tape and Reel:	T =	Tape and Reel	
Temperature Range:	E =	-40°C to +125°C	
Package:	CH =	Plastic Small Outline Transistor (SOT-23-6), 6-lead	
	MA =	Plastic Dual Flat, No Lead Package (2x2 DFN), 6-lead	

Examples:

a) MCP4706A0T-E/CH: 8-bit V_{OUT} resolution, I^2C Address "1100000", Tape and Reel, Extended Temp., 6LD SOT-23 pkg.

b) MCP4706A6T-E/CH: 8-bit V_{OUT} resolution, I^2C Address "1100110", Tape and Reel, Extended Temp., 6LD SOT-23 pkg.

c) MCP4706A0T-E/MA: 8-bit V_{OUT} resolution, I^2C Address "1100000", Tape and Reel, Extended Temp., 6LD DFN pkg.

d) MCP4706A6T-E/MA: 8-bit V_{OUT} resolution, I^2C Address "1100110", Tape and Reel, Extended Temp., 6LD DFN pkg.

a) MCP4716A0T-E/CH: 10-bit V_{OUT} resolution, I^2C Address "1100000", Tape and Reel, Extended Temp., 6LD SOT-23 pkg.

b) MCP4716A6T-E/CH: 10-bit V_{OUT} resolution, I^2C Address "1100110", Tape and Reel, Extended Temp., 6LD SOT-23 pkg.

c) MCP4716A0T-E/MA: 10-bit V_{OUT} resolution, I^2C Address "1100000", Tape and Reel, Extended Temp., 6LD DFN pkg.

d) MCP4716A6T-E/MA: 10-bit V_{OUT} resolution, I^2C Address "1100110", Tape and Reel, Extended Temp., 6LD DFN pkg.

a) MCP4726A0T-E/CH: 12-bit V_{OUT} resolution, I^2C Address "1100000", Tape and Reel, Extended Temp., 6LD SOT-23 pkg.

b) MCP4726A6T-E/CH: 12-bit V_{OUT} resolution, I^2C Address "1100110", Tape and Reel, Extended Temp., 6LD SOT-23 pkg.

c) MCP4726A0T-E/MA: 12-bit V_{OUT} resolution, I^2C Address "1100000", Tape and Reel, Extended Temp., 6LD DFN pkg.

d) MCP4726A6T-E/MA: 12-bit V_{OUT} resolution, I^2C Address "1100110", Tape and Reel, Extended Temp., 6LD DFN pkg.

NOTES:

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ISBN: 978-1-60932-896-2

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