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RGB to NTSC/PAL Encoder

AD724

FEATURES
Low Cost, Integrated Solution
+5 V Operation
Accepts FSC Clock or Crystal, or 4FSC Clock
Composite Video and Separate Y/C (S-Video) Outputs
Luma and Chroma Outputs Are Time Aligned
Minimal External Components:
No External Filters or Delay Lines Required
Onboard DC Clamp
Accepts Either HSYNC and VSYNC or CSYNC
Phase Lock to External Subcarrier
Drives 75 Ω Reverse-Terminated Loads
Logic Selectable NTSC or PAL Encoding Modes
Compact 16-Lead SOIC

APPLICATIONS
RGB to NTSC or PAL Encoding

PRODUCT DESCRIPTION

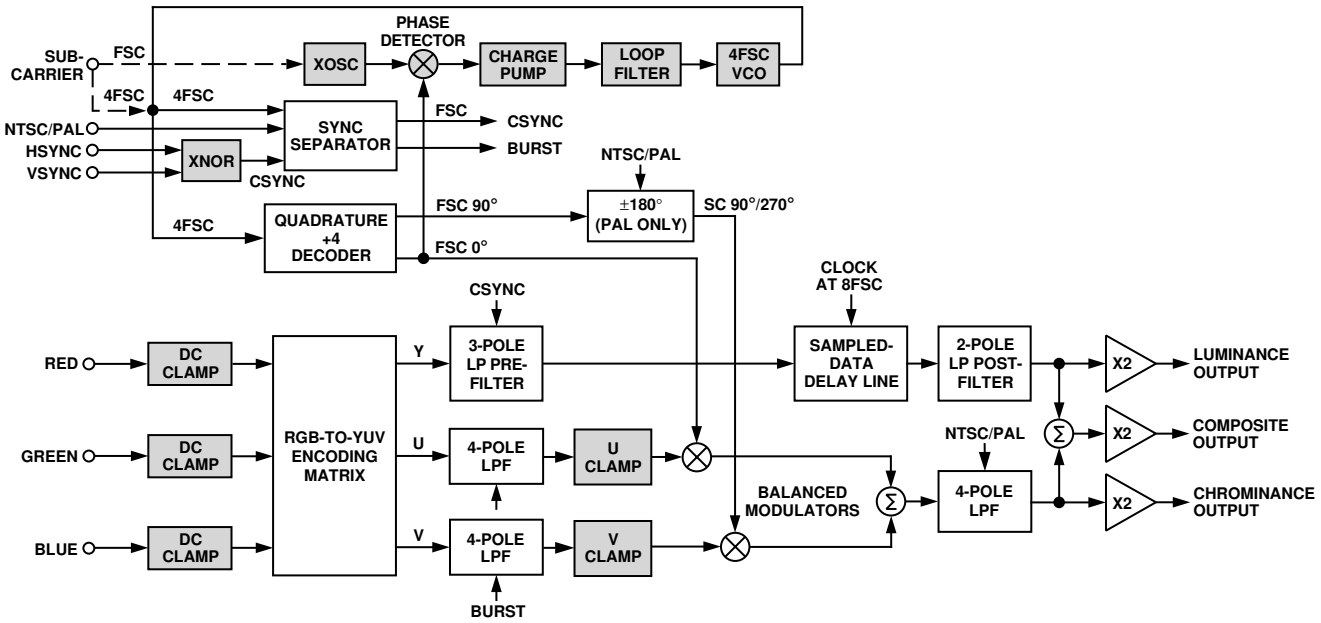
The AD724 is a low cost RGB to NTSC/PAL Encoder that converts red, green and blue color component signals into their corresponding luminance (baseband amplitude) and chrominance (subcarrier amplitude and phase) signals in accordance with either NTSC or PAL standards. These two outputs are also combined to provide composite video output. All three outputs can simultaneously drive 75 Ω, reverse-terminated cables. All logical inputs are TTL, 3 V and 5 V CMOS compatible. The chip operates from a single +5 V supply. No external delay lines or filters are required. The AD724 may be powered down when not in use.

The AD724 accepts either FSC or 4FSC clock. When a clock is not available, a low cost parallel-resonant crystal (3.58 MHz (NTSC) or 4.43 MHz (PAL)) and the AD724's on-chip oscillator generate the necessary subcarrier clock. The AD724 also accepts the subcarrier clock from an external video source.

The interface to graphics controllers is simple: an on-chip logic "XNOR" accepts the available vertical (VSYNC) and horizontal sync (HSYNC) signals and creates the composite sync (CSYNC) signal on-chip. If available, the AD724 will also accept a standard CSYNC signal by connecting VSYNC to Logic HI and applying CSYNC to the HSYNC pin. The AD724 contains decoding logic to identify valid horizontal sync pulses for correct burst insertion.

Delays in the U and V chroma filters are matched by an on-chip sampled-data delay line in the Y signal path. To prevent aliasing, a prefilter at 5 MHz is included ahead of the delay line and a post-filter at 5 MHz is added after the delay line to suppress harmonics in the output. These low-pass filters are optimized for minimum pulse overshoot. The overall luma delay, relative to chroma, has been designed to be time aligned for direct input to a television's baseband. The AD724 comes in a space-saving SOIC and is specified for the 0°C to +70°C commercial temperature range.

FUNCTIONAL BLOCK DIAGRAM



REV. B

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AD724–SPECIFICATIONS (Unless otherwise noted, V_S = +5, T_A = +25°C, using FSC synchronous clock. All loads are 150 Ω ± 5% at the IC pins. Outputs are measured at the 75 Ω reverse terminated load.)

Parameter	Conditions	Min	Typ	Max	Units
SIGNAL INPUTS (RIN, GIN, BIN)					
Input Amplitude	Full Scale			714	mV p-p
Black Level[1]			0.8		V
Input Resistance[2]	RIN, GIN, BIN	1			MΩ
Input Capacitance			5		pF
LOGIC INPUTS (HSYNC, VSYNC, FIN, ENCD, STND, SELECT)	CMOS Logic Levels				
Logic LO Input Voltage				1	V
Logic HI Input Voltage		2			V
Logic LO Input Current (DC)			<1		µA
Logic HI Input Current (DC)			<1		µA
VIDEO OUTPUTS[3]					
Luminance (LUMA)					
Roll-Off @ 5 MHz	NTSC		–7		dB
	PAL		–6		dB
Gain Error		–15	–3	+15	%
Nonlinearity			±0.3		%
Sync Level	NTSC	243	286	329	mV
	PAL		300		mV
DC Black Level			1.3		V
Chrominance (CRMA)					
Bandwidth	NTSC		3.6		MHz
	PAL		4.4		MHz
Color Burst Amplitude	NTSC	170	249	330	mV p-p
	PAL		288		mV
Color Signal to Burst Ratio Error[4]			±5		%
Color Burst Width	NTSC		2.51		µs
	PAL		2.28		µs
Phase Error[5]			±3		Degrees
DC Black Level			2.0		V
Chroma Feedthrough	R, G, B = 0		15	40	mV p-p
Composite (COMP)					
Absolute Gain Error	With Respect to Luma	–5	±1	5	%
Differential Gain	With Respect to Chroma		0.5		%
Differential Phase	With Respect to Chroma		2.0		Degrees
DC Black Level			1.5		V
Chroma/Luma Time Alignment			0		ns
POWER SUPPLIES					
Recommended Supply Range	Single Supply	+4.75		+5.25	V
Quiescent Current—Encode Mode[6]			33	42	mA
Quiescent Current—Power Down			1		mA

NOTES
[1]R, G, and B signals are inputted via an external ac coupling capacitor.
[2]Except during dc restore period (back porch clamp).
[3]All outputs measured at a 75 Ω reverse-terminated load; ac voltages at the IC output pins are twice those specified here.
[4]Ratio of chroma amplitude to burst amplitude, difference from ideal.
[5]Difference between ideal color-bar phases and the actual values.
[6]Driving the logic inputs with VOH < 4 V will increase static supply current approximately 150 µA per input.

Specifications are subject to change without notice.

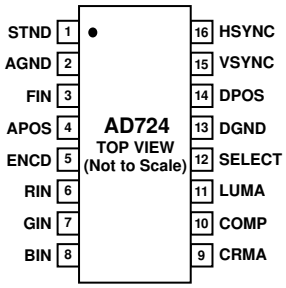
ABSOLUTE MAXIMUM RATINGS*

Supply Voltage, APOS to AGND . . . . . +6 V
Supply Voltage, DPOS to DGND . . . . . +6 V
AGND to DGND . . . . . –0.3 V to +0.3 V
Inputs . . . . . DGND – 0.3 V to DPOS + 0.3 V
Internal Power Dissipation . . . . . 800 mW
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . –65°C to +125°C
Lead Temperature Range (Soldering 30 sec) . . . . . +230°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics: 16-Lead SOIC Package: θ_{JA} = 100°C/W.

PIN CONFIGURATION
16-Lead Wide Body (SOIC)
(R-16)



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD724JR	0°C to +70°C	16-Lead SOIC	R-16
AD724JR-REEL	0°C to +70°C	16-Lead SOIC	R-16
AD724JR-REEL7	0°C to +70°C	16-Lead SOIC	R-16
AD724-EB		Evaluation Board	

CAUTION

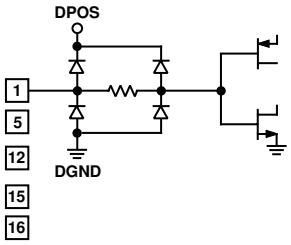
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD724 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



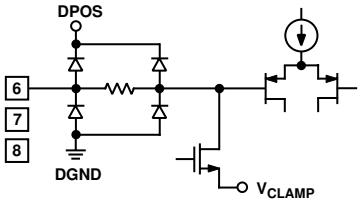
PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Description	Equivalent Circuit
1	STND	A Logical HIGH input selects NTSC encoding. A Logical LOW input selects PAL encoding. CMOS/TTL Logic Levels.	Circuit A
2	AGND	Analog Ground Connection.	
3	FIN	FSC clock or parallel-resonant crystal, or 4FSC clock input. For NTSC: 3.579 545 MHz or 14.318 180 MHz. For PAL: 4.433 619 MHz or 17.734 480 MHz. CMOS/TTL Logic Levels for subcarrier clocks.	Circuit B
4	APOS	Analog Positive Supply (+5 V ± 5%).	
5	ENCD	A Logical HIGH input enables the encode function. A Logical LOW input powers down chip when not in use. CMOS/TTL Logic Levels.	Circuit A
6	RIN	Red Component Video Input. 0 to 714 mV AC-Coupled.	Circuit C
7	GIN	Green Component Video Input. 0 to 714 mV AC-Coupled.	Circuit C
8	BIN	Blue Component Video Input. 0 to 714 mV AC-Coupled.	Circuit C
9	CRMA	Chrominance Output.* Approximately 1.8 V peak-to-peak for both NTSC and PAL.	Circuit D
10	COMP	Composite Video Output.* Approximately 2.5 V peak-to-peak for both NTSC and PAL.	Circuit D
11	LUMA	Luminance plus SYNC Output.* Approximately 2 V peak-to-peak for both NTSC and PAL.	Circuit D
12	SELECT	A Logical LOW input selects the FSC operating mode. A Logical HIGH input selects the 4FSC operating mode. CMOS/TTL Logic Levels.	Circuit A
13	DGND	Digital Ground Connections.	
14	DPOS	Digital Positive Supply (+5 V ± 5%).	
15	VSYNC	Vertical Sync Signal (if using external CSYNC set at > +2 V). CMOS/TTL Logic Levels.	Circuit A
16	HSYNC	Horizontal Sync Signal (or CSYNC signal). CMOS/TTL Logic Levels.	Circuit A

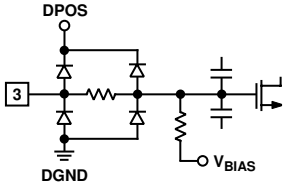
*The Luminance, Chrominance and Composite Outputs are at twice normal levels for driving 75 Ω reverse-terminated lines.



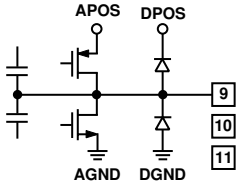
Circuit A



Circuit C



Circuit B



Circuit D

Equivalent Circuits

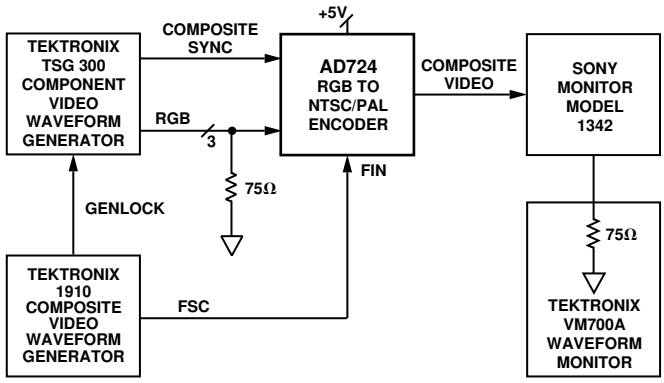


Figure 1. Evaluation Setup

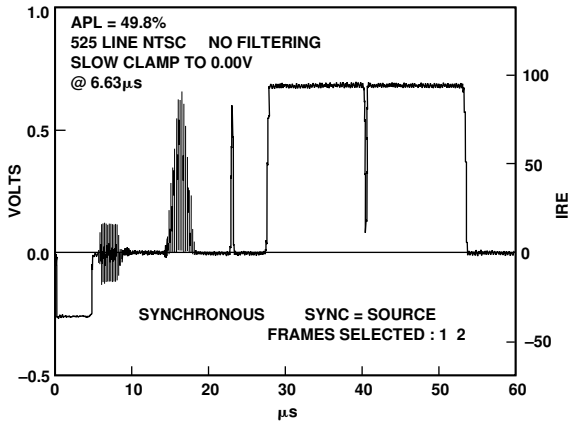


Figure 2. Modulated Pulse and Bar, NTSC

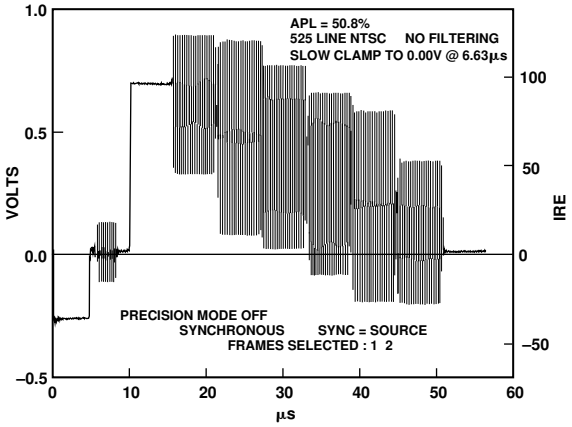


Figure 4. 100% Color Bars, NTSC

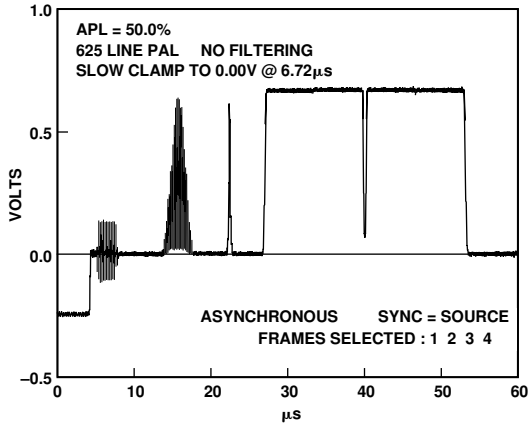


Figure 3. Modulated Pulse and Bar, PAL

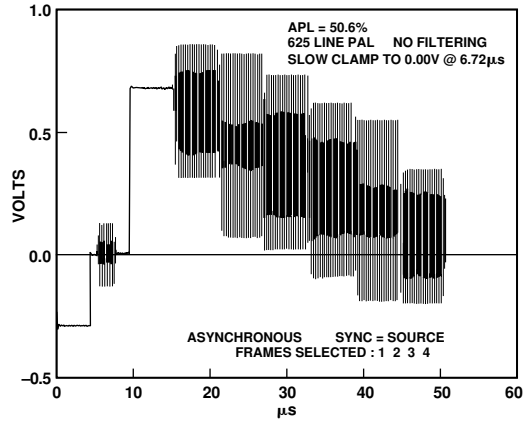


Figure 5. 100% Color Bars, PAL

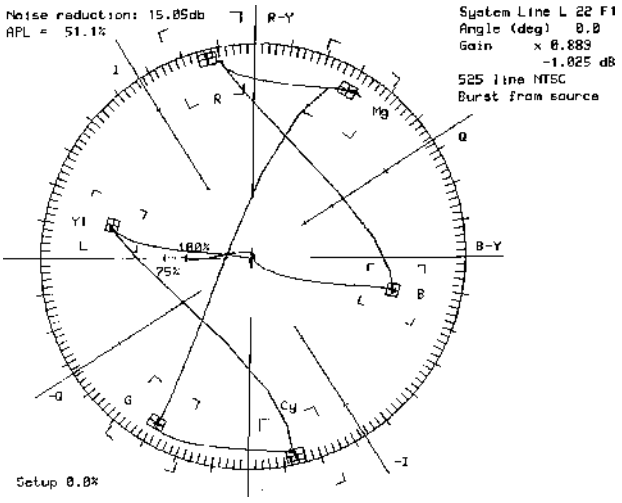


Figure 6. 100% Color Bars on Vector Scope, NTSC

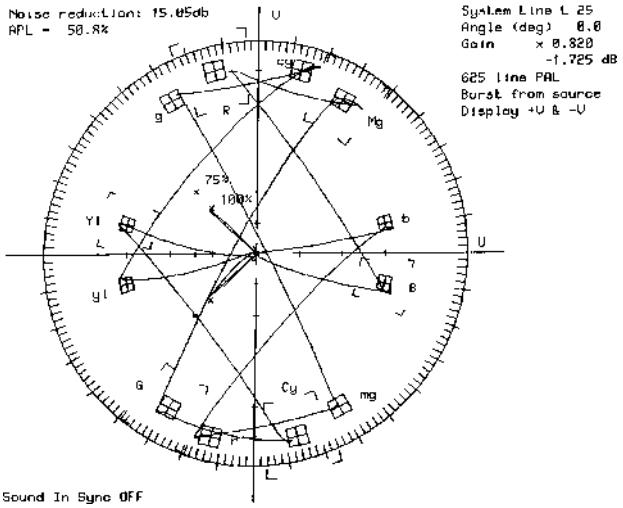


Figure 7. 100% Color Bars on Vector Scope, PAL

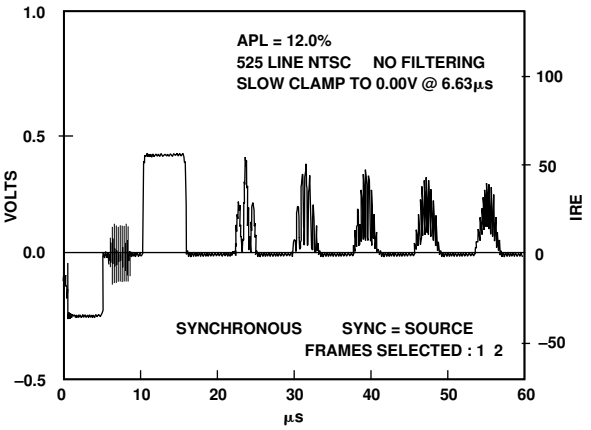


Figure 8. Multipulse, NTSC

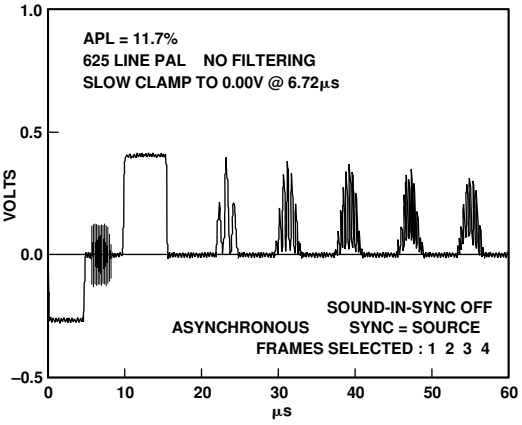


Figure 9. Multipulse, PAL

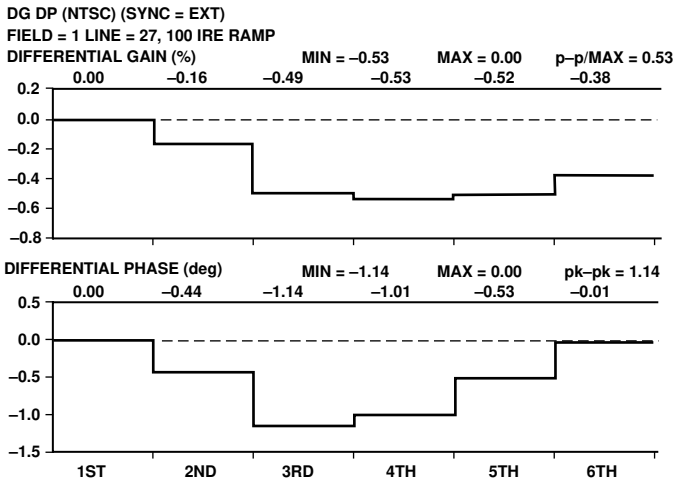


Figure 10. Composite Output Differential Phase and Gain, NTSC

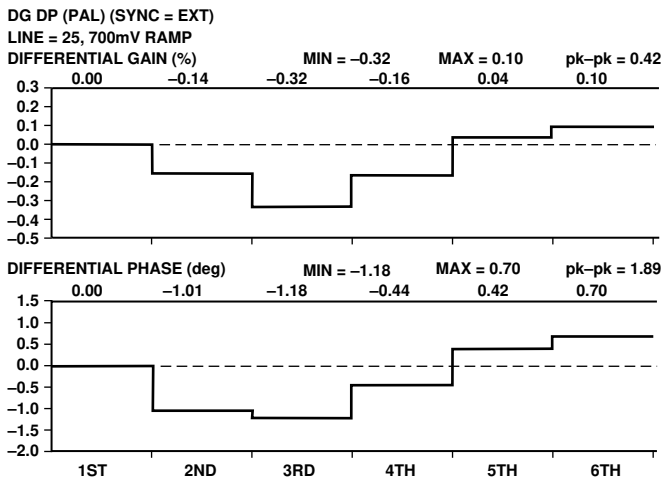


Figure 11. Composite Output Differential Phase and Gain, PAL

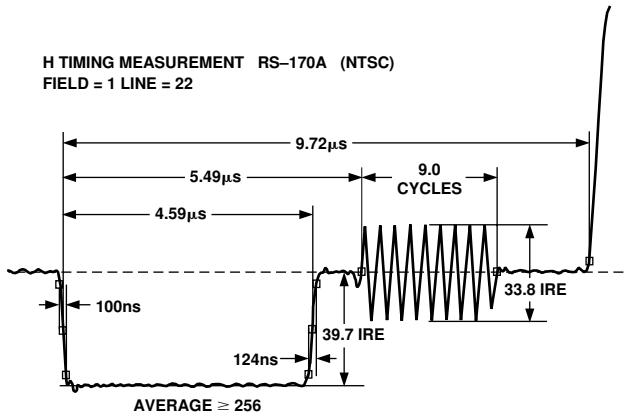


Figure 12. Horizontal Timing, NTSC

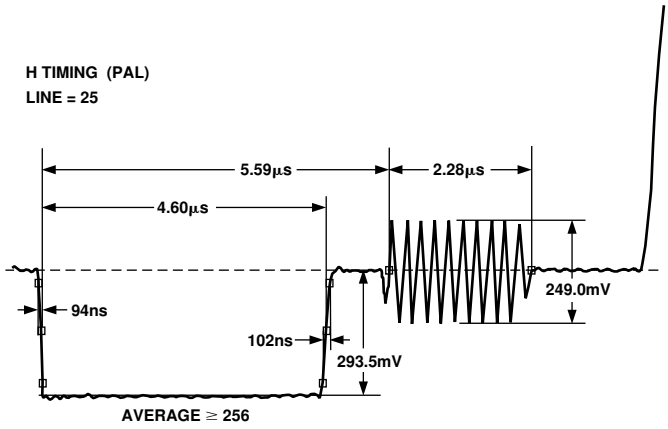


Figure 13. Horizontal Timing, PAL

THEORY OF OPERATION

The AD724 was designed to have three allowable modes of applying a clock via the FIN pin. These are FSC (frequency of subcarrier) mode with CMOS clock applied, FSC mode using on-chip crystal oscillator, and 4FSC mode with CMOS clock applied. The FSC frequency is 3.579545 MHz for NTSC or 4.433618 MHz for PAL.

To use FSC mode the SELECT pin is pulled low and either a CMOS FSC clock is applied to FIN, or a parallel-resonant crystal and appropriate tuning capacitor is placed between the FIN pin and AGND to utilize the on-chip oscillator. The on-chip Phase Locked Loop (PLL) is used in these modes to generate an internal 4FSC clock that is divided to perform the digital timing as well as create the quadrature subcarrier signals for the chrominance modulation.

In 4FSC mode, the SELECT pin is pulled high and the PLL is bypassed.

Referring to the AD724 block diagram (Figure 14), the RGB inputs (each 714 mV p-p max) are dc clamped using external coupling capacitors. These clamps allow the user to have a black level that is not at 0 V. The clamps will adjust to an on-chip black input signal level of approximately 0.8 V. This clamping occurs on the back porch during the burst period.

The RGB inputs then pass into an analog encoding matrix, which creates the luminance ("Y") signal and the chrominance color difference ("U" and "V") signals. The RGB to YUV encoding is performed using the following standard transformations:

$$Y = 0.299 \times R + 0.587 \times G + 0.114 \times B$$

$$U = 0.493 \times (B–Y)$$

$$V = 0.877 \times (R–Y)$$

After the encoding matrix, the AD724 has two parallel analog paths. The Y (luminance) signal is first passed through a 3-pole 4.85 MHz/6 MHz (NTSC/PAL) Bessel low-pass filter to prevent aliasing in the sampled-data delay line. In this first low-pass filter, the unclocked sync is injected into the Y signal. The Y signal then passes through the sampled-data delay line, which is clocked at 8FSC. The delay line was designed to match the overall chrominance and luminance delays. Following the sampled-data delay line is a 5.25 MHz/6.5 MHz (NTSC/PAL) 2-pole low-pass Bessel filter to smooth the reconstructed luminance signal.

The second analog path is the chrominance path in which the U and V color difference signals are processed. The U and V signals first pass through 4-pole modified Bessel low-pass filters with –3 dB frequencies of 1.2 MHz/1.5 MHz (NTSC/PAL) to prevent aliasing in the modulators. The color burst levels are injected into the U channel for NTSC (U and V for PAL) in these premodulation filters. The U and V signals are then independently modulated by a pair of balanced switching modulators driven in quadrature by the color subcarrier.

The bandwidths of the on-chip filters are tuned using proprietary auto-tuning circuitry. The basic principle is to match an RC time constant to a reference time period, that time being one cycle of a subcarrier clock. The auto-tuning is performed during the vertical blanking interval and has added hysteresis so that once an acceptable tuning value is reached the part won't toggle tuning values from field to field. The bandwidths stated in the above discussion are the design target bandwidths for NTSC and PAL.

The AD724's 4FSC clock (either produced by the on-chip PLL or user supplied) drives a digital divide-by-four circuit to create the quadrature signals for modulation. The reference phase 0° is used for the U signal. In the NTSC mode, the V signal is modulated at 90°, but in PAL mode, the V modulation alternates between 90° and 270° at the horizontal line rate as required by the PAL standard. The outputs of the U and V balanced modulators are summed and passed through a 3-pole low-pass filter with 3.6 MHz/4.4 MHz bandwidths (NTSC/PAL) in order to remove the harmonics generated during the switching modulation.

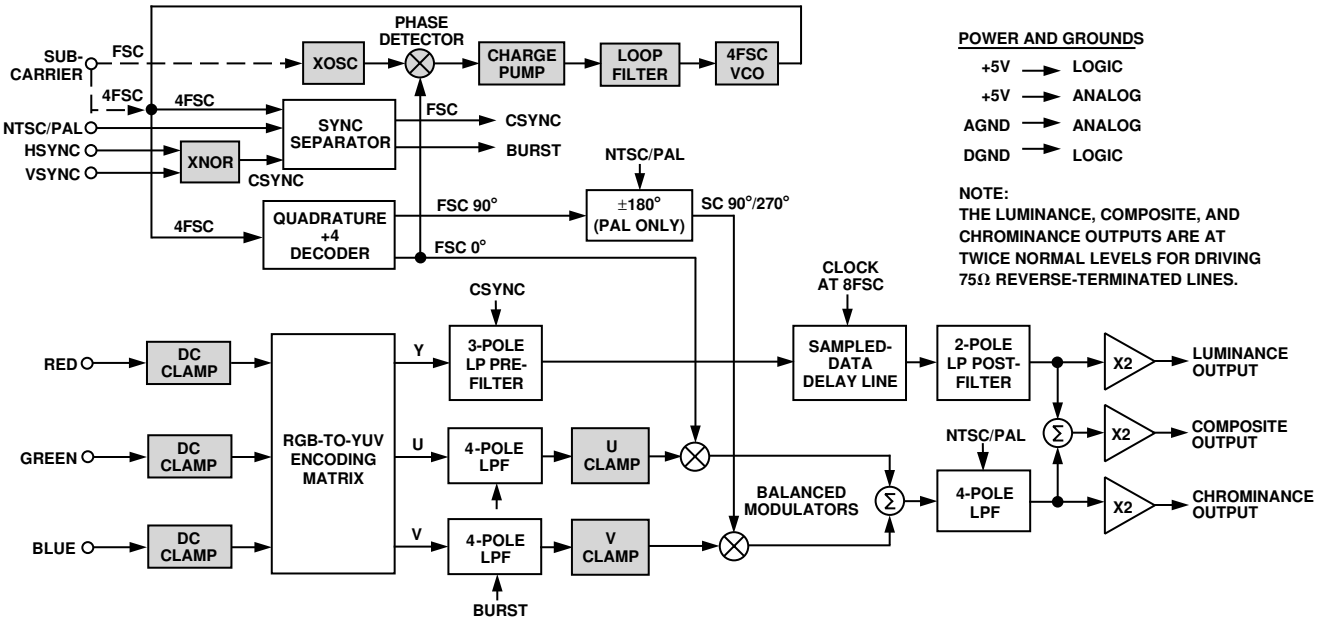


Figure 14. Functional Block Diagram

The filtered chrominance signal is then summed with the filtered luminance signal to create the composite video signal. The separate luminance, chrominance and composite video voltages are amplified by two in order to drive 75 Ω reverse-terminated lines. The separate luminance and chrominance outputs together are known as S-video. The composite and S-video outputs are simultaneously available.

The two sync inputs HSYNC and VSYNC drive an XNOR gate to create a CSYNC signal for the AD724. If the user produces a true composite sync signal, it can be input to the HSYNC pin while the VSYNC pin is held high. In either case the CSYNC signal that is present after the XNOR gate is used to generate the sync and burst signals that are injected into the analog signal chain. The unclocked CSYNC signal is sent to a reference cell on the chip which, when CSYNC is low, allows a reference voltage to be injected into the luminance chain. The width of the injected sync is the same as the width of the supplied sync signal.

The CSYNC signal (after the XNOR gate) is also routed to the digital section of the AD724 where it is clocked in by a 2FSC clock. The digital circuitry then measures the width of the CSYNC pulses to separate horizontal pulses from equalization and serration pulses. A burst flag is generated only after valid horizontal sync pulses, and drives a reference cell to inject the proper voltages into the U and V low-pass filters. This burst flag is timed from the falling edge of the clocked-in CSYNC signal. In synchronous systems (systems in which the subcarrier clock, sync signals, and RGB signals are all synchronous) this will give a fixed burst position relative to the falling edge of the output sync. However, in asynchronous systems the sync to burst position can change line to line by as much as 140 ns (the period of a 2FSC clock cycle) due to the fact that the burst flag is generated from a clocked CSYNC while the sync is injected unclocked. This phenomenon may or may not create visual artifacts in some high-end video systems.

APPLYING THE AD724

Inputs

RIN, BIN, GIN are analog inputs that should be terminated to ground with 75 Ω in close proximity to the IC. When properly terminated the peak-to-peak voltage for a maximum input level should be 714 mV p-p. The horizontal blanking interval should be the most negative part of each signal.

The inputs should be held at the input signal's black level during the horizontal blanking interval. The internal dc clamps will clamp this level during color burst to a reference that is used internally as the black level. Any noise present on the RIN, GIN, BIN or AGND pins during this interval will be sampled onto the input capacitors. This can result in varying dc levels from line to line in all outputs or, if imbalanced, subcarrier feedthrough in the COMP and CRMA outputs.

For increased noise rejection, larger input capacitors are desired. A capacitor of 0.1 μF is usually adequate.

Similarly, the U and V clamps balance the modulators during an interval shortly after the falling CSYNC input. Noise present during this interval will be sampled in the modulators, resulting in residual subcarrier in the COMP and CRMA outputs.

HSYNC and VSYNC are two logic level inputs that are combined internally to produce a composite sync signal. If a composite sync signal is to be used, it can be input to HSYNC while VSYNC is pulled to logic HI (> +2 V).

The form of the input sync signal(s) will determine the form of the composite sync on the composite video (COMP) and luminance (LUMA) outputs. If no equalization or serration pulses are included in the HSYNC input there won't be any in the outputs. Although sync signals without equalization and serration pulses do not technically meet the video standards' specifications, many monitors do not require these pulses in order to display good pictures. The decision whether to include these signals is a system tradeoff between cost and complexity and adhering strictly to the video standards.

The HSYNC and VSYNC logic inputs have a small amount of built-in hysteresis to avoid interpreting noisy input edges as multiple sync edges. This is critical to proper device operation, as the sync pulses are timed for vertical blanking interval detection.

The HSYNC and VSYNC inputs have been designed for VIL > 1.0 V and VIH < 2.0 V for the entire temperature and supply range of operation. The remaining logic inputs do not have hysteresis, and their switching points are centered around 1.4 V. This allows the AD724 to directly interface to TTL or 3 V CMOS compatible outputs, as well as 5 V CMOS outputs where VOL is less than 1.0 V.

The SELECT input is a CMOS logic level that programs the AD724 to use a subcarrier at a 1FSC (LO) frequency or a 4FSC (HI) frequency for the appropriate standard being used. A 4FSC clock is used directly, while a 1FSC input is multiplied up to 4FSC by an internal phase locked loop.

The FIN input can be a logic level clock at either FSC or 4FSC frequency or can be a parallel resonant crystal at 1FSC frequency. An on-chip oscillator will drive the crystal. Most crystals will require a shunt capacitance of between 10 pF and 30 pF for reliable start up and proper frequency of operation.

The NTSC specification calls for a frequency accuracy of ±10 Hz from the nominal subcarrier frequency of 3.579545 MHz. While maintaining this accuracy in a broadcast studio might not be a severe hardship, it can be quite expensive in a low cost consumer application.

The AD724 will operate with subcarrier frequencies that deviate quite far from those specified by the TV standards. However, the monitor will in general not be quite so forgiving. Most monitors can tolerate a subcarrier frequency that deviates several hundred Hz from the nominal standard without any degradation in picture quality. These conditions imply that the subcarrier frequency accuracy is a system specification and not a specification of the AD724 itself.

The STND pin is used to select between NTSC and PAL operation. Various blocks inside the AD724 use this input to program their operation. Most of the more common variants of NTSC and PAL are supported. There are, however, two known specific standards not supported. These are NTSC 4.43 and M-PAL.

Basically these two standards use most of the features of the standard that their names imply, but use the subcarrier that is equal to, or approximately equal to, the frequency of the other standard. Because of the automatic programming of the filters in the chrominance path and other timing considerations, it is not possible to support these standards.

Layout Considerations

The AD724 is an all CMOS mixed signal part. It has separate pins for the analog and digital +5 V and ground power supplies.

Both the analog and digital ground pins should be tied to the ground plane by a short, low inductance path. Each power supply pin should be bypassed to ground by a low inductance 0.1 μF capacitor and a larger tantalum capacitor of about 10 μF.

The three analog inputs (RIN, GIN, BIN) should be terminated with 75 Ω to ground close to the respective pins. However, as these are high impedance inputs, they can be in a loop-through configuration. This technique is used to drive two or more devices with high frequency signals that are separated by some distance. A connection is made to the AD724 with no local termination, and the signals are run to another distant device where the termination for these signals is provided.

The output amplitudes of the AD724 are double that required by the devices that it drives. This compensates for the halving of the signal levels by the required terminations. A 75 Ω series resistor is required close to each AD724 output, while 75 Ω to ground should terminate the far end of each line.

The outputs have a dc bias and must be ac coupled for proper operation. The COMP and LUMA outputs have information down to 30 Hz for NTSC (25 MHz for PAL) that must be transmitted. Each output requires a 220 μF series capacitor to work with the 75 Ω resistance to pass these low frequencies. The CRMA signal has information mostly up at the chroma frequency and can use a smaller capacitor if desired, but 220 μF can be used to minimize the number of different components used in the design.

Displaying VGA Output on a TV

The AD724 can be used to convert the analog RGB output from a personal computer's VGA card to the NTSC or PAL television standards. To accomplish this it is important to understand that the AD724 requires interlaced RGB video and clock rates that are consistent with those required by the television standards. In most computers the default output is a noninterlaced RGB signal at a frame rate higher than used by either NTSC or PAL.

Most VGA controllers support a wide variety of output modes that are controlled by altering the contents of internal registers. It is best to consult with the VGA controller manufacturer to determine the exact configuration required to provide an interlaced output at 60 Hz (50 Hz for PAL).

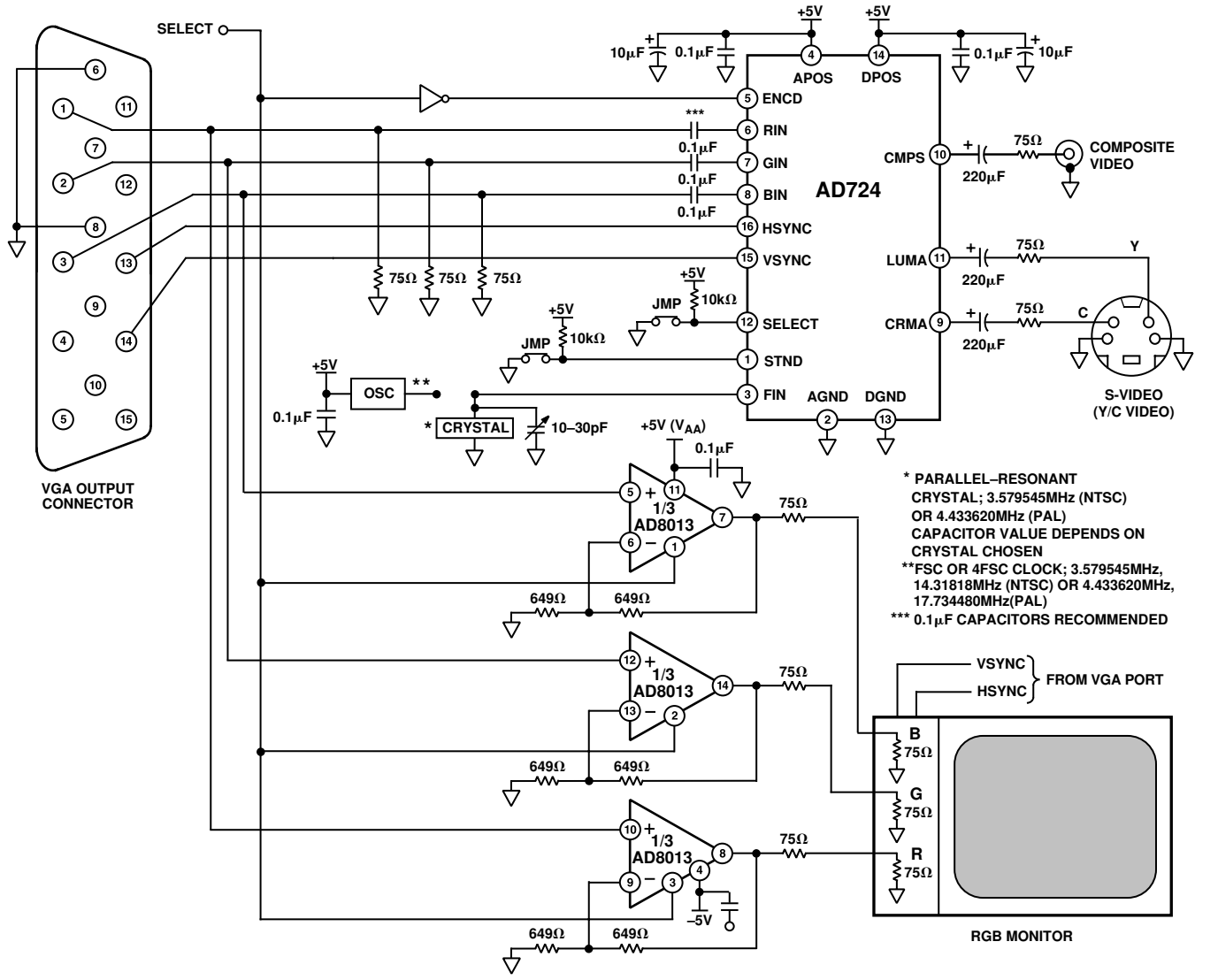


Figure 15. Interfacing the AD724 to the (Interlaced) VGA Port of a PC

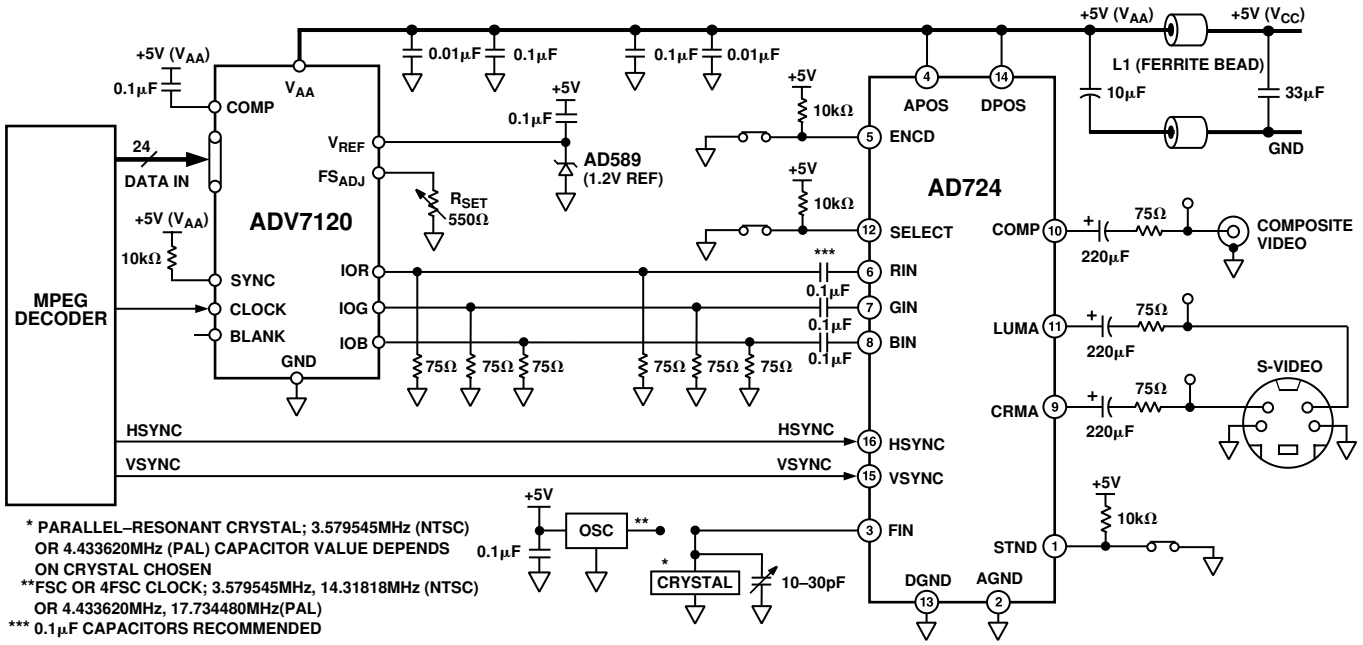


Figure 16. AD724 and ADV7120/ADV7122 Providing MPEG Video Solution

Figure 15 shows a circuit for connection to the VGA port of a PC. The RGB outputs are ac coupled to the respective inputs of the AD724. These signals should each be terminated to ground with 75 Ω.

The standard 15-pin VGA connector has HSYNC on Pin 13 and VSYNC on Pin 14. These signals also connect directly to the same name signals on the AD724. The FIN signal can be provided by any of the means described elsewhere in the data sheet. For a synchronous NTSC system, the internal 4FSC (14.31818 MHz) clock that drives the VGA controller can be used for FIN on the AD724. This signal is not directly accessible from outside the computer, but it does appear on the VGA card.

If a separate RGB monitor is also to be used, it is not possible to simply connect it to the R, G and B signals. The monitor provides a termination that would double terminate these signals. The R, G and B signals should be buffered by three amplifiers with high input impedances. These should be configured for a gain of two, which is normalized by the divide-by-two termination scheme used for the RGB monitor.

The AD8013 is a triple video amplifier that can provide the necessary buffering in a single package. It also provides a disable pin for each amplifier, which can be used to disable the drive to the RGB monitor when interlaced video is used (SELECT = LO). When the RGB signals are noninterlaced, setting SELECT HI will enable the AD8013 to drive the RGB monitor and disable the encoding function of the AD724 via Pin 5. HSYNC and VSYNC are logic level signals that can drive both the AD724 and RGB monitor in parallel. If the disable feature is not required, the AD8073 triple video op amp can provide a lower cost solution.

AD724 Used with an MPEG Decoder

MPEG decoding of compressed video signals is becoming a more prevalent feature in many PC systems. To display images on the computer monitor, video in RGB format is required. However, to display the images on a TV monitor, or to record the images on a VCR, video in composite format is required. Figure 16 shows a schematic for taking the 24-bit wide RGB video from an MPEG decoder and creating both analog RGB video and composite video.

The 24-bit wide RGB video is converted to analog RGB by the ADV7120 (Triple 8-bit video DAC—available in 48-lead LQFP). The analog current outputs from the DAC are terminated to ground at both ends with 75 Ω as called for in the data sheet. These signals are ac coupled to the analog inputs of the AD724. The HSYNC and VSYNC signals from the MPEG Controller are directly applied to the AD724.

If the set of termination resistors closest to the AD724 are removed, an RGB monitor can be connected to these signals and will provide the required second termination. This is acceptable as long as the RGB monitor is always present and connected. If it is to be removed on occasion, another termination scheme is required.

The AD8013 or AD8073 triple video op amp can provide buffering for such applications. Each channel is set for a gain of two while the outputs are back terminated with a series 75 Ω resistor. This provides the proper signal levels at the monitor, which terminates the lines with 75 Ω.

AD724 APPLICATION DISCUSSION—NTSC/PAL CRYSTAL SELECT CIRCUIT

For systems that support both NTSC and PAL, and will use a crystal for the subcarrier, a low cost crystal selection circuit can be made that, in addition to the two crystals, requires two low cost diodes, two resistors and a logic inverter gate. The circuit selection can be driven by the STND signal that already drives Pin 1 to select between NTSC and PAL operation for the AD724.

A schematic for such a circuit is shown in Figure 17. Each crystal ties directly to FIN (Pin 3) with one terminal and has the other terminal connected via a series diode to ground. Each diode serves as a switch, depending on whether it is forward biased or has no bias.

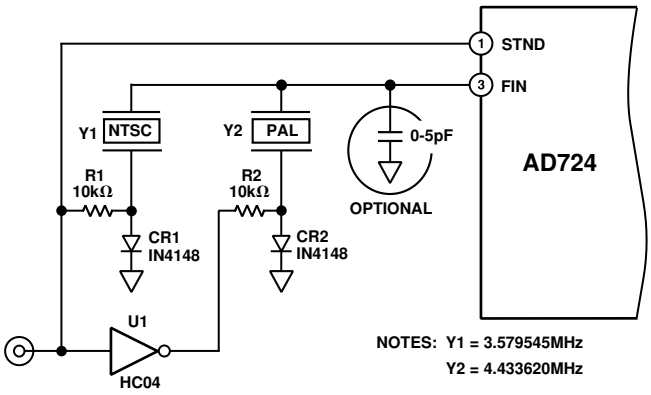


Figure 17. Crystal Selection Circuit

Pin 1 (STND) of the AD724 is used to program the internal operation for either NTSC (HIGH) or PAL (LOW). For NTSC operation in this application the HIGH signal is also used to drive R1 and the input of inverter U1. This creates a LOW signal at the output of U1.

The HIGH (+5 V) signal applied to R1 forward biases CR1 with approximately 450 μA of current. This turns the diode "on" (low impedance with a forward voltage of approximately 0.6 V) and selects Y1 as the crystal to run the oscillator on the AD724. The bias across the diode does not affect the operation of the oscillator.

The LOW (0 V) output of the inverter U1 is applied to R2. This creates a 0 V bias condition across CR2 because its cathode is also at ground potential. This diode is now in the "off" (high impedance) state, because it takes approximately 600 mV of forward bias to turn a diode "on" to any significant degree. The "off" condition of the diode does, however, look like a capacitor of a few pF.

For PAL operation, the STND signal that drives Pin 1 is set LOW (0 V). This programs the AD724 for PAL operation, deselects the NTSC crystal (Y1), because CR1 has no bias voltage across it and selects the PAL crystal (Y2) by forward biasing CR2.

In order to ensure that the circuits described above operate under the same conditions with either crystal selected, it is important to use a logic signal from a CMOS type logic family whose output swings fully from ground to +5 V when operating on a +5 V supply. Other TTL type logic families don't swing this far and might cause problems as a result of variations in the diode bias voltages between the two different crystal selection modes.

FREQUENCY TUNING

A parallel resonant crystal, is the type required for the AD724 oscillator, will work at its operating frequency when it has a specified capacitance in parallel with its terminals. For the AD724 evaluation board, it was found that approximately 10 pF was required across either the PAL or NTSC crystal for proper tuning. The parallel capacitance specified for these crystals is 17 pF for the NTSC crystal and 20 pF for the PAL crystal. The parasitic capacitance of the PC board, packaging and the internal circuitry of the AD724 appear to be contributing 7 pF–10 pF in shunt with the crystal. A direct measurement of this was not made, but the value is inferred from the measured results.

With the crystal selection circuit described above, the unselected crystal and diode provide additional shunt capacitance across the selected crystal. The evaluation board tested actually required no additional capacitance in order to run at the proper frequency for each video standard. However, depending on the layout, some circuits might require a small capacitor from FIN (Pin 3) to ground to operate with the chrominance at the proper frequency.

SUBCARRIER FREQUENCY MEASUREMENT

It is extremely difficult to measure the oscillation frequency of the AD724 when operating with a crystal. The only place where a CW oscillation is present is at the FIN pin. However, probing with any type of probe (even a low capacitance FET probe) at this node will either kill the oscillation or change the frequency of oscillation, so the unprobed oscillating frequency cannot be discerned. Neither the composite video nor chroma signals have the subcarrier represented in a CW fashion. (The LUMA signal does not contain any of the subcarrier.) This makes it virtually impossible to accurately measure the subcarrier frequency of these signals with any oscilloscope technique.

Two methods have been found to accurately measure the subcarrier oscillating frequency. The first uses a spectrum analyzer like the HP3585A that has an accurate frequency counter built in. By looking at either the COMP or CHROMA output of the AD724, a spectrum can be observed that displays the tone of the subcarrier frequency as the largest lobe.

The CHROMA or COMP output of the AD724 should be input into the spectrum analyzer either by means of a scope probe into the 1 MΩ input port or a 75 Ω cable that can be directly terminated by the 75 Ω input termination selection of the HP3585A. Each of these signals has present at least the color burst signal on almost every line, which will be the dominant tone in the frequency band near its nominal frequency. Sidelobes will be observed on either side of the central lobe spaced at 50 Hz (PAL) or 60 Hz (NTSC) intervals due to the vertical scanning rate of the video signals. There will also be sidelobes on either side at about 15.75 kHz intervals, but these will not be observable with the span set to only a few kHz.

The center frequency of the spectrum analyzer should be set to the subcarrier frequency of the standard that is to be observed. The span should be set to 1 kHz–3 kHz and the resolution bandwidth (RBW) set to between 10 Hz to 100 Hz. A combination of wider frequency span and narrower RBW will require a long time for sweeping the entire range. Increasing the RBW will speed up the sweep at the expense of widening the "humps" in the subcarrier tone and the sideband tones.

Once the subcarrier is located, it can be moved to the center of the display and the span can be narrowed to cover only that range necessary to see it. The RBW can then be narrowed to produce an acceptably fast sweep with good resolution.

The marker can now be placed at the location of the subcarrier tone and the frequency counter turned on. The next scan across the location of the marker will measure and display the subcarrier frequency to better than 1 Hz resolution.

A second means for measuring the subcarrier frequency of an AD724 operating from a crystal involves equipment more specialized than a spectrum analyzer. The technique requires a Tektronix VM700A video system measurement instrument.

The VM700A has a special measurement mode that enables it to directly measure the frequency of one subcarrier in a video waveform with respect to an internally stored reference or a simultaneously supplied reference. The instrument gives a reading of the relative frequencies of the reference and test signals in units of 0.1 Hz. This is not a direct reading of the subcarrier frequency in MHz but a relative reading in Hz of the difference in frequency between the two signals.

If the reference video source is supplied by a video generator that has a CW subcarrier output, its CW subcarrier can be measured with a frequency counter to accurately determine its frequency. The AD724 circuit under test can then be measured relative to this reference by using the built in color burst measuring function of the VM700A, and the offset frequency measured can be added to or subtracted from the measured frequency of the CW subcarrier to determine the operating frequency of the DUT.

It should be noted that the VM700A is a highly specialized video measurement instrument. In order for it to synchronize on a video signal, the synchronization pattern of the signal must adhere very closely to the appropriate video standard. In particular, a video signal that is missing equalization and serration pulses from the vertical blanking interval will cause the "Loss of Sync" message to be displayed by the VM700A. Many such signals might make a perfectly acceptable picture on a monitor, but will not be recognized by the VM700A.

Low Cost Crystal Oscillator

If a crystal is used with the on-chip oscillator of the AD724, there will be no CW clock available that can be used elsewhere in the system: the only AD724 signals that output this frequency are the chrome and composite that have only colorburst and chrominance at the subcarrier frequency. These cannot be used for clocking other devices.

A low cost oscillator can be made to provide a CW clock that can be used to drive both the AD724 FIN and other devices in the system that require a clock at this frequency. In addition, the same technique can be used to make a clock signal at a 4FSC, which might be required by other devices and can also be used to drive the FIN pin of the AD724.

Figure 18 shows a circuit that uses one inverter of a 74HC04 package to create a crystal oscillator and another inverter to buffer the oscillator and drive other loads. The logic family must be a CMOS type that can support the frequency of operation, and it must NOT be a Schmitt trigger type of inverter. Resistor R1 from input to output of U1A linearizes the inverter's gain so it provides useful gain and a 180 degree phase shift to drive the oscillator.

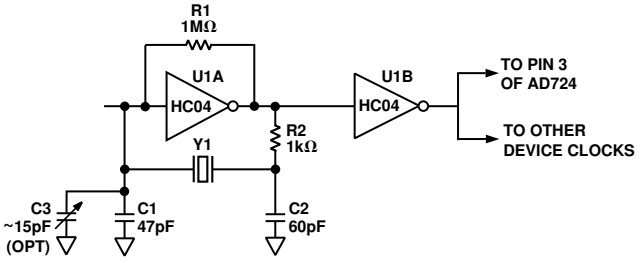


Figure 18. Low Cost Crystal Oscillator

The crystal should be a parallel resonant type at the appropriate frequency (NTSC or PAL, 1FSC or 4FSC). The series combination of C1 and C2 should be approximately equal to the crystal manufacturer's specification for the parallel capacitance required for the crystal to operate at its specified frequency. C1 will usually want to be a somewhat smaller value because of the input parasitic capacitance of the inverter. If it is desired to tune the frequency to greater accuracy, C1 can be made still smaller and a parallel adjustable capacitor can be used to adjust the frequency to the desired accuracy.

Resistor R2 serves to provide the additional phase shift required by the circuit to sustain oscillation. It can be sized by $R2 = 1/(2 \times \pi \times f \times C2)$. Other functions of R2 are to provide a low-pass filter that suppresses oscillations at harmonics of the fundamental of the crystal, and to isolate the output of the inverter from the strange load that the crystal network presents.

The basic oscillator described above is buffered by U1B to drive the AD724 FIN pin and other devices in the system. For a system that requires both an NTSC and PAL oscillator, the circuit can be duplicated by using a different pair of inverters from the same package.

Dot Crawl

Numerous distortions are apparent in the presentation of composite signals on TV monitors. These effects will vary in degree, depending on the circuitry used by the monitor to process the signal, and on the nature of the image being displayed. It is generally not possible to produce pictures on a composite monitor that are as high quality as those produced by standard quality RGB, VGA monitors.

One well known distortion of composite video images is called dot crawl. It shows up as a moving dot pattern at the interface between two areas of different color. It is caused by the inability of the monitor circuitry to adequately separate the luminance and chrominance signals.

One way to prevent dot crawl is to use a video signal with separate luminance and chrominance. Such a signal is referred to as S-video or Y/C video. Since the luminance and chrominance are already separated, the monitor does not have to perform this function. The S-Video outputs of the AD724 can be used to create higher quality pictures when there is an S-Video input available on the monitor.

Flicker

In a VGA conversion application, where the software controlled registers are correctly set, two techniques are commonly used by VGA controller manufacturers to generate the interlaced signal. Each of these techniques introduces a unique characteristic into the display created by the AD724. The artifacts described below are not due to the encoder or its encoding algorithm as all encoders will generate the same display when presented with these inputs. They are due to the method used by the controller display chip to convert a noninterlaced output to an interlaced signal.

The first interlacing technique outputs a true interlaced signal with odd and even fields (one each to a frame Figure 19a). This provides the best picture quality when displaying photography, CD video and animation (games, etc.). It will, however introduce a defect, commonly referred to as flicker, into the display.

Flicker is a fundamental defect of all interlaced displays and is caused by the alternating field characteristic of the interlace technique. Consider a one pixel high black line that extends horizontally across a white screen. This line will exist in only one field and will be refreshed at a rate of 30 Hz (25 Hz for PAL). During the time that the other field is being displayed the line will not be displayed. The human eye is capable of detecting this, and the display will be perceived to have a pulsating or flickering black line. This effect is highly content-sensitive and is most pronounced in applications where text and thin horizontal lines are present. In applications such as CD video, photography and animation, portions of objects naturally occur in both odd and even fields and the effect of flicker is imperceptible.

The second commonly used technique is to output an identical odd and even field (Figure 19b). This ignores the data that naturally occurs in one of the fields. In this case the same one pixel high line mentioned above would appear as a two pixel high line (one pixel high in both the odd and even field) or will not appear at all if it is in the data that is ignored by the controller. Which of these cases occurs is dependent on the placement of the line on the screen. This technique provides a stable (i.e., nonflickering) display for all applications, but small text can be difficult to read and lines in drawings (or spreadsheets) can disappear. As above, graphics and animation are not particularly affected although some resolution is lost.

There are methods to dramatically reduce the effect of flicker and maintain high resolution. The most common is to ensure that display data never exists solely in a single line. This can be accomplished by averaging/weighting the contents of successive/multiple noninterlaced lines prior to creating a true interlaced output (Figure 19c). In a sense this provides an output that will lie between the two extremes described above. The weight or percentage of one line that appears in another, and the number of lines used, are variables that must be considered in developing a system of this type. If this type of signal processing is performed, it must be completed prior to the data being presented to the AD724 for encoding.

Vertical Scaling

In addition to converting the computer generated image from noninterlaced to interlaced format, it is also necessary to scale the image down to fit into NTSC or PAL format. The most common vertical lines/screen for VGA display are 480 and 600 lines. NTSC can accommodate approximately 400 visible lines/frame (200 per field), PAL can accommodate 576 lines/frame (288 per field). If scaling is not performed, portions of the original image will not appear in the television display.

This line reduction can be performed by merely eliminating every Nth (6th line in converting 480 lines to NSTC or every 25th line in converting 600 lines to PAL). This risks generation of jagged edges and jerky movement. It is best to combine the scaling with the interpolation/averaging technique discussed above to ensure that valuable data is not arbitrarily discarded in the scaling process. Like the flicker reduction technique mentioned above, the line reduction must be accomplished prior to the AD724 encoding operation.

There is a new generation of VGA controllers on the market specifically designed to utilize these techniques to provide a crisp and stable display for both text and graphics oriented applications. In addition, these chips rescale the output from the computer to fit correctly on the screen of a television. A list of known devices is available through Analog Devices' Applications group, but the most complete and current information will be available from the manufacturers of graphics controller ICs.

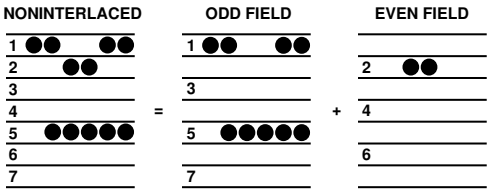
Synchronous vs. Asynchronous Operation

The source of RGB video and synchronization used as an input to the AD724 in some systems is derived from the same clock signal as used for the AD724 subcarrier input (FIN). These systems are said to be operating synchronously. In systems where two different clock sources are used for these signals, the operation is called asynchronous.

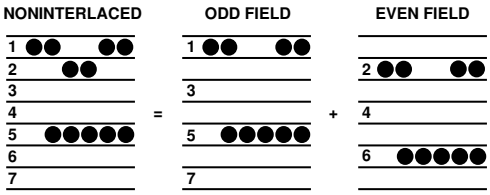
The AD724 supports both synchronous and asynchronous operation, but some minor differences might be noticed between them. These can be caused by some details of the internal circuitry of the AD724.

There is an attempt to process all of the video and synchronization signals totally asynchronous with respect to the subcarrier signal. This was achieved everywhere except for the sampled delay line used in the luminance channel to time align the luminance and chrominance. This delay line uses a signal at eight times the subcarrier frequency as its clock.

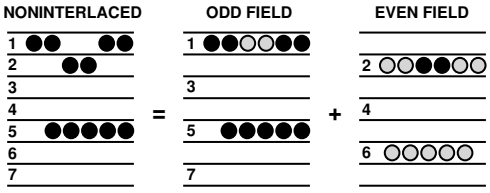
The phasing between the delay line clock and the luminance signal (with inserted composite sync) will be constant during synchronous operation, while the phasing will demonstrate a periodic variation during asynchronous operation. The jitter of the asynchronous video output will be slightly greater due to these periodic phase variations.



a. Conversion of Noninterlace to Interlace



b. Line Doubled Conversion Technique



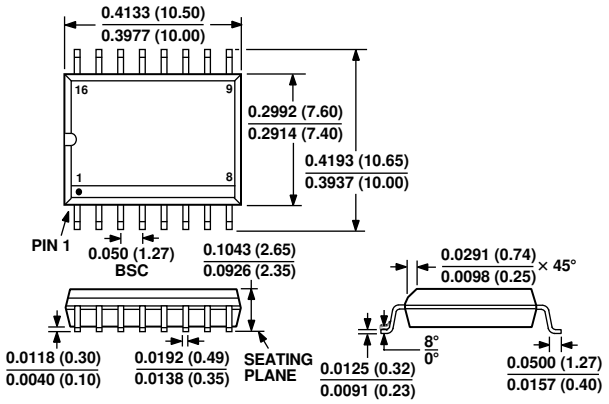
c. Line Averaging Technique

Figure 19.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Wide Body SOIC
(R-16)



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