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Vishay Siliconix

N-Channel 40 V (D-S) 175 °C MOSFET

DESCRIPTION

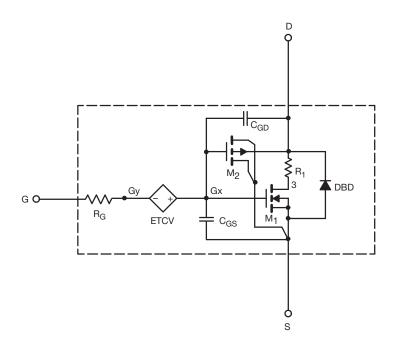
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - $55\,^{\circ}$ C to + $125\,^{\circ}$ C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPICE Device Model SQD50N04-4m1

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SPECIFICATIONS T _J = 25 °C, unless otherwise noted					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	2.7	-	V
Drain-Source On-State Resistancea	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	0.0029	0.0030	Ω
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 15 A	92	120	S
Body Diode Voltage	V _{SD}	I _S = 30 A	0.84	0.90	V
Dynamic ^b					
Input Capacitance	C _{iss}		5380	5360	
Output Capacitance	C _{oss}	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	516	500	pF
Reverse Transfer Capacitance	C _{rss}		256	250	
Total Gate Charge	Qg		80	70	
Gate-Source Charge	Q_{gs}	$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$	16	16	nC
Gate-Drain Charge	Q _{gd}		13	13	

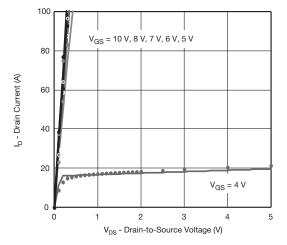
Notes

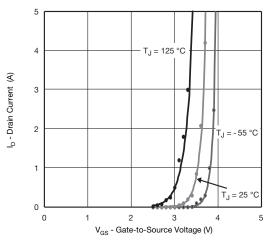
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

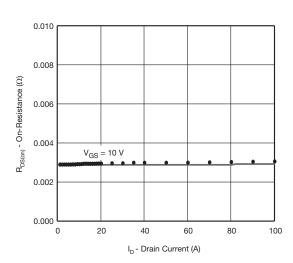
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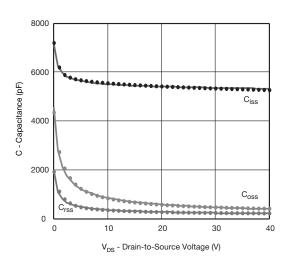
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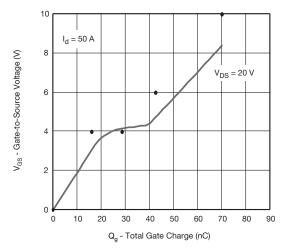
COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25~^{\circ}\text{C}$, unless otherwise noted

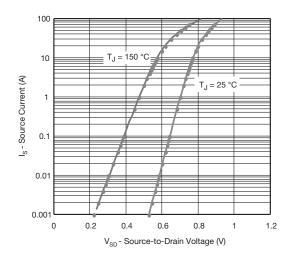












Note

• Dots and squares represent measured data.



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