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DLP-USB232M USB – SERIAL UART Interface Module

The DLP-USB232M uses FTDI's 2nd generation FT232BM USB-UART chip that adds extra functionality to its predecessor (the FT8U232AM) and reduces external component count.

HARDWARE FEATURES

- Single Chip USB Asynchronous Serial Data Transfer
- Full Handshaking & Modem Interface Signals
- UART I/F Supports 7 / 8 Bit Data, 1 / 2 Stop Bits and Odd/Even/Mark/Space/No Parity
- Data rate 300 => 3M Baud (TLL)
- Data rate 300 => 1M Baud (RS232)
- Data rate 300 => 3M Baud (RS422/RS485)
- 384 Byte Receive Buffer / 128 Byte Transmit Buffer for high data throughput
- Adjustable RX buffer timeout
- Full hardware assisted hardware or X-On / X-Off handshaking
- In-built support for event characters and line break condition
- Auto Transmit Buffer control for RS485
- Support for USB Suspend / Resume through SLEEP# and RI# pins
- Support for high power USB Bus powered devices through PWREN# pin
- Integrated level converter on UART and control signals for interfacing to 5v and 3.3v logic
- Integrated 3.3v regulator for USB IO
- Integrated Power-On-Reset circuit
- Integrated 6MHz – 48Mhz clock multiplier PLL
- USB Bulk or Isocronous data transfer modes
- 4.4v to 5.25v single supply operation
- UHCI / OHCI / EHCI host controller compatible
- USB 1.1 and USB 2.0 compatible
- USB VID, PID , Serial Number and Product Description strings in external EEPROM
- EEPROM programmable on-board via USB

VIRTUAL COM PORT (VCP) DRIVERS for

- Windows 98 and Windows 98 SE
- Windows 2000 / ME / XP
- Windows CE **
- MAC OS-8 and OS-9
- MAC OS-X **
- Linux 2.40 and greater

D2XX (USB Direct Drivers + DLL S/W Interface)

- Windows 98 and Windows 98 SE
- Windows 2000 / ME / XP

[** = In planning or under development]

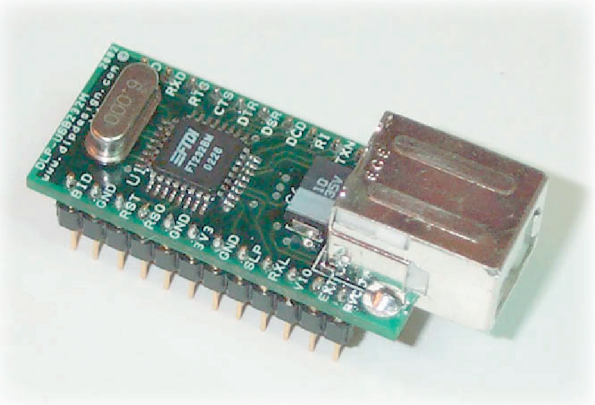
APPLICATION AREAS

- USB - RS232 Converters
- USB - RS422 / RS485 Converters
- Upgrading RS232 Legacy Peripherals to USB
- Cellular and Cordless Phone USB data transfer cables and interfaces
- Interfacing MCU based designs to USB
- USB Audio and Low Bandwidth Video data transfer
- PDA - USB data transfer
- USB Smart Card Readers
- Set Top Box (S.T.B) PC - USB interface
- USB Hardware Modems
- USB Wireless Modems
- USB Instrumentation
- USB Bar Code Readers

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ENHANCEMENTS

This section summarizes the enhancements of the 2nd generation silicon from FTDI compared to its FT8U232AM predecessor. For further details, consult the device pin-out description and functional descriptions.



• Integrated Level Converter on UART interface and control signals

The previous devices would drive the UART and control signals at 5v CMOS logic levels. The new device has a separate VCC-IO pin allowing the device to directly interface to 3.3v and other logic families without the need for external level converter i.c.'s.

• Improved Power Management control for USB Bus Powered, high current devices

The previous devices had a USBEN pin, which became active when the device was enumerated by USB. To provide power control, this signal had to be externally gated with SLEEP# and RESET#. This gating is now done on-chip. USBEN has now been replaced with the new PWREN# signal which can be used to directly drive a transistor or P-Channel MOSFET in applications where power switching of external circuitry is required. A new EEPROM based option makes the device pull gently down its UART interface lines when the power is shut off (PWREN# is High). In this mode, any residual voltage on external circuitry is bled to GND when power is removed thus ensuring that external circuitry controlled by PWREN# resets reliably when power is restored.

• Lower Suspend Current

Integration of RCCLK within the device and internal design improvements reduce the suspend current of the FT232BM to under 200uA (excluding the 1.5k pull-up on USB DP) in USB suspend mode. This allows greater margin for peripherals to meet the USB Suspend current limit of 500uA.

• Support for USB Isocronous Transfers

While USB Bulk transfer is usually the best choice for data transfer, the scheduling time of the data is not guaranteed. For applications where scheduling latency takes priority over data integrity such as transferring audio and low bandwidth video data, the new device now offers an option of USB Isocronous transfer via an option bit in the EEPROM.

• Programmable Receive Buffer Timeout

In the previous device, the receive buffer timeout used to flush remaining data from the receive buffer was fixed at 16ms timeout. This timeout is now programmable over USB in 1ms increments from 1ms to 255ms, thus allowing the device to be better optimized for protocols requiring faster response times from short data packets.

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• TXDEN Timing fix

TXDEN timing has now been fixed to remove the external delay that was previously required for RS485 applications at high baud rates. TXDEN now works correctly during a transmit send-break condition.

• Improved PreScaler Granularity

The previous version of the Prescaler supported division by (n + 0), (n + 0.125), (n + 0.25) and (n + 0.5) where n is an integer between 2 and 16,384 (214). To these have been added (n + 0.375), (n + 0.625), (n + 0.75) and (n+ 0.875) which can be used to improve the accuracy of some baud rates and generate new baud rates which were previously impossible (especially with higher baud rates).

• PreScaler Divide By 1 Fix

The previous device had a problem when the integer part of the divisor was set to 1. In the 2nd generation device, setting the prescaler value to 1 gives a baud rate of 2 million baud and setting it to zero gives a baud rate of 3 million baud. Non-integer division is not supported with divisor values of 0 and 1.

• Bit Bang Mode

The 2nd generation device has a new option referred to as "Bit Bang" mode. In Bit Bang mode, the eight UART interface control lines can be switched between UART interface mode and an 8-bit Parallel IO port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by the prescaler setting. As well as allowing the device to be used stand-alone as a general purpose IO controller for example controlling lights, relays and switches, some other interesting possibilities exist. For instance, it may be possible to connect the device to an SRAM configurable FPGA as supplied by vendors such as Altera and Xilinx. The FPGA device would normally be un-configured (i.e. have no defined function) at power-up.

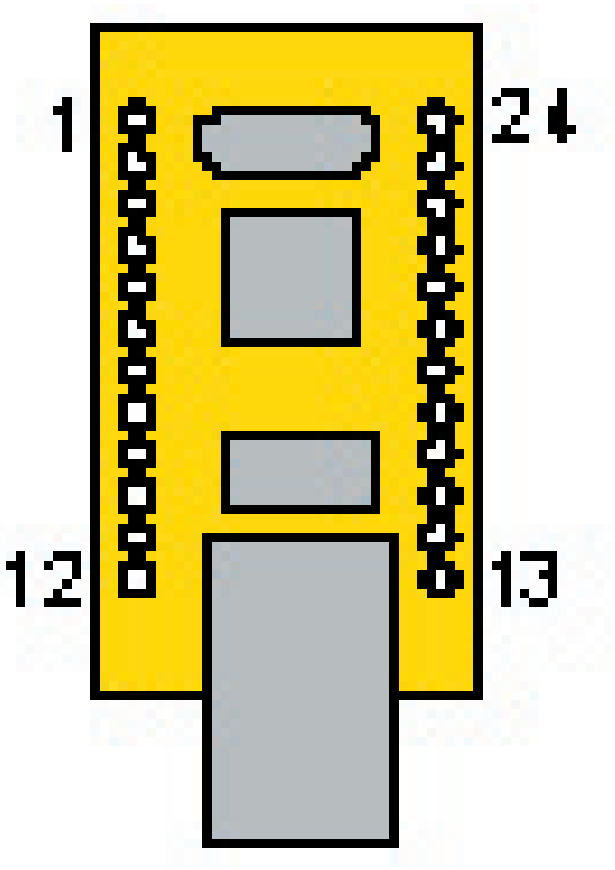
Application software on the PC could use Bit Bang Mode to download configuration data to the FPGA which would define it's hardware function, then after the FPGA device is configured the FT232BM can switch back into UART interface mode to allow the programmed FPGA device to communicate with the PC over USB. This approach allows a customer to create a "generic" USB peripheral whose hardware function can be defined under control of the application software. The FPGA based hardware can be easily upgraded or totally changed simply by changing the FPGA configuration data file. Application notes, software and development modules for this application area will be available from FTDI and other 3rd party developers.

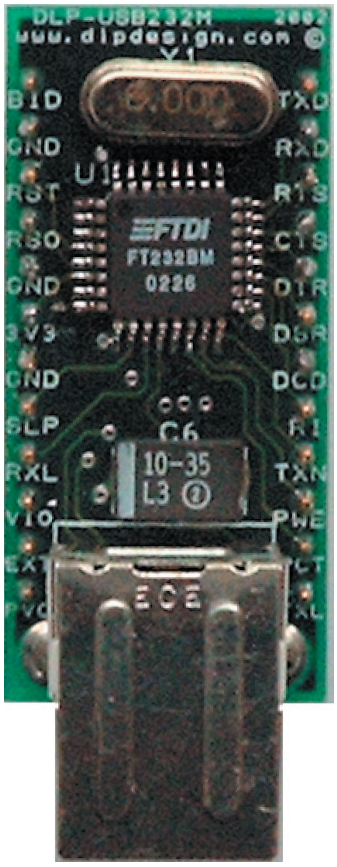
• USB 2.0 (full speed option)

A new EEPROM based option allows the FT232BM to return a USB 2.0 device descriptor as opposed to USB 1.1. Note: The device would be a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).

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Table 1 - DLP-USB232M PINOUT DESCRIPTION





Pin#	Description
1	**BOARD ID** (Out) Identifies the board as either a DLP-USB245M or DLP-USB232M. High for DLP-USB232M and low for DLP-USB245M.
2	**Ground**
3	**RESET#** (In) Can be used by an external device to reset the FT245BM. If not required, this pin must be tied to VCC.
4	**RESETO#** (Out) Output of the internal Reset Generator. Stays high impedance for ~ 2ms after VCC > 3.5v and the internal clock starts up, then clamps it's output to the 3.3v output of the internal regulator. Taking RESET# low will also force RSTOUT# to go high impedance. RSTOUT# is NOT affected by a USB Bus Reset.
5	**Ground**
6	**3V3OUT** (Out) Output from the integrated L.D.O. regulator. It's primary purpose is to provide the internal 3.3v supply to the USB transceiver cell and the RSTOUT# pin. A small amount of current (<= 5mA) can be drawn from this pin to power external 3.3v logic if required.
7	**Ground**
8	**SLEEP#** (Out) Goes Low during USB suspend mode. Typically used to power-down an external TTL to RS232 level converter IC in USB-> RS232 converter designs.
9	**RXLED#** (O.C.) LED Drive - Pulses Low when Receiving Data via USB

10	**VCC-IO** (In) 3.0 volt to +5.25 volt VCC to the UART interface pins 10..12, 14..16 and 18..25. When interfacing with 3.3v external logic connect VCC-IO to the 3.3v supply of the external logic, otherwise connect to VCC to drive out at 5v CMOS level. This pin must be connected to VCC from the target electronics or EXTVCC.
11	**EXTVCC** – (In) Use for applying main power (4.4 to 5.25 Volts) to the module. Connect to PORTVCC if module is to be powered by the USB port (typical configuration)
12	**PORTVCC** - (Out) Power from USB port. Connect to EXTVCC if module is to be powered by the USB port (typical configuration). 500mA maximum current available to USB adapter and target electronics if USB device is configured for high power.
13	**TXLED#** - (O.C.) LED Drive - Pulses Low when Transmitting Data via USB
14	**PWRCTL** (IN) Bus Powered – Tie Low / Self Powered – Tie High
15	**POWEREN#** (OUT) Goes Low after the device is configured via USB, then high during USB suspend. Can be used to control power to external logic using a P-Channel Logic Level MOSFET switch. Enable the Interface Pull-Down Option in EEPROM when using the PWREN# pin in this way.
16	**TXDEN** (OUT) Enable Transmit Data for RS485
17	**RI#** (IN) Ring Indicator Control Input. When the Remote Wakeup option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend.
18	**DCD#** (IN)Data Carrier Detect Control Input
19	**DSR#** (IN)Data Set Ready Control Input / Handshake signal
20	**DTR#** (OUT)Data Terminal Ready Control Output / Handshake signal
21	**CTS#** (IN) Clear To Send Control Input / Handshake signal
22	**RTS#** (OUT) Request To Send Control Output / Handshake signal
23	**RXD** (IN) Receive Asynchronous Data Input
24	**TXD** (OUT)Transmit Asynchronous Data Output

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DEVICE CONFIGURATION EXAMPLES

USB Bus Powered and Self Powered Configuration

Figure 1

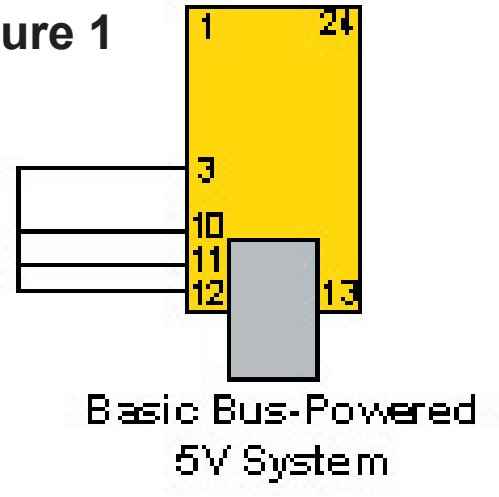


Figure 1 illustrates a typical USB bus powered configuration. A USB Bus Powered device gets its power from the USB bus. Basic rules for USB Bus power devices are as follows –

a) On plug-in, the device must draw no more than 100mA

b) On USB Suspend the device must draw no more than 500uA.

c) A Bus Powered High Power Device (one that draws more than 100mA) should use the SLEEP# pin to keep the current below 100mA on plug-in and 500uA on USB suspend.

d) A device that consumes more than 100mA can not be plugged into a USB Bus Powered Hub

e) No device can draw more that 500mA from the USB Bus.

f) The power descriptor in the

Figure 2

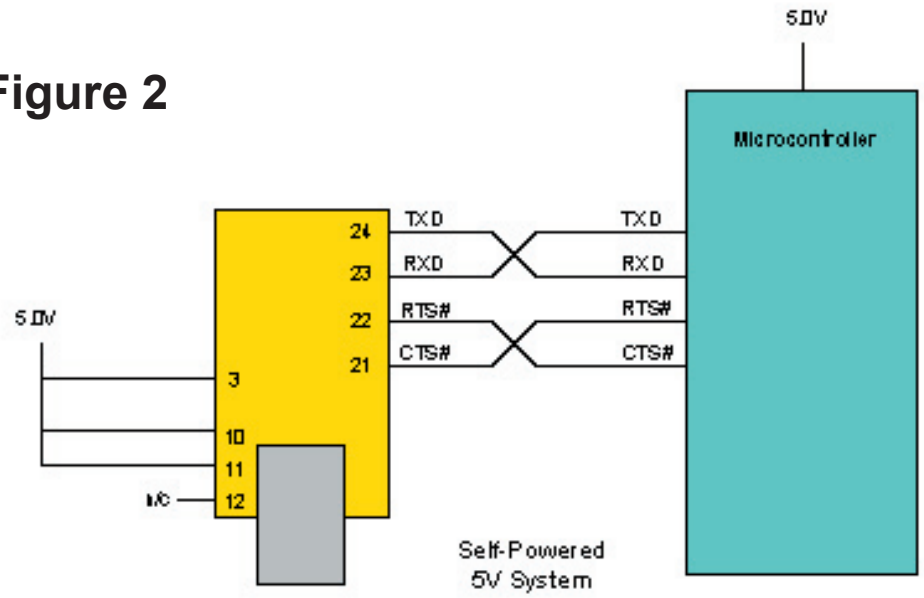


Figure 2 illustrates a typical USB self powered configuration. A USB Self Powered device gets its power from its own Power Supply and does not draw current from the USB bus.

Basic rules for USB Self power devices are as follows –

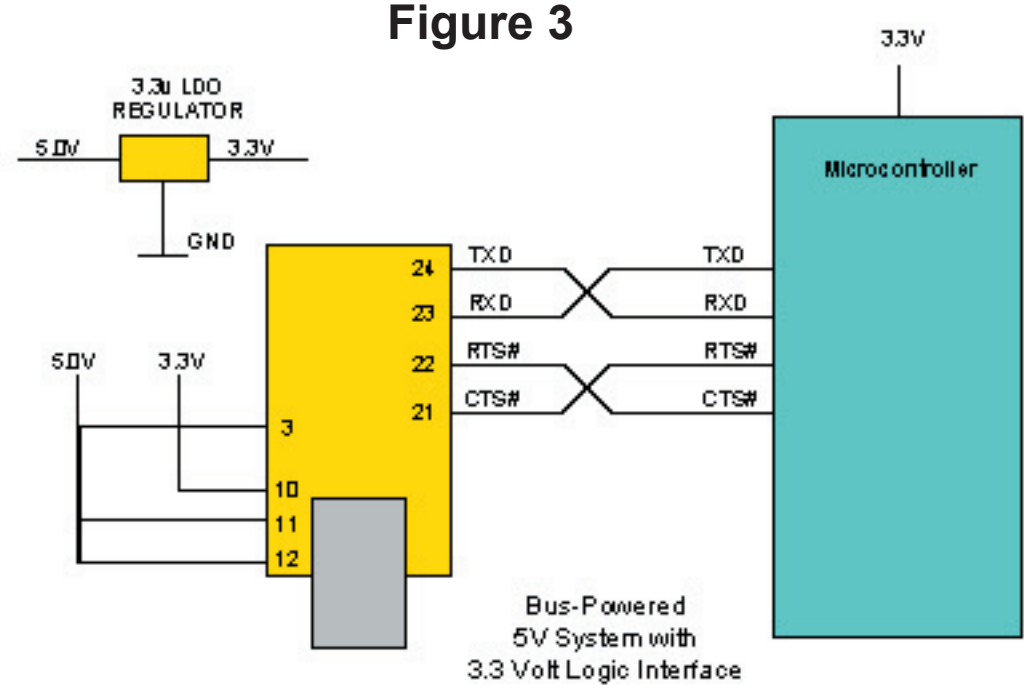
a) A Self-Powered device should not force current down the USB bus when the USB Host or Hub Controller is powered down.

b) A Self Powered Device can take as much current as it likes during normal operation and USB suspend as it has its own Power Supply.

c) A Self Powered Device can be used with any USB Host and both Bus and Self Powered USB Hubs.

Figure 3 shows how to configure the DLP-USB232M to interface with a 3.3v logic device in Bus-Powered configuration. In this example, a LDO regulator provides 3.3 volts from the USB Bus to the target microcontroller and the VCCIO line (pin 10) which in turn will cause the UART interface IO pins to drive out at 3.3v level.

Figure 3

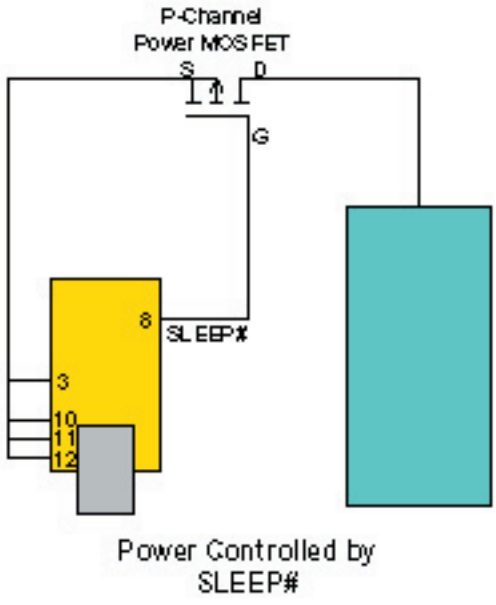


Bus Powered Circuit with Power Control

USB Bus powered circuits need to be able to power down in USB suspend mode in order to meet the <= 500uA total suspend current requirement (including external logic).

Figure 4 shows how to use a discrete P-Channel Logic Level MOSFET to control the power to external logic circuits. A suitable device could be a Fairchild NDT456P or equivalent. This configuration is suitable for powering external logic where the normal supply current is <= 100mA and the logic to be controlled does not generate an appreciable current surge at power-up. For power switching external logic that takes over 100mA or generates a current surge on powerup we recommend that a dedicated power switch i.c with inbuilt "soft-start" is used instead of a MOSFET. A suitable power switch i.c. for such an application would be a Micrel (www.micrel.com) MIC2025-2BM or equivalent.

Figure 4



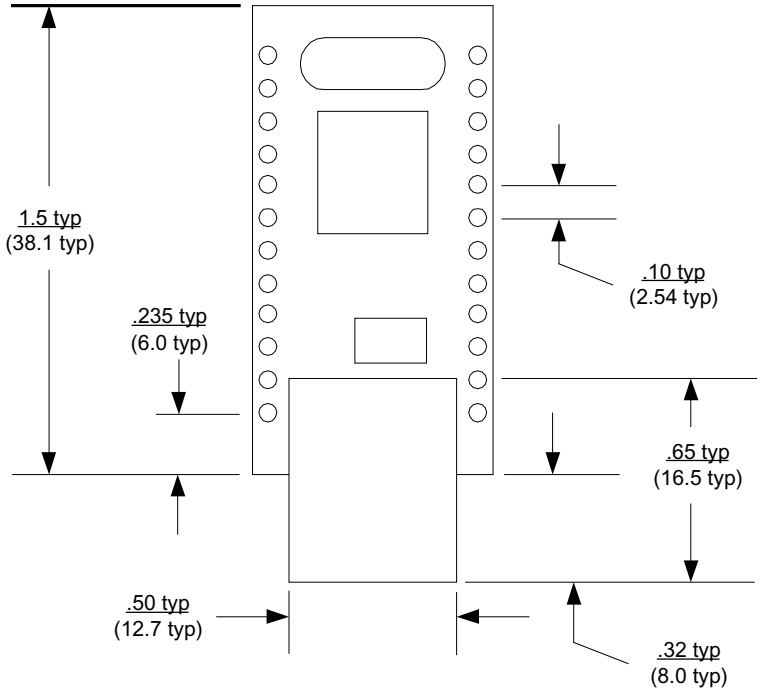
Please note the following points in connection with power controlled designs:

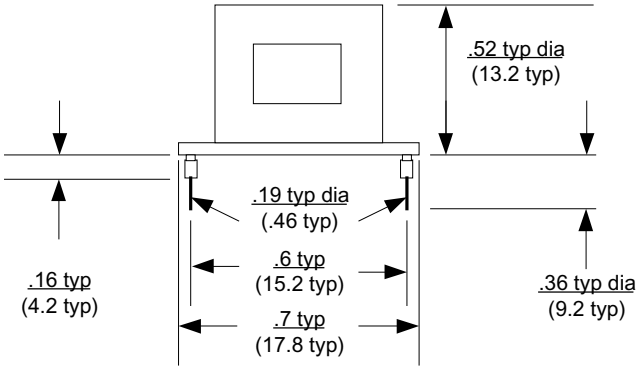
a) The logic to be controlled must have it's own reset circuitry so that it will automatically reset itself when power is re-applied on coming out of suspend.

b) Set the soft pull-down option bit in the FT232BM EEPROM.

c) For 3.3v power controlled circuits VCCIO must not be powered down with the external circuitry (PWREN# gets it's VCC supply from VCCIO).

MECHANICAL DRAWINGS (PRELIMINARY)
INCHES (MILLIMETERS) UNLESS OTHERWISE NOTED





These are the absolute maximum ratings for the DLP-USB232M module in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

- Storage Temperature ..... –65°C to + 150°C
- Ambient Temperature (Power Applied)..... 0°C to + 70°C
- VCC Supply Voltage ..... -0.5v to +6.00v
- DC Input Voltage - Inputs ..... -0.5v to VCC + 0.5v
- DC Input Voltage - High Impedance Bidirectionals ..... -0.5v to VCC + 0.5v
- DC Output Current – Outputs 24mA
- DC Output Current – Low Impedance Bidirectionals 24mA
- Power Dissipation (VCC = 5.25v) 500mW
- Electrostatic Discharge Voltage (I < 1uA) ..... +/- 2000v
- Latch Up Current (Vi < 0 or Vi > Vcc) 100mA

D.C. Characteristics

DC Characteristics (Ambient Temperature = 0 .. 70°C)

Operating Voltage and Current

	Description	Min	Typ	Max	Units	Conditions
Vcc1	VCC Operating Supply Voltage	4.4	5.0	5.25	V	
Vcc2	VCCIO Operating Supply Voltage	3.0	-	5.25	V	
Icc1	Operating Supply Current	-	25	-	mA	Normal Operation
Icc2	Operating Supply Current	-	300	400	uA	USB Suspend Note 1

Note 2 – Supply current excludes the 200uA nominal drawn by the external pull-up resistor on USB DP.

UART IO Pin Characteristics (VCCIO = 5.0v)

	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	4.4	-	4.9	V	I source = 2mA
Vol	Output Voltage Low	0.1	-	0.7	V	I sink = 4 mA
Vin	Input Switching Threshold	1.1	1.5	1.9	V	Note 2
VHys	Input Switching Hysteresis		200		mV	

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UART IO Pin Characteristics (VCCIO = 3.3v)

	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.7	-	3.2	V	I source = 2mA
Vol	Output Voltage Low	0.1	-	0.7	V	I sink = 4 mA
Vin	Input Switching Threshold	1.0	1.4	1.8	V	Note 2
VHys	Input Switching Hysteresis		200		mV	

RESET# IO Pin Characteristics

	Description	Min	Typ	Max	Units	Conditions
Vin	Input Switching Threshold	1.1	1.5	1.9	V	Note 2
VHys	Input Switching Hysteresis		200		mV	

RSTOUT Pin Characteristics

	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	3.0	-	3.6	V	I source = 2mA
Iol	Leakage Current Tri-State	-	-	5	uA	

USB IO Pin Characteristics

	Description	Min	Typ	Max	Units	Conditions
UVoh	IO Pins Static Output (High)	2.8		3.6v	V	
UVol	IO Pins Static Output (Low)	0		0.3	V	
UVse	Single Ended Rx Threshold	0.8		2.0	V	
UCom	Differential Common Mode	0.8		2.5	V	
UVDif	Differential Input Sensitivity	0.2			V	
UDrvZ	Driver Output Impedance	29		44	ohm	Note 3

Note 2 – Inputs have an internal 200k pull-up resistor to VCCIO.

Note 3 – Driver Output Impedance includes the external 27R series resistors on USBDP and

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Appendix A – DLP USB232M Schematic

