GTL2003

8-bit bidirectional low voltage translator

Rev. 01 — 27 July 2007 Product data sheet

1. General description

The Gunning Transceiver Logic - Transceiver Voltage Clamps (GTL-TVC) provide high-speed voltage translation with low ON-state resistance and minimal propagation delay. The GTL2003 provides 8 NMOS pass transistors (Sn and Dn) with a common gate (GREF) and a reference transistor (SREF and DREF). The device allows bidirectional voltage translations between 1.0 V and 5.0 V without use of a direction pin.

When the Sn or Dn port is LOW, the clamp is in the ON-state and a low resistance connection exists between the Sn and Dn ports. Assuming the higher voltage is on the Dn port, when the Dn port is HIGH, the voltage on the Sn port is limited to the voltage set by the reference transistor (SREF). When the Sn port is HIGH, the Dn port is pulled to V_{CC} by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control.

All transistors have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the transistors is symmetrical. Because all transistors in the device are identical, SREF and DREF can be located on any of the other eight matched Sn/Dn transistors, allowing for easier board layout. The translator's transistors provide excellent ESD protection to lower voltage devices and at the same time protect less ESD-resistant devices.

2. Features

- 8-bit bidirectional low voltage translator
- Allows voltage level translation between 1.0 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5 V buses which allows direct interface with GTL, GTL+, LVTTL/TTL and 5 V CMOS levels
- Provides bidirectional voltage translation with no direction pin
- Low 6.5 Ω ON-state resistance (R_{on}) between input and output pins (Sn/Dn)
- Supports hot insertion
- No power supply required: will not latch up
- 5 V tolerant inputs
- Low standby current
- Flow-through pinout for ease of printed-circuit board trace routing
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Packages offered: TSSOP20, DHVQFN20

3. Applications

- Any application that requires bidirectional or unidirectional voltage level translation from any voltage from 1.0 V to 5.0 V to any voltage from 1.0 V to 5.0 V
- The open-drain construction with no direction pin is ideal for bidirectional low voltage (for example, 1.0 V, 1.2 V, 1.5 V, or 1.8 V) processor I^2C-bus port translation to the normal 3.3 V and/or 5.0 V I^2C-bus signal levels or GTL/GTL+ translation to LVTTL/TTL signal levels.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
GTL2003BQ	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
GTL2003PW	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4.1 Ordering options

Table 2. Ordering options

Type number	Topside mark	Temperature range
GTL2003BQ	2003	–40 °C to +85 °C
GTL2003PW	GTL2003	–40 °C to +85 °C

5. Functional diagram

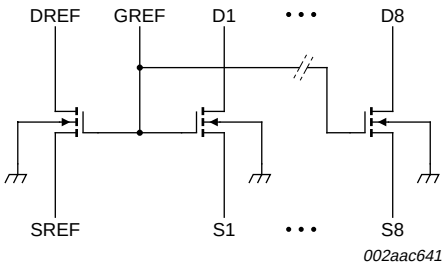


Fig 1. Functional diagram

6. Pinning information

6.1 Pinning

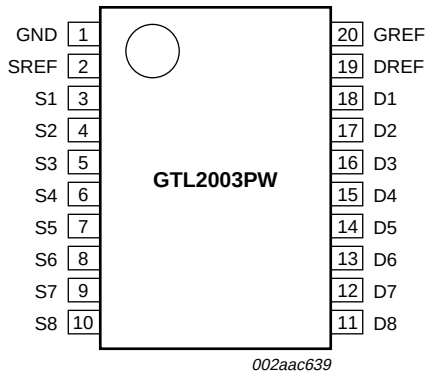
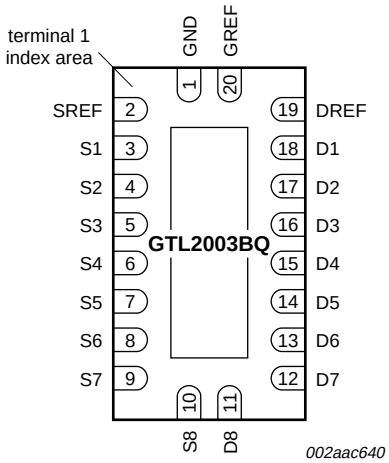


Fig 2. Pin configuration for TSSOP20



Transparent top view

Fig 3. Pin configuration for DHVQFN20

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
GND	1[1]	ground (0 V)
SREF	2	source of reference transistor
S1 to S8	3, 4, 5, 6, 7, 8, 9, 10	Port S1 to Port S8
D1 to D8	18, 17, 16, 15, 14, 13, 12, 11	Port D1 to Port D8
DREF	19	drain of reference transistor
GREF	20	gate of reference transistor

[1] DHVQFN package die supply ground is connected to both GND pin and exposed center pad. GND pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

7. Functional description

Refer also to Figure 1 “Functional diagram”.

7.1 Function selection

Table 4. Function selection, HIGH-to-LOW translation

Assumes Dn is at the higher voltage level.
H = HIGH voltage level; L = LOW voltage level; X = Don’t care

GREF[1]	DREF	SREF	Input Dn	Output Sn	Transistor
H	H	0 V	X	X	off
H	H	V_T[2]	H	V_T[2][3]	on
H	H	V_T[2]	L	L[4]	on
L	L	0 V – V_T[2]	X	X	off

[1] GREF should be at least 1.5 V higher than SREF for best translator operation.

[2] V_T is equal to the SREF voltage.

[3] Sn is not pulled up or pulled down.

[4] Sn follows the Dn input LOW.

Table 5. Function selection, LOW-to-HIGH translation

Assumes Dn is at the higher voltage level.
H = HIGH voltage level; L = LOW voltage level; X = Don’t care

GREF[1]	DREF	SREF	Input Sn	Output Dn	Transistor
H	H	0 V	X	X	off
H	H	V_T[2]	V_T[2]	H[3]	nearly off
H	H	V_T[2]	L	L[4]	on
L	L	0 V – V_T[2]	X	X	off

[1] GREF should be at least 1.5 V higher than SREF for best translator operation.

[2] V_T is equal to the SREF voltage.

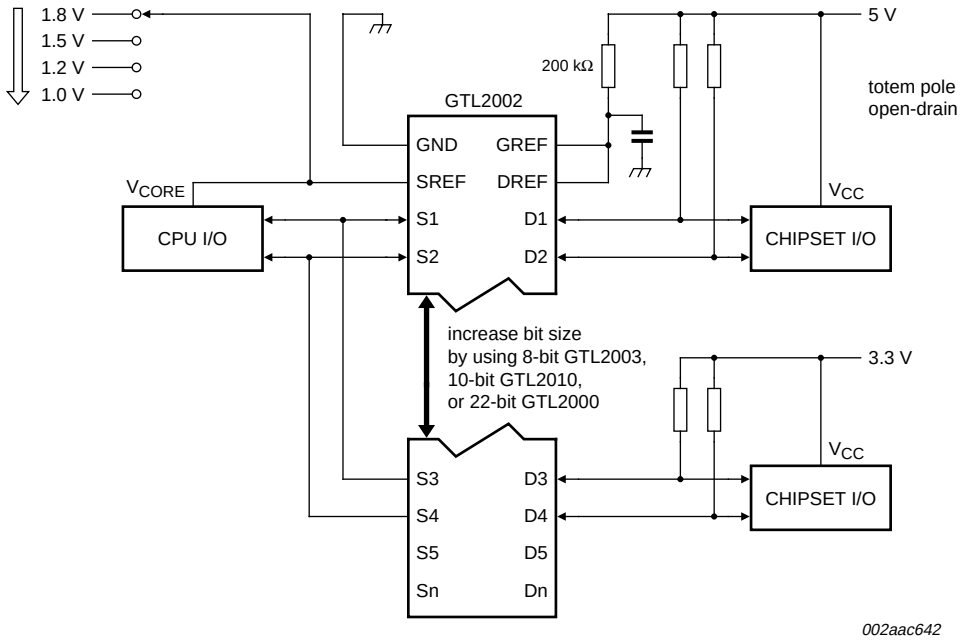
[3] Dn is pulled up to V_{CC} through an external resistor.

[4] Dn follows the Sn input LOW.

8. Application design-in information

8.1 Bidirectional translation

For the bidirectional clamping configuration, higher voltage to lower voltage or lower voltage to higher voltage, the GREF input must be connected to DREF and both pins pulled to HIGH side V_{CC} through a pull-up resistor (typically 200 kΩ). A filter capacitor on DREF is recommended. The processor output can be totem pole or open-drain (pull-up resistors may be required) and the chip set output can be totem pole or open-drain (pull-up resistors are required to pull the Dn outputs to V_{CC}). However, if either output is totem pole, data must be unidirectional or the outputs must be 3-stateable and the outputs must be controlled by some direction control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed. The opposite side of the reference transistor (SREF) is connected to the processor core power supply voltage. When DREF is connected through a 200 kΩ resistor to a 3.3 V to 5.5 V V_{CC} supply and SREF is set between 1.0 V to (V_{CC} − 1.5 V), the output of each Sn has a maximum output voltage equal to SREF and the output of each Dn has a maximum output voltage equal to V_{CC}.

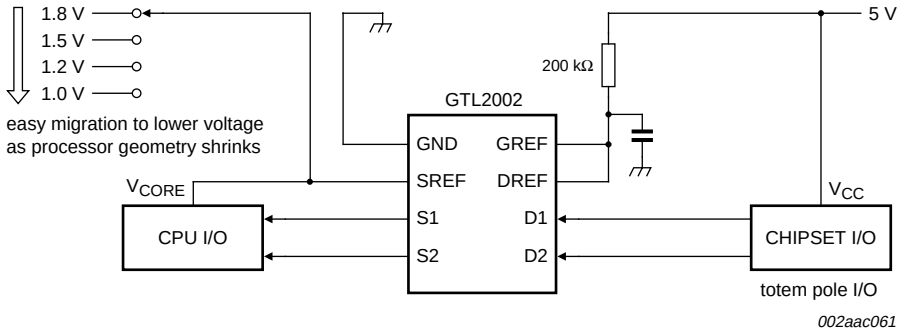


Typical bidirectional voltage translation.

Fig 4. Bidirectional translation to multiple higher voltage levels such as an I²C-bus application

8.2 Unidirectional down translation

For unidirectional clamping, higher voltage to lower voltage, the GREF input must be connected to DREF and both pins pulled to the higher side V_{CC} through a pull-up resistor (typically 200 kΩ). A filter capacitor on DREF is recommended. Pull-up resistors are required if the chip set I/O are open-drain. The opposite side of the reference transistor (SREF) is connected to the processor core supply voltage. When DREF is connected through a 200 kΩ resistor to a 3.3 V to 5.5 V V_{CC} supply and SREF is set between 1.0 V to (V_{CC} − 1.5 V), the output of each Sn has a maximum output voltage equal to SREF.

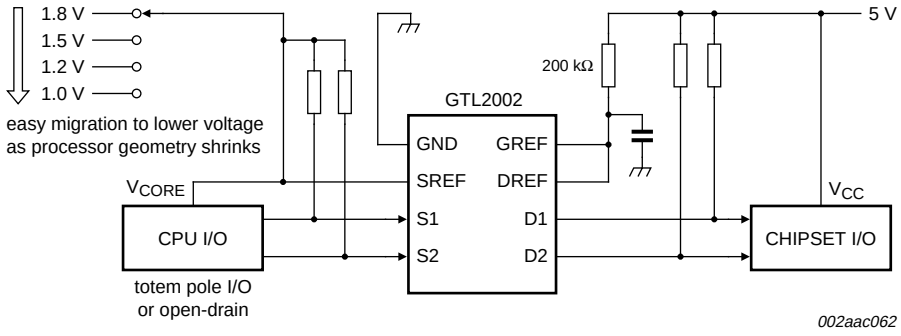


Typical unidirectional HIGH-to-LOW voltage translation.

Fig 5. Unidirectional down translation to protect low voltage processor pins

8.3 Unidirectional up translation

For unidirectional up translation, lower voltage to higher voltage, the reference transistor is connected the same as for a down translation. A pull-up resistor is required on the higher voltage side (Dn or Sn) to get the full HIGH level, since the GTL-TVC device will only pass the reference source (SREF) voltage as a HIGH when doing an up translation. The driver on the lower voltage side only needs pull-up resistors if it is open-drain.



Typical unidirectional LOW-to-HIGH voltage translation.

Fig 6. Unidirectional down translation to protect low voltage processor pins

8.4 Sizing pull-up resistor

The pull-up resistor value needs to limit the current through the pass transistor when it is in the 'on' state to about 15 mA. This will guarantee a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage will also be higher in the 'on' state. To set the current through each pass transistor at 15 mA, the pull-up resistor value is calculated as follows:

$$resistor\ value\ (\Omega) = \frac{pull\text{-}up\ voltage\ (V) - 0.35\ V}{0.015\ A}$$

Table 6 summarizes resistor values for various reference voltages and currents at 15 mA and also at 10 mA and 3 mA. The resistor value shown in the +10 % column or a larger value should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the GTL-TVC device at 0.175 V, although the 15 mA only applies to current flowing through the GTL-TVC device. See application note *AN10145 Bidirectional low voltage translators* for more information.

Table 6. Pull-up resistor values

Calculated for V_{OL} = 0.35 V. Assumes output driver V_{OL} = 0.175 V at stated current.

Pull-up resistor value (Ω)						
Voltage	**15 mA**		**10 mA**		**3 mA**	
	Nominal	**+ 10 %[1]**	**Nominal**	**+ 10 %[1]**	**Nominal**	**+ 10 %[1]**
5.0 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

[1] + 10 % to compensate for V_{DD} range and resistor tolerance.

9. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SREF}	voltage on pin SREF		–0.5[2]	+7.0	V
V_{DREF}	voltage on pin DREF		–0.5[2]	+7.0	V
V_{GREF}	voltage on pin GREF		–0.5[2]	+7.0	V
V_{Sn}	voltage on port Sn		–0.5[2]	+7.0	V
V_{Dn}	voltage on port Dn		–0.5[2]	+7.0	V
I_{IK}	input clamping current	SREF, DREF, GREF; $V_I < 0$ V	-	–50	mA
		port Sn; $V_I < 0$ V	-	–50	mA
		port Dn; $V_I < 0$ V	-	–50	mA
I_{ch}	channel current (DC)	channel in ON-state	-	±128	mA
T_{stg}	storage temperature		–65	+150	°C

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[2] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

10. Recommended operating conditions

Table 8. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{I/O}$	voltage on an input/output pin	Sn, Dn		0	-	5.5	V
V_{SREF}	voltage on pin SREF		[1]	0	-	5.5	V
V_{DREF}	voltage on pin DREF			0	-	5.5	V
V_{GREF}	voltage on pin GREF			0	-	5.5	V
$I_{sw(pass)}$	pass switch current			-	-	64	mA
T_{amb}	ambient temperature	operating in free-air		–40	-	+85	°C

[1] $V_{SREF} \leq V_{DREF} - 1.5$ V for best results in level shifting applications.

11. Static characteristics

Table 9. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OL}	LOW-level output voltage	V_{DD} = 3.0 V; V_{SREF} = 1.365 V; V_{Sn} or V_{Dn} = 0.175 V; I_{IK} = 15.2 mA		-	260	350	mV
V_{IK}	input clamping voltage	I_I = −18 mA; V_{GREF} = 0 V		-	-	−1.2	V
$I_{LI(G)}$	gate input leakage current	V_I = 5 V; V_{GREF} = 0 V		-	-	5	µA
C_{ig}	input capacitance at gate	GREF; V_I = 3 V or 0 V		-	56	-	pF
$C_{io(off)}$	off-state input/output capacitance	V_O = 3 V or 0 V; V_{GREF} = 0 V		-	7.4	-	pF
$C_{io(on)}$	on-state input/output capacitance	V_O = 3 V or 0 V; V_{GREF} = 3 V		-	18.6	-	pF
R_{on}	ON-state resistance	V_I = 0 V; I_O = 64 mA	[2]				
		V_{GREF} = 4.5 V		-	3.5	5	Ω
		V_{GREF} = 3 V		-	4.4	7	Ω
		V_{GREF} = 2.3 V		-	5.5	9	Ω
		V_{GREF} = 1.5 V		-	67	105	Ω
		V_I = 0 V; I_O = 30 mA; V_{GREF} = 1.5 V	[2]	-	9	15	Ω
		V_I = 2.4 V; I_O = 15 mA; V_{GREF} = 4.5 V	[2]	-	7	10	Ω
		V_I = 2.4 V; I_O = 15 mA; V_{GREF} = 3 V	[2]	-	58	80	Ω
		V_I = 1.7 V; I_O = 15 mA; V_{GREF} = 2.3 V	[2]	-	50	70	Ω

[1] All typical values are measured at T_{amb} = 25 °C.

[2] Measured by the voltage drop between the Sn and the Dn terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two (Sn or Dn) terminals.

12. Dynamic characteristics

12.1 Dynamic characteristics for translator-type application

Table 10. Dynamic characteristics

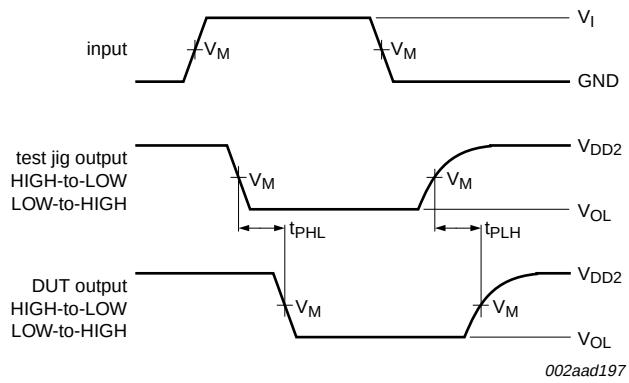
T_{amb} = −40 °C to +85 °C; V_{ref} = 1.365 V to 1.635 V; V_{DD1} = 3.0 V to 3.6 V; V_{DD2} = 2.36 V to 2.64 V; GND = 0 V; $t_r = t_f \leq 3.0$ ns; unless otherwise specified. Refer to Figure 9.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{PLH}	LOW-to-HIGH propagation delay	Sn to Dn; Dn to Sn	[2][3]	0.5	1.5	5.5	ns
t_{PHL}	HIGH-to-LOW propagation delay	Sn to Dn; Dn to Sn	[2][3]	0.5	1.5	5.5	ns

[1] All typical values are measured at V_{DD1} = 3.3 V, V_{DD2} = 2.5 V, V_{ref} = 1.5 V and T_{amb} = 25 °C.

[2] Propagation delay is measured using Figure 9 and is a difference measurement. It is not production tested and is guaranteed by ON-state resistance.

[3] $C_{io(on)}$ maximum of 30 pF and $C_{io(off)}$ maximum of 15 pF is guaranteed by design.



V_M = 1.5 V; V_I = GND to 3.0 V.

Fig 7. The input (Sn) to output (Dn) propagation delays

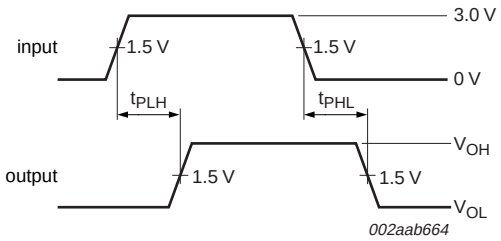
12.2 Dynamic characteristics for CBT-type application

Table 11. Dynamic characteristics

T_{amb} = −40 °C to +85 °C; V_{GREF} = 5 V ± 0.5 V; GND = 0 V; C_L = 50 pF; unless otherwise specified. Refer to Figure 10.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PD}	propagation delay		[1]	-	-	250	ps

[1] This parameter is warranted by the ON-state resistance, but is not production tested. The propagation delay is based on the RC time constant of the typical ON-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).



V_M = 1.5 V; V_I = GND to 3.0 V.

t_{PD} is equal to the maximum of t_{PLH} or t_{PHL}.

Fig 8. Input (Sn) to output (Dn) propagation delays

13. Test information

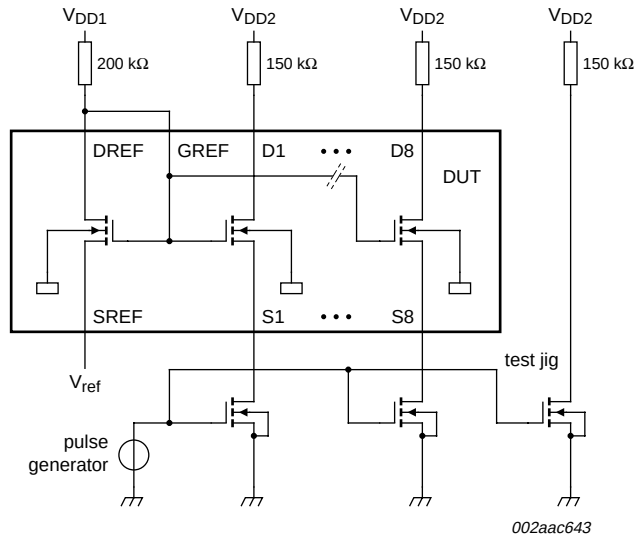
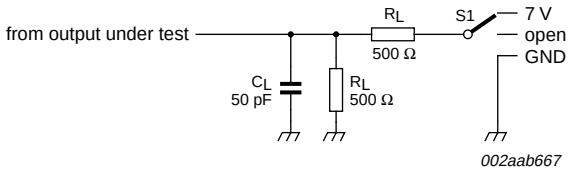


Fig 9. Load circuit for translator-type applications



Test data are given in Table 12.

C_L = load capacitance; includes jig and probe capacitance.

R_L = load resistance.

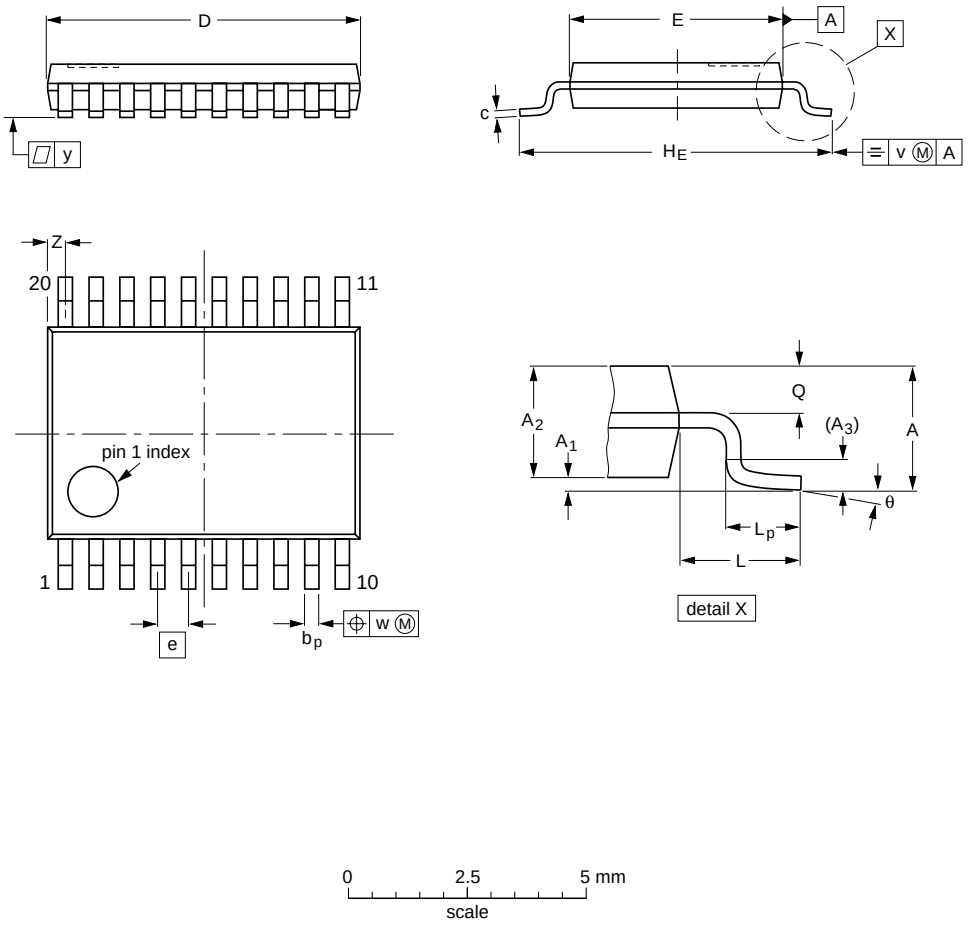
Fig 10. Load circuit for CBT-type application

Table 12. Test data

Test	Load		Switch
	C_L	R_L	
t_{PD}	50 pF	500 Ω	open
t_{PLZ}, t_{PZL}	50 pF	500 Ω	7 V
t_{PHZ}, t_{PZH}	50 pF	500 Ω	open

14. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

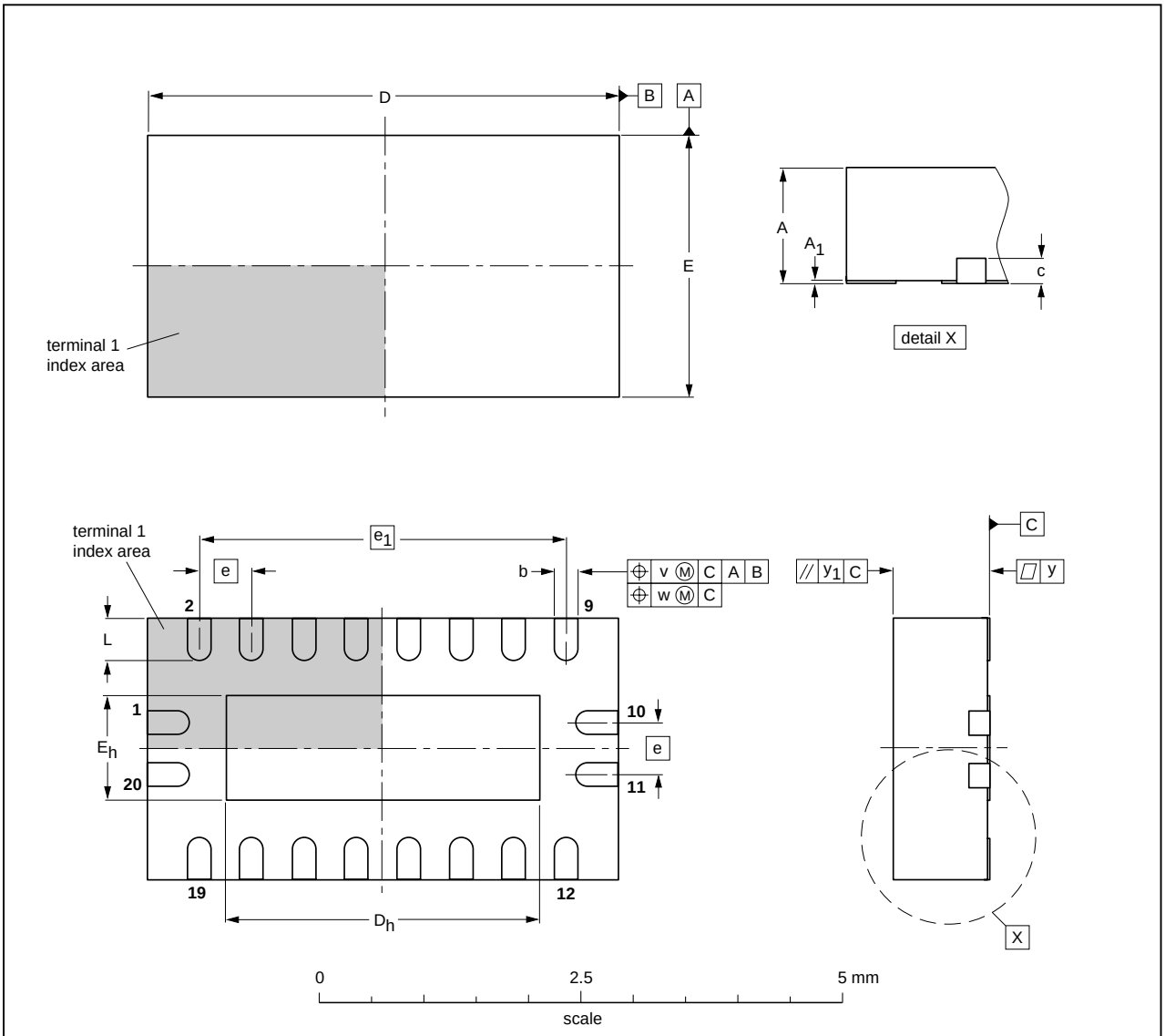
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.6 4.4	3.15 2.85	2.6 2.4	1.15 0.85	0.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 12. Package outline SOT764-1 (DHVQFN20)

15. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 13 and 14

Table 13. SnPb eutectic process (from J-STD-020C)

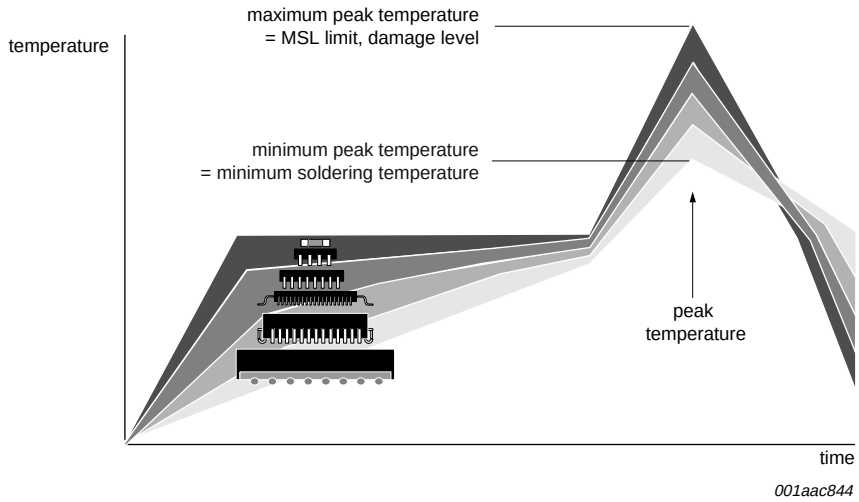
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 14. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 13.



MSL: Moisture Sensitivity Level

Fig 13. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Abbreviations

Table 15. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
GTL	Gunning Transceiver Logic
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
LVTTL	Low Voltage Transistor-Transistor Logic
MM	Machine Model
NMOS	Negative-channel Metal Oxide Semiconductor
TTL	Transistor-Transistor Logic
TVC	Transceiver Voltage Clamps

17. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
GTL2003_1	20070727	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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