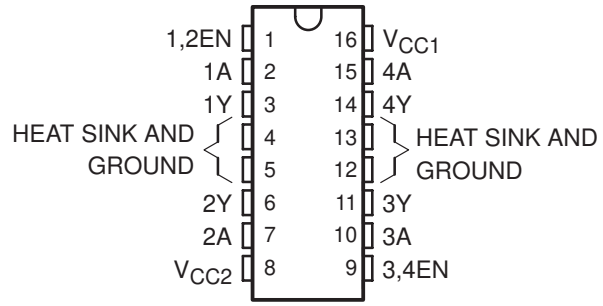
**EN:** This Datasheet/Document is presented by the manufacturer.

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- **1-A Output-Current Capability Per Driver**
- **Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers**
- **Designed for Positive-Supply Applications**
- **Wide Supply-Voltage Range of 4.5 V to 36 V**
- **TTL- and CMOS-Compatible High-Impedance Diode-Clamped Inputs**
- **Separate Input-Logic Supply**
- **Thermal Shutdown**
- **Internal ESD Protection**
- **Input Hysteresis Improves Noise Immunity**
- **3-State Outputs**
- **Minimized Power Dissipation**
- **Sink/Source Interlock Circuitry Prevents Simultaneous Conduction**
- **No Output Glitch During Power Up or Power Down**
- **Improved Functional Replacement for the SGS L293**

**NE PACKAGE**
**(TOP VIEW)**




**FUNCTION TABLE**
**(each driver)**

| INPUTS† | | OUTPUT |
|---|---|---|
| A | EN | Y |
| H | H | H |
| L | H | L |
| X | L | Z |

H = high-level, L = low-level
X = irrelevant
Z = high-impedance (off)
† In the thermal shutdown mode, the output is in a high-impedance state regardless of the input levels.

## description

The SN754410 is a quadruple high-current half-H driver designed to provide bidirectional drive currents up to 1 A at voltages from 4.5 V to 36 V. The device is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are compatible with TTL-and low-level CMOS logic. Each output (Y) is a complete totem-pole driver with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs become active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

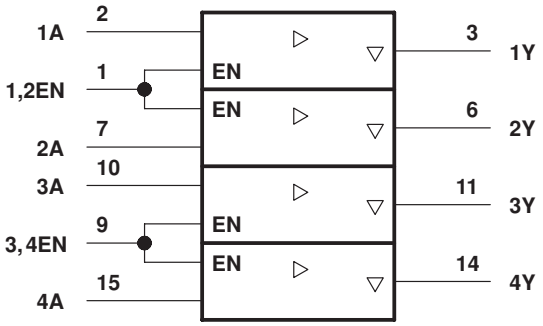
A separate supply voltage ($V_{CC1}$) is provided for the logic input circuits to minimize device power dissipation. Supply voltage $V_{CC2}$ is used for the output circuits.

The SN754410 is designed for operation from −40°C to 85°C.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

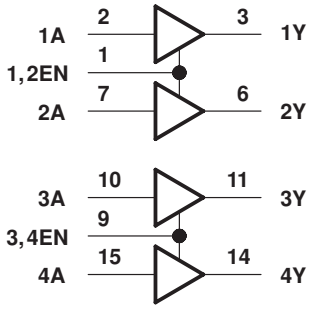
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## logic symbol†

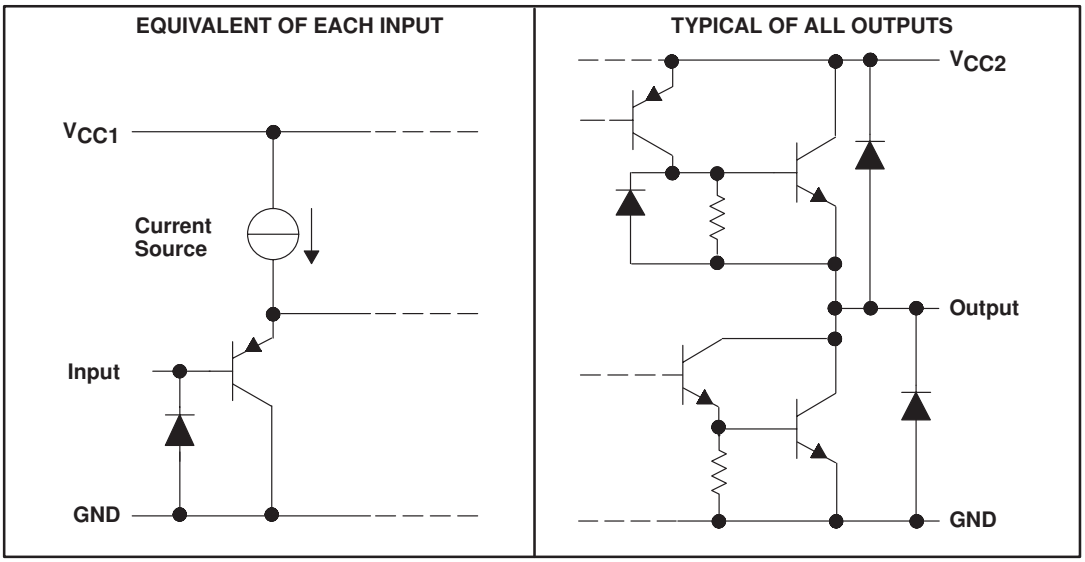



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram




## schematics of inputs and outputs



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Output supply voltage range, $V_{CC1}$ (see Note 1) . . . . . −0.5 V to 36 V
Output supply voltage range, $V_{CC2}$ . . . . . −0.5 V to 36 V
Input voltage, $V_I$ . . . . . 36 V
Output voltage range, $V_O$ . . . . . −3 V to $V_{CC2}$ + 3 V
Peak output current (nonrepetitive, $t_w \leq 5$ ms) . . . . . ±2 A
Continuous output current, $I_O$ . . . . . ±1.1 A
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 2075 mW
Operating free-air temperature range, $T_A$ . . . . . −40°C to 85°C
Operating virtual junction temperature range, $T_J$ . . . . . −40°C to 150°C
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network GND.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection can be activated at power levels slightly above or below the rated dissipation.

### recommended operating conditions

| | MIN | MAX | UNIT |
|---|---|---|---|
| Output supply voltage, $V_{CC1}$ | 4.5 | 5.5 | V |
| Output supply voltage, $V_{CC2}$ | 4.5 | 36 | V |
| High-level input voltage, $V_{IH}$ | 2 | 5.5 | V |
| Low-level input voltage, $V_{IL}$ | −0.3‡ | 0.8 | V |
| Operating virtual junction temperature, $T_J$ | −40 | 125 | °C |
| Operating free-air temperature, $T_A$ | −40 | 85 | °C |

‡ The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.

## electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | $I_I = -12$ mA | | | −0.9 | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH} = -0.5$ A | | $V_{CC2}-1.5$ | $V_{CC2}-1.1$ | | V |
| | | $I_{OH} = -1$ A | | $V_{CC2}-2$ | | | |
| | | $I_{OH} = -1$ A, | $T_J = 25°C$ | $V_{CC2}-1.8$ | $V_{CC2}-1.4$ | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL} = 0.5$ A | | | 1 | 1.4 | V |
| | | $I_{OL} = 1$ A | | | | 2 | |
| | | $I_{OL} = 1$ A, | $T_J = 25°C$ | | 1.2 | 1.8 | |
| $V_{OKH}$ | High-level output clamp voltage | $I_{OK} = -0.5$ A | | | $V_{CC2}+1.4$ | $V_{CC2}+2$ | V |
| | | $I_{OK} = 1$ A | | | $V_{CC2}+1.9$ | $V_{CC2}+2.5$ | |
| $V_{OKL}$ | Low-level output clamp voltage | $I_{OK} = 0.5$ A | | | −1.1 | −2 | V |
| | | $I_{OK} = -1$ A | | | −1.3 | −2.5 | |
| $I_{OZ(off)}$ | Off-state high-impedance-state output current | $V_O = V_{CC2}$ | | | | 500 | μA |
| | | $V_O = 0$ | | | | −500 | |
| $I_{IH}$ | High-level input current | $V_I = 5.5$ V | | | | 10 | μA |
| $I_{IL}$ | Low-level input current | $V_I = 0$ | | | | −10 | μA |
| $I_{CC1}$ | Output supply current | $I_O = 0$ | All outputs at high level | | | 38 | mA |
| | | | All outputs at low level | | | 70 | |
| | | | All outputs at high impedance | | | 25 | |
| $I_{CC2}$ | Output supply current | $I_O = 0$ | All outputs at high level | | | 33 | mA |
| | | | All outputs at low level | | | 20 | |
| | | | All outputs at high impedance | | | 5 | |

† All typical values are at $V_{CC1} = 5$ V, $V_{CC2} = 24$ V, $T_A = 25°C$.

## switching characteristics, $V_{CC1} = 5$ V, $V_{CC2} = 24$ V, $C_L = 30$ pF, $T_A = 25°C$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{d1}$ | Delay time, high-to-low-level output from A input | See Figure 1 | | 400 | | ns |
| $t_{d2}$ | Delay time, low-to-high-level output from A input | | | 800 | | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 300 | | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 300 | | ns |
| $t_r$ | Rise time, pulse input | | | | | |
| $t_f$ | Fall time, pulse input | | | | | |
| $t_w$ | Pulse duration | | | | | |
| $t_{en1}$ | Enable time to the high level | See Figure 2 | | 700 | | ns |
| $t_{en2}$ | Enable time to the low level | | | 400 | | ns |
| $t_{dis1}$ | Disable time from the high level | | | 900 | | ns |
| $t_{dis2}$ | Disable time from the low level | | | 600 | | ns |

## PARAMETER MEASUREMENT INFORMATION

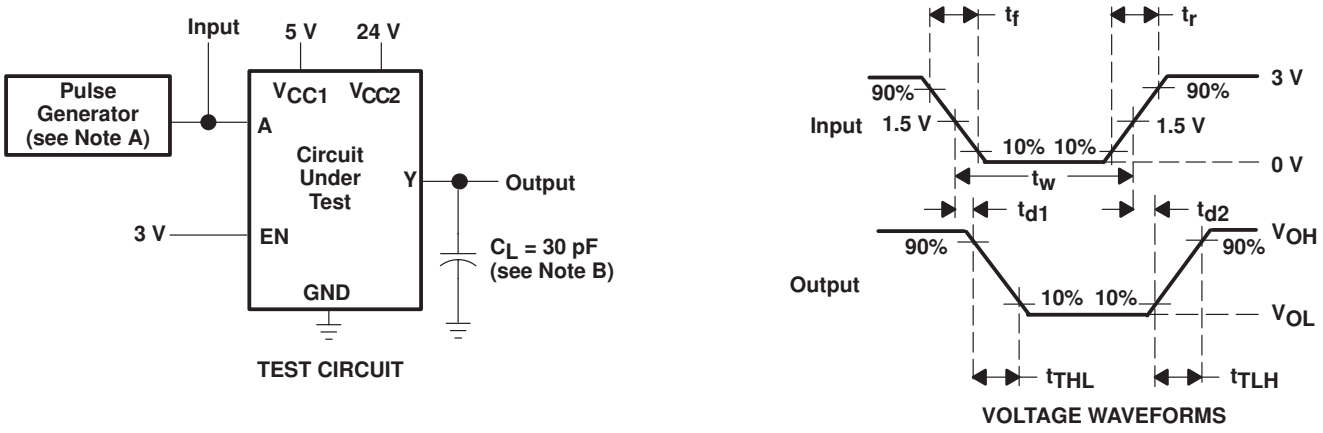



**Figure 1. Test Circuit and Switching Times From Data Inputs**

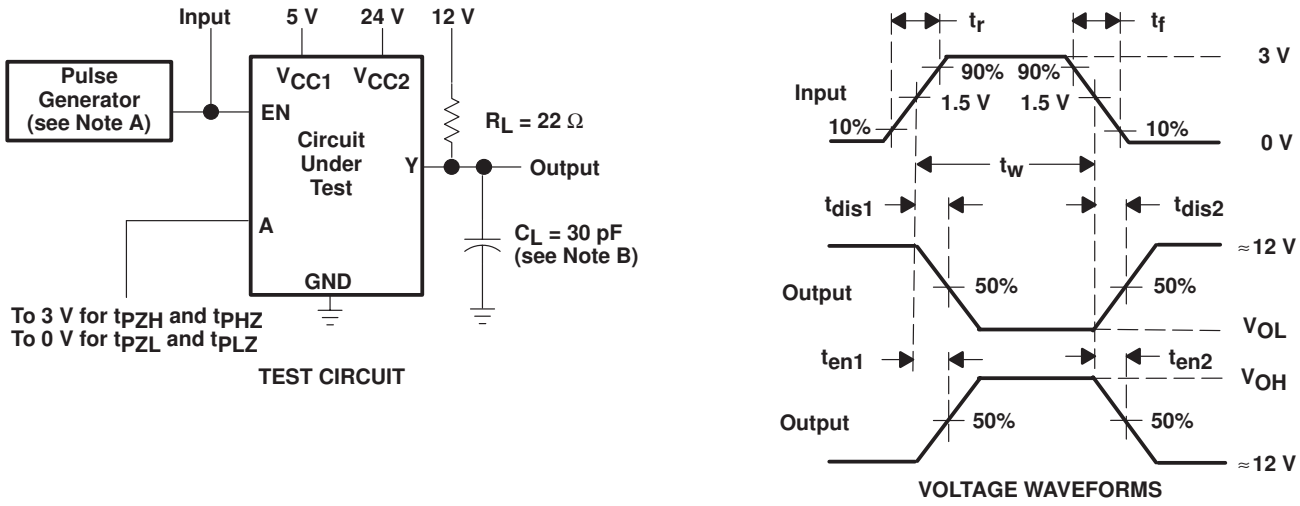



**Figure 2. Test Circuit and Switching Times From Enable Inputs**

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10$ µs, PRR = 5 kHz, $Z_O = 50$ Ω.
B. $C_L$ includes probe and jig capacitance.

## APPLICATION INFORMATION

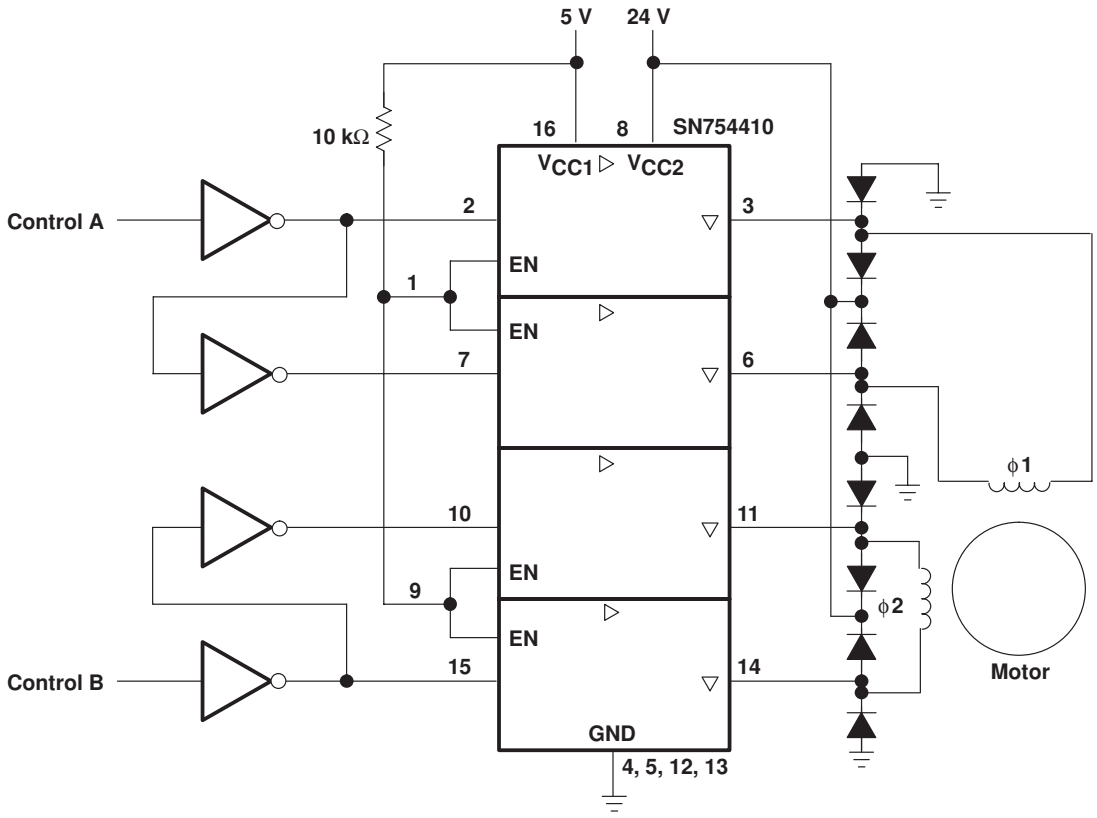



**Figure 3. Two-Phase Motor Driver**



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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN754410NE | ACTIVE | PDIP | NE | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN754410NEE4 | ACTIVE | PDIP | NE | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

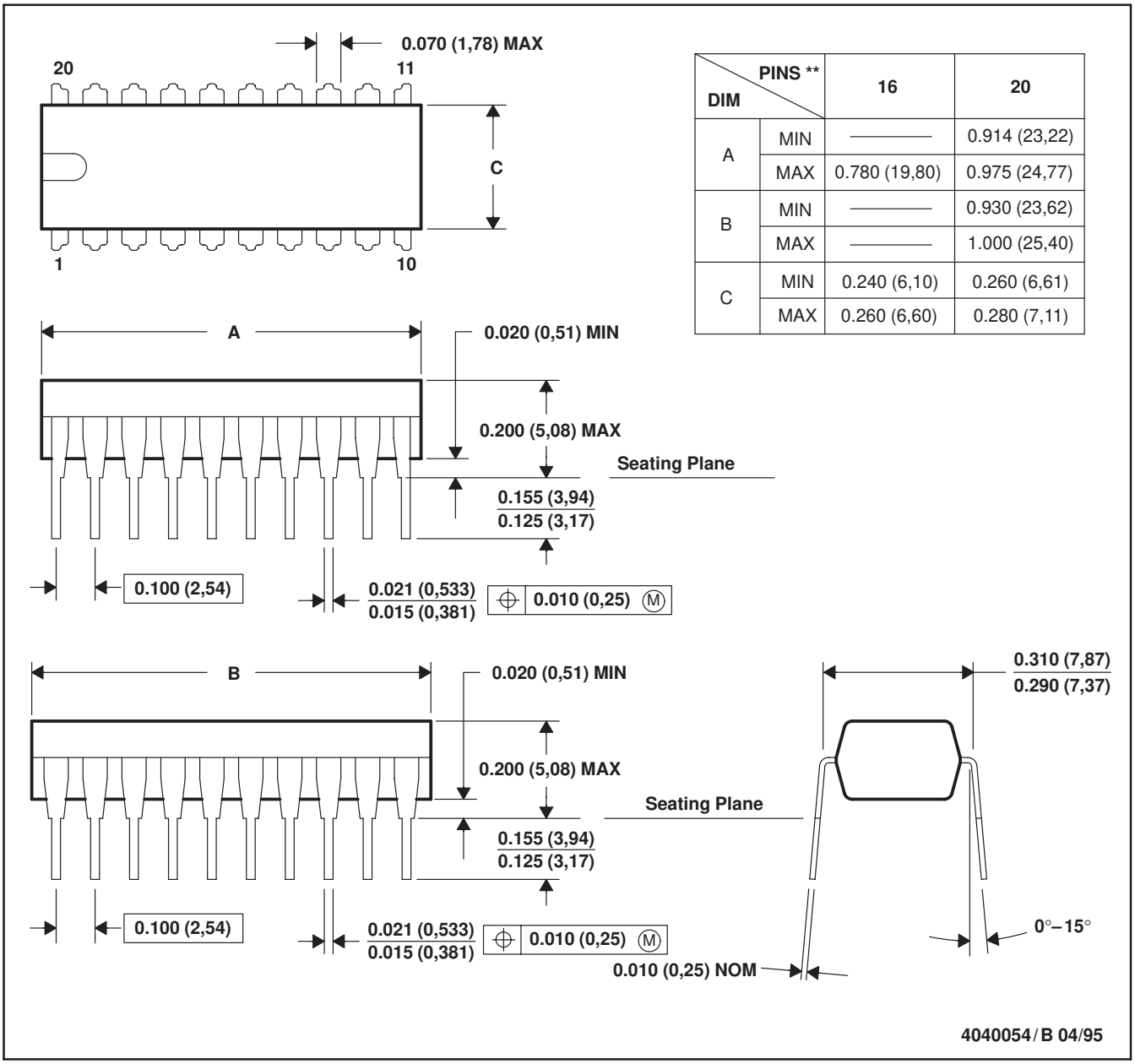
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MPDI003 – OCTOBER 1994

**NE (R-PDIP-T**)** **PLASTIC DUAL-IN-LINE PACKAGE**

**20 PIN SHOWN**




| DIM \ PINS ** | | 16 | 20 |
|---|---|---|---|
| A | MIN | ——— | 0.914 (23,22) |
| | MAX | 0.780 (19,80) | 0.975 (24,77) |
| B | MIN | ——— | 0.930 (23,62) |
| | MAX | ——— | 1.000 (25,40) |
| C | MIN | 0.240 (6,10) | 0.260 (6,61) |
| | MAX | 0.260 (6,60) | 0.280 (7,11) |

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (16 pin only)

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