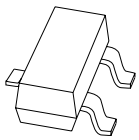
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PESD5V0S2BT

Low capacitance bi-directional double ESD protection diode in SOT23 package

Rev. 02 — 27 May 2004 Product data sheet

1. Product profile

1.1 General description

Low capacitance bi-directional double ESD protection diode in the small SOT23 plastic package designed to protect 2 data lines from the damage caused by Electro Static Discharge (ESD) and other transients.

1.2 Features

- Bi-directional ESD protection of 2 lines
- Low diode capacitance
- Max. peak pulse power: P_{pp} = 130 W at t_p = 8/20 µs
- Low clamping voltage: $V_{CL(R)}$ = 14 V at I_{pp} = 12 A
- Ultra low leakage current: I_{RM} = 5 nA at V_{RWM} = 5 V
- ESD protection > 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC-61000-4-5 (surge); I_{pp} = 12 A at t_p = 8/20 µs.

1.3 Applications

- Cellular handsets and accessories
- Portable electronics
- Computers and peripherals
- Communication systems
- Audio and video equipment.

1.4 Quick reference data

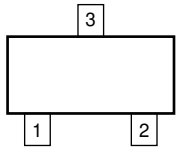
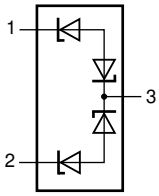
Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse stand-off voltage		-	5	-	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V	-	35	-	pF
	number of protected lines		-	2	-	

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2. Pinning information

Table 2: Discrete Pinning

Pin	Description	Simplified outline	Symbol
1	cathode 1		
2	cathode 2		
3	double cathode		

SOT23

sym031

3. Ordering information

Table 3: Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0S2BT	-	plastic surface mounted package; 3 leads	SOT23

4. Marking

Table 4: Marking

Type number	Marking code [1]
PESD5V0S2BT	*G5

[1] * = p: made in Hong Kong.
* = t: made in Malaysia.
* = W: made in China.

5. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per diode						
P_{pp}	peak pulse power	8/20 µs pulse	[1] [2]	-	130	W
I_{pp}	peak pulse current	8/20 µs pulse	[1] [2]	-	12	A
T_j	junction temperature			-	150	°C
T_{amb}	operating ambient temperature			–65	+150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform; see Figure 1.

[2] Measured between pins 1 to 3 or pin 2 to 3.

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Table 6: ESD maximum ratings

Symbol	Parameter	Conditions		Value	Unit
ESD	electro static discharge capability	IEC 61000-4-2 (contact discharge)	[1] [2]	30	kV
		HBM MIL-Std 883		10	kV

[1] Device stressed with ten non-repetitive Electro Static Discharge (ESD) pulses; see Figure 2.

[2] Measured between pins 1 to 3 or pin 2 to 3.

Table 7: ESD standards compliance

Standard	Conditions
IEC 61000-4-2; level 4 (ESD); see Figure 2	> 15 kV (air); > 8 kV (contact)
HBM MIL-Std 883; class 3	> 4 kV

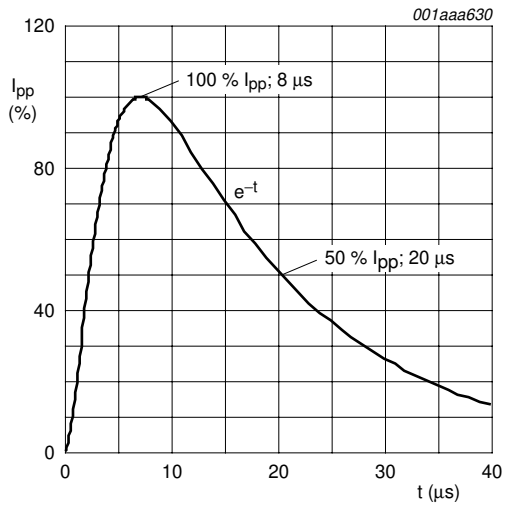


Fig 1. 8/20 µs pulse waveform according to IEC 61000-4-5.

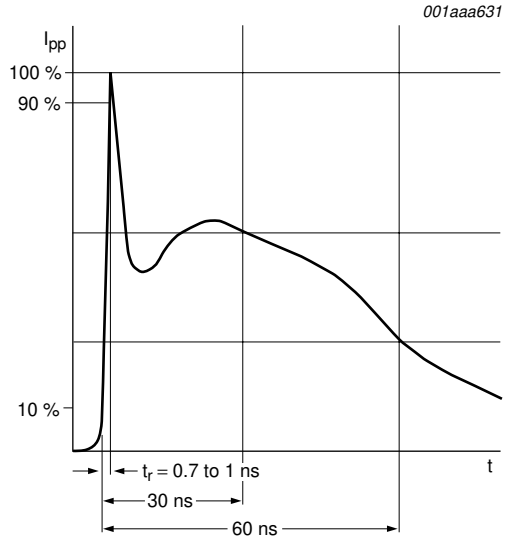


Fig 2. ElectroStatic Discharge (ESD) pulse waveform according to IEC 61000-4-2.

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6. Characteristics

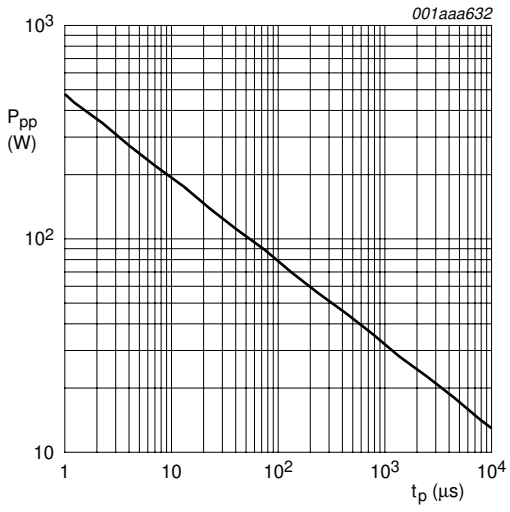
Table 8: Electrical characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per diode							
V_{RWM}	reverse stand-off voltage			-	-	5	V
I_{RM}	reverse leakage current	V_{RWM} = 5 V		-	5	100	nA
$V_{(CL)R}$	clamping voltage	I_{pp} = 1 A	[1] [2]	-	-	10	V
		I_{pp} = 12 A	[1] [2]	-	-	14	V
V_{BR}	breakdown voltage	I_R = 1 mA		5.5	-	9.5	V
r_{diff}	differential resistance	I_R = 1 mA		-	-	50	Ω
C_d	diode capacitance	f = 1 MHz; V_R = 0 V		-	35	45	pF

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform, see Figure 3.

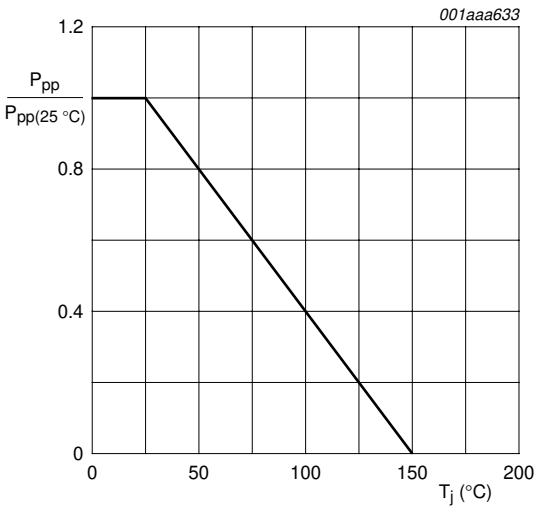
[2] Measured from pin 1 to 3 or pin 2 to 3.



T_{amb} = 25 °C.

t_p = 8/20 µs exponential decay waveform; see Figure 1.

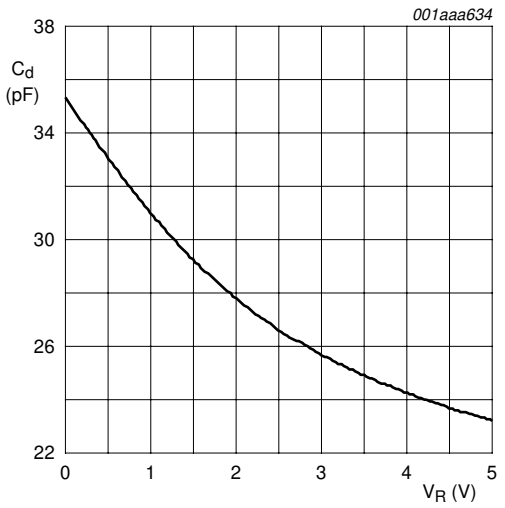
Fig 3. Peak pulse power dissipation as a function of pulse time; typical values.



T_{amb} = 25 °C.

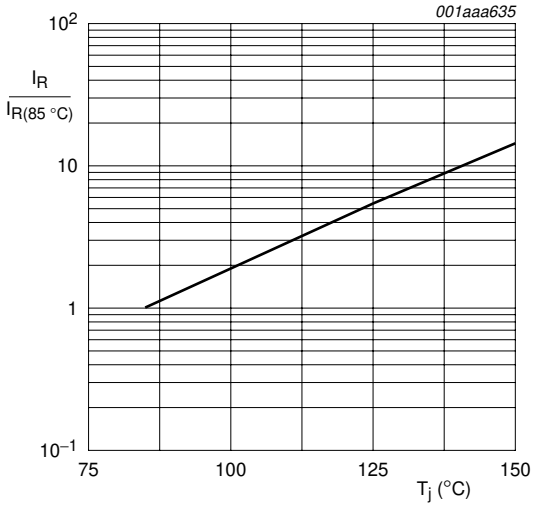
Fig 4. Relative variation of peak pulse power as a function of junction temperature; typical values.

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T_{amb} = 25 °C; f = 1 MHz.

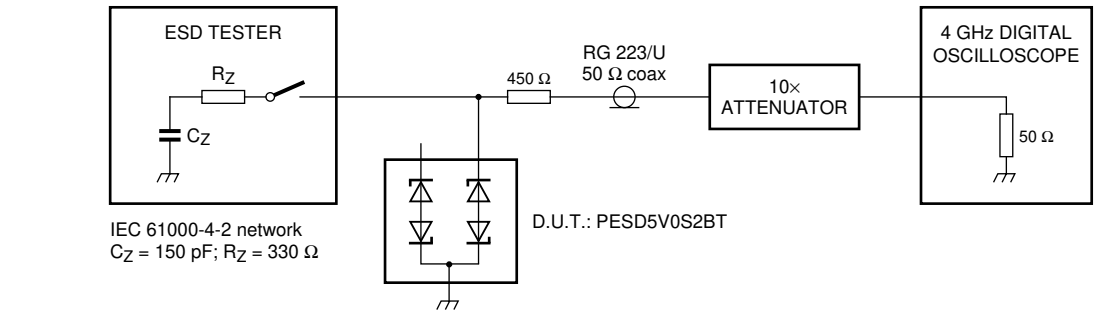
Fig 5. Diode capacitance as a function of reverse voltage; typical values.

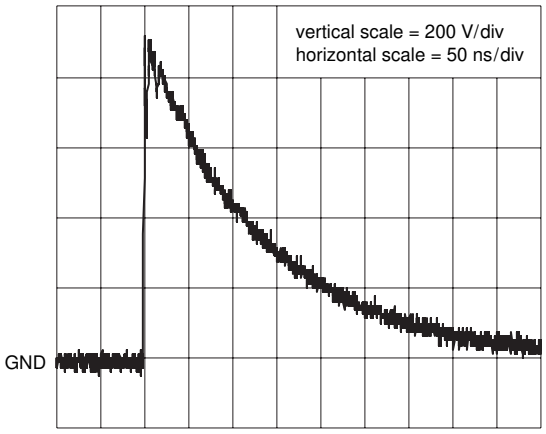


I_R < 1 nA measured at T_{amb} = 25 °C.

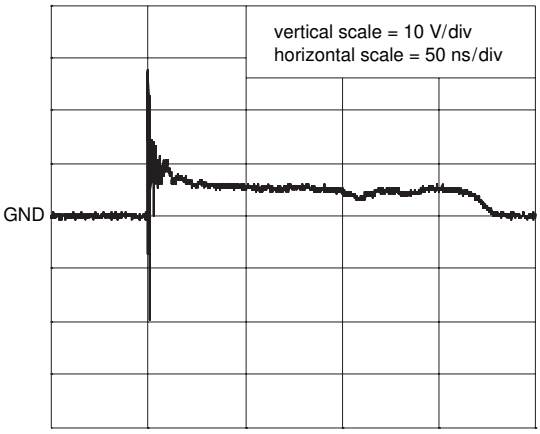
Fig 6. Relative variation of reverse leakage current as a function of junction temperature; typical values.

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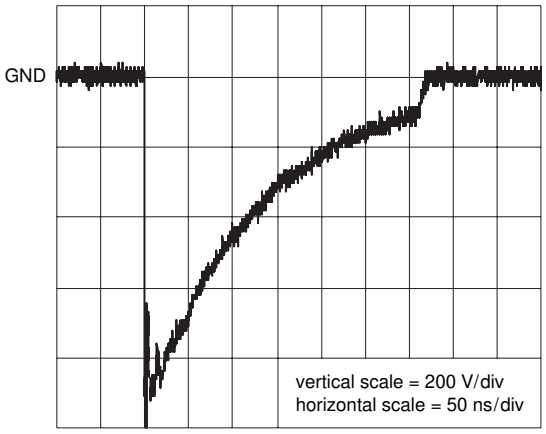




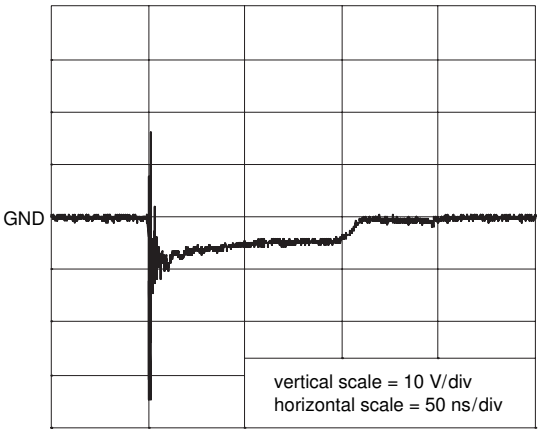
unclamped +1 kV ESD voltage waveform
(IEC61000-4-2 network)



clamped +1 kV ESD voltage waveform
(IEC61000-4-2 network)



unclamped −1 kV ESD voltage waveform
(IEC61000-4-2 network)



clamped −1 kV ESD voltage waveform
(IEC61000-4-2 network)

coa006

Fig 7. ESD clamping test set-up and waveforms.

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7. Application information

The PESD5V0S2BT is designed for the bi-directional protection of 2 lines from the damage caused by Electro Static Discharge (ESD) and surge pulses. The PESD5V0S2BT may be used on lines where the signal polarities are above and below ground. The PESD5V0S2BT provides a surge capability of 130 Watts peak P_{pp} per line for an 8/20 μs waveform.

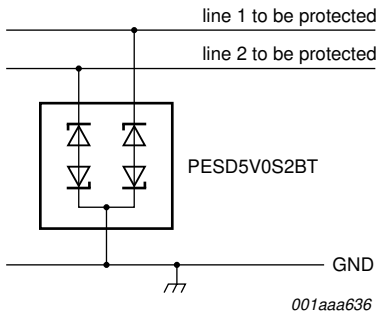


Fig 8. Typical application for bi-directional protection of two lines.

Circuit board layout and protection device placement:

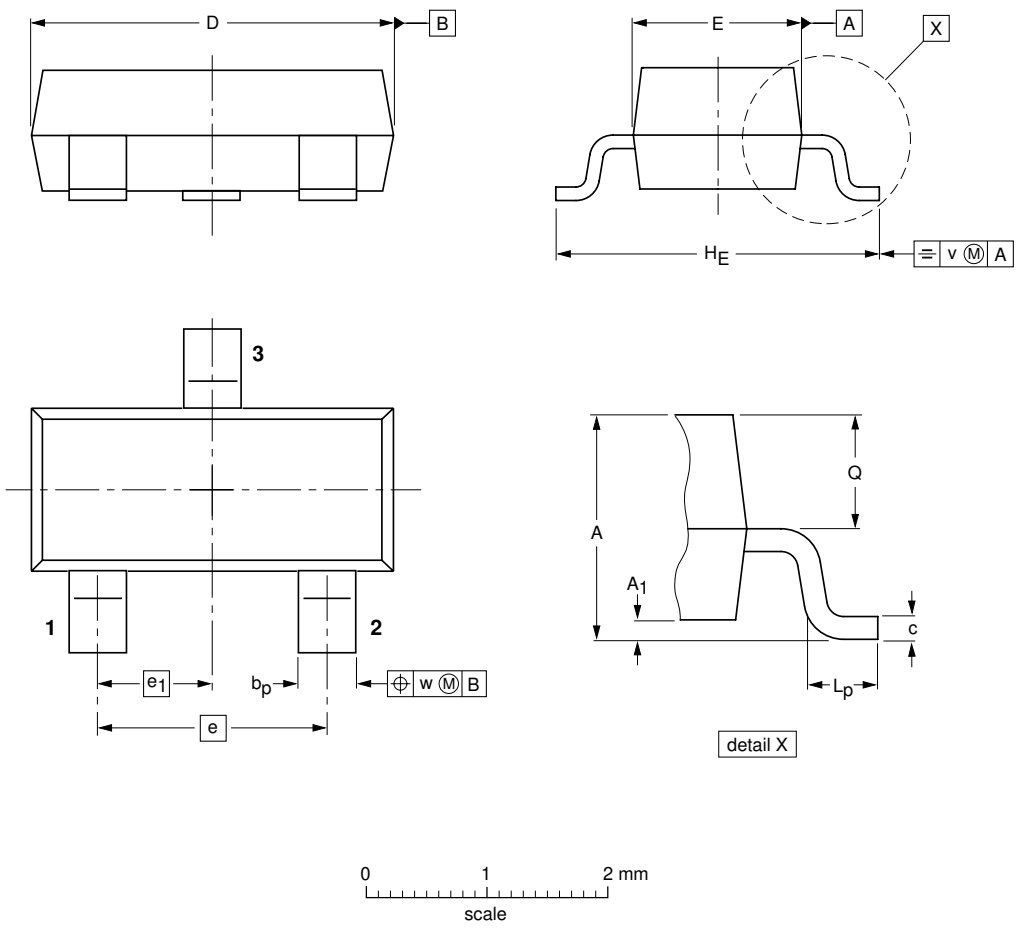
Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the PESD5V0S2BT as close to the input terminal or connector as possible.
2. The path length between the PESD5V0S2BT and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all printed-circuit board conductive loops including power and group loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer printed-circuit boards, use ground vias.

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8. Package outline

Plastic surface mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23		TO-236AB				~~97-02-28~~ 99-09-13

Fig 9. Package outline.

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9. Revision history

Table 9: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
PESD5V0S2BT_2	20040527	Product data	-	9397 750 13344	PESD5V0S2BT_1
PESD5V0S2BT_1	20040517	Product data	-	9397 750 12901	-

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10. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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