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FAIRCHILD SEMICONDUCTOR™

October 1987
Revised April 2002

CD4049UBC • CD4050BC
Hex Inverting Buffer • Hex Non-Inverting Buffer

General Description

The CD4049UBC and CD4050BC hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. These devices feature logic level conversion using only one supply voltage (V_{DD}). The input signal high level (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers, and at V_{DD} = 5.0V, they can drive directly two DTL/TTL loads over the full operating temperature range.

Features

- Wide supply voltage range: 3.0V to 15V
- Direct drive to 2 TTL loads at 5.0V over full temperature range
- High source and sink current capability
- Special input protection permits input voltages greater than V_{DD}

Applications

- CMOS hex inverter/buffer
- CMOS to DTL/TTL hex converter
- CMOS current “sink” or “source” driver
- CMOS HIGH-to-LOW logic level converter

Ordering Code:

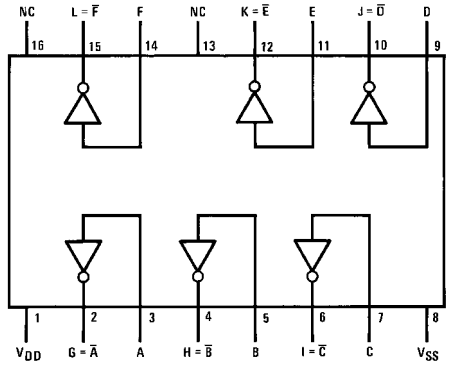
Order Number	Package Number	Package Description
CD4049UBCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4049UBCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4050BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4050BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Connection Diagrams

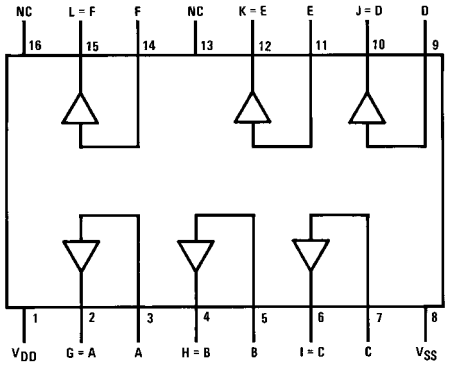
Pin Assignments for DIP

CD4049UBC



Top View

CD4050BC

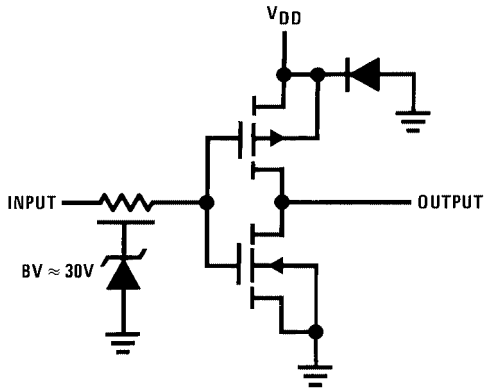


Top View

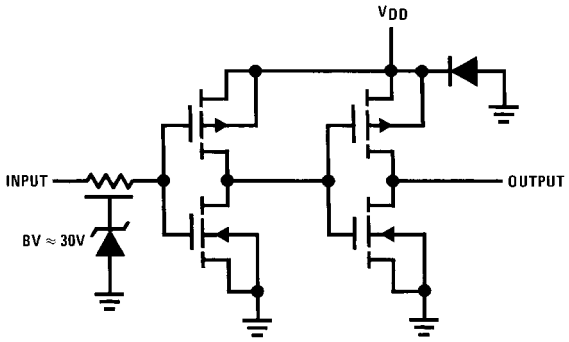
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Schematic Diagrams

CD4049UBC
1 of 6 Identical Units



CD4050BC
1 of 6 Identical Units



Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to +18V
Voltage at Any Output Pin (V_{OUT})	−0.5V to V_{DD} + 0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to 15V
Voltage at Any Output Pin (V_{OUT})	0 to V_{DD}
Operating Temperature Range (T_A)	
CD4049UBC, CD4050BC	−55°C to +125°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.01	1.0		30	
		V_{DD} = 10V		2.0		0.01	2.0		60	μA
		V_{DD} = 15V		4.0		0.03	4.0		120	
V_{OL}	LOW Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V,								
		$\|I_O\|$ < 1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	
V_{OH}	HIGH Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V,								
		$\|I_O\|$ < 1 μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		
V_{IL}	LOW Level Input Voltage	$\|I_O\|$ < 1 μA								
	(CD4050BC Only)	V_{DD} = 5V, V_O = 0.5V		1.5		2.25	1.5		1.5	
		V_{DD} = 10V, V_O = 1V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6.75	4.0		4.0	
V_{IL}	LOW Level Input Voltage	$\|I_O\|$ < 1 μA								
	(CD4049UBC Only)	V_{DD} = 5V, V_O = 4.5V		1.0		1.5	1.0		1.0	
		V_{DD} = 10V, V_O = 9V		2.0		2.5	2.0		2.0	V
		V_{DD} = 15V, V_O = 13.5V		3.0		3.5	3.0		3.0	
V_{IH}	HIGH Level Input Voltage	$\|I_O\|$ < 1 μA								
	(CD4050BC Only)	V_{DD} = 5V, V_O = 4.5V	3.5		3.5	2.75		3.5		
		V_{DD} = 10V, V_O = 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	8.25		11.0		
V_{IH}	HIGH Level Input Voltage	$\|I_O\|$ < 1 μA								
	(CD4049UBC Only)	V_{DD} = 5V, V_O = 0.5V	4.0		4.0	3.5		4.0		
		V_{DD} = 10V, V_O = 1V	8.0		8.0	7.5		8.0		V
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0	11.5		12.0		
I_{OL}	LOW Level Output Current	V_{IH} = V_{DD}, V_{IL} = 0V								
	(Note 4)	V_{DD} = 5V, V_O = 0.4V	5.6		4.6	5		3.2		
		V_{DD} = 10V, V_O = 0.5V	12		9.8	12		6.8		mA
		V_{DD} = 15V, V_O = 1.5V	35		29	40		20		
I_{OH}	HIGH Level Output Current	V_{IH} = V_{DD}, V_{IL} = 0V								
	(Note 4)	V_{DD} = 5V, V_O = 4.6V	−1.3		−1.1	−1.6		−0.72		
		V_{DD} = 10V, V_O = 9.5V	−2.6		−2.2	−3.6		−1.5		mA
		V_{DD} = 15V, V_O = 13.5V	−8.0		−7.2	−12		−5		
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	

Note 3: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Continued)

Note 4: These are peak output current capabilities. Continuous output current is rated at 12 mA maximum. The output current should not be allowed to exceed this value for extended periods of time. I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics (Note 5)

CD4049UBC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Time	$V_{DD} = 5V$		30	65	
	HIGH-to-LOW Level	$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	
t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		45	85	
	LOW-to-HIGH Level	$V_{DD} = 10V$		25	45	ns
		$V_{DD} = 15V$		20	35	
t_{THL}	Transition Time	$V_{DD} = 5V$		30	60	
	HIGH-to-LOW Level	$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	
t_{TLH}	Transition Time	$V_{DD} = 5V$		60	120	
	LOW-to-HIGH Level	$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	
C_{IN}	Input Capacitance	Any Input		15	22.5	pF

Note 5: AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics (Note 6)

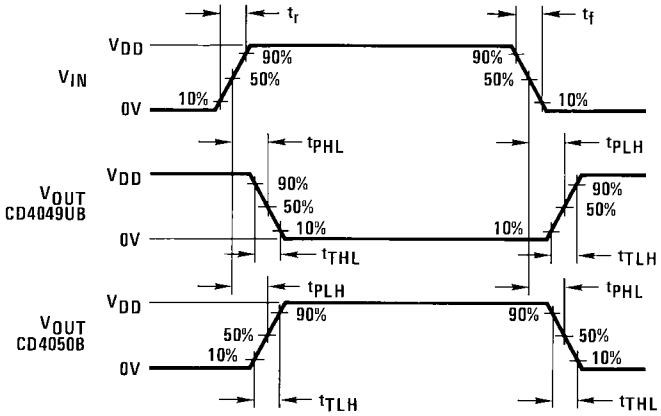
CD4050BC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Time	$V_{DD} = 5V$		60	110	
	HIGH-to-LOW Level	$V_{DD} = 10V$		25	55	ns
		$V_{DD} = 15V$		20	30	
t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		60	120	
	LOW-to-HIGH Level	$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	
t_{THL}	Transition Time	$V_{DD} = 5V$		30	60	
	HIGH-to-LOW Level	$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	
t_{TLH}	Transition Time	$V_{DD} = 5V$		60	120	
	LOW-to-HIGH Level	$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

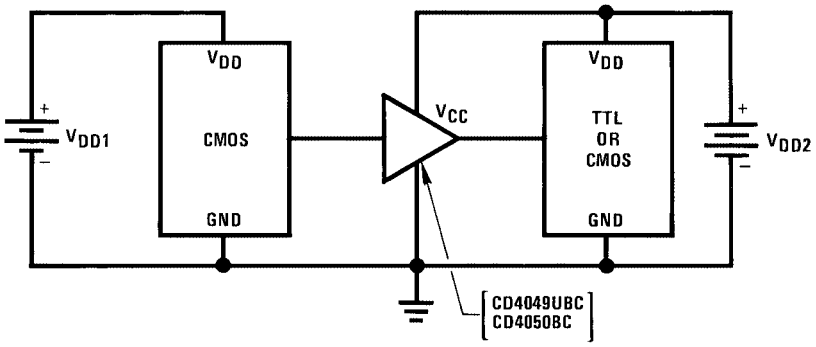
Note 6: AC Parameters are guaranteed by DC correlated testing.

Switching Time Waveforms



Typical Applications

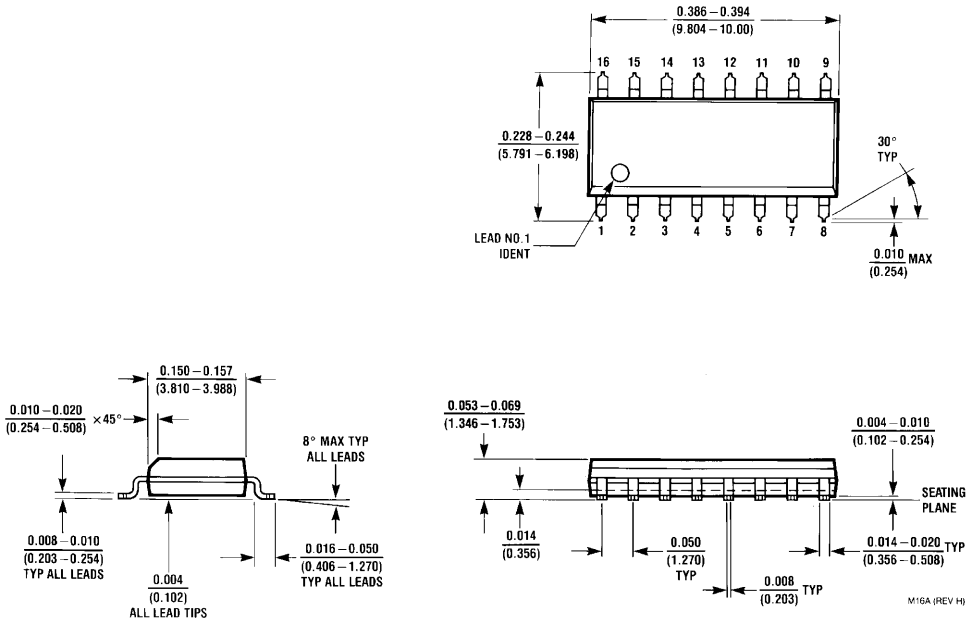
CMOS to TLL or CMOS at a Lower V_{DD}



$V_{DD1} \geq V_{DD2}$

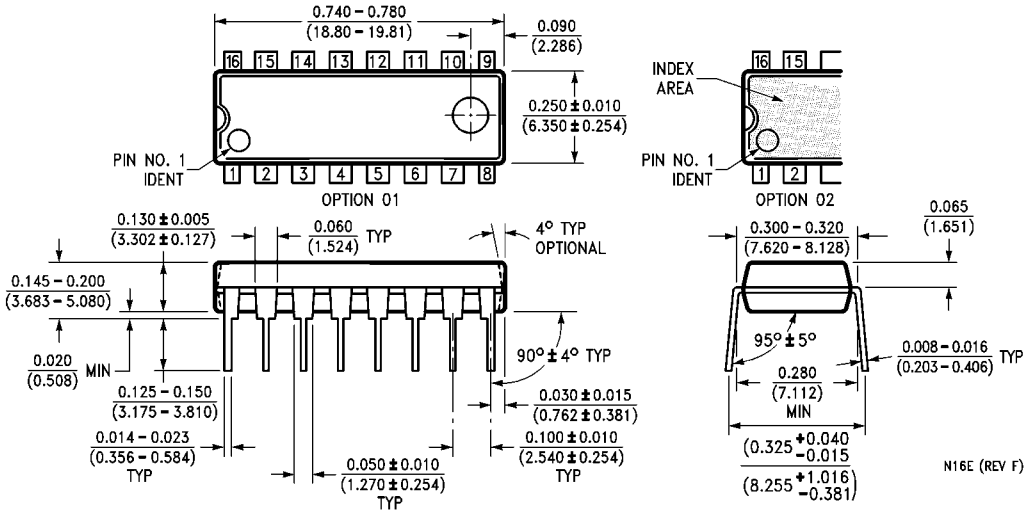
In the case of the CD4049UBC the output drive capability increases with increasing input voltage.
E.g., If V_{DD1} = 10V the CD4049UBC could drive 4 TTL loads.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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