**EN:** This Datasheet/Document is presented by the manufacturer.

Please visit our website for pricing and availability at www.hestore.hu.

# CD54/74HC533, CD54/74HCT533, CD54/74HC563, CD74HCT563

## High-Speed CMOS Logic Octal Inverting Transparent Latch, Three-State Outputs

Data sheet acquired from Harris Semiconductor
SCHS187C

January 1998 - Revised July 2003

### Features

- **Common Latch-Enable Control**
- **Common Three-State Output Enable Control**
- **Buffered Inputs**
- **Three-State Outputs**
- **Bus Line Driving Capacity**
- **Typical Propagation Delay = 13ns at $V_{CC}$ = 5V, $C_L$ = 15pF, $T_A$ = 25$^oC$ (Data to Output)**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55$^oC$ to 125$^oC$**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, $V_{IL}$= 0.8V (Max), $V_{IH}$ = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at $V_{OL}$, $V_{OH}$**

### Description

The 'HC533, 'HCT533, 'HC563, and CD74HCT563 are high-speed Octal Transparent Latches manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL devices.

The outputs are transparent to the inputs when the latch enable ($\overline{LE}$) is high. When the latch enable ($\overline{LE}$) goes low the data is latched. The output enable ($\overline{OE}$) controls the three-state outputs. When the output enable ($\overline{OE}$) is high the outputs are in the high impedance state. The latch operation is independent of the state of the output enable.

The 'HC533 and 'HCT533 are identical in function to the 'HC563 and CD74HCT563 but have different pinouts. The 'HC533 and 'HCT533 are similar to the 'HC373 and 'HCT373; the latter are non-inverting types.

### Ordering Information

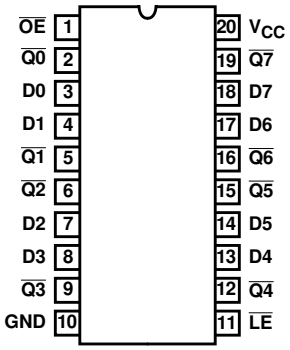
| PART NUMBER | TEMP. RANGE ($^oC$) | PACKAGE |
|---|---|---|
| CD54HC533F3A | -55 to 125 | 20 Ld CERDIP |
| CD54HC563F3A | -55 to 125 | 20 Ld CERDIP |
| CD54HCT533F3A | -55 to 125 | 20 Ld CERDIP |
| CD74HC533E | -55 to 125 | 20 Ld PDIP |
| CD74HC563E | -55 to 125 | 20 Ld PDIP |
| CD74HC563M | -55 to 125 | 20 Ld SOIC |
| CD74HCT533E | -55 to 125 | 20 Ld PDIP |
| CD74HCT563E | -55 to 125 | 20 Ld PDIP |
| CD74HCT563M | -55 to 125 | 20 Ld SOIC |

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

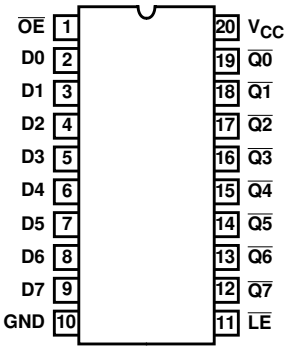
Copyright © 2003, Texas Instruments Incorporated

## Pinouts

**CD54HC533, CD54HCT533**
**(CERDIP)**
**CD74HC533, CD74HCT533**
**(PDIP)**
TOP VIEW

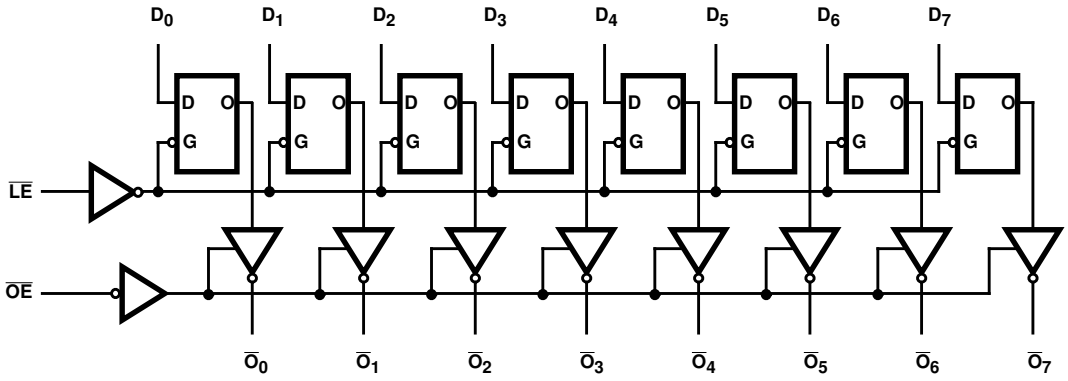



**CD54HC563**
**(CERDIP)**
**CD74HC563, CD74HCT563**
**(PDIP, SOIC)**
TOP VIEW




## Functional Block Diagram

**HC/HCT533**




**TRUTH TABLE**

| OUTPUT ENABLE | LATCH ENABLE | DATA | Q OUTPUT |
|---|---|---|---|
| L | H | H | L |
| L | H | L | H |
| L | L | l | H |
| L | L | h | L |
| H | X | X | Z |

H = High Voltage Level, L = Low Voltage Level, X = Don't Care, Z = High Impedance State, l = Low voltage level one set-up time prior to the high to low latch enable transition, h = High voltage level one set-up time prior to the high to low latch enable transition.

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . -0.5V to 7V
DC Input Diode Current, $I_{IK}$
For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Drain Current, per Output, $I_O$
For -0.5V < $V_O$ < $V_{CC}$ + 0.5V . . . . . ±35mA
DC Output Source or Sink Current per Output Pin, $I_O$
For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ . . . . . ±50mA

## Operating Conditions

Temperature Range, $T_A$ . . . . . -55°C to 125°C
Supply Voltage Range, $V_{CC}$
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . 0V to $V_{CC}$
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ (°C/W) |
|---|---|
| E (PDIP) Package | 69 |
| M (SOIC) Package | 58 |

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | | | -6 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -7.8 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 6 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 7.8 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | µA |

## DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Three-State Leakage Current | - | $V_{IL}$ or $V_{IH}$ | $V_O$ = $V_{CC}$ or GND | 6 | - | - | ±0.5 | - | ±5 | - | ±10 | µA |
| **HCT TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -6 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 6 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ to GND | - | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | µA |
| Three-State Leakage Current | - | $V_{IL}$ or $V_{IH}$ | $V_O$ = $V_{CC}$ or GND | 5.5 | - | - | ±0.5 | - | ±5 | - | ±10 | µA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note 2) | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | µA |

NOTE:

2. For dual-supply systems theoretical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| D0 - D7 | 0.15 |
| $\overline{LE}$ | 0.30 |
| $\overline{OE}$ | 0.55 |

NOTE: Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

## Prerequisite For Switching Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | |
| $\overline{LE}$ Pulse Width | $t_W$ | - | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| | | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | | 6 | 14 | - | - | 17 | - | 20 | - | ns |
| Set-up Time Data to $\overline{LE}$ | $t_{SU}$ | - | 2 | 50 | - | - | 65 | - | 75 | - | ns |
| | | | 4.5 | 10 | - | - | 13 | - | 15 | - | ns |
| | | | 6 | 9 | - | - | 11 | - | 13 | - | ns |
| Hold Time, Data to $\overline{LE}$ (533) | $t_H$ | - | 2 | 35 | - | - | 45 | - | 55 | - | ns |
| | | | 4.5 | 7 | - | - | 9 | - | 11 | - | ns |
| | | | 6 | 6 | - | - | 8 | - | 7 | - | ns |
| Hold Time, Data to $\overline{LE}$ (563) | $t_H$ | - | 2 | 4 | - | - | 4 | - | 4 | - | ns |
| | | | 4.5 | 4 | - | - | 4 | - | 4 | - | ns |
| | | | 6 | 4 | - | - | 4 | - | 4 | - | ns |
| **HCT TYPES** | | | | | | | | | | | |
| $\overline{LE}$ Pulse Width | $t_w$ | - | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| Set-up Time Data to $\overline{LE}$ | $t_w$ | - | 4.5 | 10 | - | - | 13 | - | 15 | - | ns |
| Hold Time, Data to $\overline{LE}$ (533) | $t_H$ | - | 4.5 | 8 | - | - | 10 | - | 12 | - | ns |
| Hold Time, Data to $\overline{LE}$ (563) | $t_H$ | - | 4.5 | 5 | - | - | 5 | - | 5 | - | ns |

## Switching Specifications Input $t_r$, $t_f$ = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | | TYP | MAX | MAX | MAX | |
| **HC TYPES** | | | | | | | | |
| Propagation Delay, Data to Qn (HC533) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | 165 | 205 | 250 | ns |
| | | | 4.5 | - | 33 | 41 | 50 | ns |
| | | | 6 | - | 28 | 35 | 43 | ns |
| | | $C_L$ = 15pF | 5 | 13 | - | - | - | ns |
| Propagation Delay, Data to Qn (HC563) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | 150 | 190 | 225 | ns |
| | | | 4.5 | - | 30 | 38 | 45 | ns |
| | | | 6 | - | 26 | 33 | 38 | ns |
| | | $C_L$ = 15pF | 5 | 12 | - | - | - | ns |
| Propagation Delay, $\overline{LE}$ to Qn (HC533) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | 175 | 220 | 265 | ns |
| | | | 4.5 | - | 35 | 44 | 53 | ns |
| | | | 6 | - | 30 | 37 | 45 | ns |
| | | $C_L$ = 15pF | 5 | 14 | - | - | - | ns |
| Propagation Delay, $\overline{LE}$ to Qn (HC563) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | 165 | 205 | 250 | ns |
| | | | 4.5 | - | 33 | 41 | 50 | ns |
| | | | 6 | - | 28 | 35 | 43 | ns |
| | | $C_L$ = 15pF | 5 | 13 | - | - | - | ns |

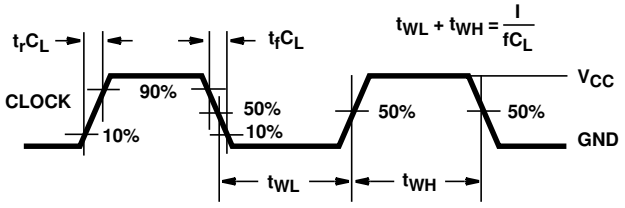
**Switching Specifications** Input $t_r$, $t_f$ = 6ns **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | | TYP | MAX | MAX | MAX | |
| Enable Times (HC533) | $t_{PZH}$, $t_{PZL}$ | $C_L$ = 50pF | 2 | - | 150 | 190 | 225 | ns |
| | | | 4.5 | - | 30 | 38 | 45 | ns |
| | | | 6 | - | 26 | 33 | 38 | ns |
| | | $C_L$ = 15pF | 5 | 12 | - | - | - | ns |
| Disable Times (HC533) | $t_{PHZ}$, $t_{PLZ}$ | $C_L$ = 50pF | 2 | - | 150 | 190 | 225 | ns |
| | | | 4.5 | - | 30 | 38 | 45 | ns |
| | | | 6 | - | 26 | 33 | 38 | ns |
| | | $C_L$ = 15pF | 5 | 12 | - | - | - | ns |
| Enable and Disable Times (HC563) | $t_{PZH}$, $t_{PZL}$, $t_{PHZ}$, $t_{PLZ}$ | $C_L$ = 50pF | 2 | - | 150 | 190 | 225 | ns |
| | | | 4.5 | - | 30 | 38 | 45 | ns |
| | | | 6 | - | 26 | 33 | 38 | ns |
| | | $C_L$ = 15pF | 5 | 12 | - | - | - | ns |
| Input Capacitance | $C_I$ | - | - | - | 10 | 10 | 10 | pF |
| Three-State Output Capacitance | $C_O$ | - | - | - | 20 | 20 | 20 | pF |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$ | - | 5 | 42 | - | - | - | pF |
| **HCT TYPES** | | | | | | | | |
| Propagation Delay, Data to Qn (HC/HCT533) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | 34 | 43 | 51 | ns |
| | | $C_L$ = 15pF | 5 | 14 | - | - | - | ns |
| Propagation Delay, Data to Qn (HC/HCT563) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | 30 | 38 | 45 | ns |
| | | $C_L$ = 15pF | 5 | 12 | - | - | - | ns |
| Propagation Delay, $\overline{LE}$ to Qn (HC/HCT533) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | 38 | 48 | 57 | ns |
| | | $C_L$ = 15pF | 5 | 16 | - | - | - | ns |
| Propagation Delay, $\overline{LE}$ to Qn (HC/HCT563) | $t_{PZL}$, $t_{PZH}$ | $C_L$ = 50pF | 4.5 | - | 35 | 44 | 53 | ns |
| | | $C_L$ = 15pF | 5 | 14 | - | - | - | ns |
| Enable Times (HC/HCT533) | $t_{PLZ}$, $t_{PZH}$ | $C_L$ = 50pF | 4.5 | - | 35 | 44 | 53 | ns |
| | | $C_L$ = 15pF | 5 | 14 | - | - | - | ns |
| Disable Times (HC/HCT533) | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | - | 30 | 38 | 45 | ns |
| | | $C_L$ = 15pF | 5 | 12 | - | - | - | ns |
| Enable and Disable Times (HC/HCT563) | $t_{PZH}$, $t_{PZL}$, $t_{PHZ}$, $t_{PLZ}$ | $C_L$ = 50pF | 4.5 | - | 35 | 44 | 53 | ns |
| | | $C_L$ = 15pF | 5 | 14 | - | - | - | ns |
| Input Capacitance | $C_I$ | - | - | - | 10 | 10 | 10 | pF |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$ | - | 5 | 42 | - | - | - | pF |

NOTES:

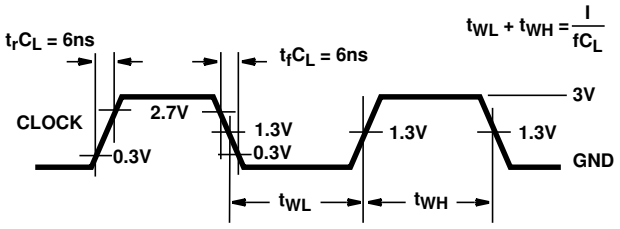
3. $C_{PD}$ is used to determine the no-load dynamic power consumption, per latch.
4. $P_D$ (total power per latch) = $C_{PD}\ V_{CC}^2\ f_i + \Sigma\ C_L\ V_{CC}^2\ f_o$ where $f_i$ = Input Frequency, $f_o$ = Output Frequency, $C_L$ = Output Load Capacitance, $V_{CC}$ = Supply Voltage.

## Test Circuits and Waveforms




NOTE: Outputs should be switching from 10% $V_{CC}$ to 90% $V_{CC}$ in accordance with device truth table. For $f_{MAX}$, input duty cycle = 50%.

**FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**




NOTE: Outputs should be switching from 10% $V_{CC}$ to 90% $V_{CC}$ in accordance with device truth table. For $f_{MAX}$, input duty cycle = 50%.

**FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**

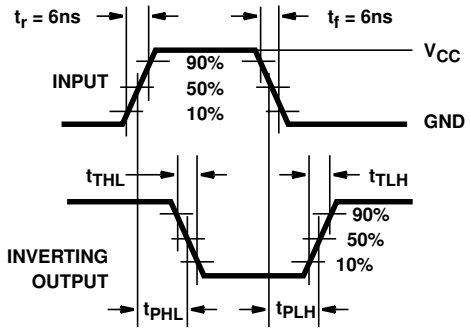



**FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

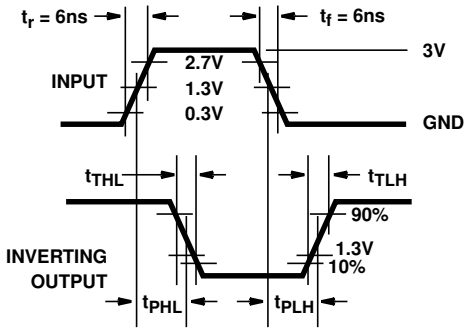



**FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

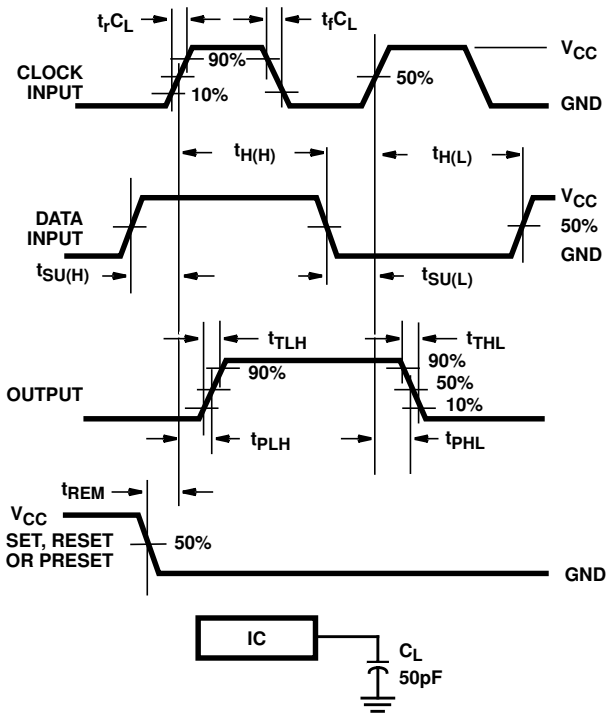



**FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**

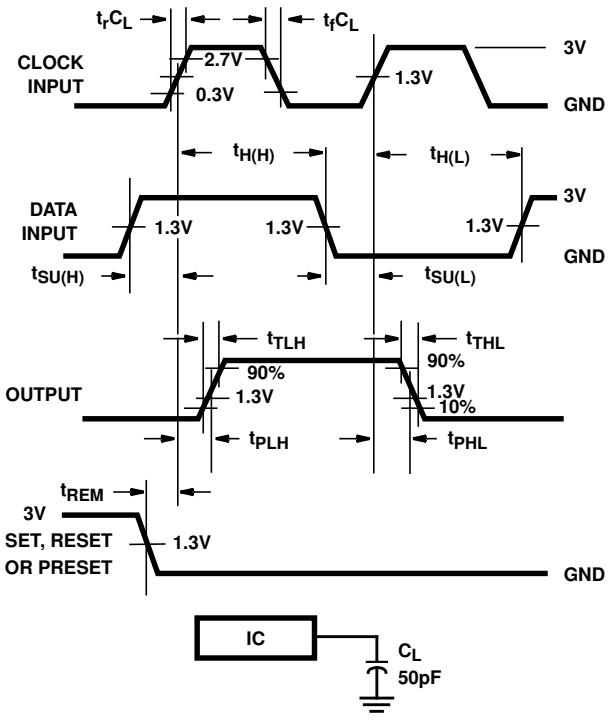



**FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**

## Test Circuits and Waveforms (Continued)

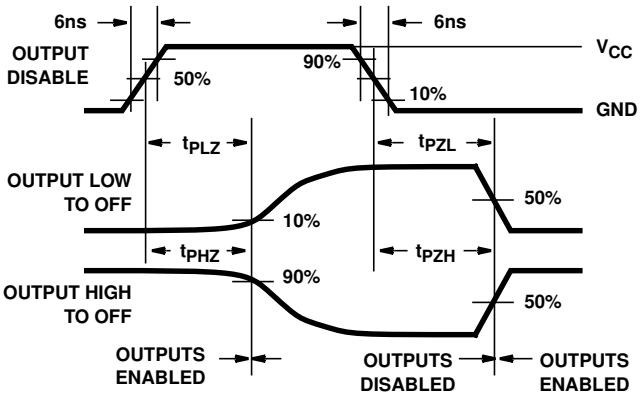



FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM

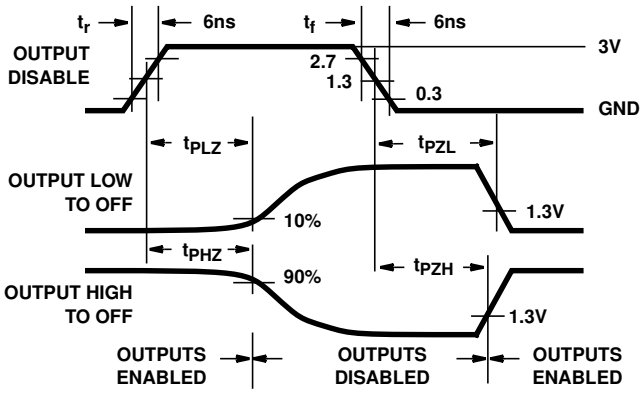
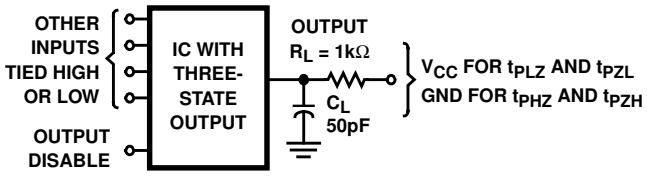



FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM




NOTE: Open drain waveforms $t_{PLZ}$ and $t_{PZL}$ are the same as those for three-state shown on the left. The test circuit is Output $R_L$ = 1kΩ to $V_{CC}$, $C_L$ = 50pF.

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| 5962-8606201RA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| 5962-8681301RA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| CD54HC533F3A | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| CD54HC563F3A | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| CD54HCT533F3A | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| CD74HC533E | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HC533EE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HC563E | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HC563EE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HCT533E | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HCT533EE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HCT563E | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HCT563EE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HCT563M | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT563ME4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT563MG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is

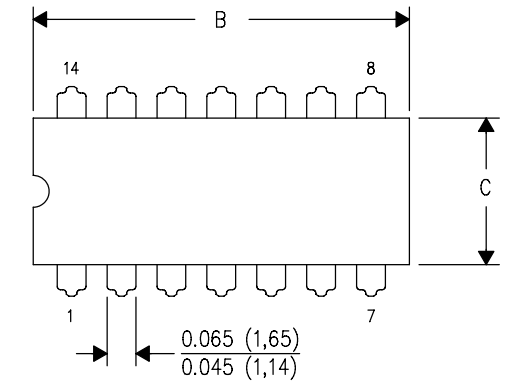
provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

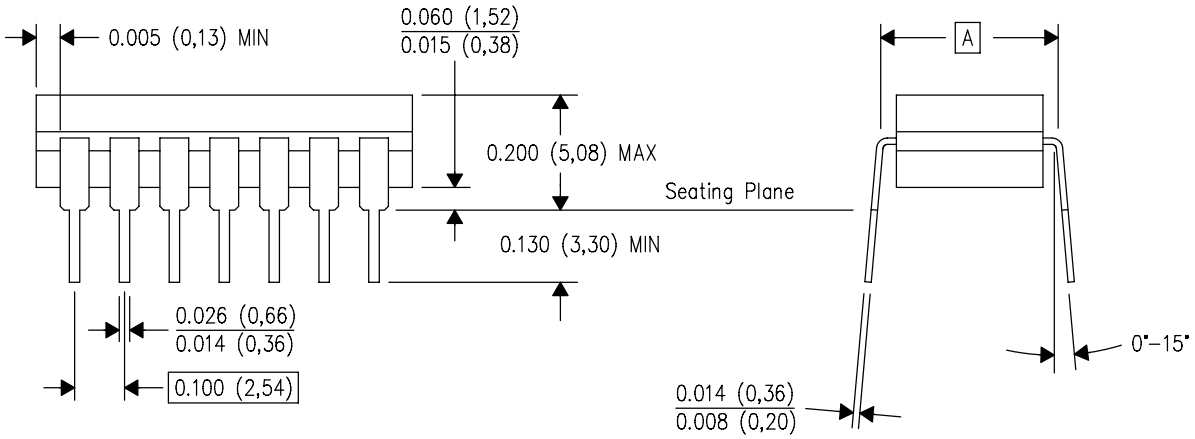
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE



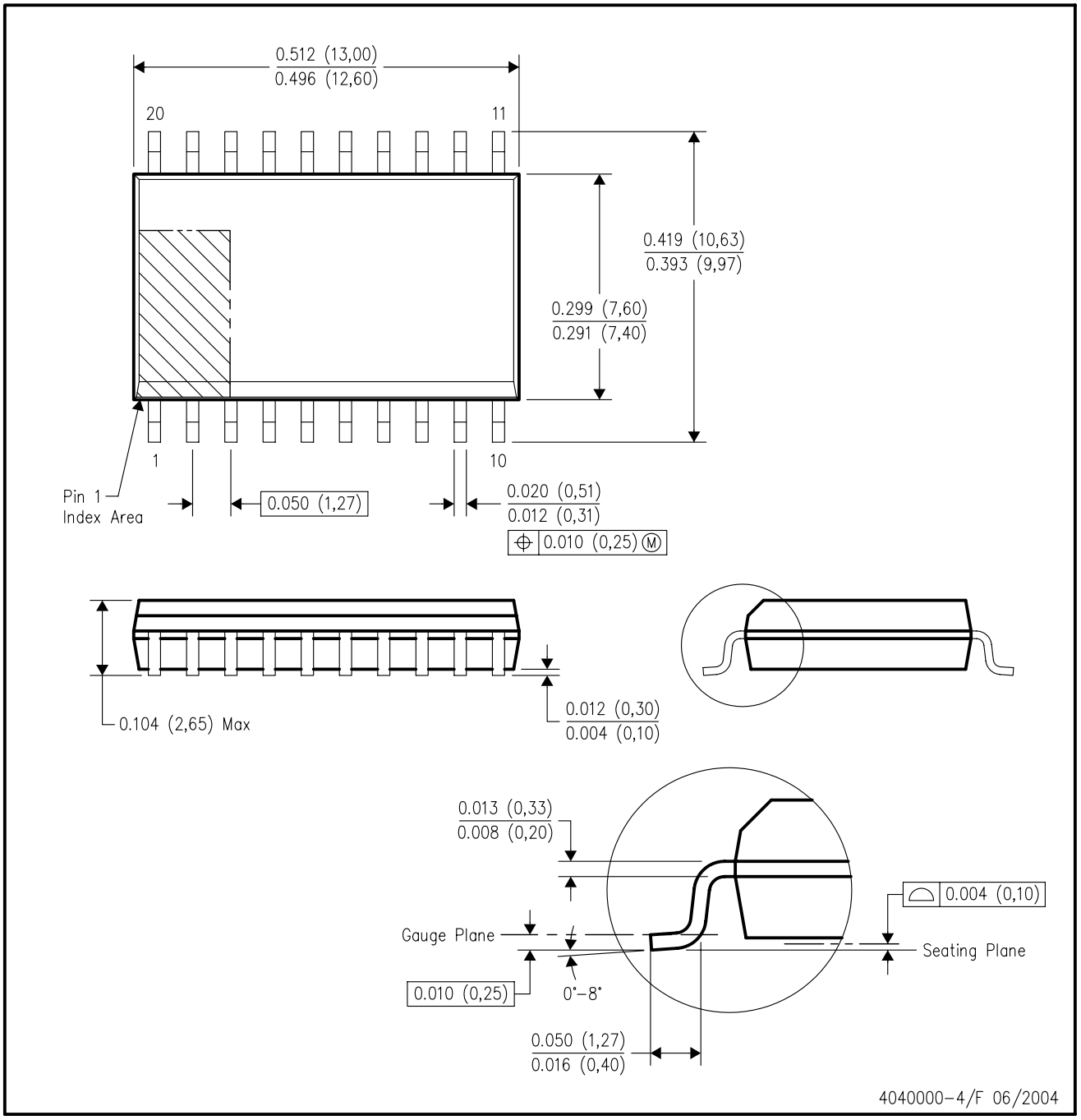

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

## DW (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE

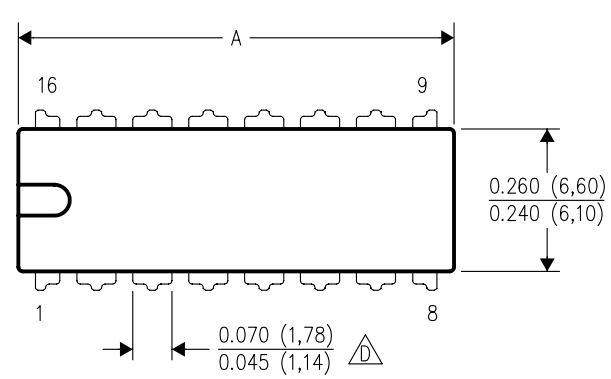



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

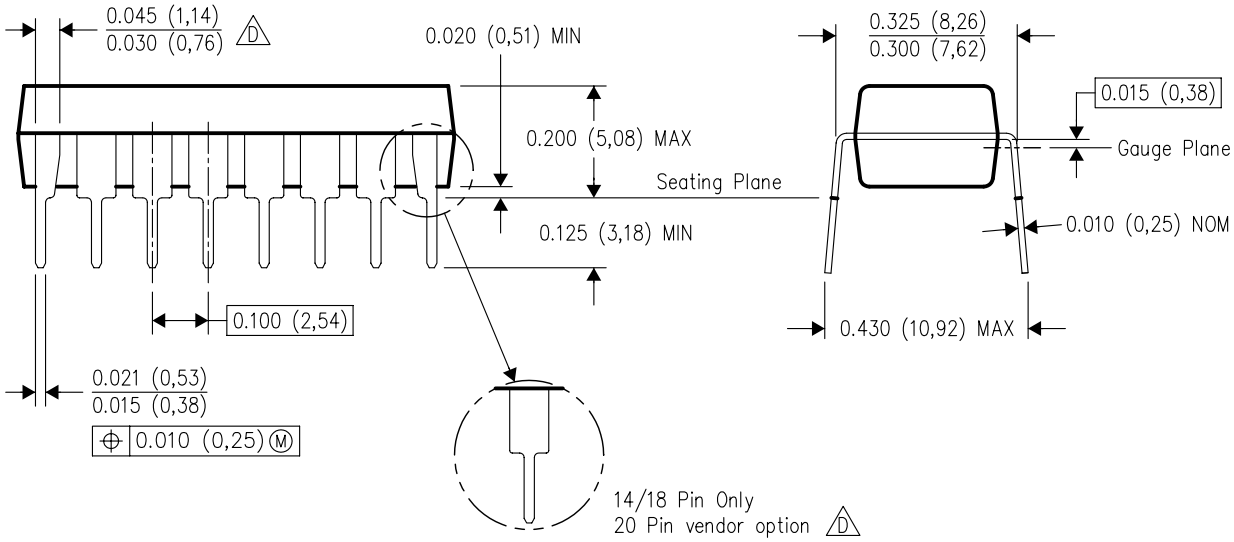
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DLP® Products | www.dlp.com | Broadband | www.ti.com/broadband |
| DSP | dsp.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Clocks and Timers | www.ti.com/clocks | Medical | www.ti.com/medical |
| Interface | interface.ti.com | Military | www.ti.com/military |
| Logic | logic.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Power Mgmt | power.ti.com | Security | www.ti.com/security |
| Microcontrollers | microcontroller.ti.com | Telephony | www.ti.com/telephony |
| RFID | www.ti-rfid.com | Video & Imaging | www.ti.com/video |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated