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# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT20** Dual 4-input NAND gate

Product specification  
File under Integrated Circuits, IC06

December 1990

## Dual 4-input NAND gate

## 74HC/HCT20

## FEATURES

- Output capability: standard
- $I_{CC}$  category: SSI

## GENERAL DESCRIPTION

The 74HC/HCT20 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT20 provide the 4-input NAND function.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

| SYMBOL            | PARAMETER                                 | CONDITIONS                                   | TYPICAL |     | UNIT |
|-------------------|-------------------------------------------|----------------------------------------------|---------|-----|------|
|                   |                                           |                                              | HC      | HCT |      |
| $t_{PHL}/t_{PLH}$ | propagation delay nA, nB, nC, nD to nY    | $C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$ | 8       | 13  | ns   |
| $C_I$             | input capacitance                         |                                              | 3.5     | 3.5 | pF   |
| $C_{PD}$          | power dissipation capacitance per package | notes 1 and 2                                | 22      | 17  | pF   |

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

$\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

## ORDERING INFORMATION

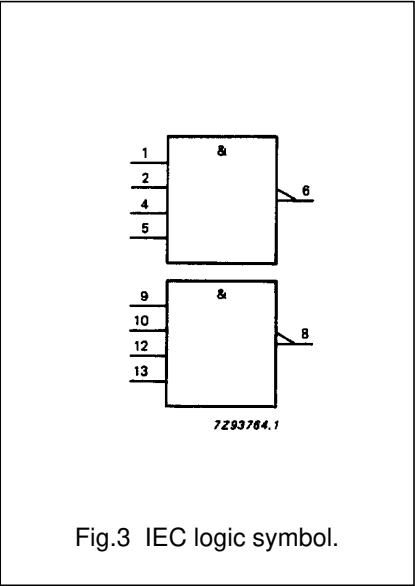
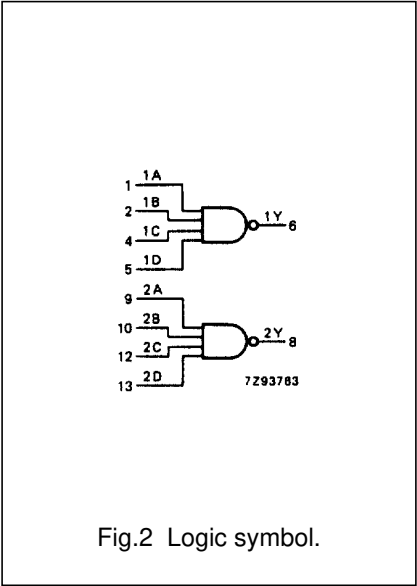
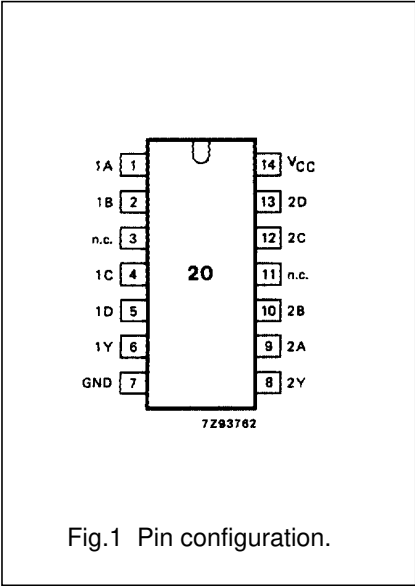
See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

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PIN DESCRIPTION

| PIN NO. | SYMBOL          | NAME AND FUNCTION       |
|---------|-----------------|-------------------------|
| 1, 9    | 1A, 2A          | data inputs             |
| 2, 10   | 1B, 2B          | data inputs             |
| 3, 11   | n.c.            | not connected           |
| 4, 12   | 1C, 2C          | data inputs             |
| 5, 13   | 1D, 2D          | data inputs             |
| 6, 8    | 1Y, 2Y          | data outputs            |
| 7       | GND             | ground (0 V)            |
| 14      | V <sub>CC</sub> | positive supply voltage |



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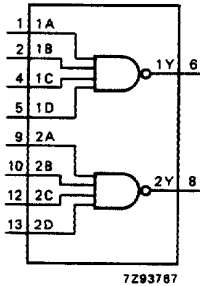


Fig.4 Functional diagram.

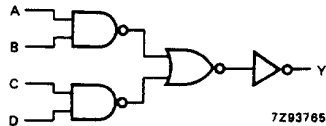


Fig.5 HC logic diagram (one gate).

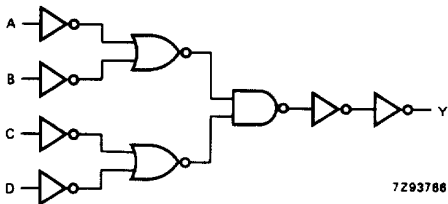


Fig.6 HCT logic diagram (one gate).

FUNCTION TABLE

| INPUTS |    |    |    | OUTPUT |
|--------|----|----|----|--------|
| nA     | nB | nC | nD | nY     |
| L      | X  | X  | X  | H      |
| X      | L  | X  | X  | H      |
| X      | X  | L  | X  | H      |
| X      | X  | X  | L  | H      |
| H      | H  | H  | H  | L      |

Notes

- 1. H = HIGH voltage level  
L = LOW voltage level  
X = don't care

## Dual 4-input NAND gate

## 74HC/HCT20

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: SSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                                 | T <sub>amb</sub> (°C) |               |                |            |                 |             |                 | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|-------------------------------------------|-----------------------|---------------|----------------|------------|-----------------|-------------|-----------------|------|------------------------|-----------|
|                                     |                                           | 74HC                  |               |                |            |                 |             |                 |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                           | +25                   |               |                | −40 to +85 |                 | −40 to +125 |                 |      |                        |           |
|                                     |                                           | min.                  | typ.          | max.           | min.       | max.            | min.        | max.            |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>nA, nB, nC, nD to nY |                       | 28<br>10<br>8 | 90<br>18<br>15 |            | 115<br>23<br>20 |             | 135<br>27<br>23 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                    |                       | 19<br>7<br>6  | 75<br>15<br>13 |            | 95<br>19<br>16  |             | 110<br>22<br>19 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |

Dual 4-input NAND gate

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *“74HC/HCT/HCU/HCMOS Logic Family Specifications”*.

Output capability: standard  
I<sub>CC</sub> category: SSI

Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.  
To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

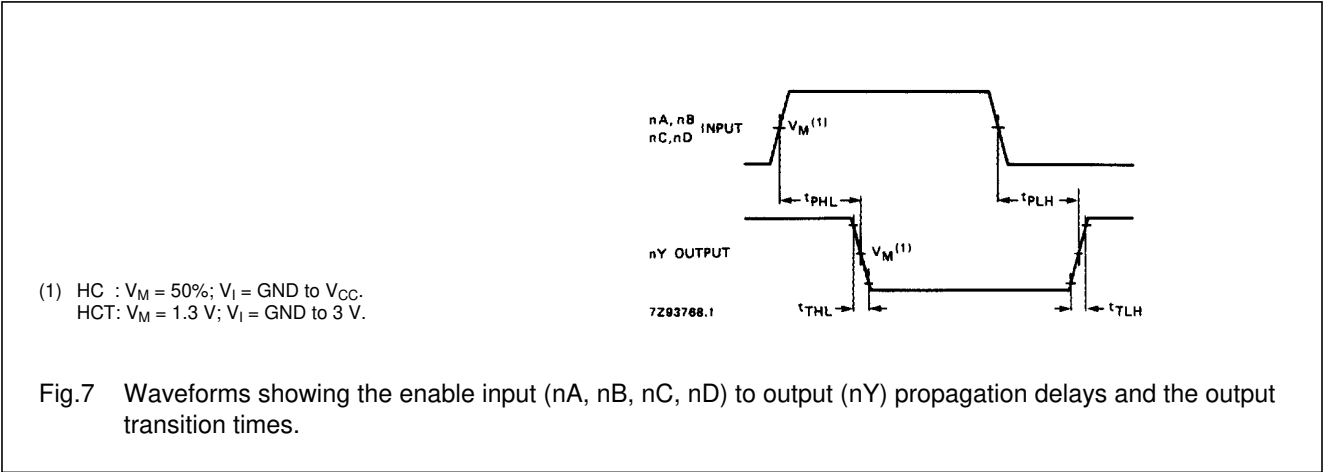
| INPUT          | UNIT LOAD COEFFICIENT |
|----------------|-----------------------|
| nA, nB, nC, nD | 0.3                   |

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                                 | T <sub>amb</sub> (°C) |      |      |            |      |             |      | UNIT | TEST CONDITIONS     |           |
|-------------------------------------|-------------------------------------------|-----------------------|------|------|------------|------|-------------|------|------|---------------------|-----------|
|                                     |                                           | 74HCT                 |      |      |            |      |             |      |      | V <sub>CC</sub> (V) | WAVEFORMS |
|                                     |                                           | +25                   |      |      | −40 to +85 |      | −40 to +125 |      |      |                     |           |
|                                     |                                           | min.                  | typ. | max. | min.       | max. | min.        | max. |      |                     |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>nA, nB, nC, nD to nY |                       | 16   | 28   |            | 35   |             | 42   | ns   | 4.5                 | Fig.7     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                    |                       | 7    | 15   |            | 19   |             | 22   | ns   | 4.5                 | Fig.7     |

AC WAVEFORMS



PACKAGE OUTLINES

See *“74HC/HCT/HCU/HCMOS Logic Package Outlines”*.