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# PIC12F609/615/617
# PIC12HV609/615

# Data Sheet

## 8-Pin, Flash-Based 8-Bit CMOS Microcontrollers

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# PIC12F609/615/617/12HV609/615

## 8-Pin Flash-Based, 8-Bit CMOS Microcontrollers

### High-Performance RISC CPU:

- Only 35 Instructions to Learn:
  - All single-cycle instructions except branches
- Operating Speed:
  - DC – 20 MHz oscillator/clock input
  - DC – 200 ns instruction cycle
- Interrupt Capability
- 8-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes

### Special Microcontroller Features:

- Precision Internal Oscillator:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency: 4 MHz or 8 MHz
- Power-Saving Sleep mode
- Voltage Range:
  - PIC12F609/615/617: 2.0V to 5.5V
  - PIC12HV609/615: 2.0V to user defined maximum **(see note)**
- Industrial and Extended Temperature Range
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR)
- Watchdog Timer (WDT) with independent Oscillator for Reliable Operation
- Multiplexed Master Clear with Pull-up/Input Pin
- Programmable Code Protection
- High Endurance Flash:
  - 100,000 write Flash endurance
  - Flash retention: > 40 years
- Self Read/ Write Program Memory (PIC12F617 only)

### Low-Power Features:

- Standby Current:
  - 50 nA @ 2.0V, typical
- Operating Current:
  - 11 μA @ 32 kHz, 2.0V, typical
  - 260 μA @ 4 MHz, 2.0V, typical
- Watchdog Timer Current:
  - 1 μA @ 2.0V, typical

**Note:** Voltage across the shunt regulator should not exceed 5V.

### Peripheral Features:

- Shunt Voltage Regulator (PIC12HV609/615 only):
  - 5 volt regulation
  - 4 mA to 50 mA shunt range
- 5 I/O Pins and 1 Input Only
- High Current Source/Sink for Direct LED Drive
  - Interrupt-on-pin change or pins
  - Individually programmable weak pull-ups
- Analog Comparator module with:
  - One analog comparator
  - Programmable on-chip voltage reference ($CV_{REF}$) module (% of $V_{DD}$)
  - Comparator inputs and output externally accessible
  - Built-In Hysteresis (software selectable)
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Timer1 Gate (count enable)
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator if INTOSC mode selected
  - Option to use system clock as Timer1
- In-Circuit Serial Programming™ (ICSP™) via Two Pins

PIC12F615/617/HV615 ONLY:

- Enhanced Capture, Compare, PWM module:
  - 16-bit Capture, max. resolution 12.5 ns
  - Compare, max. resolution 200 ns
  - 10-bit PWM with 1 or 2 output channels, 1 output channel programmable “dead time,” max. frequency 20 kHz, auto-shutdown
- A/D Converter:
  - 10-bit resolution and 4 channels, samples internal voltage references
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler

| Device | Program Memory | Data Memory | Self Read/ Self Write | I/O | 10-bit A/D (ch) | Comparators | ECCP | Timers 8/16-bit | Voltage Range |
|---|---|---|---|---|---|---|---|---|---|
| | Flash (words) | SRAM (bytes) | | | | | | | |
| PIC12F609 | 1024 | 64 | — | 5 | 0 | 1 | — | 1/1 | 2.0V-5.5V |
| PIC12HV609 | 1024 | 64 | — | 5 | 0 | 1 | — | 1/1 | 2.0V-user defined |
| PIC12F615 | 1024 | 64 | — | 5 | 4 | 1 | YES | 2/1 | 2.0V-5.5V |
| PIC12HV615 | 1024 | 64 | — | 5 | 4 | 1 | YES | 2/1 | 2.0V-user defined |
| PIC12F617 | 2048 | 128 | YES | 5 | 4 | 1 | YES | 2/1 | 2.0V-5.5V |

## 8-Pin Diagram, PIC12F609/HV609 (PDIP, SOIC, MSOP, DFN)

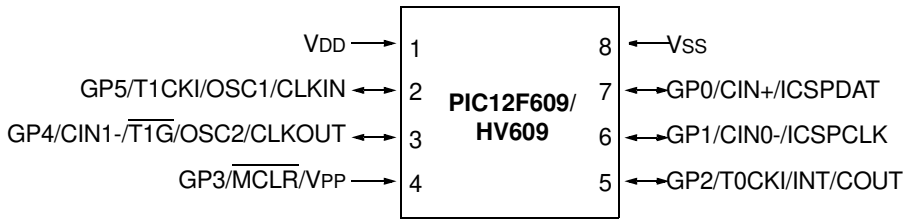


**TABLE 1: PIC12F609/HV609 PIN SUMMARY (PDIP, SOIC, MSOP, DFN)**

| I/O | Pin | Comparators | Timer | Interrupts | Pull-ups | Basic |
|---|---|---|---|---|---|---|
| GP0 | 7 | CIN+ | — | IOC | Y | ICSPDAT |
| GP1 | 6 | CIN0- | — | IOC | Y | ICSPCLK |
| GP2 | 5 | COUT | T0CKI | INT/IOC | Y | — |
| GP3(1) | 4 | — | — | IOC | Y(2) | $\overline{MCLR}$/VPP |
| GP4 | 3 | CIN1- | $\overline{T1G}$ | IOC | Y | OSC2/CLKOUT |
| GP5 | 2 | — | T1CKI | IOC | Y | OSC1/CLKIN |
| — | 1 | — | — | — | — | VDD |
| — | 8 | — | — | — | — | VSS |

**Note 1:** Input only.

**2:** Only when pin is configured for external $\overline{MCLR}$.


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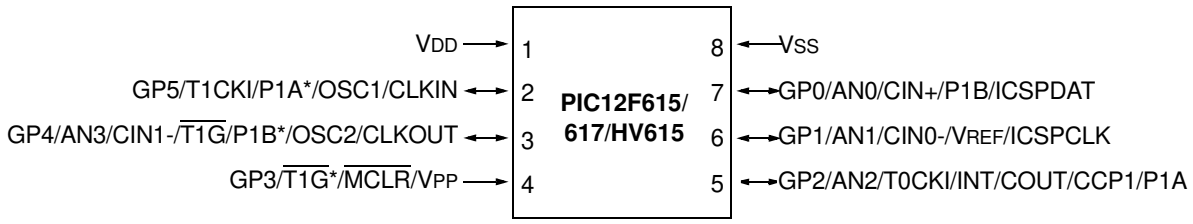
### 8-Pin Diagram, PIC12F615/617/HV615 (PDIP, SOIC, MSOP, DFN)




* Alternate pin function.

**TABLE 2: PIC12F615/617/HV615 PIN SUMMARY (PDIP, SOIC, MSOP, DFN)**

| I/O | Pin | Analog | Comparators | Timer | CCP | Interrupts | Pull-ups | Basic |
|---|---|---|---|---|---|---|---|---|
| GP0 | 7 | AN0 | CIN+ | — | P1B | IOC | Y | ICSPDAT |
| GP1 | 6 | AN1 | CIN0- | — | — | IOC | Y | ICSPCLK/VREF |
| GP2 | 5 | AN2 | COUT | T0CKI | CCP1/P1A | INT/IOC | Y | — |
| GP3(1) | 4 | — | — | $\overline{T1G}$* | — | IOC | Y(2) | $\overline{MCLR}$/VPP |
| GP4 | 3 | AN3 | CIN1- | $\overline{T1G}$ | P1B* | IOC | Y | OSC2/CLKOUT |
| GP5 | 2 | — | — | T1CKI | P1A* | IOC | Y | OSC1/CLKIN |
| — | 1 | — | — | — | — | — | — | VDD |
| — | 8 | — | — | — | — | — | — | VSS |

* Alternate pin function.

**Note 1:** Input only.

**2:** Only when pin is configured for external $\overline{MCLR}$.

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## 1.0 DEVICE OVERVIEW

The PIC12F609/615/617/12HV609/615 devices are covered by this data sheet. They are available in 8-pin PDIP, SOIC, MSOP and DFN packages.

Block Diagrams and pinout descriptions of the devices are as follows:

- PIC12F609/HV609 (Figure 1-1, Table 1-1)
- PIC12F615/617/HV615 (Figure 1-2, Table 1-2)

**FIGURE 1-1: PIC12F609/HV609 BLOCK DIAGRAM**

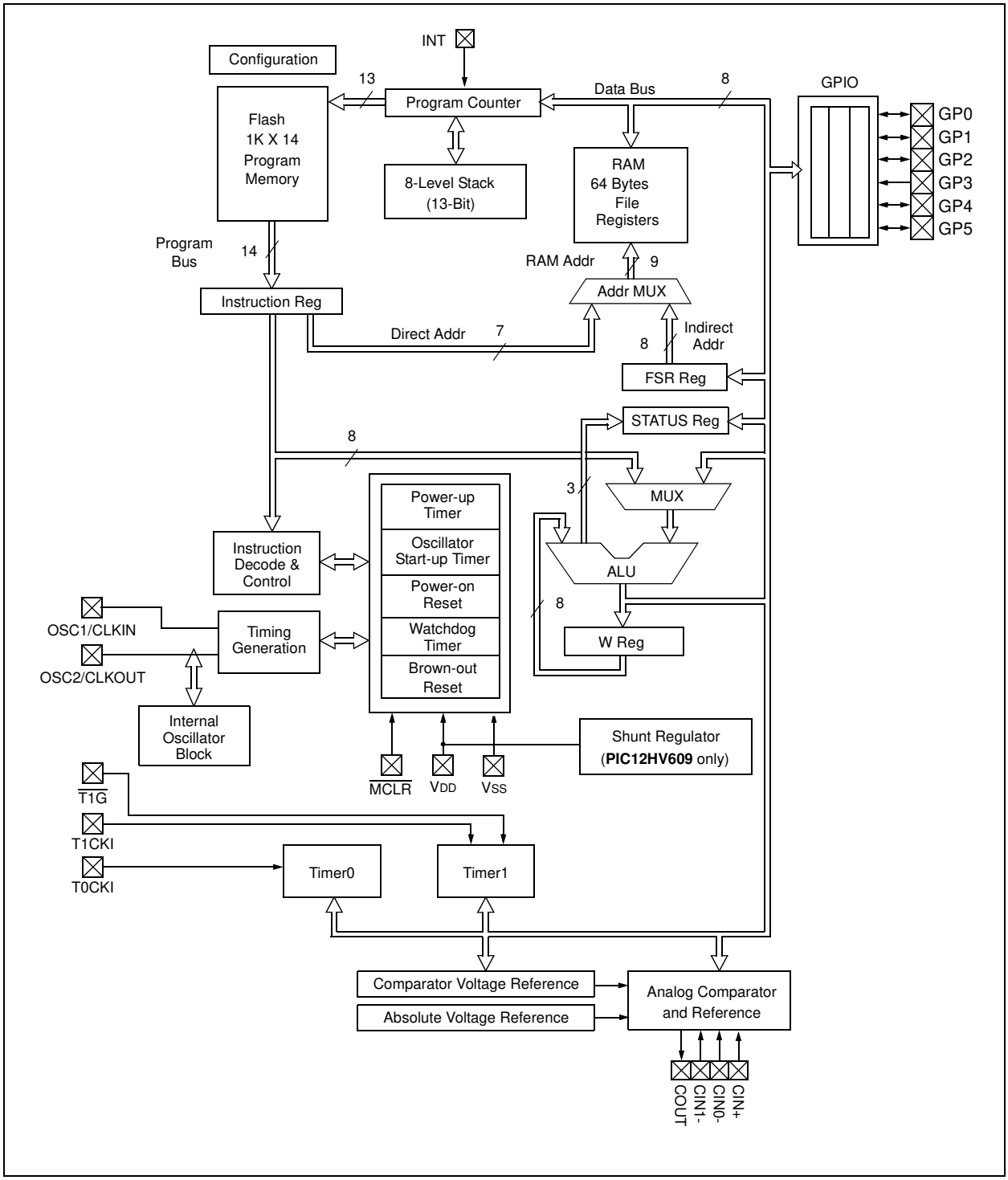
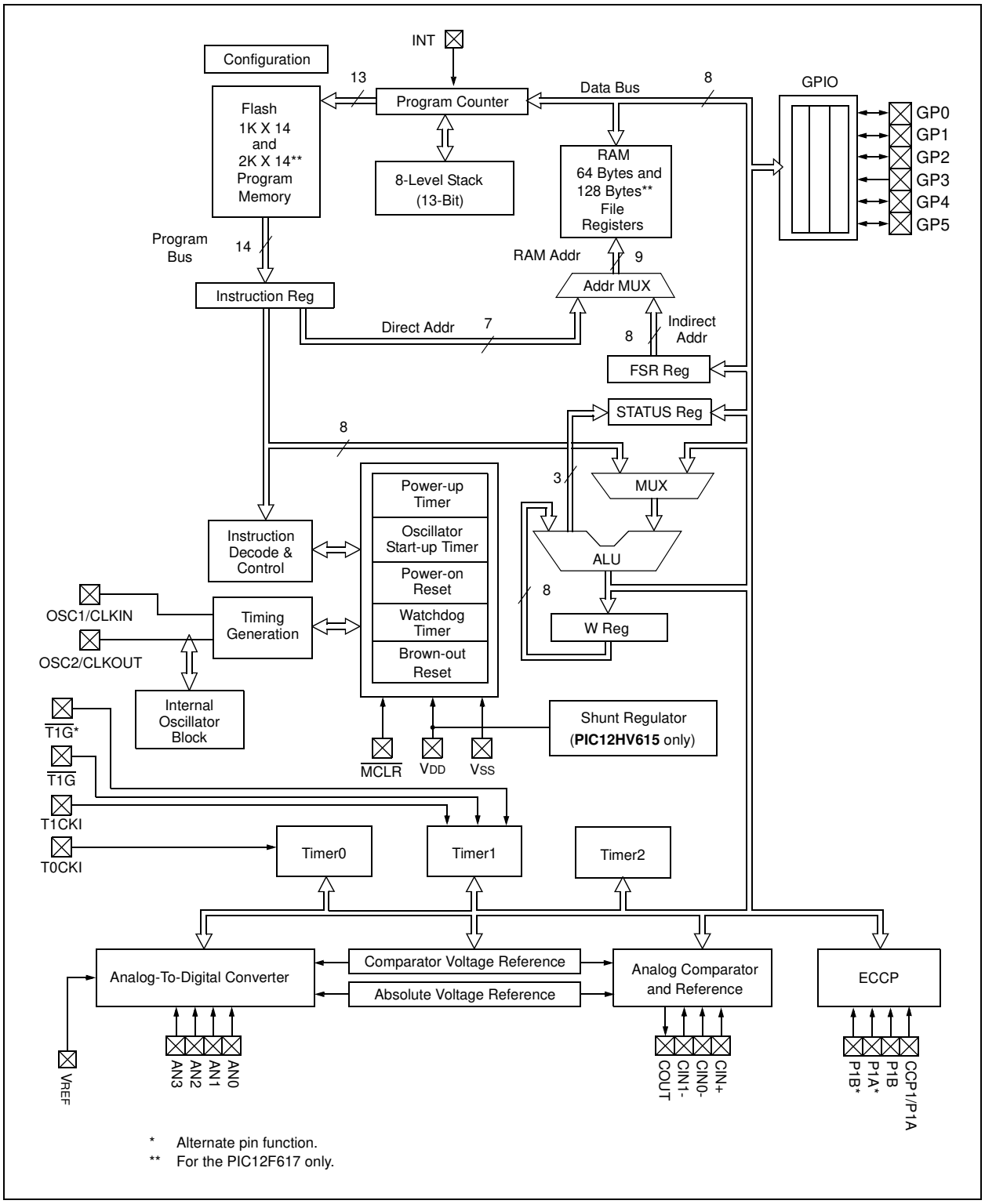


**FIGURE 1-2: PIC12F615/617/HV615 BLOCK DIAGRAM**




* Alternate pin function.
** For the PIC12F617 only.


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**TABLE 1-1: PIC12F609/HV609 PINOUT DESCRIPTION**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| GP0/CIN+/ICSPDAT | GP0 | TTL | CMOS | General purpose I/O with prog. pull-up and interrupt-on-change |
| | CIN+ | AN | — | Comparator non-inverting input |
| | ICSPDAT | ST | CMOS | Serial Programming Data I/O |
| GP1/CIN0-/ICSPCLK | GP1 | TTL | CMOS | General purpose I/O with prog. pull-up and interrupt-on-change |
| | CIN0- | AN | — | Comparator inverting input |
| | ICSPCLK | ST | — | Serial Programming Clock |
| GP2/T0CKI/INT/COUT | GP2 | ST | CMOS | General purpose I/O with prog. pull-up and interrupt-on-change |
| | T0CKI | ST | — | Timer0 clock input |
| | INT | ST | — | External Interrupt |
| | COUT | — | CMOS | Comparator output |
| GP3/$\overline{\text{MCLR}}$/VPP | GP3 | TTL | — | General purpose input with interrupt-on-change |
| | $\overline{\text{MCLR}}$ | ST | — | Master Clear w/internal pull-up |
| | VPP | HV | — | Programming voltage |
| GP4/CIN1-/$\overline{\text{T1G}}$/OSC2/CLKOUT | GP4 | TTL | CMOS | General purpose I/O with prog. pull-up and interrupt-on-change |
| | CIN1- | AN | — | Comparator inverting input |
| | $\overline{\text{T1G}}$ | ST | — | Timer1 gate (count enable) |
| | OSC2 | — | XTAL | Crystal/Resonator |
| | CLKOUT | — | CMOS | FOSC/4 output |
| GP5/T1CKI/OSC1/CLKIN | GP5 | TTL | CMOS | General purpose I/O with prog. pull-up and interrupt-on-change |
| | T1CKI | ST | — | Timer1 clock input |
| | OSC1 | XTAL | — | Crystal/Resonator |
| | CLKIN | ST | — | External clock input/RC oscillator connection |
| VDD | VDD | Power | — | Positive supply |
| VSS | VSS | Power | — | Ground reference |

**Legend:** AN=Analog input or output; ST=Schmitt Trigger input with CMOS levels; CMOS = CMOS compatible input or output; TTL = TTL compatible input; HV= High Voltage; XTAL=Crystal

**TABLE 1-2: PIC12F615/617/HV615 PINOUT DESCRIPTION**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| GP0/AN0/CIN+/P1B/ICSPDAT | GP0 | TTL | CMOS | General purpose I/O with prog. pull-up and interrupt-on-change |
| | AN0 | AN | — | A/D Channel 0 input |
| | CIN+ | AN | — | Comparator non-inverting input |
| | P1B | — | CMOS | PWM output |
| | ICSPDAT | ST | CMOS | Serial Programming Data I/O |
| GP1/AN1/CIN0-/VREF/ICSPCLK | GP1 | TTL | CMOS | General purpose I/O with prog. pull-up and interrupt-on-change |
| | AN1 | AN | — | A/D Channel 1 input |
| | CIN0- | AN | — | Comparator inverting input |
| | VREF | AN | — | External Voltage Reference for A/D |
| | ICSPCLK | ST | — | Serial Programming Clock |
| GP2/AN2/T0CKI/INT/COUT/CCP1/P1A | GP2 | ST | CMOS | General purpose I/O with prog. pull-up and interrupt-on-change |
| | AN2 | AN | — | A/D Channel 2 input |
| | T0CKI | ST | — | Timer0 clock input |
| | INT | ST | — | External Interrupt |
| | COUT | — | CMOS | Comparator output |
| | CCP1 | ST | CMOS | Capture input/Compare input/PWM output |
| | P1A | — | CMOS | PWM output |
| GP3/$\overline{\text{T1G}}$*/$\overline{\text{MCLR}}$/VPP | GP3 | TTL | — | General purpose input with interrupt-on-change |
| | $\overline{\text{T1G}}$* | ST | — | Timer1 gate (count enable), alternate pin |
| | $\overline{\text{MCLR}}$ | ST | — | Master Clear w/internal pull-up |
| | VPP | HV | — | Programming voltage |
| GP4/AN3/CIN1-/$\overline{\text{T1G}}$/P1B*/OSC2/CLKOUT | GP4 | TTL | CMOS | General purpose I/O with prog. pull-up and interrupt-on-change |
| | AN3 | AN | — | A/D Channel 3 input |
| | CIN1- | AN | — | Comparator inverting input |
| | $\overline{\text{T1G}}$ | ST | — | Timer1 gate (count enable) |
| | P1B* | — | CMOS | PWM output, alternate pin |
| | OSC2 | — | XTAL | Crystal/Resonator |
| | CLKOUT | — | CMOS | FOSC/4 output |
| GP5/T1CKI/P1A*/OSC1/CLKIN | GP5 | TTL | CMOS | General purpose I/O with prog. pull-up and interrupt-on-change |
| | T1CKI | ST | — | Timer1 clock input |
| | P1A* | — | CMOS | PWM output, alternate pin |
| | OSC1 | XTAL | — | Crystal/Resonator |
| | CLKIN | ST | — | External clock input/RC oscillator connection |
| VDD | VDD | Power | — | Positive supply |
| VSS | VSS | Power | — | Ground reference |

* Alternate pin function.

**Legend:** AN=Analog input or output; CMOS=CMOS compatible input or output; HV= High Voltage; ST=Schmitt Trigger input with CMOS levels; TTL = TTL compatible input; XTAL=Crystal


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# 2.0 MEMORY ORGANIZATION

## 2.1 Program Memory Organization

The PIC12F609/615/617/12HV609/615 has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 1K x 14 (0000h-03FFh) for the PIC12F609/615/12HV609/615 is physically implemented. For the PIC12F617, the first 2K x 14 (0000h-07FFh) is physically implemented. Accessing a location above these boundaries will cause a wrap-around within the first 1K x 14 space for PIC12F609/615/12HV609/615 devices, and within the first 2K x 14 space for the PIC12F617 device. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

**FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC12F609/615/12HV609/615**

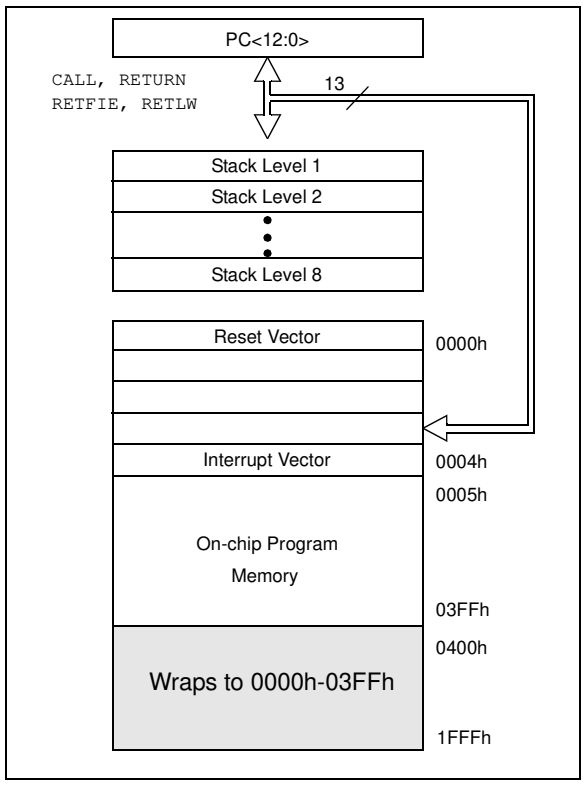
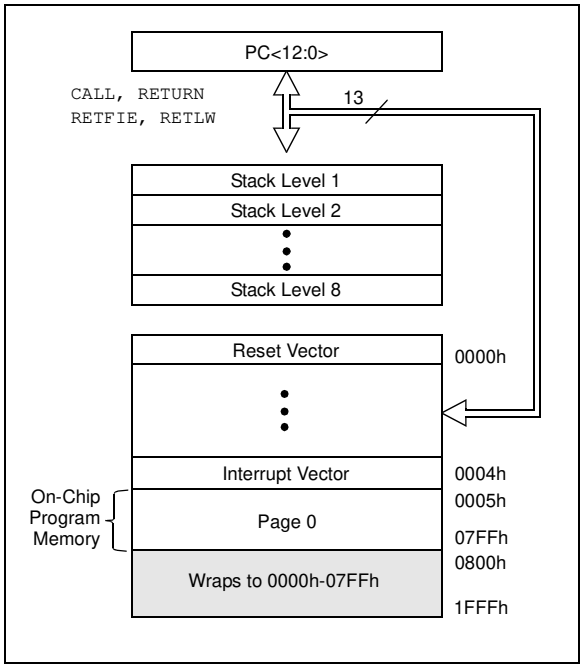



**FIGURE 2-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC12F617**




## 2.2 Data Memory Organization

The data memory (see Figure 2-3) is partitioned into two banks, which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. Register locations 40h-7Fh in Bank 0 are General Purpose Registers, implemented as static RAM. For the PIC12F617, the register locations 20h-7Fh in Bank 0 and A0h-EFh in Bank 1 are general purpose registers implemented as Static RAM. Register locations F0h-FFh in Bank 1 point to addresses 70h-7Fh in Bank 0. All other RAM is unimplemented and returns '0' when read. The RP0 bit of the STATUS register is the bank select bit.

RP0

0 → Bank 0 is selected

1 → Bank 1 is selected

| | |
|---|---|
| **Note:** | The IRP and RP1 bits of the STATUS register are reserved and should always be maintained as '0's. |

### 2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 64 x 8 in the PIC12F609/615/12HV609/615, and as 128 x 8 in the PIC12F617. Each register is accessed, either directly or indirectly, through the File Select Register (FSR) (see **Section 2.4 "Indirect Addressing, INDF and FSR Registers"**).

### 2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

**FIGURE 2-3: DATA MEMORY MAP OF THE PIC12F609/HV609**

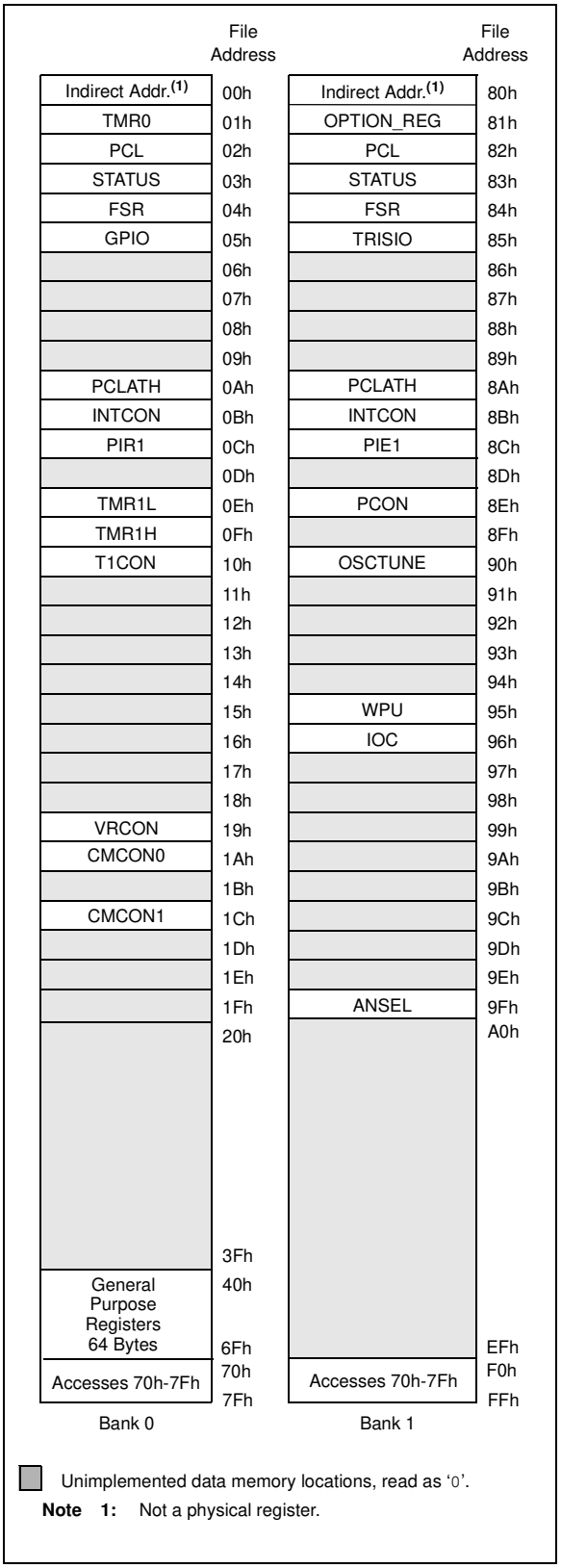




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**FIGURE 2-4: DATA MEMORY MAP OF THE PIC12F615/617/HV615**

| Bank 0 | File Address | Bank 1 | File Address |
|---|---|---|---|
| Indirect Addr.(1) | 00h | Indirect Addr.(1) | 80h |
| TMR0 | 01h | OPTION_REG | 81h |
| PCL | 02h | PCL | 82h |
| STATUS | 03h | STATUS | 83h |
| FSR | 04h | FSR | 84h |
| GPIO | 05h | TRISIO | 85h |
| | 06h | | 86h |
| | 07h | | 87h |
| | 08h | | 88h |
| | 09h | | 89h |
| PCLATH | 0Ah | PCLATH | 8Ah |
| INTCON | 0Bh | INTCON | 8Bh |
| PIR1 | 0Ch | PIE1 | 8Ch |
| | 0Dh | | 8Dh |
| TMR1L | 0Eh | PCON | 8Eh |
| TMR1H | 0Fh | | 8Fh |
| T1CON | 10h | OSCTUNE | 90h |
| TMR2 | 11h | | 91h |
| T2CON | 12h | PR2 | 92h |
| CCPR1L | 13h | APFCON | 93h |
| CCPR1H | 14h | | 94h |
| CCP1CON | 15h | WPU | 95h |
| PWM1CON | 16h | IOC | 96h |
| ECCPAS | 17h | | 97h |
| | 18h | PMCON1(2) | 98h |
| VRCON | 19h | PMCON2(2) | 99h |
| CMCON0 | 1Ah | PMADRL(2) | 9Ah |
| | 1Bh | PMADRH(2) | 9Bh |
| CMCON1 | 1Ch | PMDATL(2) | 9Ch |
| | 1Dh | PMDATH(2) | 9Dh |
| ADRESH | 1Eh | ADRESL | 9Eh |
| ADCON0 | 1Fh | ANSEL | 9Fh |
| General Purpose Registers 96 Bytes from 20h-7Fh(2) Unimplemented for PIC12F615/HV615 | 20h … 3Fh | General Purpose Registers 32 Bytes(2) Unimplemented for PIC12F615/HV615 | A0h … BFh |
| General Purpose Registers 64 Bytes | 40h … 6Fh | | C0h … EFh |
| Accesses 70h-7Fh | 70h … 7Fh | Accesses 70h-7Fh | F0h … FFh |

Unimplemented data memory locations, read as '0'.

**Note 1:** Not a physical register.

**2:** Used for the PIC12F617 only.

### TABLE 2-1: PIC12F609/HV609 SPECIAL FUNCTION REGISTERS SUMMARY BANK 0

| Addr | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Page |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Bank 0 | | | | | | | | | | | |
| 00h | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx | 25, 115 |
| 01h | TMR0 | Timer0 Module's Register | | | | | | | | xxxx xxxx | 53, 115 |
| 02h | PCL | Program Counter's (PC) Least Significant Byte | | | | | | | | 0000 0000 | 25, 115 |
| 03h | STATUS | IRP(1) | RP1(1) | RP0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | 0001 1xxx | 18, 115 |
| 04h | FSR | Indirect Data Memory Address Pointer | | | | | | | | xxxx xxxx | 25, 115 |
| 05h | GPIO | — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | --x0 x000 | 43, 115 |
| 06h | — | Unimplemented | | | | | | | | — | — |
| 07h | — | Unimplemented | | | | | | | | — | — |
| 08h | — | Unimplemented | | | | | | | | — | — |
| 09h | — | Unimplemented | | | | | | | | — | — |
| 0Ah | PCLATH | — | — | — | Write Buffer for upper 5 bits of Program Counter | | | | | ---0 0000 | 25, 115 |
| 0Bh | INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF | 0000 0000 | 20, 115 |
| 0Ch | PIR1 | — | — | — | — | CMIF | — | — | TMR1IF | ---- 0--0 | 22, 115 |
| 0Dh | — | Unimplemented | | | | | | | | — | — |
| 0Eh | TMR1L | Holding Register for the Least Significant Byte of the 16-bit TMR1 Register | | | | | | | | xxxx xxxx | 57, 115 |
| 0Fh | TMR1H | Holding Register for the Most Significant Byte of the 16-bit TMR1 Register | | | | | | | | xxxx xxxx | 57, 115 |
| 10h | T1CON | T1GINV | TMR1GE | T1CKPS1 | T1CKPS0 | T1OSCEN | $\overline{T1SYNC}$ | TMR1CS | TMR1ON | 0000 0000 | 62, 115 |
| 11h | — | Unimplemented | | | | | | | | — | — |
| 12h | — | Unimplemented | | | | | | | | — | — |
| 13h | — | Unimplemented | | | | | | | | — | — |
| 14h | — | Unimplemented | | | | | | | | — | — |
| 15h | — | Unimplemented | | | | | | | | — | — |
| 16h | — | Unimplemented | | | | | | | | — | — |
| 17h | — | Unimplemented | | | | | | | | — | — |
| 18h | — | Unimplemented | | | | | | | | — | — |
| 19h | VRCON | CMVREN | — | VRR | FVREN | VR3 | VR2 | VR1 | VR0 | 0-00 0000 | 76, 116 |
| 1Ah | CMCON0 | CMON | COUT | CMOE | CMPOL | — | CMR | — | CMCH | 0000 -0-0 | 72, 116 |
| 1Bh | — | | | | | — | | — | | — | — |
| 1Ch | CMCON1 | — | — | — | T1ACS | CMHYS | — | T1GSS | CMSYNC | ---0 0-10 | 73, 116 |
| 1Dh | — | Unimplemented | | | | | | | | — | — |
| 1Eh | — | Unimplemented | | | | | | | | — | — |
| 1Fh | — | Unimplemented | | | | | | | | — | — |

**Legend:** – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

**1:** IRP and RP1 bits are reserved, always maintain these bits clear.

**2:** Read only register.


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### TABLE 2-2: PIC12F615/617/HV615 SPECIAL FUNCTION REGISTERS SUMMARY BANK 0

| Addr | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Page |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Bank 0 | | | | | | | | | | | |
| 00h | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx | 25, 116 |
| 01h | TMR0 | Timer0 Module's Register | | | | | | | | xxxx xxxx | 53, 116 |
| 02h | PCL | Program Counter's (PC) Least Significant Byte | | | | | | | | 0000 0000 | 25, 116 |
| 03h | STATUS | IRP(1) | RP1(1) | RP0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | 0001 1xxx | 18, 116 |
| 04h | FSR | Indirect Data Memory Address Pointer | | | | | | | | xxxx xxxx | 25, 116 |
| 05h | GPIO | — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | --x0 x000 | 43, 116 |
| 06h | — | Unimplemented | | | | | | | | — | — |
| 07h | — | Unimplemented | | | | | | | | — | — |
| 08h | — | Unimplemented | | | | | | | | — | — |
| 09h | — | Unimplemented | | | | | | | | — | — |
| 0Ah | PCLATH | — | — | — | Write Buffer for upper 5 bits of Program Counter | | | | | ---0 0000 | 25, 116 |
| 0Bh | INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF | 0000 0000 | 20, 116 |
| 0Ch | PIR1 | — | ADIF | CCP1IF | — | CMIF | — | TMR2IF | TMR1IF | -00- 0-00 | 22, 116 |
| 0Dh | — | Unimplemented | | | | | | | | — | — |
| 0Eh | TMR1L | Holding Register for the Least Significant Byte of the 16-bit TMR1 Register | | | | | | | | xxxx xxxx | 57, 116 |
| 0Fh | TMR1H | Holding Register for the Most Significant Byte of the 16-bit TMR1 Register | | | | | | | | xxxx xxxx | 57, 116 |
| 10h | T1CON | T1GINV | TMR1GE | T1CKPS1 | T1CKPS0 | T1OSCEN | $\overline{T1SYNC}$ | TMR1CS | TMR1ON | 0000 0000 | 62, 116 |
| 11h | TMR2(3) | Timer2 Module Register | | | | | | | | 0000 0000 | 65, 116 |
| 12h | T2CON(3) | — | TOUTPS3 | TOUTPS2 | TOUTPS1 | TOUTPS0 | TMR2ON | T2CKPS1 | T2CKPS0 | -000 0000 | 66, 116 |
| 13h | CCPR1L(3) | Capture/Compare/PWM Register 1 Low Byte | | | | | | | | XXXX XXXX | 90, 116 |
| 14h | CCPR1H(3) | Capture/Compare/PWM Register 1 High Byte | | | | | | | | XXXX XXXX | 90, 116 |
| 15h | CCP1CON(3) | P1M | — | DC1B1 | DC1B0 | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 | 0-00 0000 | 89, 116 |
| 16h | PWM1CON(3) | PRSEN | PDC6 | PDC5 | PDC4 | PDC3 | PDC2 | PDC1 | PDC0 | 0000 0000 | 105, 116 |
| 17h | ECCPAS(3) | ECCPASE | ECCPAS2 | ECCPAS1 | ECCPAS0 | PSSAC1 | PSSAC0 | PSSBD1 | PSSBD0 | 0000 0000 | 102, 116 |
| 18h | — | Unimplemented | | | | | | | | — | — |
| 19h | VRCON | CMVREN | — | VRR | FVREN | VR3 | VR2 | VR1 | VR0 | 0-00 0000 | 76, 116 |
| 1Ah | CMCON0 | CMON | COUT | CMOE | CMPOL | — | CMR | — | CMCH | 0000 -0-0 | 72, 116 |
| 1Bh | — | | | | | — | | — | | — | — |
| 1Ch | CMCON1 | — | — | — | T1ACS | CMHYS | — | T1GSS | CMSYNC | ---0 0-10 | 73, 116 |
| 1Dh | — | Unimplemented | | | | | | | | — | — |
| 1Eh | ADRESH(2, 3) | Most Significant 8 bits of the left shifted A/D result or 2 bits of right shifted result | | | | | | | | xxxx xxxx | 85, 116 |
| 1Fh | ADCON0(3) | ADFM | VCFG | — | CHS2 | CHS1 | CHS0 | GO/$\overline{DONE}$ | ADON | 00-0 0000 | 84, 116 |

**Legend:** – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

**Note 1:** IRP and RP1 bits are reserved, always maintain these bits clear.

**2:** Read only register.

**3:** PIC12F615/617/HV615 only.

### TABLE 2-3: PIC12F609/HV609 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

| Addr | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Page |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Bank 1 | | | | | | | | | | | |
| 80h | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx | 25, 116 |
| 81h | OPTION_REG | $\overline{\text{GPPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 19, 116 |
| 82h | PCL | Program Counter's (PC) Least Significant Byte | | | | | | | | 0000 0000 | 25, 116 |
| 83h | STATUS | IRP(1) | RP1(1) | RP0 | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ | Z | DC | C | 0001 1xxx | 18, 116 |
| 84h | FSR | Indirect Data Memory Address Pointer | | | | | | | | xxxx xxxx | 25, 116 |
| 85h | TRISIO | — | — | TRISIO5 | TRISIO4 | TRISIO3(4) | TRISIO2 | TRISIO1 | TRISIO0 | --11 1111 | 44, 116 |
| 86h | — | Unimplemented | | | | | | | | — | — |
| 87h | — | Unimplemented | | | | | | | | — | — |
| 88h | — | Unimplemented | | | | | | | | — | — |
| 89h | — | Unimplemented | | | | | | | | — | — |
| 8Ah | PCLATH | — | — | — | Write Buffer for upper 5 bits of Program Counter | | | | | ---0 0000 | 25, 116 |
| 8Bh | INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF(3) | 0000 0000 | 20, 116 |
| 8Ch | PIE1 | — | — | — | — | CMIE | — | — | TMR1IE | ---- 0--0 | 21, 116 |
| 8Dh | — | Unimplemented | | | | | | | | — | — |
| 8Eh | PCON | — | — | — | — | — | — | $\overline{\text{POR}}$ | $\overline{\text{BOR}}$ | ---- --qq | 23, 116 |
| 8Fh | — | Unimplemented | | | | | | | | — | — |
| 90h | OSCTUNE | — | — | — | TUN4 | TUN3 | TUN2 | TUN1 | TUN0 | ---0 0000 | 41, 116 |
| 91h | — | Unimplemented | | | | | | | | — | — |
| 92h | — | Unimplemented | | | | | | | | — | — |
| 93h | — | Unimplemented | | | | | | | | — | — |
| 94h | — | Unimplemented | | | | | | | | — | — |
| 95h | WPU(2) | — | — | WPU5 | WPU4 | — | WPU2 | WPU1 | WPU0 | --11 -111 | 46, 116 |
| 96h | IOC | — | — | IOC5 | IOC4 | IOC3 | IOC2 | IOC1 | IOC0 | --00 0000 | 46, 116 |
| 97h | — | Unimplemented | | | | | | | | — | — |
| 98h | — | Unimplemented | | | | | | | | — | — |
| 99h | — | Unimplemented | | | | | | | | — | — |
| 9Ah | — | Unimplemented | | | | | | | | — | — |
| 9Bh | — | Unimplemented | | | | | | | | — | — |
| 9Ch | — | Unimplemented | | | | | | | | — | — |
| 9Dh | — | Unimplemented | | | | | | | | — | — |
| 9Eh | — | Unimplemented | | | | | | | | — | — |
| 9Fh | ANSEL | — | — | — | — | ANS3 | — | ANS1 | ANS0 | ---- 1-11 | 45, 117 |

**Legend:** – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

**Note 1:** IRP and RP1 bits are reserved, always maintain these bits clear.

**2:** GP3 pull-up is enabled when MCLRE is '1' in the Configuration Word register.

**3:** MCLR and WDT Reset does not affect the previous value data latch. The GPIF bit will clear upon Reset but will set again if the mismatch exists.

**4:** TRISIO3 always reads as '1' since it is an input only pin.


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### TABLE 2-4: PIC12F615/617/HV615 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

| Addr | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Page |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Bank 1 | | | | | | | | | | | |
| 80h | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx | 25, 116 |
| 81h | OPTION_REG | $\overline{\text{GPPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 19, 116 |
| 82h | PCL | Program Counter's (PC) Least Significant Byte | | | | | | | | 0000 0000 | 25, 116 |
| 83h | STATUS | IRP(1) | RP1(1) | RP0 | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ | Z | DC | C | 0001 1xxx | 18, 116 |
| 84h | FSR | Indirect Data Memory Address Pointer | | | | | | | | xxxx xxxx | 25, 116 |
| 85h | TRISIO | — | — | TRISIO5 | TRISIO4 | TRISIO3(4) | TRISIO2 | TRISIO1 | TRISIO0 | --11 1111 | 44, 116 |
| 86h | — | Unimplemented | | | | | | | | — | — |
| 87h | — | Unimplemented | | | | | | | | — | — |
| 88h | — | Unimplemented | | | | | | | | — | — |
| 89h | — | Unimplemented | | | | | | | | — | — |
| 8Ah | PCLATH | — | — | — | Write Buffer for upper 5 bits of Program Counter | | | | | ---0 0000 | 25, 116 |
| 8Bh | INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF(3) | 0000 0000 | 20, 116 |
| 8Ch | PIE1 | — | ADIE | CCP1IE | — | CMIE | — | TMR2IE | TMR1IE | -00- 0-00 | 21, 116 |
| 8Dh | — | Unimplemented | | | | | | | | — | — |
| 8Eh | PCON | — | — | — | — | — | — | $\overline{\text{POR}}$ | $\overline{\text{BOR}}$ | ---- --qq | 23, 116 |
| 8Fh | — | Unimplemented | | | | | | | | — | — |
| 90h | OSCTUNE | — | — | — | TUN4 | TUN3 | TUN2 | TUN1 | TUN0 | ---0 0000 | 41, 116 |
| 91h | — | Unimplemented | | | | | | | | — | — |
| 92h | PR2 | Timer2 Module Period Register | | | | | | | | 1111 1111 | 65, 116 |
| 93h | APFCON | — | — | — | T1GSEL | — | — | P1BSEL | P1ASEL | ---0 --00 | 21, 116 |
| 94h | — | Unimplemented | | | | | | | | — | — |
| 95h | WPU(2) | — | — | WPU5 | WPU4 | — | WPU2 | WPU1 | WPU0 | --11 -111 | 46, 116 |
| 96h | IOC | — | — | IOC5 | IOC4 | IOC3 | IOC2 | IOC1 | IOC0 | --00 0000 | 46, 116 |
| 97h | — | Unimplemented | | | | | | | | — | — |
| 98h | PMCON1(7) | — | — | — | — | — | WREN | WR | RD | ---- -000 | 29 |
| 99h | PMCON2(7) | Program Memory Control Register 2 (not a physical register). | | | | | | | | ---- ---- | — |
| 9Ah | PMADRL(7) | PMADRL7 | PMADRL6 | PMADRL5 | PMADRL4 | PMADRL3 | PMADRL2 | PMADRL1 | PMADRL0 | 0000 0000 | 28 |
| 9Bh | PMADRH(7) | — | — | — | — | — | PMADRH2 | PMADRH1 | PMADRH0 | ---- -000 | 28 |
| 9Ch | PMDATL(7) | PMDATL7 | PMDATL6 | PMDATL5 | PMDATL4 | PMDATL3 | PMDATL2 | PMDATL1 | PMDATL0 | 0000 0000 | 28 |
| 9Dh | PMDATH(7) | — | — | Program Memory Data Register High Byte. | | | | | | --00 0000 | 28 |
| 9Eh | ADRESL(5, 6) | Least Significant 2 bits of the left shifted result or 8 bits of the right shifted result | | | | | | | | xxxx xxxx | 85, 117 |
| 9Fh | ANSEL | — | ADCS2 | ADCS1 | ADCS0 | ANS3 | ANS2 | ANS1 | ANS0 | -000 1111 | 45, 117 |

**Legend:** – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

**Note 1:** IRP and RP1 bits are reserved, always maintain these bits clear.

**2:** GP3 pull-up is enabled when MCLRE is '1' in the Configuration Word register.

**3:** $\overline{\text{MCLR}}$ and WDT Reset does not affect the previous value data latch. The GPIF bit will clear upon Reset but will set again if the mismatch exists.

**4:** TRISIO3 always reads as '1' since it is an input only pin.

**5:** Read only register.

**6:** PIC12F615/617/HV615 only.

**7:** PIC12F617 only.

#### 2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- the Reset status
- the bank select bits for data memory (RAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS,` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `'000u u1uu'` (where `u` = unchanged).

It is recommended, therefore, that only `BCF, BSF, SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see the **Section 14.0 "Instruction Set Summary"**.

> **Note 1:** Bits IRP and RP1 of the STATUS register are not used by the PIC12F609/615/617/12HV609/615 and should be maintained as clear. Use of these bits is not recommended, since this may affect upward compatibility with future products.
>
> **2:** The C and DC bits operate as a $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

**REGISTER 2-1: STATUS: STATUS REGISTER**

| Reserved | Reserved | R/W-0 | R-1 | R-1 | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| IRP | RP1 | RP0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **IRP:** This bit is reserved and should be maintained as '0'

bit 6 **RP1:** This bit is reserved and should be maintained as '0'

bit 5 **RP0:** Register Bank Select bit (used for direct addressing)
1 = Bank 1 (80h – FFh)
0 = Bank 0 (00h – 7Fh)

bit 4 **$\overline{TO}$:** Time-out bit
1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions), For $\overline{Borrow}$, the polarity is reversed.
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit[(1)] (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

**Note 1:** For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.


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#### 2.2.2.2 OPTION Register

The OPTION register is a readable and writable register, which contains various control bits to configure:

- Timer0/WDT prescaler
- External GP2/INT interrupt
- Timer0
- Weak pull-ups on GPIO

> **Note:** To achieve a 1:1 prescaler assignment for Timer0, assign the prescaler to the WDT by setting PSA bit to '1' of the OPTION register. See **Section 6.1.3 "Software Programmable Prescaler"**.

**REGISTER 2-2: OPTION_REG: OPTION REGISTER**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{GPPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **$\overline{\text{GPPU}}$:** GPIO Pull-up Enable bit
1 = GPIO pull-ups are disabled
0 = GPIO pull-ups are enabled by individual PORT latch values

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of GP2/INT pin
0 = Interrupt on falling edge of GP2/INT pin

bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on GP2/T0CKI pin
0 = Internal instruction cycle clock (FOSC/4)

bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on GP2/T0CKI pin
0 = Increment on low-to-high transition on GP2/T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

| BIT VALUE | TIMER0 RATE | WDT RATE |
|---|---|---|
| 000 | 1 : 2 | 1 : 1 |
| 001 | 1 : 4 | 1 : 2 |
| 010 | 1 : 8 | 1 : 4 |
| 011 | 1 : 16 | 1 : 8 |
| 100 | 1 : 32 | 1 : 16 |
| 101 | 1 : 64 | 1 : 32 |
| 110 | 1 : 128 | 1 : 64 |
| 111 | 1 : 256 | 1 : 128 |

#### 2.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, GPIO change and external GP2/INT pin interrupts.

> **Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

**REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE:** Timer0 Overflow Interrupt Enable bit
1 = Enables the Timer0 interrupt
0 = Disables the Timer0 interrupt

bit 4 **INTE:** GP2/INT External Interrupt Enable bit
1 = Enables the GP2/INT external interrupt
0 = Disables the GP2/INT external interrupt

bit 3 **GPIE:** GPIO Change Interrupt Enable bit(1)
1 = Enables the GPIO change interrupt
0 = Disables the GPIO change interrupt

bit 2 **T0IF:** Timer0 Overflow Interrupt Flag bit(2)
1 = Timer0 register has overflowed (must be cleared in software)
0 = Timer0 register did not overflow

bit 1 **INTF:** GP2/INT External Interrupt Flag bit
1 = The GP2/INT external interrupt occurred (must be cleared in software)
0 = The GP2/INT external interrupt did not occur

bit 0 **GPIF:** GPIO Change Interrupt Flag bit
1 = When at least one of the GPIO <5:0> pins changed state (must be cleared in software)
0 = None of the GPIO <5:0> pins have changed state

**Note 1:** IOC register must also be enabled.
**2:** T0IF bit is set when TMR0 rolls over. TMR0 is unchanged on Reset and should be initialized before clearing T0IF bit.


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#### 2.2.2.4 PIE1 Register

The PIE1 register contains the Peripheral Interrupt Enable bits, as shown in Register 2-4.

**Note:** Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

**REGISTER 2-4: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1**

| U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | ADIE(1) | CCP1IE(1) | — | CMIE | — | TMR2IE(1) | TMR1IE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **ADIE:** A/D Converter (ADC) Interrupt Enable bit(1)
1 = Enables the ADC interrupt
0 = Disables the ADC interrupt

bit 5 **CCP1IE:** CCP1 Interrupt Enable bit(1)
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **CMIE:** Comparator Interrupt Enable bit
1 = Enables the Comparator interrupt
0 = Disables the Comparator interrupt

bit 2 **Unimplemented:** Read as ‘0’

bit 1 **TMR2IE:** Timer2 to PR2 Match Interrupt Enable bit(1)
1 = Enables the Timer2 to PR2 match interrupt
0 = Disables the Timer2 to PR2 match interrupt

bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit
1 = Enables the Timer1 overflow interrupt
0 = Disables the Timer1 overflow interrupt

**Note 1:** PIC12F615/617/HV615 only. PIC12F609/HV609 unimplemented, read as ‘0’.

### 2.2.2.5 PIR1 Register

The PIR1 register contains the Peripheral Interrupt flag bits, as shown in Register 2-5.

> **Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

**REGISTER 2-5: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1**

| U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | ADIF(1) | CCP1IF(1) | — | CMIF | — | TMR2IF(1) | TMR1IF |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **ADIF:** A/D Interrupt Flag bit(1)
1 = A/D conversion complete
0 = A/D conversion has not completed or has not been started

bit 5 **CCP1IF:** CCP1 Interrupt Flag bit(1)
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM mode:
Unused in this mode

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **CMIF:** Comparator Interrupt Flag bit
1 = Comparator output has changed (must be cleared in software)
0 = Comparator output has not changed

bit 2 **Unimplemented:** Read as ‘0’

bit 1 **TMR2IF:** Timer2 to PR2 Match Interrupt Flag bit(1)
1 = Timer2 to PR2 match occurred (must be cleared in software)
0 = Timer2 to PR2 match has not occurred

bit 0 **TMR1IF:** Timer1 Overflow Interrupt Flag bit
1 = Timer1 register overflowed (must be cleared in software)
0 = Timer1 has not overflowed

**Note 1:** PIC12F615/617/HV615 only. PIC12F609/HV609 unimplemented, read as ‘0’.


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#### 2.2.2.6 PCON Register

The Power Control (PCON) register (see Table 12-2) contains flag bits to differentiate between a:

- Power-on Reset ($\overline{POR}$)
- Brown-out Reset ($\overline{BOR}$)
- Watchdog Timer Reset (WDT)
- External $\overline{MCLR}$ Reset

The PCON register also controls the software enable of the $\overline{BOR}$.

The PCON register bits are shown in Register 2-6.

**REGISTER 2-6: PCON: POWER CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0(1) |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | $\overline{POR}$ | $\overline{BOR}$ |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **$\overline{POR}$:** Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

**Note 1:** Reads as ‘0’ if Brown-out Reset is disabled.

### 2.2.2.7 APFCON Register (PIC12F615/617/HV615 only)

The Alternate Pin Function Control (APFCON) register is used to steer specific peripheral input and output functions between different pins. For this device, the P1A, P1B and Timer1 Gate functions can be moved between different pins.

The APFCON register bits are shown in Register 2-7.

**REGISTER 2-7: APFCON:ALTERNATE PIN FUNCTION REGISTER(1)**

| U-0 | U-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | T1GSEL | — | — | P1BSEL | P1ASEL |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **T1GSEL:** TMR1 Input Pin Select bit
1 = T1G function is on GP3/$\overline{\text{T1G}}$(2)/$\overline{\text{MCLR}}$/VPP
0 = T1G function is on GP4/AN3/CIN1-/$\overline{\text{T1G}}$/P1B(2)/OSC2/CLKOUT

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1 **P1BSEL:** P1B Output Pin Select bit
1 = P1B function is on GP4/AN3/CIN1-/$\overline{\text{T1G}}$/P1B(2)/OSC2/CLKOUT
0 = P1B function is on GP0/AN0/CIN+/P1B/ICSPDAT

bit 0 **P1ASEL:** P1A Output Pin Select bit
1 = P1A function is on GP5/T1CKI/P1A(2)/OSC1/CLKIN
0 = P1A function is on GP2/AN2/T0CKI/INT/COUT/CCP1/P1A

**Note 1:** PIC12F615/617/HV615 only.
**2:** Alternate pin function.


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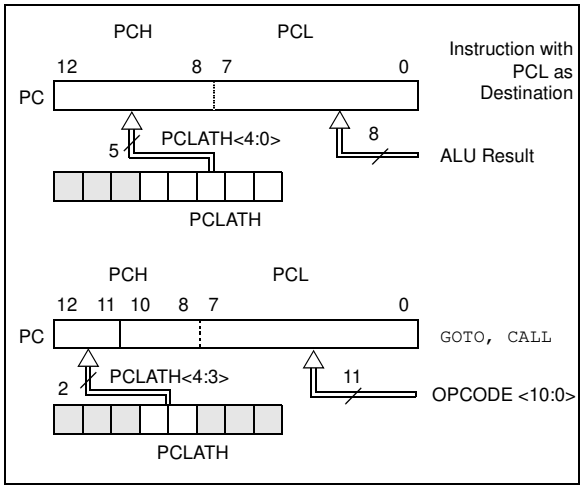
## 2.3 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-5 shows the two situations for the loading of the PC. The upper example in Figure 2-5 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in Figure 2-5 shows how the PC is loaded during a `CALL` or `GOTO` instruction (PCLATH<4:3> → PCH).

**FIGURE 2-5: LOADING OF PC IN DIFFERENT SITUATIONS**




### 2.3.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<12:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper 5 bits to the PCLATH register. When the lower 8 bits are written to the PCL register, all 13 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

A computed `GOTO` is accomplished by adding an offset to the program counter (`ADDWF PCL`). Care should be exercised when jumping into a look-up table or program branch table (computed `GOTO`) by modifying the PCL register. Assuming that PCLATH is set to the table start address, if the table length is greater than 255 instructions or if the lower 8 bits of the memory address rolls over from 0xFF to 0x00 in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and the target location within the table.

For more information refer to Application Note AN556, "*Implementing a Table Read*" (DS00556).

### 2.3.2 STACK

The PIC12F609/615/617/12HV609/615 Family has an 8-level x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a `CALL` instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a `RETURN`, `RETLW` or a `RETFIE` instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

> **Note 1:** There are no Status bits to indicate stack overflow or stack underflow conditions.
>
> **2:** There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the `CALL`, `RETURN`, `RETLW` and `RETFIE` instructions or the vectoring to an interrupt address.

## 2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

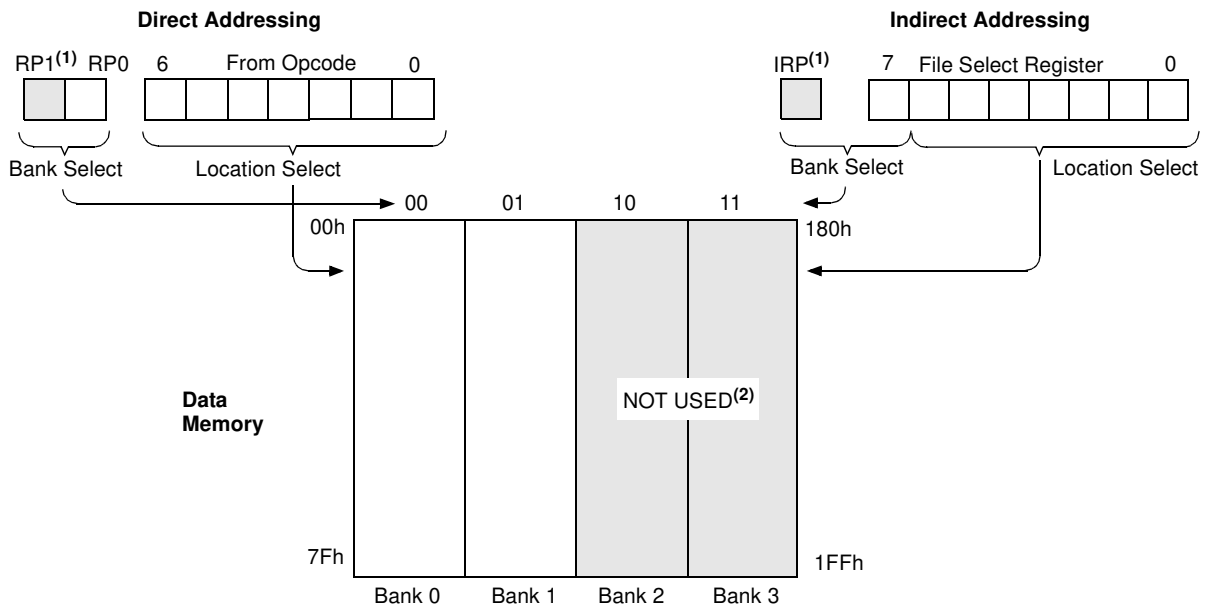
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR and the IRP bit of the STATUS register, as shown in Figure 2-6.

A simple program to clear RAM location 40h-7Fh using indirect addressing is shown in Example 2-1.

**EXAMPLE 2-1: INDIRECT ADDRESSING**

```
        MOVLW   0x40    ;initialize pointer
        MOVWF   FSR     ;to RAM
NEXT    CLRF    INDF    ;clear INDF register
        INCF    FSR     ;inc pointer
        BTFSS   FSR,7   ;all done?
        GOTO    NEXT    ;no clear next
CONTINUE                ;yes continue
```

**FIGURE 2-6: DIRECT/INDIRECT ADDRESSING PIC12F609/615/617/12HV609/615**




For memory map detail, see Figure 2-3.

**Note 1:** The RP1 and IRP bits are reserved; always maintain these bits clear.

**2:** Accesses in this area are mirrored back into Bank 0 and Bank 1.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## 3.0 FLASH PROGRAM MEMORY SELF READ/SELF WRITE CONTROL (FOR PIC12F617 ONLY)

The Flash program memory is readable and writable during normal operation (full $V_{DD}$ range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers (see Registers 3-1 to 3-5). There are six SFRs used to read and write this memory:

- PMCON1
- PMCON2
- PMDATL
- PMDATH
- PMADRL
- PMADRH

When interfacing the program memory block, the PMDATL and PMDATH registers form a two-byte word which holds the 14-bit data for read/write, and the PMADRL and PMADRH registers form a two-byte word which holds the 13-bit address of the Flash location being accessed. These devices have 2K words of program Flash with an address range from 0000h to 07FFh.

The program memory allows single word read and a by four word write. A four word write automatically erases the row of the location and writes the new data (erase before write).

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the voltage range of the device for byte or word operations.

When the device is code-protected, the CPU may continue to read and write the Flash program memory.

Depending on the settings of the Flash Program Memory Enable (WRT<1:0>) bits, the device may or may not be able to write certain blocks of the program memory, however, reads of the program memory are allowed.

When the Flash program memory Code Protection ($\overline{CP}$) bit in the Configuration Word register is enabled, the program memory is code-protected, and the device programmer (ICSP™) cannot access data or program memory.

### 3.1 PMADRH and PMADRL Registers

The PMADRH and PMADRL registers can address up to a maximum of 8K words of program memory.

When selecting a program address value, the Most Significant Byte (MSB) of the address is written to the PMADRH register and the Least Significant Byte (LSB) is written to the PMADRL register.

### 3.2 PMCON1 and PMCON2 Registers

PMCON1 is the control register for the data program memory accesses.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear.

PMCON2 is not a physical register. Reading PMCON2 will read all '0's. The PMCON2 register is used exclusively in the Flash memory write sequence.

### REGISTER 3-1: PMDATL: PROGRAM MEMORY DATA REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PMDATL7 | PMDATL6 | PMDATL5 | PMDATL4 | PMDATL3 | PMDATL2 | PMDATL1 | PMDATL0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-0 **PMDATL<7:0>**: 8 Least Significant Address bits to Write or Read from Program Memory

### REGISTER 3-2: PMADRL: PROGRAM MEMORY ADDRESS REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PMADRL7 | PMADRL6 | PMADRL5 | PMADRL4 | PMADRL3 | PMADRL2 | PMADRL1 | PMADRL0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-0 **PMADRL<7:0>**: 8 Least Significant Address bits for Program Memory Read/Write Operation

### REGISTER 3-3: PMDATH: PROGRAM MEMORY DATA HIGH BYTE REGISTER

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | PMDATH5 | PMDATH4 | PMDATH3 | PMDATH2 | PMDATH1 | PMDATH0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **PMDATH<5:0>**: 6 Most Significant Data bits from Program Memory

### REGISTER 3-4: PMADRH: PROGRAM MEMORY ADDRESS HIGH BYTE REGISTER

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | PMADRH2 | PMADRH1 | PMADRH0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **PMADRH<2:0>**: Specifies the 3 Most Significant Address bits or high bits for program memory reads.


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**REGISTER 3-5: PMCON1 – PROGRAM MEMORY CONTROL REGISTER 1 (ADDRESS: 93h)**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| U-1 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/S-0 | R/S-0 |
| — | — | — | — | — | WREN | WR | RD |
| bit 7 | | | | | | | bit 0 |

bit 7 **Unimplemented:** Read as '1'

bit 6-3 **Unimplemented:** Read as '0'

bit 2 **WREN:** Program Memory Write Enable bit

1 = Allows write cycles
0 = Inhibits write to the EEPROM

bit 1 **WR:** Write Control bit

1 = Initiates a write cycle to program memory. (The bit is cleared by hardware when write is complete. The WR bit can only be set (not cleared) in software.)
0 = Write cycle to the Flash memory is complete

bit 0 **RD:** Read Control bit

1 = Initiates a program memory read (The read takes one cycle. The RD is cleared in hardware; the RD bit can only be set (not cleared) in software).
0 = Does not initiate a Flash memory read

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | 1 = bit is set | 0 = bit is cleared | x = bit is unknown |

## 3.3 Reading the Flash Program Memory

To read a program memory location, the user must write two bytes of the address to the PMADRL and PMADRH registers, and then set control bit RD (PMCON1<0>). Once the read control bit is set, the program memory Flash controller will use the second instruction cycle after to read the data. This causes the second instruction immediately following the "`BSF PMCON1,RD`" instruction to be ignored. The data is available in the very next cycle in the PMDATL and PMDATH registers; it can be read as two bytes in the following instructions. PMDATL and PMDATH registers will hold this value until another read or until it is written to by the user (during a write operation).

**EXAMPLE 3-1: FLASH PROGRAM READ**

```
BANKSEL PM_ADR            ; Change STATUS bits RP1:0 to select bank with PMADRL
MOVLW   MS_PROG_PM_ADDR   ;
MOVWF   PMADRH            ; MS Byte of Program Address to read
MOVLW   LS_PROG_PM_ADDR   ;
MOVWF   PMADRL            ; LS Byte of Program Address to read
BANKSEL PMCON1            ; Bank to containing PMCON1
BSF     PMCON1, RD        ; PM Read

NOP                       ; First instruction after BSF PMCON1,RD executes normally

NOP                       ; Any instructions here are ignored as program
                          ; memory is read in second cycle after BSF PMCON1,RD
                          ;
BANKSEL PMDATL            ; Bank to containing PMADRL
MOVF    PMDATL, W         ; W = LS Byte of Program PMDATL
MOVF    PMDATH, W         ; W = MS Byte of Program PMDATL
```


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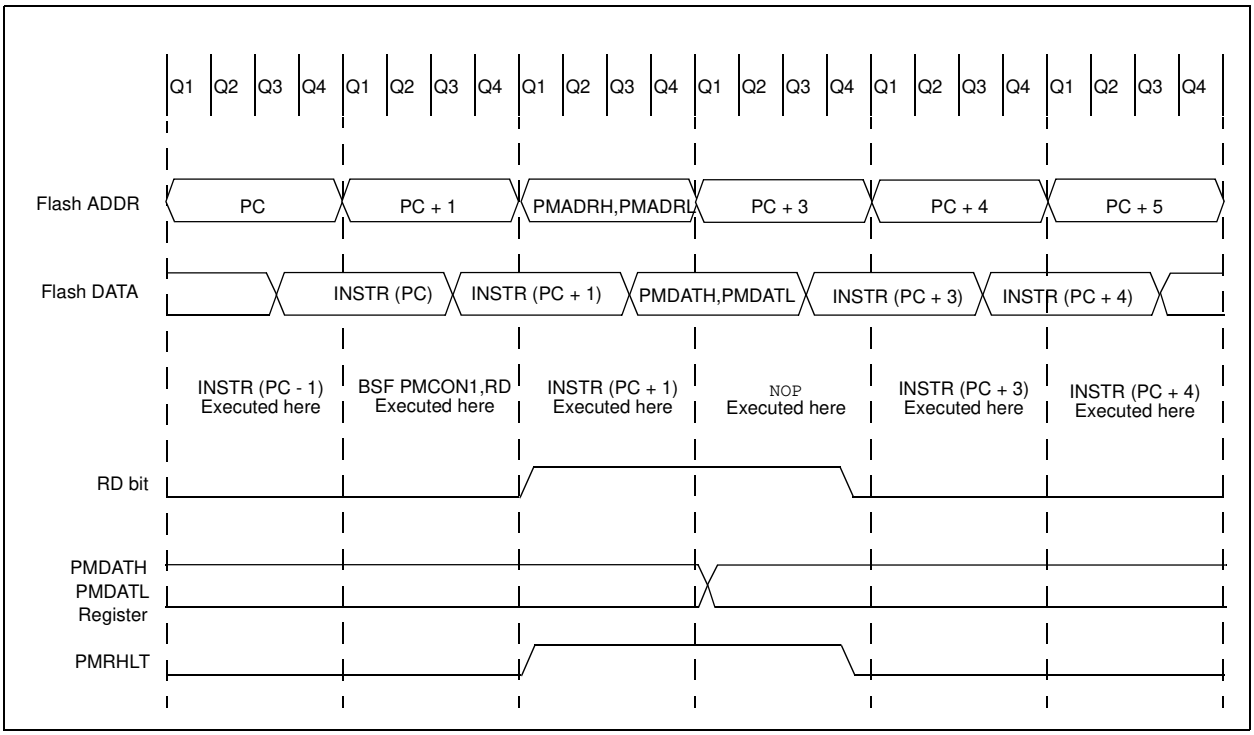
**FIGURE 3-1: FLASH PROGRAM MEMORY READ CYCLE EXECUTION**



## 3.4 Writing the Flash Program Memory

A word of the Flash program memory may only be written to if the word is in an unprotected segment of memory.

Flash program memory must be written in four-word blocks. See Figure 3-2 and Figure 3-3 for more details. A block consists of four words with sequential addresses, with a lower boundary defined by an address, where PMADRL<1:0> = `00`. All block writes to program memory are done as 16-word erase by four-word write operations. The write operation is edge-aligned and cannot occur across boundaries.

To write program data, it must first be loaded into the buffer registers (see Figure 3-2). This is accomplished by first writing the destination address to PMADRL and PMADRH and then writing the data to PMDATL and PMDATH. After the address and data have been set up, then the following sequence of events must be executed:

1. Write 55h, then AAh, to PMCON2 (Flash programming sequence).
2. Set the WR control bit of the PMCON1 register.

All four buffer register locations should be written to with correct data. If less than four words are being written to in the block of four words, then a read from the program memory location(s) not being written to must be performed. This takes the data from the program location(s) not being written and loads it into the PMDATL and PMDATH registers. Then the sequence of events to transfer data to the buffer registers must be executed.

To transfer data from the buffer registers to the program memory, the PMADRL and PMADRH must point to the last location in the four-word block (PMADRL<1:0> = `11`). Then the following sequence of events must be executed:

1. Write 55h, then AAh, to PMCON2 (Flash programming sequence).
2. Set control bit WR of the PMCON1 register to begin the write operation.

The user must follow the same specific sequence to initiate the write for each word in the program block, writing each program word in sequence (`000`, `001`, `010`, `011`). When the write is performed on the last word (PMADRL<1:0> = `11`), a block of sixteen words is automatically erased and the content of the four-word buffer registers are written into the program memory.

After the "`BSF PMCON1,WR`" instruction, the processor requires two cycles to set up the erase/write operation. The user must place two `NOP` instructions after the WR bit is set. Since data is being written to buffer registers, the writing of the first three words of the block appears to occur immediately. The processor will halt internal operations for the typical 4 ms, only during the cycle in which the erase takes place (i.e., the last word of the sixteen-word block erase). This is not Sleep mode as the clocks and peripherals will continue to run. After the four-word write cycle, the processor will resume operation with the third instruction after the PMCON1 write instruction. The above sequence must be repeated for the higher 12 words.

## 3.5 Protection Against Spurious Write

There are conditions when the device should not write to the program memory. To protect against spurious writes, various mechanisms have been built in. On power-up, WREN is cleared. Also, the Power-up Timer (64 ms duration) prevents program memory writes.

The write initiate sequence and the WREN bit help prevent an accidental write during brown-out, power glitch or software malfunction.

## 3.6 Operation During Code-Protect

When the device is code-protected, the CPU is able to read and write unscrambled data to the program memory. The test mode access is disabled.

## 3.7 Operation During Write Protect

When the program memory is write-protected, the CPU can read and execute from the program memory. The portions of program memory that are write protected can be modified by the CPU using the PMCON registers, but the protected program memory cannot be modified using ICSP mode.


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**FIGURE 3-2: BLOCK WRITES TO 2K FLASH PROGRAM MEMORY**

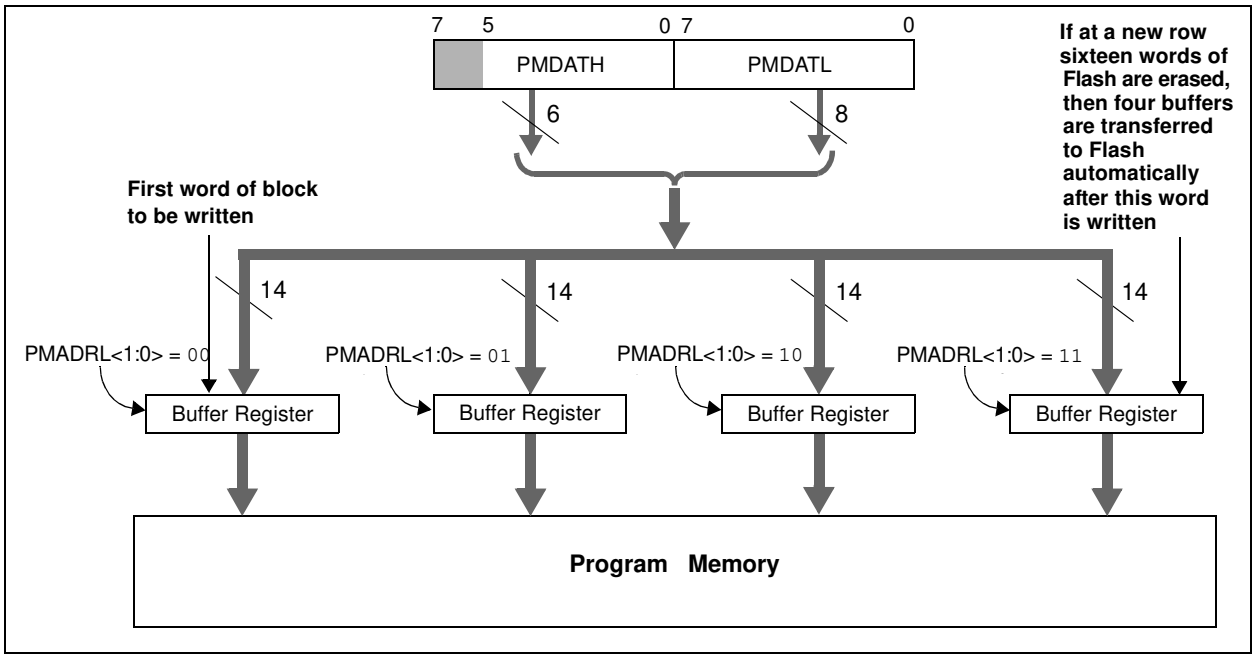
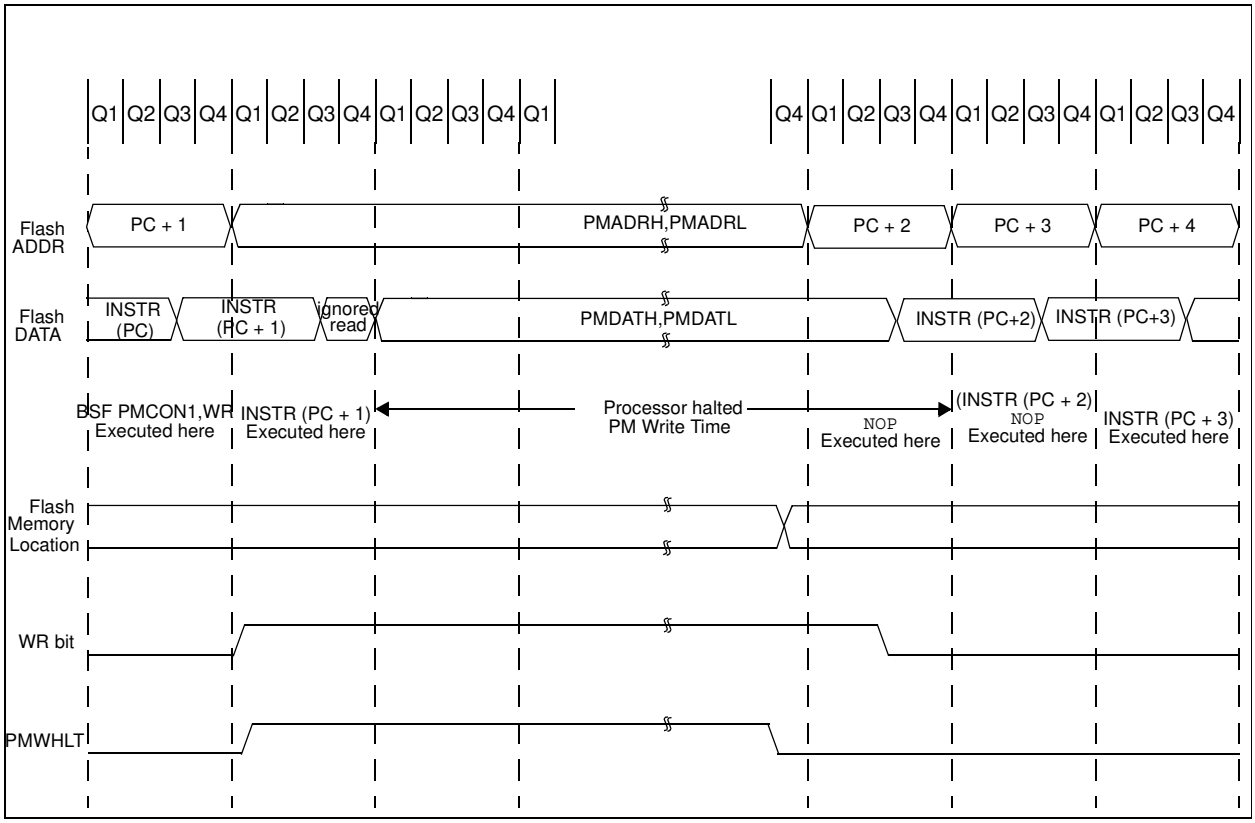



**FIGURE 3-3: FLASH PROGRAM MEMORY LONG WRITE CYCLE EXECUTION**



An example of the complete four-word write sequence is shown in Example 3-2. The initial address is loaded into the PMADRH and PMADRL register pair; the eight words of data are loaded using indirect addressing.

**EXAMPLE 3-2: WRITING TO FLASH PROGRAM MEMORY**

```
        ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
        ; This write routine assumes the following:
        ;     A valid starting address (the least significant bits = '00')
        ;     is loaded in ADDRH:ADDRL
        ;     ADDRH, ADDRL and DATADDR are all located in data memory
        ;
        BANKSEL  PMADRH
        MOVF     ADDRH,W      ; Load initial address
        MOVWF    PMADRH       ;
        MOVF     ADDRL,W      ;
        MOVWF    PMADRL       ;
        MOVF     DATAADDR,W   ; Load initial data address
        MOVWF    FSR          ;
LOOP    MOVF     INDF,W       ; Load first data byte into lower
        MOVWF    PMDATL       ;
        INCF     FSR,F        ; Next byte
        MOVF     INDF,W       ; Load second data byte into upper
        MOVWF    PMDATH       ;
        INCF     FSR,F        ;
        BANKSEL  PMCON1
        BSF      PMCON1,WREN  ; Enable writes
        BCF      INTCON,GIE   ; Disable interrupts (if using)
        BTFSC    INTCON,GIE   ; See AN576
        GOTO     $-2
        ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
        ;                         Required Sequence
        MOVLW    55h          ; Start of required write sequence:
        MOVWF    PMCON2       ; Write 55h
        MOVLW    0AAh         ;
        MOVWF    PMCON2       ; Write 0AAh
        BSF      PMCON1,WR    ; Set WR bit to begin write
        NOP                   ; Required to transfer data to the buffer
        NOP                   ; registers
        ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
        BCF      PMCON1,WREN  ; Disable writes
        BSF      INTCON,GIE   ; Enable interrupts (comment out if not using interrupts)
        BANKSEL  PMADRL
        MOVF     PMADRL, W
        INCF     PMADRL,F     ; Increment address
        ANDLW    0x03         ; Indicates when sixteen words have been programmed
        SUBLW    0x03         ;   0x0F = 16 words
                              ;   0x0B = 12 words
                              ;   0x07 = 8 words
                              ;   0x03 = 4 words
        BTFSS    STATUS,Z     ; Exit on a match,
        GOTO     LOOP         ; Continue if more data needs to be written
```


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**TABLE 3-1: SUMMARY OF REGISTERS ASSOCIATED WITH PROGRAM MEMORY**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| PMCON1 | — | — | — | — | — | WREN | WR | RD | ---- -000 | ---- -000 |
| PMCON2 | Program Memory Control Register 2 (not a physical register) | | | | | | | | ---- ---- | ---- ---- |
| PMADRL | PMADRL7 | PMADRL6 | PMADRL5 | PMADRL4 | PMADRL3 | PMADRL2 | PMADRL1 | PMADRL0 | 0000 0000 | 0000 0000 |
| PMADRH | — | — | — | — | — | PMADRH2 | PMADRH1 | PMADRH0 | ---- -000 | ---- -000 |
| PMDATL | PMDATL7 | PMDATL6 | PMDATL5 | PMDATL4 | PMDATL3 | PMDATL2 | PMDATL1 | PMDATL0 | 0000 0000 | 0000 0000 |
| PMDATH | — | — | PMDATH5 | PMDATH4 | PMDATH3 | PMDATH2 | PMDATH1 | PMDATH0 | --00 0000 | --00 0000 |

**Legend:** x = unknown, u = unchanged, — = unimplemented read as '0', q = value depends upon condition.
Shaded cells are not used by Program Memory module.

**NOTES:**


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# 4.0 OSCILLATOR MODULE

## 4.1 Overview

The Oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 4-1 illustrates a block diagram of the Oscillator module.

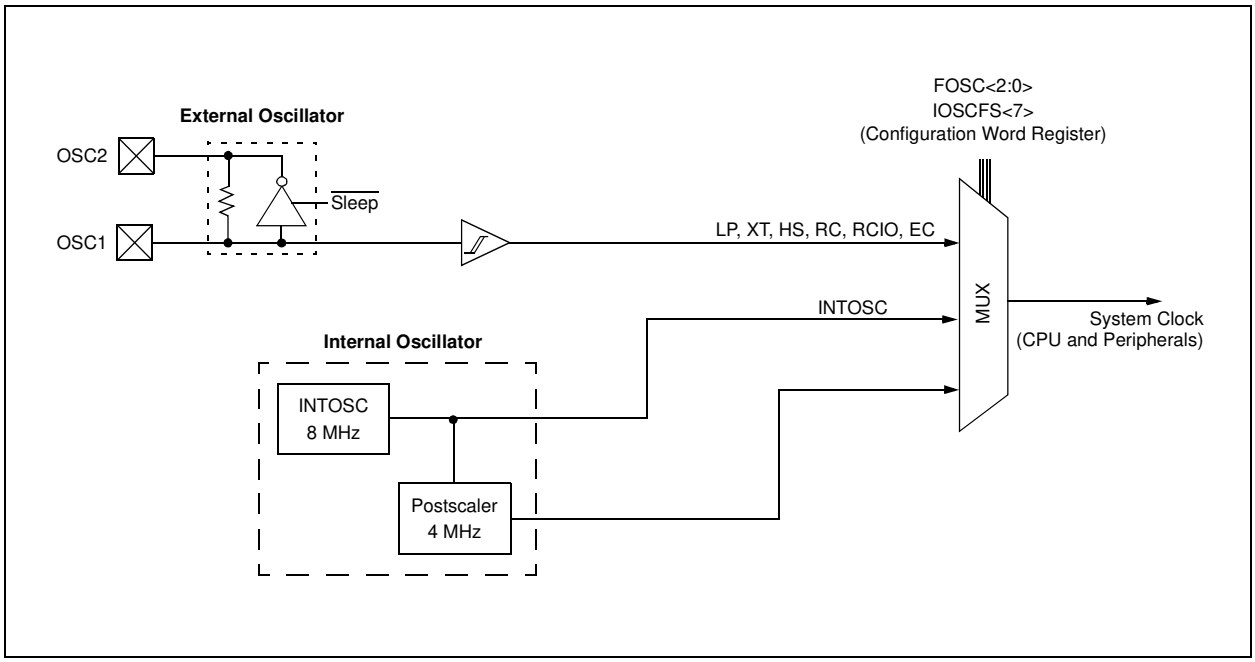
Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be configured with a choice of two selectable speeds: internal or external system clock source.

The Oscillator module can be configured in one of eight clock modes.

3. EC – External clock with I/O on OSC2/CLKOUT.
4. LP – 32 kHz Low-Power Crystal mode.
5. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode.
6. HS – High Gain Crystal or Ceramic Resonator mode.
7. RC – External Resistor-Capacitor (RC) with FOSC/4 output on OSC2/CLKOUT.
8. RCIO – External Resistor-Capacitor (RC) with I/O on OSC2/CLKOUT.
9. INTOSC – Internal oscillator with FOSC/4 output on OSC2 and I/O on OSC1/CLKIN.
10. INTOSCIO – Internal oscillator with I/O on OSC1/CLKIN and OSC2/CLKOUT.

Clock Source modes are configured by the FOSC<2:0> bits in the Configuration Word register (CONFIG). The Internal Oscillator module provides a selectable system clock mode of either 4 MHz (Postscaler) or 8 MHz (INTOSC).

**FIGURE 4-1: PIC® MCU CLOCK SOURCE BLOCK DIAGRAM**



## 4.2 Clock Source Modes

Clock Source modes can be classified as external or internal.

- External Clock modes rely on external circuitry for the clock source. Examples are: Oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.
- Internal clock sources are contained internally within the Oscillator module. The Oscillator module has two selectable clock frequencies: 4 MHz and 8 MHz

The system clock can be selected between external or internal clock sources via the FOSC<2:0> bits of the Configuration Word register.

## 4.3 External Clock Modes

### 4.3.1 OSCILLATOR START-UP TIMER (OST)

If the Oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the Oscillator module. When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 4-1.

**TABLE 4-1: OSCILLATOR DELAY EXAMPLES**

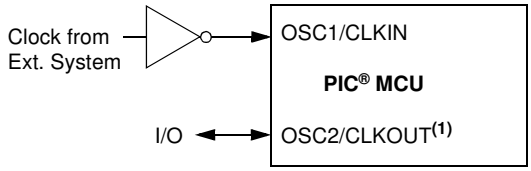
| Switch From | Switch To | Frequency | Oscillator Delay |
|---|---|---|---|
| Sleep/POR | INTOSC | 125 kHz to 8 MHz | Oscillator Warm-Up Delay (TWARM) |
| Sleep/POR | EC, RC | DC – 20 MHz | 2 instruction cycles |
| Sleep/POR | LP, XT, HS | 32 kHz to 20 MHz | 1024 Clock Cycles (OST) |

### 4.3.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input and the OSC2 is available for general purpose I/O. Figure 4-2 shows the pin connections for EC mode.

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

**FIGURE 4-2: EXTERNAL CLOCK (EC) MODE OPERATION**




**Note 1:** Alternate pin functions are listed in the **Section 1.0 "Device Overview"**.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### 4.3.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 4-3). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

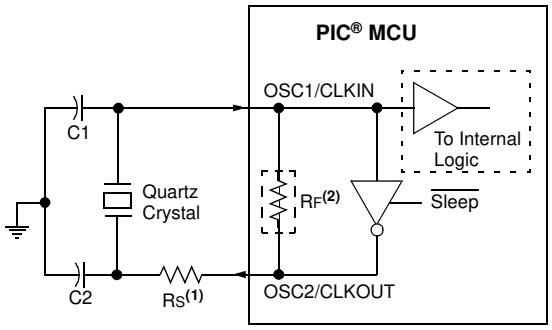
**LP** Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

**XT** Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

**HS** Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 4-3 and Figure 4-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

**FIGURE 4-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)**




**Note 1:** A series resistor (RS) may be required for quartz crystals with low drive level.

**2:** The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

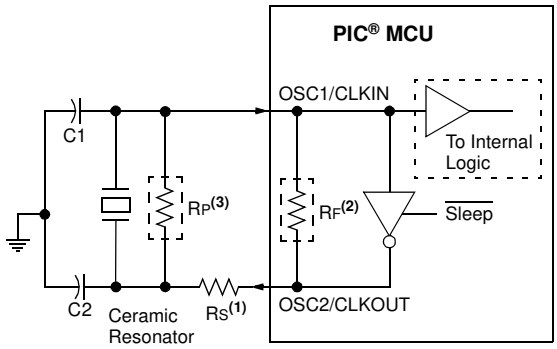
**Note 1:** Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

**2:** Always verify oscillator performance over the VDD and temperature range that is expected for the application.

**3:** For oscillator design assistance, reference the following Microchip Applications Notes:

- AN826, "*Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices*" (DS00826)
- AN849, "*Basic PIC® Oscillator Design*" (DS00849)
- AN943, "*Practical PIC® Oscillator Analysis and Design*" (DS00943)
- AN949, "*Making Your Oscillator Work*" (DS00949)

**FIGURE 4-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)**




**Note 1:** A series resistor (RS) may be required for ceramic resonators with low drive level.

**2:** The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

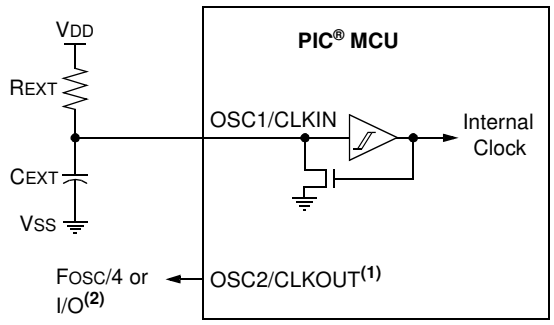
**3:** An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation.

### 4.3.4 EXTERNAL RC MODES

The external Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required. There are two modes: RC and RCIO.

In RC mode, the RC circuit connects to OSC1. OSC2/CLKOUT outputs the RC oscillator frequency divided by 4. This signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements. Figure 4-5 shows the external RC mode connections.

**FIGURE 4-5: EXTERNAL RC MODES**




Recommended values: 10 kΩ ≤ REXT ≤ 100 kΩ, <3V
3 kΩ ≤ REXT ≤ 100 kΩ, 3-5V
CEXT > 20 pF, 2-5V

**Note 1:** Alternate pin functions are listed in **Section 1.0 "Device Overview"**.

**2:** Output depends upon RC or RCIO Clock mode.

In RCIO mode, the RC circuit is connected to OSC1. OSC2 becomes an additional general purpose I/O pin.

The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. Other factors affecting the oscillator frequency are:

- threshold voltage variation
- component tolerances
- packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

## 4.4 Internal Clock Modes

The Oscillator module provides a selectable system clock source of either 4 MHz or 8 MHz. The selectable frequency is configured through the IOSCFS bit of the Configuration Word.

The frequency of the internal oscillator can be trimmed with a calibration value in the OSCTUNE register.

### 4.4.1 INTOSC AND INTOSCIO MODES

The INTOSC and INTOSCIO modes configure the internal oscillators as the system clock source when the device is programmed using the oscillator selection or the FOSC<2:0> bits in the Configuration Word register (CONFIG). See **Section 12.0 "Special Features of the CPU"** for more information.

In **INTOSC** mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT outputs the selected internal oscillator frequency divided by 4. The CLKOUT signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements.

In **INTOSCIO** mode, OSC1/CLKIN and OSC2/CLKOUT are available for general purpose I/O.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#### 4.4.1.1 OSCTUNE Register

The oscillator is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 4-1).

The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number.

When the OSCTUNE register is modified, the frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

**REGISTER 4-1: OSCTUNE: OSCILLATOR TUNING REGISTER**

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | TUN4 | TUN3 | TUN2 | TUN1 | TUN0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TUN<4:0>:** Frequency Tuning bits
01111 = Maximum frequency
01110 =
•
•
•
00001 =
00000 = Oscillator module is running at the calibrated frequency.
11111 =
•
•
•
10000 = Minimum frequency

**TABLE 4-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets(1) |
|---|---|---|---|---|---|---|---|---|---|---|
| CONFIG(2) | IOSCFS | $\overline{CP}$ | MCLRE | $\overline{PWRTE}$ | WDTE | FOSC2 | FOSC1 | FOSC0 | — | — |
| OSCTUNE | — | — | — | TUN4 | TUN3 | TUN2 | TUN1 | TUN0 | ---0 0000 | ---u uuuu |

**Legend:** x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by oscillators.
**Note 1:** Other (non Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.
**2:** See Configuration Word register (Register 12-1) for operation of all register bits.

**NOTES:**


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## 5.0 I/O PORT

There are as many as six general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

### 5.1 GPIO and the TRISIO Registers

GPIO is a 6-bit wide port with 5 bidirectional and 1 input-only pin. The corresponding data direction register is TRISIO (Register 5-2). Setting a TRISIO bit (= 1) will make the corresponding GPIO pin an input (i.e., disable the output driver). Clearing a TRISIO bit (= 0) will make the corresponding GPIO pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). The exception is GP3, which is input only and its TRIS bit will always read as '1'. Example 5-1 shows how to initialize GPIO.

| **Note:** | GPIO = PORTA<br>TRISIO = TRISA |
|---|---|

Reading the GPIO register (Register 5-1) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch. GP3 reads '0' when MCLRE = 1.

The TRISIO register controls the direction of the GPIO pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISIO register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

| **Note:** | The ANSEL register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0' and cannot generate an interrupt. |
|---|---|

**EXAMPLE 5-1: INITIALIZING GPIO**

```
BANKSEL  GPIO     ;
CLRF     GPIO     ;Init GPIO
BANKSEL  ANSEL    ;
CLRF     ANSEL    ;digital I/O, ADC clock
                  ;setting 'don't care'
MOVLW    0Ch      ;Set GP<3:2> as inputs
MOVWF    TRISIO    ;and set GP<5:4,1:0>
                   ;as outputs
```

**REGISTER 5-1: GPIO: GPIO REGISTER**

| U-0 | U-0 | R/W-x | R/W-x | R-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **GP<5:0>**: GPIO I/O Pin bit
1 = GPIO pin is > $V_{IH}$
0 = GPIO pin is < $V_{IL}$

**REGISTER 5-2: TRISIO: GPIO TRI-STATE REGISTER**

| U-0 | U-0 | R/W-1 | R/W-1 | R-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | TRISIO5 | TRISIO4 | TRISIO3 | TRISIO2 | TRISIO1 | TRISIO0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-0 **TRISIO<5:0>:** GPIO Tri-State Control bit
1 = GPIO pin configured as an input (tri-stated)
0 = GPIO pin configured as an output

**Note 1:** TRISIO<3> always reads ‘1’.
**2:** TRISIO<5:4> always reads ‘1’ in XT, HS and LP Oscillator modes.

## 5.2 Additional Pin Functions

Every GPIO pin on the PIC12F609/615/617/12HV609/615 has an interrupt-on-change option and a weak pull-up option. The next three sections describe these functions.

### 5.2.1 ANSEL REGISTER

The ANSEL register is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSEL bit high will cause all digital reads on the pin to be read as ‘0’ and allow analog functions on the pin to operate correctly.

The state of the ANSEL bits has no affect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

### 5.2.2 WEAK PULL-UPS

Each of the GPIO pins, except GP3, has an individually configurable internal weak pull-up. Control bits WPUx enable or disable each pull-up. Refer to Register 5-5. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the $\overline{\text{GPPU}}$ bit of the OPTION register). A weak pull-up is automatically enabled for GP3 when configured as $\overline{\text{MCLR}}$ and disabled when GP3 is an I/O. There is no software control of the $\overline{\text{MCLR}}$ pull-up.

### 5.2.3 INTERRUPT-ON-CHANGE

Each GPIO pin is individually configurable as an interrupt-on-change pin. Control bits IOCx enable or disable the interrupt function for each pin. Refer to Register 5-6. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of GPIO. The ‘mismatch’ outputs of the last read are OR’d together to set the GPIO Change Interrupt Flag bit (GPIF) in the INTCON register (Register 2-3).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

a) Any read of GPIO AND Clear flag bit GPIF. This will end the mismatch condition;

OR

b) Any write of GPIO AND Clear flag bit GPIF will end the mismatch condition;

A mismatch condition will continue to set flag bit GPIF. Reading GPIO will end the mismatch condition and allow flag bit GPIF to be cleared. The latch holding the last read value is not affected by a $\overline{\text{MCLR}}$ nor BOR Reset. After these resets, the GPIF flag will continue to be set if a mismatch is present.

**Note:** If a change on the I/O pin should occur when any GPIO operation is being executed, then the GPIF interrupt flag may not get set.


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### REGISTER 5-3: ANSEL: ANALOG SELECT REGISTER (PIC12F609/HV609)

| U-0 | U-0 | U-0 | U-0 | R/W-1 | U-0 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | ANS3 | — | ANS1 | ANS0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-4 **Unimplemented**: Read as ‘0’

bit 3 **ANS3**: Analog Select Between Analog or Digital Function on Pin GP4
1 = Analog input. Pin is assigned as analog input(1).
0 = Digital I/O. Pin is assigned to port or special function.

bit 2 **Unimplemented**: Read as ‘0’

bit 1 **ANS1:** Analog Select Between Analog or Digital Function on Pin GP1
1 = Analog input. Pin is assigned as analog input.(1)
0 = Digital I/O. Pin is assigned to port or special function.

bit 0 **ANS0:** Analog Select Between Analog or Digital Function on Pin GP0
0 = Digital I/O. Pin is assigned to port or special function.
1 = Analog input. Pin is assigned as analog input.(1)

**Note 1:** Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

### REGISTER 5-4: ANSEL: ANALOG SELECT REGISTER (PIC12F615/617/HV615)

| U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | ADCS2 | ADCS1 | ADCS0 | ANS3 | ANS2 | ANS1 | ANS0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **Unimplemented**: Read as ‘0’

bit 6-4 **ADCS<2:0>:** A/D Conversion Clock Select bits
000 = FOSC/2
001 = FOSC/8
010 = FOSC/32
x11 = FRC (clock derived from a dedicated internal oscillator = 500 kHz max)
100 = FOSC/4
101 = FOSC/16
110 = FOSC/64

bit 3-0 **ANS<3:0>**: Analog Select Between Analog or Digital Function on Pins GP4, GP2, GP1, GP0, respectively.
1 = Analog input. Pin is assigned as analog input(1).
0 = Digital I/O. Pin is assigned to port or special function.

**Note 1:** Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

### REGISTER 5-5: WPU: WEAK PULL-UP GPIO REGISTER

| U-0 | U-0 | R/W-1 | R/W-1 | U-0 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | WPU5 | WPU4 | — | WPU2 | WPU1 | WPU0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-4 **WPU<5:4>:** Weak Pull-up Control bits
1 = Pull-up enabled
0 = Pull-up disabled

bit 3 **WPU<3>:** Weak Pull-up Register bit(3)

bit 2-0 **WPU<2:0>:** Weak Pull-up Control bits
1 = Pull-up enabled
0 = Pull-up disabled

**Note 1:** Global $\overline{\text{GPPU}}$ must be enabled for individual pull-ups to be enabled.
**2:** The weak pull-up device is automatically disabled if the pin is in Output mode (TRISIO = 0).
**3:** The GP3 pull-up is enabled when configured as $\overline{\text{MCLR}}$ in the Configuration Word, otherwise it is disabled as an input and reads as ‘0’.
**4:** WPU<5:4> always reads ‘1’ in XT, HS and LP Oscillator modes.

### REGISTER 5-6: IOC: INTERRUPT-ON-CHANGE GPIO REGISTER

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | IOC5 | IOC4 | IOC3 | IOC2 | IOC1 | IOC0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-0 **IOC<5:0>:** Interrupt-on-change GPIO Control bit
1 = Interrupt-on-change enabled
0 = Interrupt-on-change disabled

**Note 1:** Global Interrupt Enable (GIE) must be enabled for individual interrupts to be recognized.
**2:** IOC<5:4> always reads ‘1’ in XT, HS and LP Oscillator modes.


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### 5.2.4 PIN DESCRIPTIONS AND DIAGRAMS

Each GPIO pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the Comparator or the ADC, refer to the appropriate section in this data sheet.

#### 5.2.4.1 GP0/AN0(1)/CIN+/P1B(1)/ICSPDAT

Figure 5-1 shows the diagram for this pin. The GP0 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC(1)
- an analog non-inverting input to the comparator
- a PWM output(1)
- In-Circuit Serial Programming data

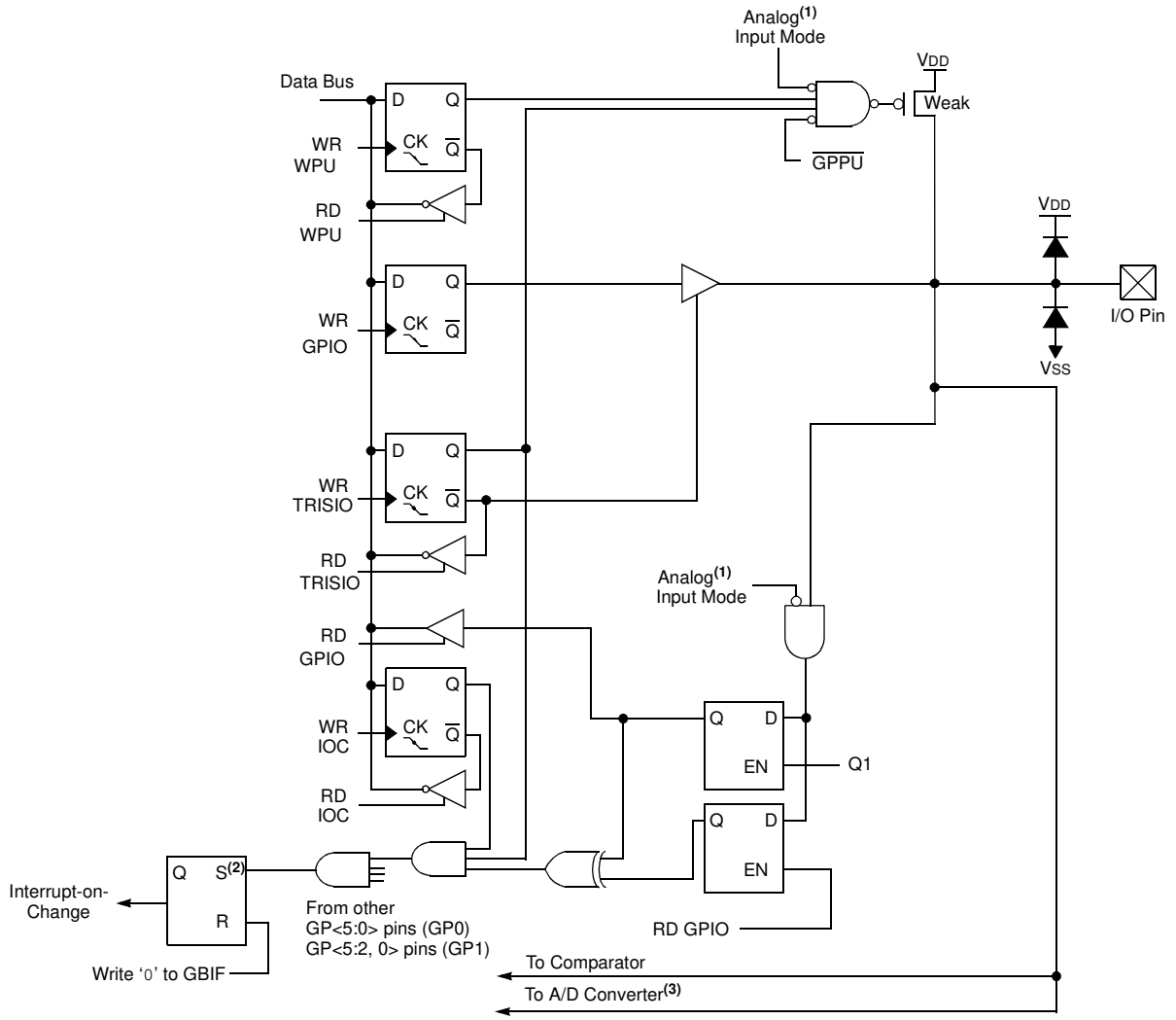
#### 5.2.4.2 GP1/AN1(1)/CIN0-/VREF(1)/ICSPCLK

Figure 5-1 shows the diagram for this pin. The GP1 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC(1)
- an analog inverting input to the comparator
- a voltage reference input for the ADC(1)
- In-Circuit Serial Programming clock

**Note 1:** PIC12F615/617/HV615 only.

**FIGURE 5-1: BLOCK DIAGRAM OF GP<1:0>**




**Note 1:** Comparator mode and ANSEL determines Analog Input mode.
**2:** Set has priority over Reset.
**3:** PIC12F615/617/HV615 only.

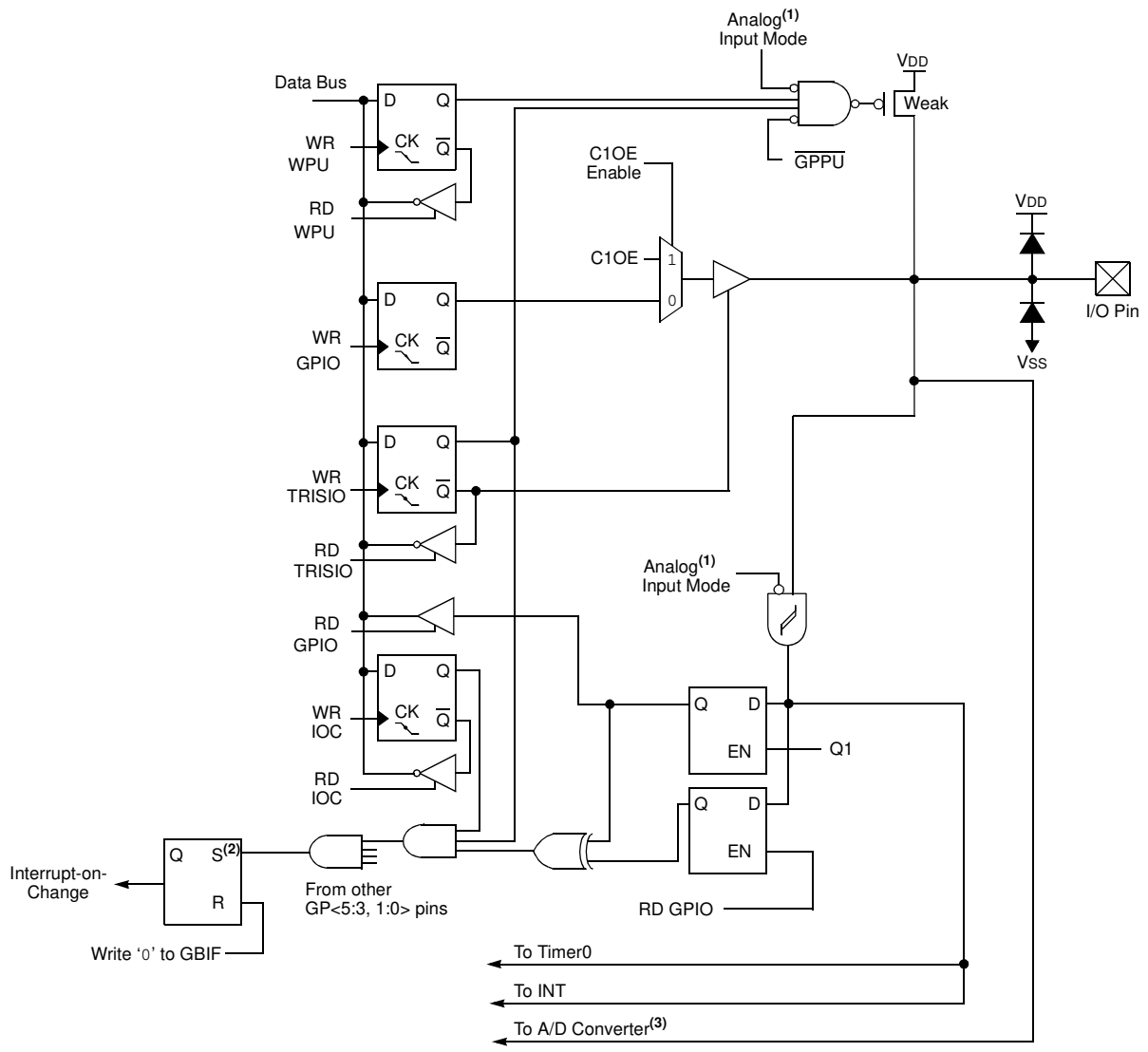
### 5.2.4.3 GP2/AN2(1)/T0CKI/INT/COUT/CCP1(1)/P1A(1)

**Note 1:** PIC12F615/617/HV615 only.

Figure 5-2 shows the diagram for this pin. The GP2 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC(1)
- the clock input for TMR0
- an external edge triggered interrupt
- a digital output from Comparator
- a Capture input/Compare input/PWM output(1)
- a PWM output(1)

**FIGURE 5-2: BLOCK DIAGRAM OF GP2**




**Note 1:** Comparator mode and ANSEL determines Analog Input mode.
**2:** Set has priority over Reset.
**3:** PIC12F615/617/HV615 only.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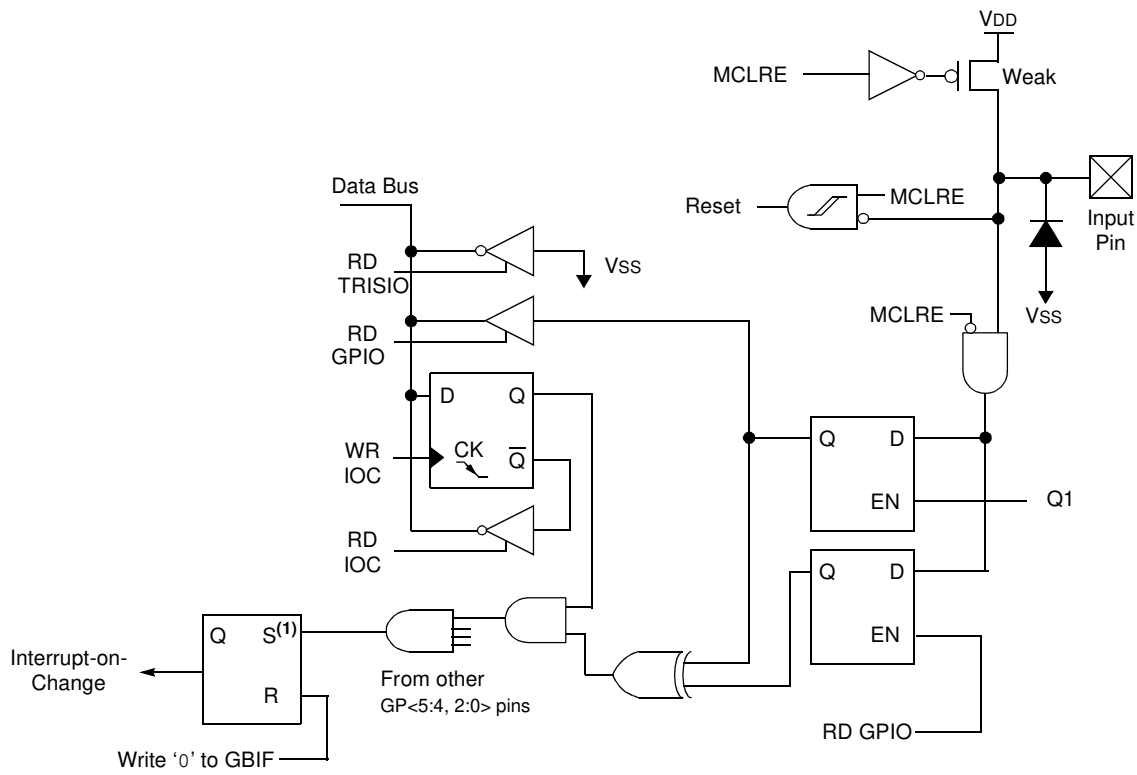
#### 5.2.4.4 GP3/$\overline{\text{T1G}}$[1, 2]/$\overline{\text{MCLR}}$/VPP

Figure 5-3 shows the diagram for this pin. The GP3 pin is configurable to function as one of the following:

- a general purpose input
- a Timer1 gate (count enable), alternate pin[1, 2]
- as Master Clear Reset with weak pull-up

| | |
|---|---|
| **Note 1:** | Alternate pin function. |
| **2:** | PIC12F615/617/HV615 only. |

**FIGURE 5-3: BLOCK DIAGRAM OF GP3**




**Note 1:** Set has priority over Reset

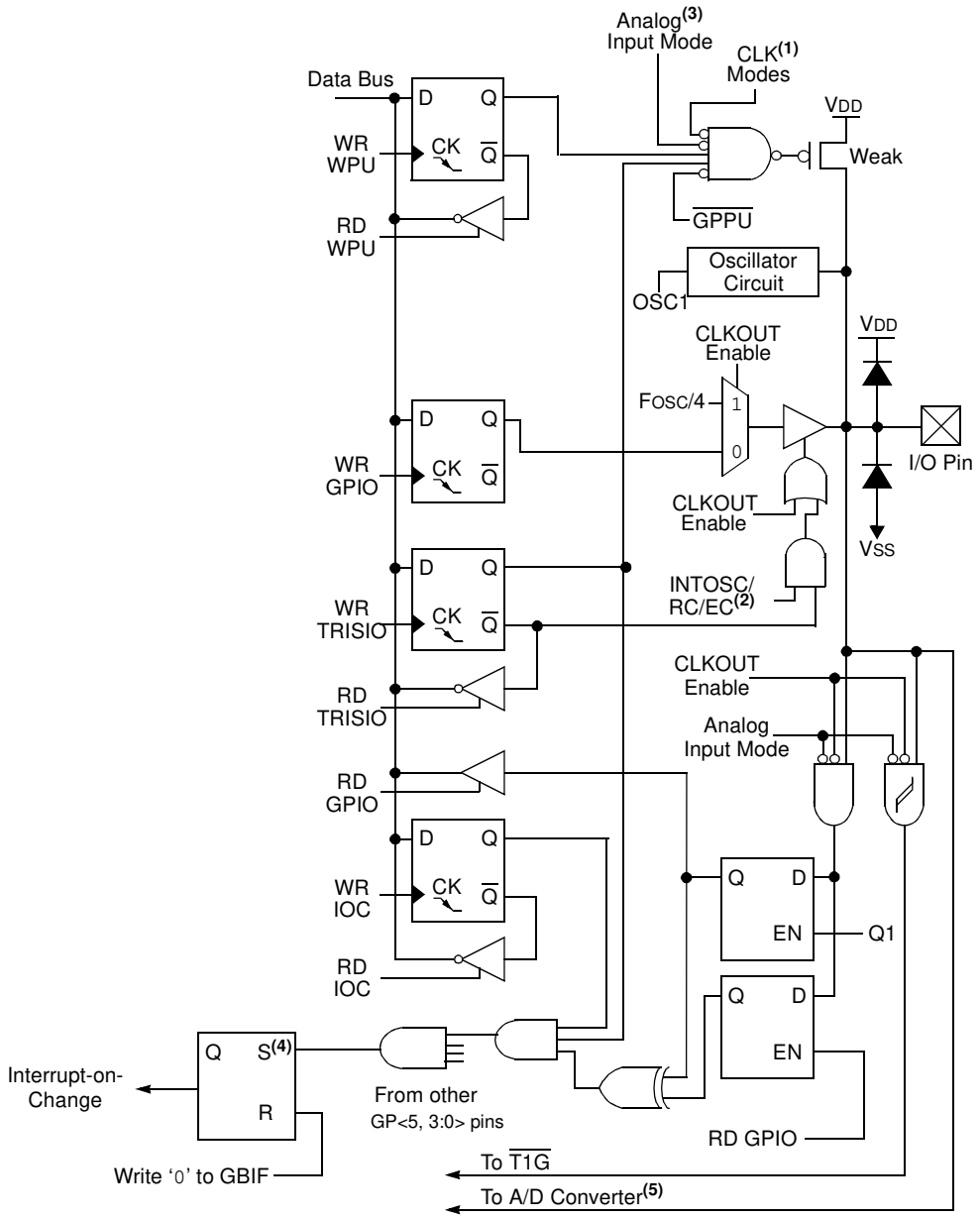
#### 5.2.4.5 GP4/AN3(2)/CIN1-/$\overline{\text{T1G}}$/P1B(1, 2)/OSC2/CLKOUT

Figure 5-4 shows the diagram for this pin. The GP4 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC(2)
- Comparator inverting input
- a Timer1 gate (count enable)
- PWM output, alternate pin(1, 2)
- a crystal/resonator connection
- a clock output

**Note 1:** Alternate pin function.
**2:** PIC12F615/617/HV615 only.

**FIGURE 5-4: BLOCK DIAGRAM OF GP4**




**Note 1:** CLK modes are XT, HS, LP, TMR1 LP and CLKOUT Enable.
**2:** With CLKOUT option.
**3:** Analog Input mode comes from ANSEL.
**4:** Set has priority over Reset.
**5:** PIC12F615/617/HV615 only.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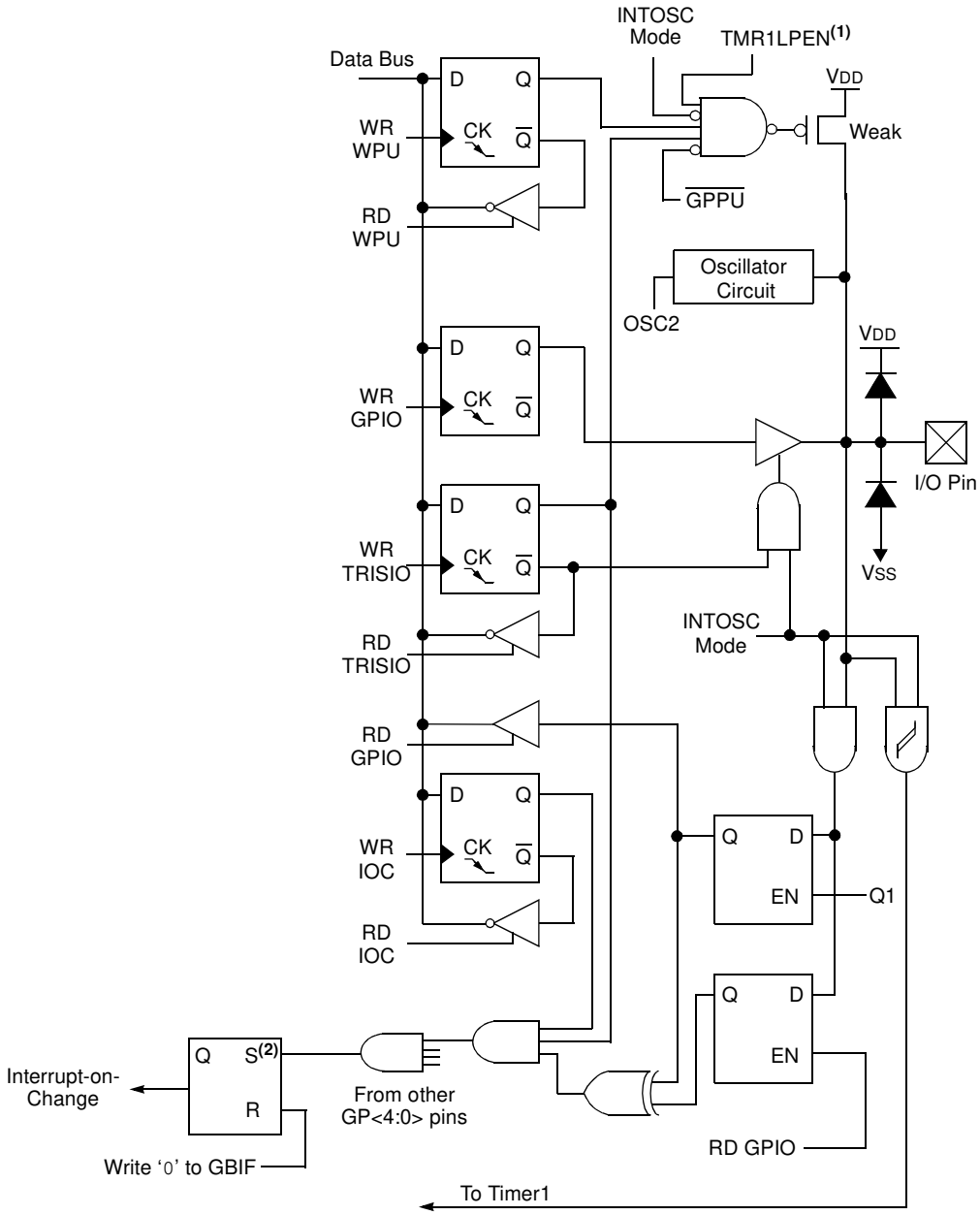
### 5.2.4.6 GP5/T1CKI/P1A(1, 2)/OSC1/CLKIN

Figure 5-5 shows the diagram for this pin. The GP5 pin is configurable to function as one of the following:

- a general purpose I/O
- a Timer1 clock input
- PWM output, alternate pin(1, 2)
- a crystal/resonator connection
- a clock input

**Note 1:** Alternate pin function.
**2:** PIC12F615/617/HV615 only.

**FIGURE 5-5: BLOCK DIAGRAM OF GP5**




**Note 1:** Timer1 LP Oscillator enabled.
**2:** Set has priority over Reset.

### TABLE 5-1: SUMMARY OF REGISTERS ASSOCIATED WITH GPIO

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| ANSEL | — | ADCS2(1) | ADCS1(1) | ADCS0(1) | ANS3 | ANS2(1) | ANS1 | ANS0 | -000 1111 | -000 1111 |
| CMCON0 | CMON | COUT | CMOE | CMPOL | — | CMR | — | CMCH | 0000 -0-0 | 0000 -0-0 |
| INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF | 0000 0000 | 0000 0000 |
| IOC | — | — | IOC5 | IOC4 | IOC3 | IOC2 | IOC1 | IOC0 | --00 0000 | --00 0000 |
| OPTION_REG | $\overline{\text{GPPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| GPIO | — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | --xx xxxx | --u0 u000 |
| TRISIO | — | — | TRISIO5 | TRISIO4 | TRISIO3 | TRISIO2 | TRISIO1 | TRISIO0 | --11 1111 | --11 1111 |
| WPU | — | — | WPU5 | WPU4 | WPU3 | WPU2 | WPU1 | WPU0 | --11 1111 | --11 -111 |
| T1CON | T1GINV | TMR1GE | TICKPS1 | T1CKPS0 | T1OSCEN | $\overline{\text{T1SYNC}}$ | TMR1CS | TMR1ON | 0000 0000 | uuuu uuuu |
| CCP1CON(1) | P1M | — | DC1B1 | DC1B0 | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 | 0-00 0000 | 0-00 0000 |
| APFCON(1) | — | — | — | T1GSEL | — | — | P1BSEL | P1ASEL | ---0 --00 | ---0 --00 |

**Legend:** x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by GPIO.
**Note 1:** PIC12F615/617/HV615 only.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## 6.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (shared with Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- Interrupt on overflow

Figure 6-1 is a block diagram of the Timer0 module.

### 6.1 Timer0 Operation

When used as a timer, the Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

#### 6.1.1 8-BIT TIMER MODE

When used as a timer, the Timer0 module will increment every instruction cycle (without prescaler). Timer mode is selected by clearing the T0CS bit of the OPTION register to '0'.

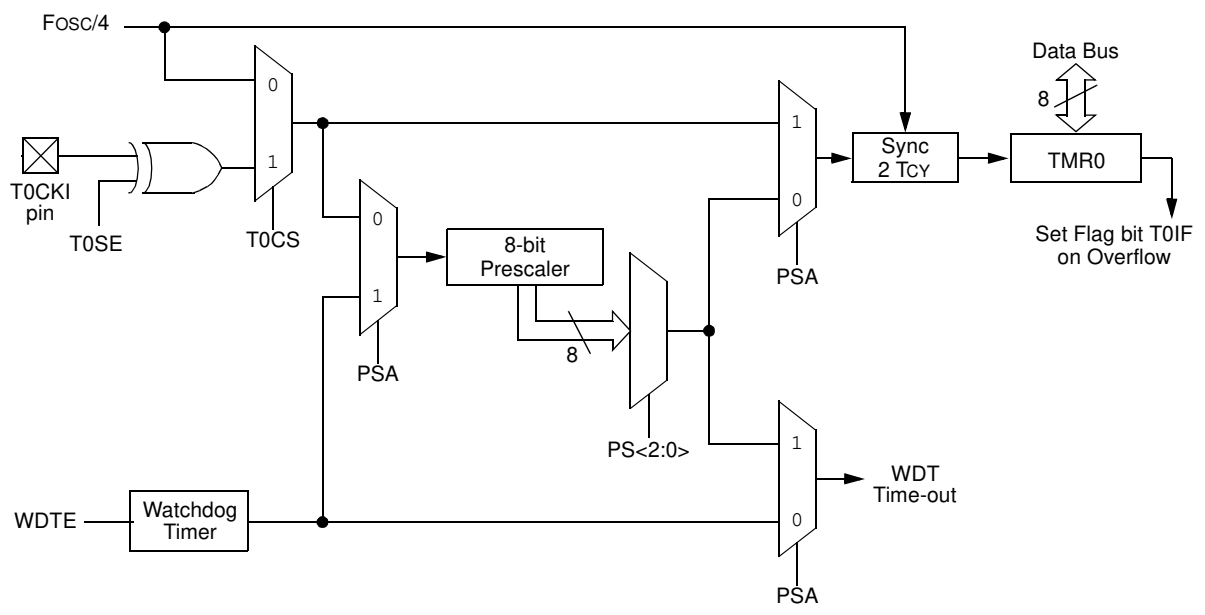
When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

| | |
|---|---|
| **Note:** | The value written to the TMR0 register can be adjusted, in order to account for the two instruction cycle delay when TMR0 is written. |

#### 6.1.2 8-BIT COUNTER MODE

When used as a counter, the Timer0 module will increment on every rising or falling edge of the T0CKI pin. The incrementing edge is determined by the T0SE bit of the OPTION register. Counter mode is selected by setting the T0CS bit of the OPTION register to '1'.

**FIGURE 6-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER**




**Note 1:** T0SE, T0CS, PSA, PS<2:0> are bits in the OPTION register.

**2:** WDTE bit is in the Configuration Word register.

### 6.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A single software programmable prescaler is available for use with either Timer0 or the Watchdog Timer (WDT), but not both simultaneously. The prescaler assignment is controlled by the PSA bit of the OPTION register. To assign the prescaler to Timer0, the PSA bit must be cleared to a '0'.

There are 8 prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be assigned to the WDT module.

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register will clear the prescaler.

When the prescaler is assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT.

#### 6.1.3.1 Switching Prescaler Between Timer0 and WDT Modules

As a result of having the prescaler assigned to either Timer0 or the WDT, it is possible to generate an unintended device Reset when switching prescaler values. When changing the prescaler assignment from Timer0 to the WDT module, the instruction sequence shown in Example 6-1, must be executed.

**EXAMPLE 6-1: CHANGING PRESCALER (TIMER0 → WDT)**

```
BANKSEL  TMR0            ;
CLRWDT                   ;Clear WDT
CLRF     TMR0            ;Clear TMR0 and
                         ;prescaler
BANKSEL  OPTION_REG      ;
BSF      OPTION_REG,PSA  ;Select WDT
CLRWDT                   ;
                         ;
MOVLW    b'11111000'     ;Mask prescaler
ANDWF    OPTION_REG,W    ;bits
IORLW    b'00000101'     ;Set WDT prescaler
MOVWF    OPTION_REG      ;to 1:32
```

When changing the prescaler assignment from the WDT to the Timer0 module, the following instruction sequence must be executed (see Example 6-2).

**EXAMPLE 6-2: CHANGING PRESCALER (WDT → TIMER0)**

```
CLRWDT                   ;Clear WDT and
                         ;prescaler
BANKSEL OPTION_REG       ;
MOVLW   b'11110000'      ;Mask TMR0 select and
ANDWF   OPTION_REG,W     ;prescaler bits
IORLW   b'00000011'      ;Set prescale to 1:16
MOVWF   OPTION_REG       ;
```

### 6.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from FFh to 00h. The T0IF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The T0IF bit must be cleared in software. The Timer0 interrupt enable is the T0IE bit of the INTCON register.

> **Note:** The Timer0 interrupt cannot wake the processor from Sleep since the timer is frozen during Sleep.

### 6.1.5 USING TIMER0 WITH AN EXTERNAL CLOCK

When Timer0 is in Counter mode, the synchronization of the T0CKI input and the Timer0 register is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, the high and low periods of the external clock source must meet the timing requirements as shown in **Section 16.0 "Electrical Specifications"**.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### REGISTER 6-1: OPTION_REG: OPTION REGISTER

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{GPPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **$\overline{\text{GPPU}}$:** GPIO Pull-up Enable bit
1 = GPIO pull-ups are disabled
0 = GPIO pull-ups are enabled by individual PORT latch values in WPU register

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of INT pin
0 = Interrupt on falling edge of INT pin

bit 5 **T0CS:** TMR0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (FOSC/4)

bit 4 **T0SE:** TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

| BIT VALUE | TMR0 RATE | WDT RATE |
|---|---|---|
| 000 | 1 : 2 | 1 : 1 |
| 001 | 1 : 4 | 1 : 2 |
| 010 | 1 : 8 | 1 : 4 |
| 011 | 1 : 16 | 1 : 8 |
| 100 | 1 : 32 | 1 : 16 |
| 101 | 1 : 64 | 1 : 32 |
| 110 | 1 : 128 | 1 : 64 |
| 111 | 1 : 256 | 1 : 128 |

### TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| TMR0 | Timer0 Module Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF | 0000 000x | 0000 000x |
| OPTION_REG | $\overline{\text{GPPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| TRISIO | — | — | TRISIO5 | TRISIO4 | TRISIO3 | TRISIO2 | TRISIO1 | TRISIO0 | --11 1111 | --11 1111 |

**Legend:** – = Unimplemented locations, read as ‘0’, u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

**NOTES:**


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## 7.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:

- 16-bit timer/counter register pair (TMR1H:TMR1L)
- Programmable internal or external clock source
- 3-bit prescaler
- Optional LP oscillator
- Synchronous or asynchronous operation
- Timer1 gate (count enable) via comparator or $\overline{\text{T1G}}$ pin
- Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Time base for the Capture/Compare function
- Special Event Trigger (with ECCP)
- Comparator output synchronization to Timer1 clock

Figure 7-1 is a block diagram of the Timer1 module.

### 7.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

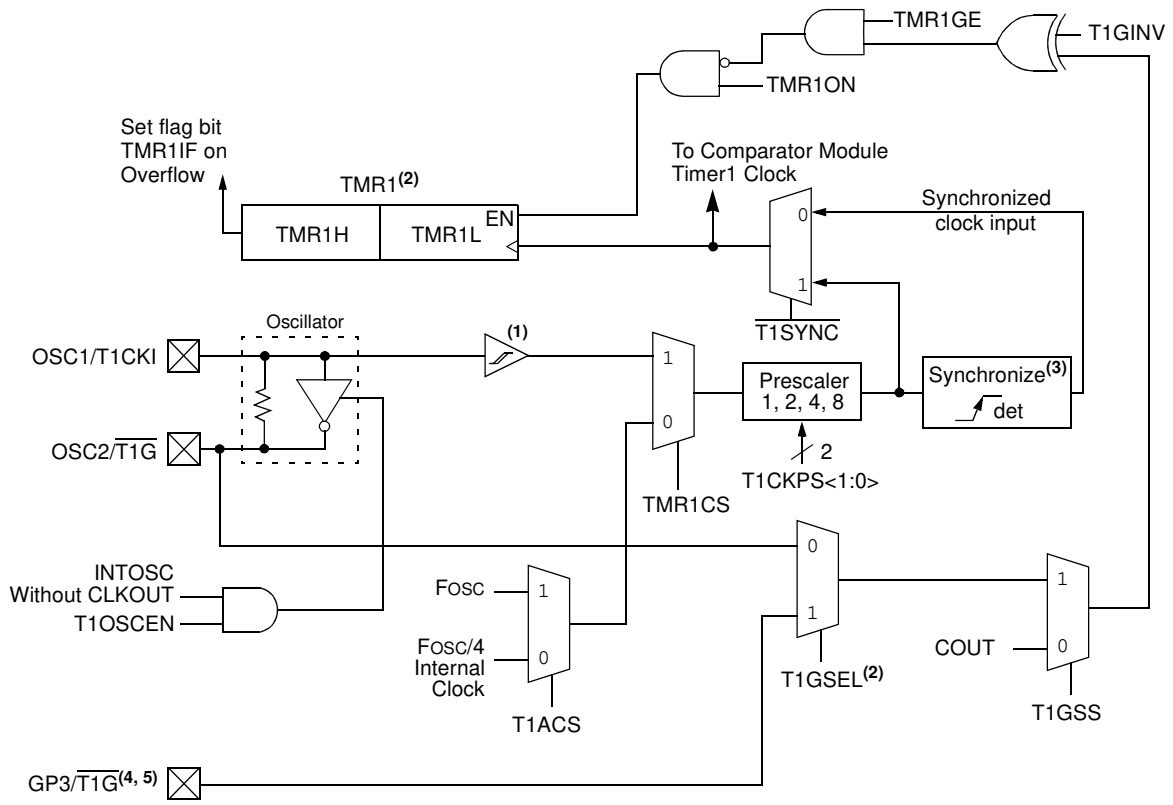
When used with an internal clock source, the module is a timer. When used with an external clock source, the module can be used as either a timer or counter.

### 7.2 Clock Source Selection

The TMR1CS bit of the T1CON register is used to select the clock source. When TMR1CS = 0, the clock source is FOSC/4. When TMR1CS = 1, the clock source is supplied externally.

| Clock Source | TMR1CS | T1ACS |
|---|---|---|
| FOSC/4 | 0 | 0 |
| FOSC | 0 | 1 |
| T1CKI pin | 1 | x |

**FIGURE 7-1: TIMER1 BLOCK DIAGRAM**




**Note 1:** ST Buffer is low power type when using LP oscillator, or high speed type when using T1CKI.
**2:** Timer1 register increments on rising edge.
**3:** Synchronize does not operate while in Sleep.
**4:** Alternate pin function.
**5:** PIC12F615/617/HV615 only.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### 7.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, the TMR1H:TMR1L register pair will increment on multiples of TCY as determined by the Timer1 prescaler.

### 7.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1 module may work as a timer or a counter.

When counting, Timer1 is incremented on the rising edge of the external clock input T1CKI. In addition, the Counter mode clock can be synchronized to the microcontroller system clock or run asynchronously.

If an external clock oscillator is needed (and the microcontroller is using the INTOSC without CLKOUT), Timer1 can use the LP oscillator as a clock source.

In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after one or more of the following conditions:

- Timer1 is enabled after POR or BOR Reset
- A write to TMR1H or TMR1L
- T1CKI is high when Timer1 is disabled and when Timer1 is re-enabled T1CKI is low. See Figure 7-2.

## 7.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

## 7.4 Timer1 Oscillator

A low-power 32.768 kHz crystal oscillator is built-in between pins OSC1 (input) and OSC2 (output). The oscillator is enabled by setting the T1OSCEN control bit of the T1CON register. The oscillator will continue to run during Sleep.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the primary system clock is derived from the internal oscillator or when in LP oscillator mode. The user must provide a software time delay to ensure proper oscillator start-up.

TRISIO5 and TRISIO4 bits are set when the Timer1 oscillator is enabled. GP5 and GP4 bits read as '0' and TRISIO5 and TRISIO4 bits read as '1'.

| | |
|---|---|
| **Note:** | The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1. |

## 7.5 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{\text{T1SYNC}}$ of the T1CON register is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 7.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

| | |
|---|---|
| **Note:** | When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce a single spurious increment. |

| | |
|---|---|
| **Note:** | In asynchronous counter mode or when using the internal oscillator and T1ACS=1, Timer1 can not be used as a time base for the capture or compare modes of the ECCP module (for PIC12F615/617/HV615 only). |

### 7.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TTMR1L register pair.

## 7.6 Timer1 Gate

Timer1 gate source is software configurable to be the $\overline{T1G}$ pin (or the alternate $\overline{T1G}$ pin) or the output of the Comparator. This allows the device to directly time external events using $\overline{T1G}$ or analog events using the Comparator. See the CMCON1 Register (Register 9-2) for selecting the Timer1 gate source. This feature can simplify the software for a Delta-Sigma A/D converter and many other applications. For more information on Delta-Sigma A/D converters, see the Microchip web site (www.microchip.com).

| | |
|---|---|
| **Note:** | TMR1GE bit of the T1CON register must be set to use either $\overline{T1G}$ or COUT as the Timer1 gate source. See Register 9-2 for more information on selecting the Timer1 gate source. |

Timer1 gate can be inverted using the T1GINV bit of the T1CON register, whether it originates from the $\overline{T1G}$ pin or the Comparator output. This configures Timer1 to measure either the active-high or active-low time between events.

## 7.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- Timer1 interrupt enable bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

| | |
|---|---|
| **Note:** | The TMR1H:TTMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts. |

## 7.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set

The device will wake-up on an overflow and execute the next instruction. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine (0004h).

## 7.9 ECCP Capture/Compare Time Base (PIC12F615/617/HV615 only)

The ECCP module uses the TMR1H:TMR1L register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMR1H:TMR1L register pair is copied into the CCPR1H:CCPR1L register pair on a configured event.

In Compare mode, an event is triggered when the value CCPR1H:CCPR1L register pair matches the value in the TMR1H:TMR1L register pair. This event can be a Special Event Trigger.

For more information, see **Section 11.0 “Enhanced Capture/Compare/PWM (With Auto-Shutdown and Dead Band) Module (PIC12F615/617/HV615 only)”**.


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## 7.10 ECCP Special Event Trigger (PIC12F615/617/HV615 only)

If a ECCP is configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The ECCP module may still be configured to generate a ECCP interrupt.

In this mode of operation, the CCPR1H:CCPR1L register pair effectively becomes the period register for Timer1.

Timer1 should be synchronized to the FOSC to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the ECCP, the write will take precedence.

For more information, see **Section 11.0 "Enhanced Capture/Compare/PWM (With Auto-Shutdown and Dead Band) Module (PIC12F615/617/HV615 only)"**.

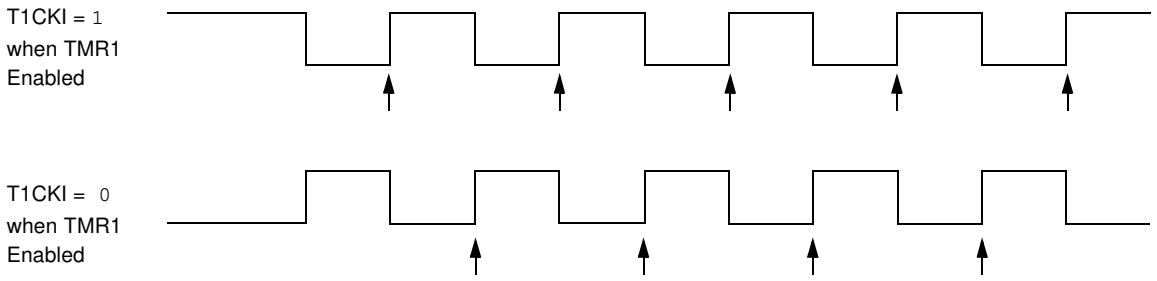
## 7.11 Comparator Synchronization

The same clock used to increment Timer1 can also be used to synchronize the comparator output. This feature is enabled in the Comparator module.

When using the comparator for Timer1 gate, the comparator output should be synchronized to Timer1. This ensures Timer1 does not miss an increment if the comparator changes.

For more information, see **Section 9.0 "Comparator Module"**.

**FIGURE 7-2: TIMER1 INCREMENTING EDGE**




**Note 1:** Arrows indicate counter increments.

**2:** In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

## 7.12 Timer1 Control Register

The Timer1 Control register (T1CON), shown in Register 7-1, is used to control Timer1 and select the various features of the Timer1 module.

### REGISTER 7-1: T1CON: TIMER 1 CONTROL REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| T1GINV(1) | TMR1GE(2) | T1CKPS1 | T1CKPS0 | T1OSCEN | $\overline{\text{T1SYNC}}$ | TMR1CS | TMR1ON |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **T1GINV:** Timer1 Gate Invert bit(1)
1 = Timer1 gate is active-high (Timer1 counts when gate is high)
0 = Timer1 gate is active-low (Timer1 counts when gate is low)

bit 6 **TMR1GE:** Timer1 Gate Enable bit(2)
If TMR1ON = 0:
This bit is ignored
If TMR1ON = 1:
1 = Timer1 is on if Timer1 gate is active
0 = Timer1 is on

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale Value
10 = 1:4 Prescale Value
01 = 1:2 Prescale Value
00 = 1:1 Prescale Value

bit 3 **T1OSCEN:** LP Oscillator Enable Control bit
If INTOSC without CLKOUT oscillator is active:
1 = LP oscillator is enabled for Timer1 clock
0 = LP oscillator is off
For all other system clock modes:
This bit is ignored. LP oscillator is disabled.

bit 2 **T1SYNC:** Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from T1CKI pin (on the rising edge)
0 = Internal clock (FOSC/4) or system clock (FOSC)(3)

bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

**Note 1:** T1GINV bit inverts the Timer1 gate logic, regardless of source.
**2:** TMR1GE bit must be set to use either $\overline{\text{T1G}}$ pin or COUT, as selected by the T1GSS bit of the CMCON1 register, as a Timer1 gate source.
**3:** See T1ACS bit in CMCON1 register.


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**TABLE 7-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| APFCON(1) | — | — | — | T1GSEL | — | — | P1BSEL | P1ASEL | ---0 --00 | ---0 --00 |
| CMCON0 | CMON | COUT | CMOE | CMPOL | — | CMR | — | CMCH | 0000 -0-0 | 0000 -0-0 |
| CMCON1 | — | — | — | T1ACS | CMHYS | — | T1GSS | CMSYNC | ---0 0-10 | ---0 0-10 |
| INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF | 0000 000x | 0000 000x |
| PIE1 | — | ADIE(1) | CCP1IE(1) | — | CMIE | — | TMR2IE(1) | TMR1IE | -00- 0-00 | -00- 0-00 |
| PIR1 | — | ADIF(1) | CCP1IF(1) | — | CMIF | — | TMR2IF(1) | TMR1IF | -00- 0-00 | -00- 0-00 |
| TMR1H | Holding Register for the Most Significant Byte of the 16-bit TMR1 Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| TMR1L | Holding Register for the Least Significant Byte of the 16-bit TMR1 Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| T1CON | T1GINV | TMR1GE | T1CKPS1 | T1CKPS0 | T1OSCEN | $\overline{\text{T1SYNC}}$ | TMR1CS | TMR1ON | 0000 0000 | uuuu uuuu |

**Legend:** x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

**Note 1:** PIC12F615/617/HV615 only.

**NOTES:**


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## 8.0 TIMER2 MODULE (PIC12F615/617/HV615 ONLY)

The Timer2 module is an 8-bit timer with the following features:

- 8-bit timer register (TMR2)
- 8-bit period register (PR2)
- Interrupt on TMR2 match with PR2
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)

See Figure 8-1 for a block diagram of Timer2.

### 8.1 Timer2 Operation

The clock input to the Timer2 module is the system instruction clock (FOSC/4). The clock is fed into the Timer2 prescaler, which has prescale options of 1:1, 1:4 or 1:16. The output of the prescaler is then used to increment the TMR2 register.

The values of TMR2 and PR2 are constantly compared to determine when they match. TMR2 will increment from 00h until it matches the value in PR2. When a match occurs, two things happen:

- TMR2 is reset to 00h on the next increment cycle.
- The Timer2 postscaler is incremented

The match output of the Timer2/PR2 comparator is then fed into the Timer2 postscaler. The postscaler has postscale options of 1:1 to 1:16 inclusive. The output of the Timer2 postscaler is used to set the TMR2IF interrupt flag bit in the PIR1 register.

The TMR2 and PR2 registers are both fully readable and writable. On any Reset, the TMR2 register is set to 00h and the PR2 register is set to FFh.

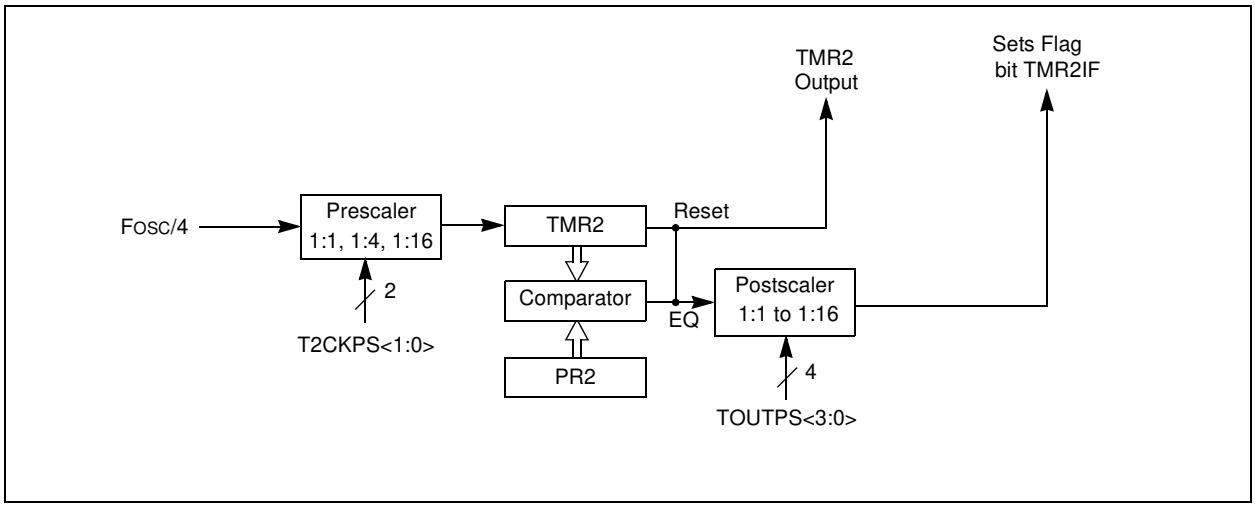
Timer2 is turned on by setting the TMR2ON bit in the T2CON register to a '1'. Timer2 is turned off by clearing the TMR2ON bit to a '0'.

The Timer2 prescaler is controlled by the T2CKPS bits in the T2CON register. The Timer2 postscaler is controlled by the TOUTPS bits in the T2CON register. The prescaler and postscaler counters are cleared when:

- A write to TMR2 occurs.
- A write to T2CON occurs.
- Any device Reset occurs (Power-on Reset, $\overline{\text{MCLR}}$ Reset, Watchdog Timer Reset, or Brown-out Reset).

**Note:** TMR2 is not cleared when T2CON is written.

**FIGURE 8-1: TIMER2 BLOCK DIAGRAM**



### REGISTER 8-1: T2CON: TIMER 2 CONTROL REGISTER

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | TOUTPS3 | TOUTPS2 | TOUTPS1 | TOUTPS0 | TMR2ON | T2CKPS1 | T2CKPS0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **Unimplemented:** Read as ‘0’

bit 6-3 **TOUTPS<3:0>:** Timer2 Output Postscaler Select bits
0000 =1:1 Postscaler
0001 =1:2 Postscaler
0010 =1:3 Postscaler
0011 =1:4 Postscaler
0100 =1:5 Postscaler
0101 =1:6 Postscaler
0110 =1:7 Postscaler
0111 =1:8 Postscaler
1000 =1:9 Postscaler
1001 =1:10 Postscaler
1010 =1:11 Postscaler
1011 =1:12 Postscaler
1100 =1:13 Postscaler
1101 =1:14 Postscaler
1110 =1:15 Postscaler
1111 =1:16 Postscaler

bit 2 **TMR2ON:** Timer2 On bit
1 = Timer2 is on
0 = Timer2 is off

bit 1-0 **T2CKPS<1:0>:** Timer2 Clock Prescale Select bits
00 =Prescaler is 1
01 =Prescaler is 4
1x =Prescaler is 16

### TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF | 0000 0000 | 0000 0000 |
| PIE1 | — | ADIE(1) | CCP1IE(1) | — | CMIE | — | TMR2IE(1) | TMR1IE | -00- 0-00 | -00- 0-00 |
| PIR1 | — | ADIF(1) | CCP1IF(1) | — | CMIF | — | TMR2IF(1) | TMR1IF | -00- 0-00 | -00- 0-00 |
| PR2(1) | Timer2 Module Period Register | | | | | | | | 1111 1111 | 1111 1111 |
| TMR2(1) | Holding Register for the 8-bit TMR2 Register | | | | | | | | 0000 0000 | 0000 0000 |
| T2CON(1) | — | TOUTPS3 | TOUTPS2 | TOUTPS1 | TOUTPS0 | TMR2ON | T2CKPS1 | T2CKPS0 | -000 0000 | -000 0000 |

**Legend:** x = unknown, u = unchanged, - = unimplemented read as ‘0’. Shaded cells are not used for Timer2 module.
**Note 1:** For PIC12F615/617/HV615 only.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## 9.0 COMPARATOR MODULE

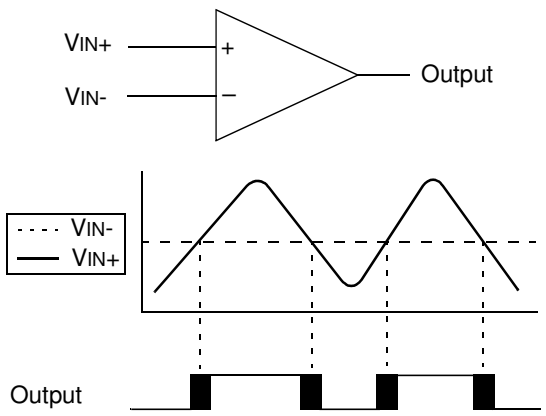
The comparator can be used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. The comparator is a very useful mixed signal building block because it provides analog functionality independent of the program execution. The Analog Comparator module includes the following features:

- Programmable input section
- Comparator output is available internally/externally
- Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- PWM shutdown
- Timer1 gate (count enable)
- Output synchronization to Timer1 clock input
- Programmable voltage reference
- User-enable Comparator Hysteresis

### 9.1 Comparator Overview

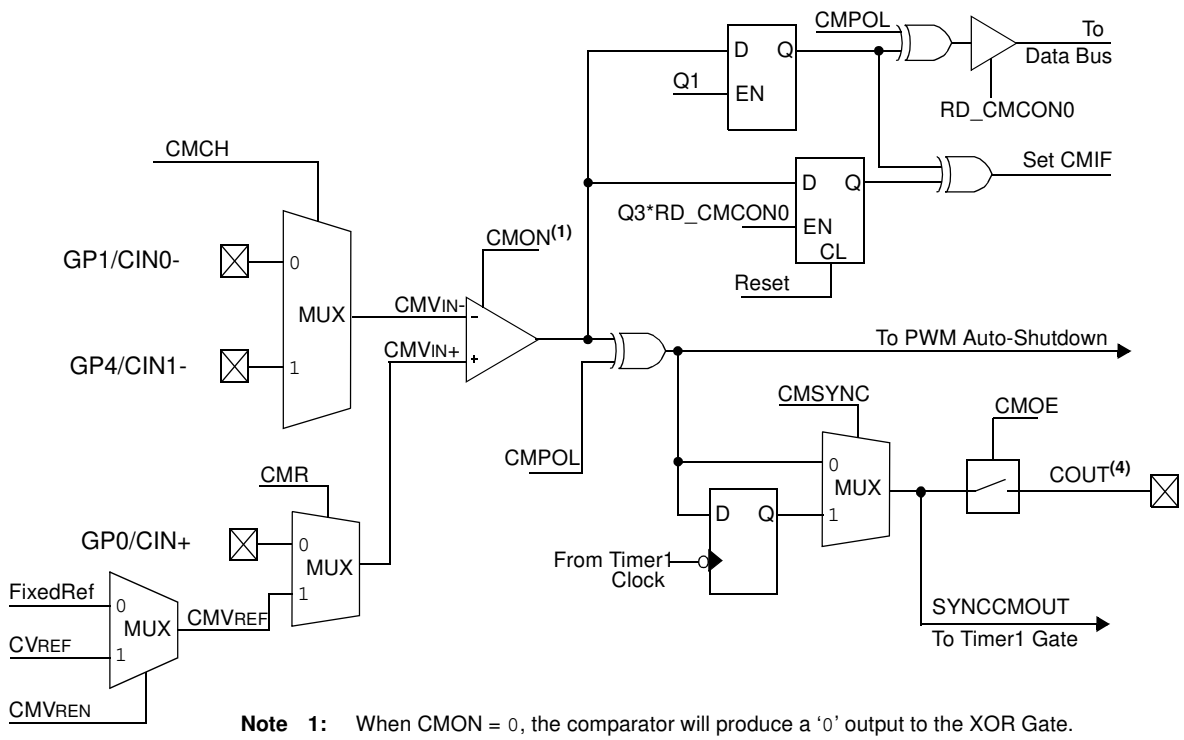
The comparator is shown in Figure 9-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

**FIGURE 9-1:SINGLE COMPARATOR**




**Note:** The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

**FIGURE 9-2: COMPARATOR SIMPLIFIED BLOCK DIAGRAM**




**Note 1:** When CMON = 0, the comparator will produce a '0' output to the XOR Gate.
**2:** Q1 and Q3 are phases of the four-phase system clock (FOSC).
**3:** Q1 is held high during Sleep mode.
**4:** Output shown for reference only. See I/O port pin diagram for more details.

## 9.2 Analog Input Connection Considerations

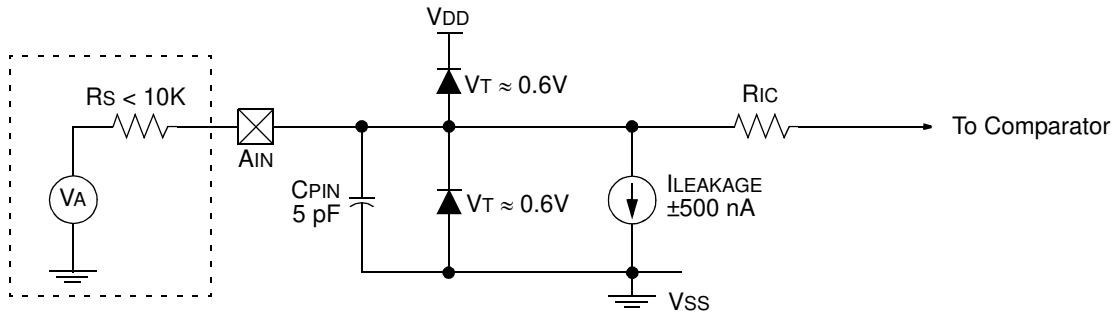
A simplified circuit for an analog input is shown in Figure 9-3. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to $V_{DD}$ and $V_{SS}$. The analog input, therefore, must be between $V_{SS}$ and $V_{DD}$. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of 10 kΩ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

**Note 1:** When reading a GPIO register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.

**2:** Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

**FIGURE 9-3: ANALOG INPUT MODEL**




**Legend:**
$C_{PIN}$ = Input Capacitance
$I_{LEAKAGE}$ = Leakage Current at the pin due to various junctions
$R_{IC}$ = Interconnect Resistance
$R_S$ = Source Impedance
$V_A$ = Analog Voltage
$V_T$ = Threshold Voltage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## 9.3 Comparator Control

The comparator has two control and Configuration registers: CMCON0 and CMCON1. The CMCON1 register is used for controlling the interaction with Timer1 and simultaneously reading the comparator output.

The CMCON0 register (Register 9-1) contain the control and Status bits for the following:

- Enable
- Input selection
- Reference selection
- Output selection
- Output polarity

### 9.3.1 COMPARATOR ENABLE

Setting the CMON bit of the CMCON0 register enables the comparator for operation. Clearing the CMON bit disables the comparator for minimum current consumption.

### 9.3.2 COMPARATOR INPUT SELECTION

The CMCH bit of the CMCON0 register directs one of four analog input pins to the comparator inverting input.

> **Note:** To use CIN+ and CIN- pins as analog inputs, the appropriate bits must be set in the ANSEL register and the corresponding TRIS bits must also be set to disable the output drivers.

### 9.3.3 COMPARATOR REFERENCE SELECTION

Setting the CMR bit of the CMxCON0 register directs an internal voltage reference or an analog input pin to the non-inverting input of the comparator. See **Section 9.10 "Comparator Voltage Reference"** for more information on the internal voltage reference module.

### 9.3.4 COMPARATOR OUTPUT SELECTION

The output of the comparator can be monitored by reading either the COUT bit of the CMCON0 register. In order to make the output available for an external connection, the following conditions must be true:

- CMOE bit of the CMxCON0 register must be set
- Corresponding TRIS bit must be cleared
- CMON bit of the CMCON0 register must be set.

> **Note 1:** The CMOE bit overrides the PORT data latch. Setting the CMON has no impact on the port override.
>
> **2:** The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

### 9.3.5 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CMPOL bit of the CMCON0 register. Clearing CMPOL results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 9-1.

**TABLE 9-1: OUTPUT STATE VS. INPUT CONDITIONS**

| Input Conditions | CMPOL | COUT |
|---|---|---|
| $CMV_{IN-} > CMV_{IN+}$ | 0 | 0 |
| $CMV_{IN-} < CMV_{IN+}$ | 0 | 1 |
| $CMV_{IN-} > CMV_{IN+}$ | 1 | 1 |
| $CMV_{IN-} < CMV_{IN+}$ | 1 | 0 |

**Note:** COUT refers to both the register bit and output pin.

## 9.4 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See **Section 16.0 "Electrical Specifications"** for more details.

## 9.5 Comparator Interrupt Operation

The comparator interrupt flag can be set whenever there is a change in the output value of the comparator. Changes are recognized by means of a mismatch circuit which consists of two latches and an exclusive-or gate (see Figure 9-4 and Figure 9-5). One latch is updated with the comparator output level when the CMCON0 register is read. This latch retains the value until the next read of the CMCON0 register or the occurrence of a Reset. The other latch of the mismatch circuit is updated on every Q1 system clock. A mismatch condition will occur when a comparator output change is clocked through the second latch on the Q1 clock cycle. At this point the two mismatch latches have opposite output levels which is detected by the exclusive-or gate and fed to the interrupt circuitry. The mismatch condition persists until either the CMCON0 register is read or the comparator output returns to the previous state.

> **Note 1:** A write operation to the CMCON0 register will also clear the mismatch condition because all writes include a read operation at the beginning of the write cycle.
>
> **2:** Comparator interrupts will operate correctly regardless of the state of CMOE.

The comparator interrupt is set by the mismatch edge and not the mismatch level. This means that the interrupt flag can be reset without the additional step of reading or writing the CMCON0 register to clear the mismatch registers. When the mismatch registers are cleared, an interrupt will occur upon the comparator's return to the previous state, otherwise no interrupt will be generated.

Software will need to maintain information about the status of the comparator output, as read from the CMCON1 register, to determine the actual change that has occurred.

The CMIF bit of the PIR1 register is the Comparator Interrupt flag. This bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, an interrupt can be generated.

The CMIE bit of the PIE1 register and the PEIE and GIE bits of the INTCON register must all be set to enable comparator interrupts. If any of these bits are cleared, the interrupt is not enabled, although the CMIF bit of the PIR1 register will still be set if an interrupt condition occurs.

**FIGURE 9-4: COMPARATOR INTERRUPT TIMING W/O CMCON0 READ**

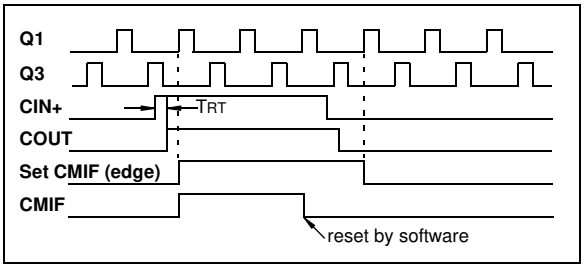
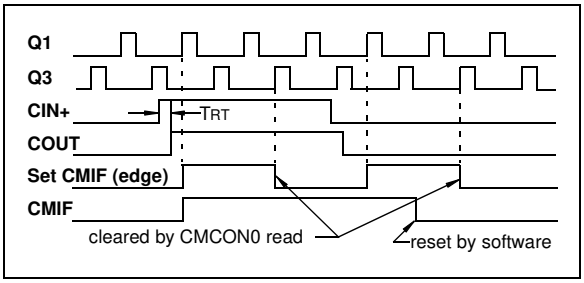



**FIGURE 9-5: COMPARATOR INTERRUPT TIMING WITH CMCON0 READ**




> **Note 1:** If a change in the CMCON0 register (COUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF of the PIR1 register interrupt flag may not get set.
>
> **2:** When a comparator is first enabled, bias circuitry in the comparator module may cause an invalid output from the comparator until the bias circuitry is stable. Allow about 1 μs for bias settling then clear the mismatch condition and interrupt flags before enabling comparator interrupts.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## 9.6 Operation During Sleep

The comparator, if enabled before entering Sleep mode, remains active during Sleep. The additional current consumed by the comparator is shown separately in the **Section 16.0 "Electrical Specifications"**. If the comparator is not used to wake the device, power consumption can be minimized while in Sleep mode by turning off the comparator. The comparator is turned off by clearing the CMON bit of the CMCON0 register.

A change to the comparator output can wake-up the device from Sleep. To enable the comparator to wake the device from Sleep, the CMIE bit of the PIE1 register and the PEIE bit of the INTCON register must be set. The instruction following the `SLEEP` instruction always executes following a wake from Sleep. If the GIE bit of the INTCON register is also set, the device will then execute the Interrupt Service Routine.

## 9.7 Effects of a Reset

A device Reset forces the CMCON1 register to its Reset state. This sets the comparator and the voltage reference to the OFF state.

### REGISTER 9-1: CMCON0: COMPARATOR CONTROL REGISTER 0

| R/W-0 | R-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CMON | COUT | CMOE | CMPOL | — | CMR | — | CMCH |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **CMON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 6 **COUT:** Comparator Output bit
If C1POL = 1 (inverted polarity):
COUT = 0 when $CMV_{IN+} > CMV_{IN-}$
COUT = 1 when $CMV_{IN+} < CMV_{IN-}$
If C1POL = 0 (non-inverted polarity):
COUT = 1 when $CMV_{IN+} > CMV_{IN-}$
COUT = 0 when $CMV_{IN+} < CMV_{IN-}$

bit 5 **CMOE:** Comparator Output Enable bit
1 = COUT is present on the COUT pin(1)
0 = COUT is internal only

bit 4 **CMPOL:** Comparator Output Polarity Select bit
1 = COUT logic is inverted
0 = COUT logic is not inverted

bit 3 **Unimplemented:** Read as ‘0’

bit 2 **CMR:** Comparator Reference Select bit (non-inverting input)
1 = $CMV_{IN+}$ connects to $CMV_{REF}$ output
0 = $CMV_{IN+}$ connects to CIN+ pin

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **CMCH:** Comparator C1 Channel Select bit
0 = $CMV_{IN-}$ pin of the Comparator connects to CIN0-
1 = $CMV_{IN-}$ pin of the Comparator connects to CIN1-

**Note 1:** Comparator output requires the following three conditions: CMOE = 1, CMON = 1 and corresponding port TRIS bit = 0.


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## 9.8 Comparator Gating Timer1

This feature can be used to time the duration or interval of analog events. Clearing the T1GSS bit of the CMCON1 register will enable Timer1 to increment based on the output of the comparator. This requires that Timer1 is on and gating is enabled. See **Section 7.0 "Timer1 Module with Gate Control"** for details.

It is recommended to synchronize the comparator with Timer1 by setting the CMSYNC bit when the comparator is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if the comparator changes during an increment.

## 9.9 Synchronizing Comparator Output to Timer1

The comparator output can be synchronized with Timer1 by setting the CMSYNC bit of the CMCON1 register. When enabled, the comparator output is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 9-2) and the Timer1 Block Diagram (Figure 7-1) for more information.

**REGISTER 9-2: CMCON1: COMPARATOR CONTROL REGISTER 1**

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | T1ACS | CMHYS | — | T1GSS | CMSYNC |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **T1ACS:** Timer1 Alternate Clock Select bit
1 = Timer 1 Clock Source is System Clock (FOSC)
0 = Timer 1 Clock Source is Instruction Clock (FOSC\4)

bit 3 **CMHYS:** Comparator Hysteresis Select bit
1 = Comparator Hysteresis enabled
0 = Comparator Hysteresis disabled

bit 2 **Unimplemented:** Read as '0'

bit 1 **T1GSS:** Timer1 Gate Source Select bit(1)
1 = Timer 1 Gate Source is $\overline{T1G}$ pin (pin should be configured as digital input)
0 = Timer 1 Gate Source is comparator output

bit 0 **CMSYNC:** Comparator Output Synchronization bit(2)
1 = Output is synchronized with falling edge of Timer1 clock
0 = Output is asynchronous

**Note 1:** Refer to **Section 7.6 "Timer1 Gate"**.
**2:** Refer to Figure 9-2.

## 9.10 Comparator Voltage Reference

The Comparator Voltage Reference module provides an internally generated voltage reference for the comparators. The following features are available:

- Independent from Comparator operation
- 16-level voltage range
- Output clamped to VSS
- Ratiometric with VDD
- Fixed Reference (0.6)

The VRCON register (Register 9-3) controls the Voltage Reference module shown in Register 9-6.

### 9.10.1 INDEPENDENT OPERATION

The comparator voltage reference is independent of the comparator configuration. Setting the VREN bit of the VRCON register will enable the voltage reference.

### 9.10.2 OUTPUT VOLTAGE SELECTION

The CVREF voltage reference has 2 ranges with 16 voltage levels in each range. Range selection is controlled by the VRR bit of the VRCON register. The 16 levels are set with the VR<3:0> bits of the VRCON register.

The CVREF output voltage is determined by the following equations:

**EQUATION 9-1: CVREF OUTPUT VOLTAGE**

$$V_{RR} = 1 \text{ (low range):}$$
$$CV_{REF} = (VR<3:0>/24) \times V_{DD}$$
$$V_{RR} = 0 \text{ (high range):}$$
$$CV_{REF} = (V_{DD}/4) + (VR<3:0> \times V_{DD}/32)$$

The full range of VSS to VDD cannot be realized due to the construction of the module. See Figure 9-6.

### 9.10.3 OUTPUT CLAMPED TO VSS

The CVREF output voltage can be set to Vss with no power consumption by configuring VRCON as follows:

- FVREN = 0

This allows the comparator to detect a zero-crossing while not consuming additional CVREF module current.

### 9.10.4 OUTPUT RATIOMETRIC TO VDD

The comparator voltage reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the Comparator Voltage Reference can be found in **Section 16.0 “Electrical Specifications”**.

### 9.10.5 FIXED VOLTAGE REFERENCE

The fixed voltage reference is independent of VDD, with a nominal output voltage of 0.6V. This reference can be enabled by setting the FVREN bit of the VRCON register to ‘1’. This reference is always enabled when the HFINTOSC oscillator is active.

### 9.10.6 FIXED VOLTAGE REFERENCE STABILIZATION PERIOD

When the Fixed Voltage Reference module is enabled, it will require some time for the reference and its amplifier circuits to stabilize. The user program must include a small delay routine to allow the module to settle. See **Section 16.0 “Electrical Specifications”** for the minimum delay requirement.

### 9.10.7 VOLTAGE REFERENCE SELECTION

Multiplexers on the output of the Voltage Reference module enable selection of either the CVREF or fixed voltage reference for use by the comparators.

Setting the CMVREN bit of the VRCON register enables current to flow in the CVREF voltage divider and selects the CVREF voltage for use by the Comparator. Clearing the CMVREN bit selects the fixed voltage for use by the Comparator.

When the CMVREN bit is cleared, current flow in the CVREF voltage divider is disabled minimizing the power drain of the voltage reference peripheral.


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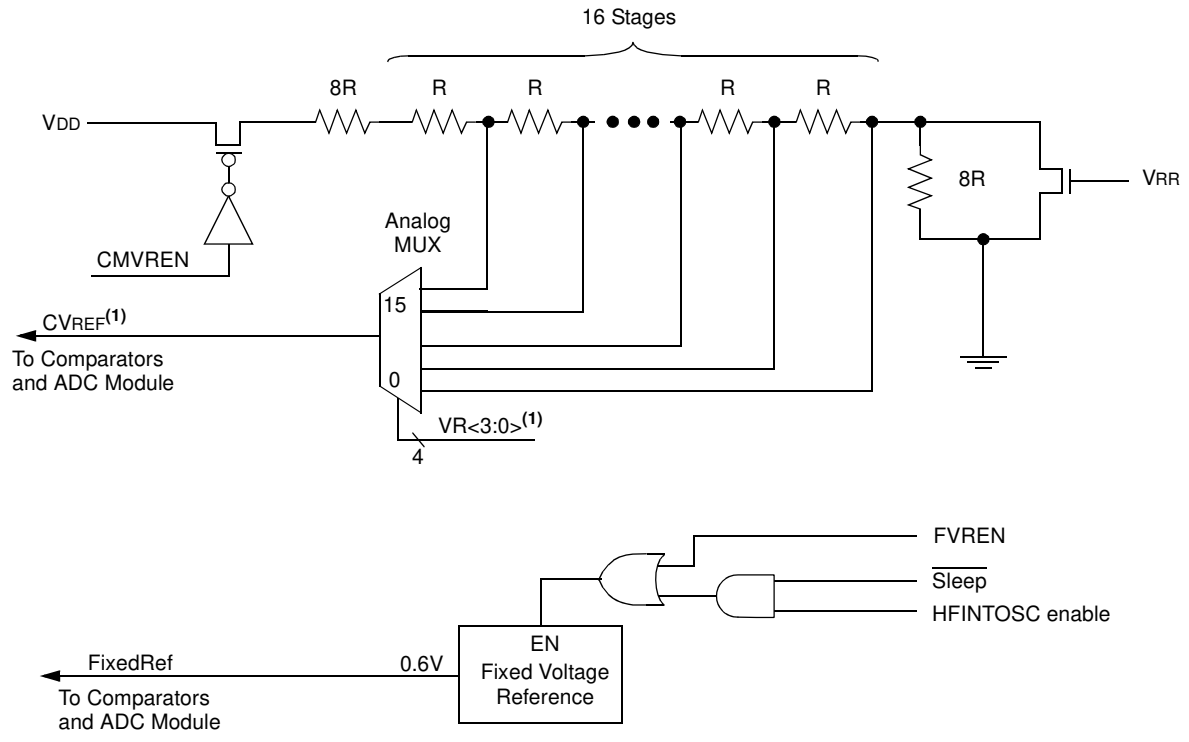
**FIGURE 9-6: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM**




**Note 1:** Care should be taken to ensure CVREF remains within the comparator common mode input range. See **Section 16.0 "Electrical Specifications"** for more detail.

### REGISTER 9-3: VRCON: VOLTAGE REFERENCE CONTROL REGISTER

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CMVREN | — | VRR | FVREN | VR3 | VR2 | VR1 | VR0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **CMVREN:** Comparator Voltage Reference Enable bit(1, 2)
1 = CVREF circuit powered on and routed to CVREF input of the Comparator
0 = 0.6 Volt constant reference routed to CVREF input of the Comparator

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **VRR:** CVREF Range Selection bit
1 = Low range
0 = High range

bit 4 **FVREN:** 0.6V Reference Enable bit(2)
1 = Enabled
0 = Disabled

bit 3-0 **VR<3:0>:** Comparator Voltage Reference CVREF Value Selection bits ($0 \leq$ VR<3:0> $\leq 15$)
When VRR = 1: CVREF = (VR<3:0>/24) * VDD
When VRR = 0: CVREF = VDD/4 + (VR<3:0>/32) * VDD

**Note 1:** When CMVREN is low, the CVREF circuit is powered down and does not contribute to IDD current.
**2:** When CMVREN is low and the FVREN bit is low, the CVREF signal should provide Vss to the comparator.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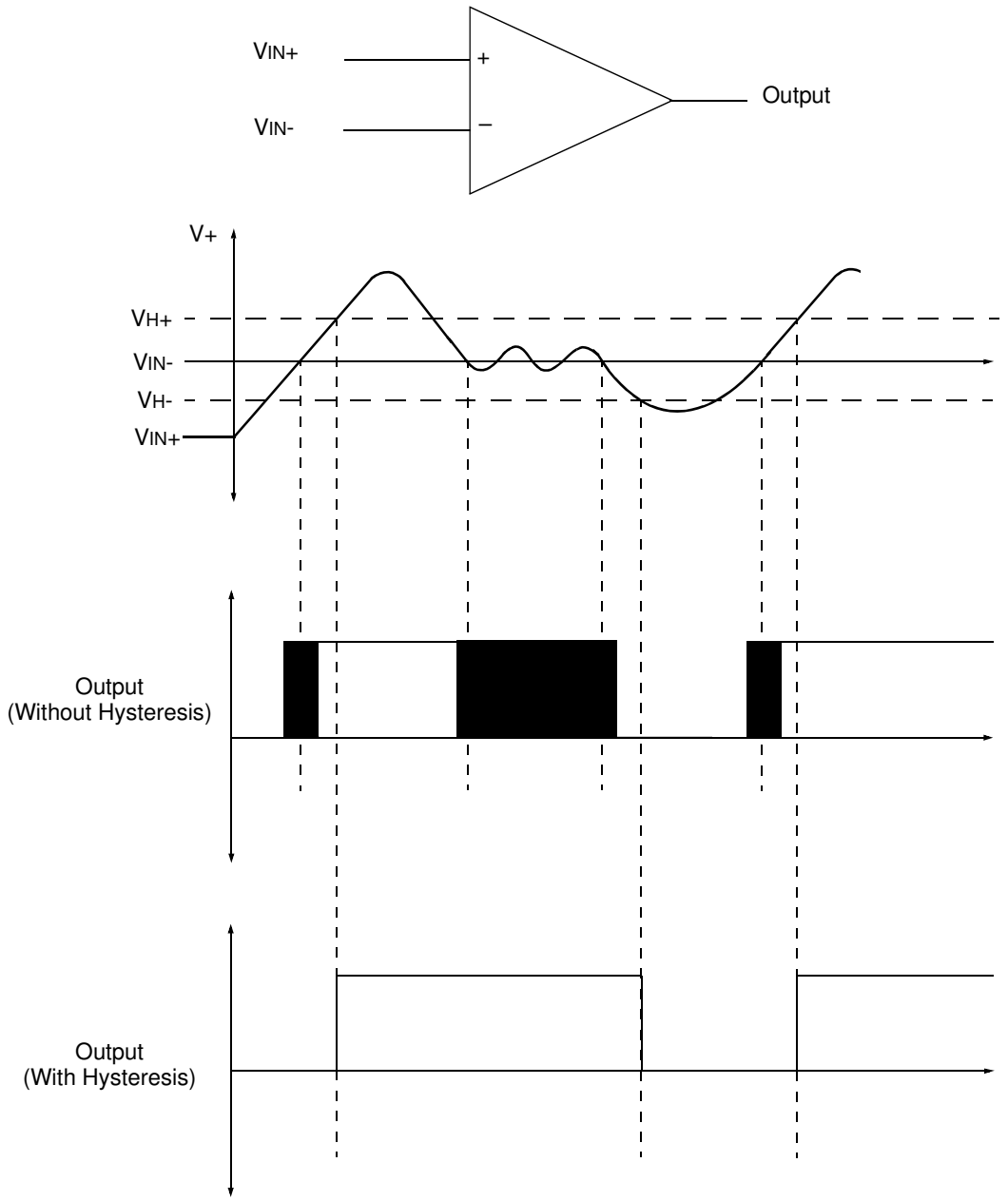
## 9.11 Comparator Hysteresis

Each comparator has built-in hysteresis that is user enabled by setting the CMHYS bit of the CMCON1 register. The hysteresis feature can help filter noise and reduce multiple comparator output transitions when the output is changing state.

Figure 9-7 shows the relationship between the analog input levels and digital output of a comparator with and without hysteresis. The output of the comparator changes from a low state to a high state only when the analog voltage at $V_{IN+}$ rises above the upper hysteresis threshold ($V_{H+}$). The output of the comparator changes from a high state to a low state only when the analog voltage at $V_{IN+}$ falls below the lower hysteresis threshold ($V_{H-}$).

**FIGURE 9-7: COMPARATOR HYSTERESIS**




**Note:** The black areas of the comparator output represents the uncertainty due to input offsets and response time.

**TABLE 9-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE COMPARATOR AND VOLTAGE REFERENCE MODULES**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| ANSEL | — | ADCS2(1) | ADCS1(1) | ADCS0(1) | ANS3 | ANS2(1) | ANS1 | ANS0 | -000 1111 | -000 1111 |
| CMCON0 | CMON | COUT | CMOE | CMPOL | — | CMR | — | CMCH | 0000 -000 | 0000 -000 |
| CMCON1 | — | — | — | T1ACS | CMHYS | — | T1GSS | CMSYNC | 0000 0000 | 0000 0000 |
| INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF | 0000 000x | 0000 000x |
| PIE1 | — | ADIE(1) | CCP1IE(1) | — | CMIE | — | TMR2IE(1) | TMR1IE | -00- 0-00 | -00- 0-00 |
| PIR1 | — | ADIF(1) | CCP1IF(1) | — | CMIF | — | TMR2IF(1) | TMR1IF | -00- 0-00 | -00- 0-00 |
| GPIO | — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | --xx xxxx | --uu uuuu |
| TRISIO | — | — | TRISIO5 | TRISIO4 | TRISIO3 | TRISIO2 | TRISIO1 | TRISIO0 | --11 1111 | --11 1111 |
| VRCON | CMVREN | — | VRR | FVREN | VR3 | VR2 | VR1 | VR0 | 0-00 0000 | 0-00 0000 |

**Legend:** x = unknown, u = unchanged, — = unimplemented, read as '0'. Shaded cells are not used for comparator.

**Note 1:** For PIC12F615/617/HV615 only.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## 10.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE (PIC12F615/617/HV615 ONLY)

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESL and ADRESH).

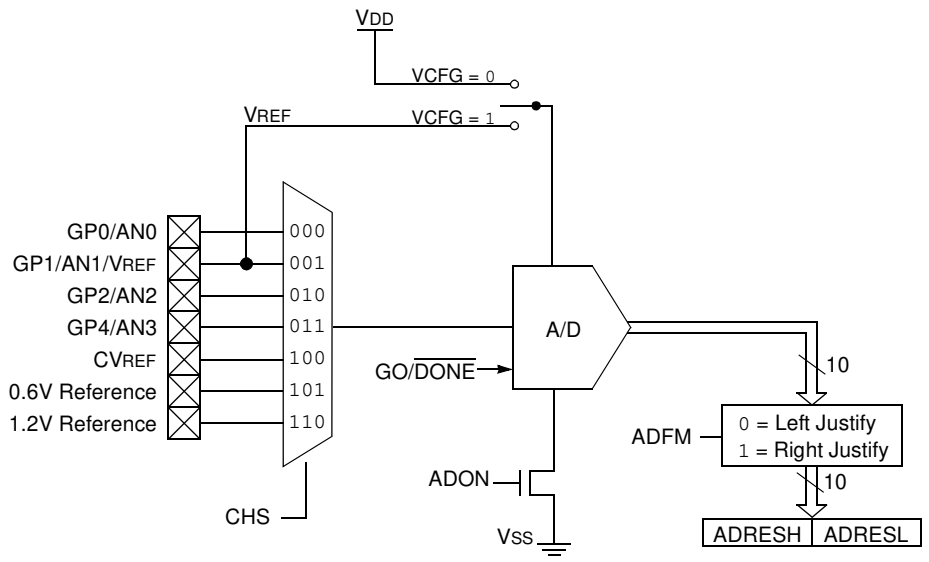
The ADC voltage reference is software selectable to either VDD or a voltage applied to the external reference pins.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

Figure 10-1 shows the block diagram of the ADC.

**Note:** The ADRESL and ADRESH registers are Read Only.

**FIGURE 10-1: ADC BLOCK DIAGRAM**



## 10.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- Port configuration
- Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Results formatting

### 10.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. See the corresponding port section for more information.

| | |
|---|---|
| **Note:** | Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current. |

### 10.1.2 CHANNEL SELECTION

The CHS bits of the ADCON0 register determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to **Section 10.2 "ADC Operation"** for more information.

### 10.1.3 ADC VOLTAGE REFERENCE

The VCFG bit of the ADCON0 register provides control of the positive voltage reference. The positive voltage reference can be either VDD or an external voltage source. The negative voltage reference is always connected to the ground reference.

### 10.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ANSEL register. There are seven possible clock options:

- FOSC/2
- FOSC/4
- FOSC/8
- FOSC/16
- FOSC/32
- FOSC/64
- FRC (dedicated internal oscillator)

The time to complete one bit conversion is defined as TAD. One full 10-bit conversion requires 11 TAD periods as shown in Figure 10-3.

For correct conversion, the appropriate TAD specification must be met. See A/D conversion requirements in **Section 16.0 "Electrical Specifications"** for more information. Table 10-1 gives examples of appropriate ADC clock selections.

| | |
|---|---|
| **Note:** | Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result. |


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**TABLE 10-1: ADC CLOCK PERIOD (TAD) VS. DEVICE OPERATING FREQUENCIES (VDD ≥ 3.0V)**

| ADC Clock Period (TAD) | | Device Frequency (FOSC) | | | |
|---|---|---|---|---|---|
| **ADC Clock Source** | **ADCS<2:0>** | **20 MHz** | **8 MHz** | **4 MHz** | **1 MHz** |
| FOSC/2 | 000 | 100 ns(2) | 250 ns(2) | 500 ns(2) | 2.0 μs |
| FOSC/4 | 100 | 200 ns(2) | 500 ns(2) | 1.0 μs(2) | 4.0 μs |
| FOSC/8 | 001 | 400 ns(2) | 1.0 μs(2) | 2.0 μs | 8.0 μs(3) |
| FOSC/16 | 101 | 800 ns(2) | 2.0 μs | 4.0 μs | 16.0 μs(3) |
| FOSC/32 | 010 | 1.6 μs | 4.0 μs | 8.0 μs(3) | 32.0 μs(3) |
| FOSC/64 | 110 | 3.2 μs | 8.0 μs(3) | 16.0 μs(3) | 64.0 μs(3) |
| FRC | x11 | 2-6 μs(1,4) | 2-6 μs(1,4) | 2-6 μs(1,4) | 2-6 μs(1,4) |

**Legend:** Shaded cells are outside of recommended range.

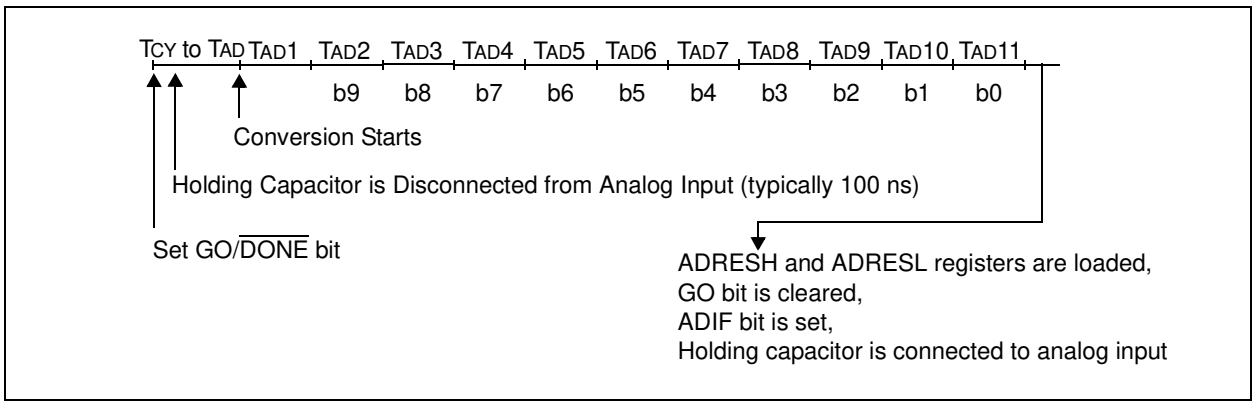
**Note 1:** The FRC source has a typical TAD time of 4 μs for VDD > 3.0V.

**2:** These values violate the minimum required TAD time.

**3:** For faster conversion times, the selection of another clock source is recommended.

**4:** When the device frequency is greater than 1 MHz, the FRC clock source is only recommended if the conversion will be performed during Sleep.

**FIGURE 10-2: ANALOG-TO-DIGITAL CONVERSION TAD CYCLES**




### 10.1.5 INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC interrupt flag is the ADIF bit in the PIR1 register. The ADC interrupt enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

| **Note:** | The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled. |
|---|---|

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the global interrupt must be disabled. If the global interrupt is enabled, execution will switch to the Interrupt Service Routine.

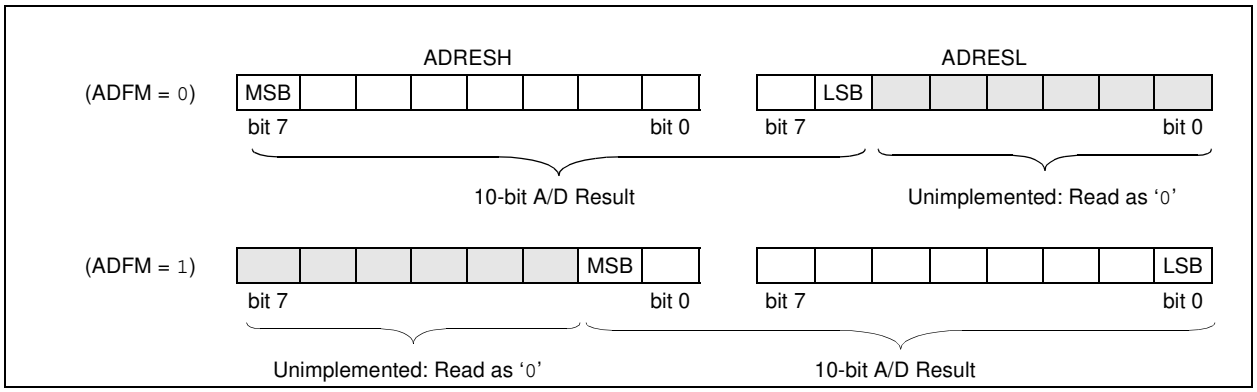
Please see **Section 10.1.5 "Interrupts"** for more information.

### 10.1.6 RESULT FORMATTING

The 10-bit A/D conversion result can be supplied in two formats, left justified or right justified. The ADFM bit of the ADCON0 register controls the output format.

Figure 10-4 shows the two output formats.

**FIGURE 10-3: 10-BIT A/D CONVERSION RESULT FORMAT**




## 10.2 ADC Operation

### 10.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. Setting the GO/$\overline{\text{DONE}}$ bit of the ADCON0 register to a '1' will start the Analog-to-Digital conversion.

| | |
|---|---|
| **Note:** | The GO/$\overline{\text{DONE}}$ bit should not be set in the same instruction that turns on the ADC. Refer to **Section 10.2.6 "A/D Conversion Procedure"**. |

### 10.2.2 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/$\overline{\text{DONE}}$ bit
- Set the ADIF flag bit
- Update the ADRESH:ADRESL registers with new conversion result

### 10.2.3 TERMINATING A CONVERSION

If a conversion must be terminated before completion, the GO/$\overline{\text{DONE}}$ bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete Analog-to-Digital conversion sample. Instead, the ADRESH:ADRESL register pair will retain the value of the previous conversion. Additionally, a 2 TAD delay is required before another acquisition can be initiated. Following this delay, an input acquisition is automatically started on the selected channel.

| | |
|---|---|
| **Note:** | A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated. |

### 10.2.4 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC clock source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

### 10.2.5 SPECIAL EVENT TRIGGER

The ECCP Special Event Trigger allows periodic ADC measurements without software intervention. When this trigger occurs, the GO/$\overline{\text{DONE}}$ bit is set by hardware and the Timer1 counter resets to zero.

Using the Special Event Trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

See **Section 11.0 "Enhanced Capture/Compare/PWM (With Auto-Shutdown and Dead Band) Module (PIC12F615/617/HV615 only)"** for more information.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### 10.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
   - Disable pin output driver (See TRIS register)
   - Configure pin as analog
2. Configure the ADC module:
   - Select ADC conversion clock
   - Configure voltage reference
   - Select ADC input channel
   - Select result format
   - Turn on ADC module
3. Configure ADC interrupt (optional):
   - Clear ADC interrupt flag
   - Enable ADC interrupt
   - Enable peripheral interrupt
   - Enable global interrupt(1)
4. Wait the required acquisition time(2).
5. Start conversion by setting the GO/$\overline{\text{DONE}}$ bit.
6. Wait for ADC conversion to complete by one of the following:
   - Polling the GO/$\overline{\text{DONE}}$ bit
   - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result
8. Clear the ADC interrupt flag (required if interrupt is enabled).

**Note 1:** The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

**2:** See **Section 10.3 "A/D Acquisition Requirements"**.

**EXAMPLE 10-1: A/D CONVERSION**

```
;This code block configures the ADC
;for polling, Vdd reference, Frc clock
;and GP0 input.
;
;Conversion start & polling for completion
; are included.
;
BANKSEL  TRISIO       ;
BSF      TRISIO,0     ;Set GP0 to input
BANKSEL  ANSEL        ;
MOVLW    B'01110001'  ;ADC Frc clock,
IORWF    ANSEL        ; and GP0 as analog
BANKSEL  ADCON0       ;
MOVLW    B'10000001'  ;Right justify,
MOVWF    ADCON0       ;Vdd Vref, AN0, On
CALL     SampleTime   ;Acquisiton delay
BSF      ADCON0,GO    ;Start conversion
BTFSC    ADCON0,GO    ;Is conversion done?
GOTO     $-1          ;No, test again
BANKSEL  ADRESH       ;
MOVF     ADRESH,W     ;Read upper 2 bits
MOVWF    RESULTHI     ;Store in GPR space
BANKSEL  ADRESL       ;
MOVF     ADRESL,W     ;Read lower 8 bits
MOVWF    RESULTLO     ;Store in GPR space
```

### 10.2.7 ADC REGISTER DEFINITIONS

The following registers are used to control the operation of the ADC.

**REGISTER 10-1: ADCON0: A/D CONTROL REGISTER 0**

| R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADFM | VCFG | — | CHS2 | CHS1 | CHS0 | GO/$\overline{\text{DONE}}$ | ADON |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **ADFM:** A/D Conversion Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **VCFG:** Voltage Reference bit
1 = $V_{REF}$ pin
0 = $V_{DD}$

bit 5 **Unimplemented:** Read as ‘0’

bit 4-2 **CHS<2:0>: Analog Channel Select bits**
000 = Channel 00 (AN0)
001 = Channel 01 (AN1)
010 = Channel 02 (AN2)
011 = Channel 03 (AN3)
100 = $CV_{REF}$
101 = 0.6V Reference
110 = 1.2V Reference
111 = Reserved. Do not use.

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress

bit 0 **ADON:** ADC Enable bit
1 = ADC is enabled
0 = ADC is disabled and consumes no operating current

**Note 1:** When the CHS<2:0> bits change to select the 1.2V or 0.6V reference, the reference output voltage will have a transient. If the Comparator module uses this 0.6V reference voltage, the comparator output may momentarily change state due to the transient.


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### REGISTER 10-2: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0 (READ-ONLY)

| R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| ADRES9 | ADRES8 | ADRES7 | ADRES6 | ADRES5 | ADRES4 | ADRES3 | ADRES2 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-0 **ADRES<9:2>**: ADC Result Register bits
Upper 8 bits of 10-bit conversion result

### REGISTER 10-3: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0 (READ-ONLY)

| R-x | R-x | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| ADRES1 | ADRES0 | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-6 **ADRES<1:0>**: ADC Result Register bits
Lower 2 bits of 10-bit conversion result

bit 5-0 **Unimplemented:** Read as ‘0’

### REGISTER 10-4: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1 (READ-ONLY)

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-x | R-x |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | ADRES9 | ADRES8 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1-0 **ADRES<9:8>**: ADC Result Register bits
Upper 2 bits of 10-bit conversion result

### REGISTER 10-5: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1 (READ-ONLY)

| R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| ADRES7 | ADRES6 | ADRES5 | ADRES4 | ADRES3 | ADRES2 | ADRES1 | ADRES0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-0 **ADRES<7:0>**: ADC Result Register bits
Lower 8 bits of 10-bit conversion result

## 10.3 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 10-4. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), see Figure 10-4. **The maximum recommended impedance for analog sources is 10 kΩ.** As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 10-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

**EQUATION 10-1: ACQUISITION TIME EXAMPLE**

*Assumptions:* *Temperature = 50°C and external impedance of 10kΩ 5.0V VDD*

$$\begin{aligned} T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= T_{AMP} + T_C + T_{COFF} \\ &= 2\mu s + T_C + [(\text{Temperature} - 25°C)(0.05\mu s/°C)] \end{aligned}$$

*The value for TC can be approximated with the following equations:*

$$V_{APPLIED}\left(1 - \frac{1}{2047}\right) = V_{CHOLD} \quad ;[1]\ V_{CHOLD}\ \text{charged to within 1/2 lsb}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{CHOLD} \quad ;[2]\ V_{CHOLD}\ \text{charge response to}\ V_{APPLIED}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{2047}\right) \quad ;\text{combining [1] and [2]}$$

*Solving for TC:*

$$\begin{aligned} T_C &= -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ \ln(1/2047) \\ &= -10pF(1k\Omega + 7k\Omega + 10k\Omega)\ \ln(0.0004885) \\ &= 1.37\mu s \end{aligned}$$

*Therefore:*

$$\begin{aligned} T_{ACQ} &= 2\mu s + 1.37\mu s + [(50°C - 25°C)(0.05\mu s/°C)] \\ &= 4.67\mu s \end{aligned}$$

**Note 1:** The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

**2:** The charge holding capacitor (CHOLD) is not discharged after each conversion.

**3:** The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.


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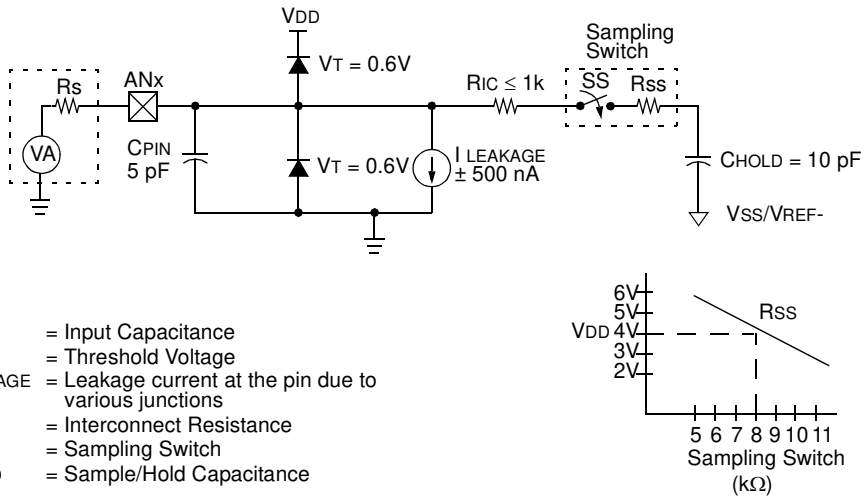
**FIGURE 10-4: ANALOG INPUT MODEL**




**Legend:** CPIN = Input Capacitance
VT = Threshold Voltage
I LEAKAGE = Leakage current at the pin due to various junctions
RIC = Interconnect Resistance
SS = Sampling Switch
CHOLD = Sample/Hold Capacitance

**FIGURE 10-5: ADC TRANSFER FUNCTION**

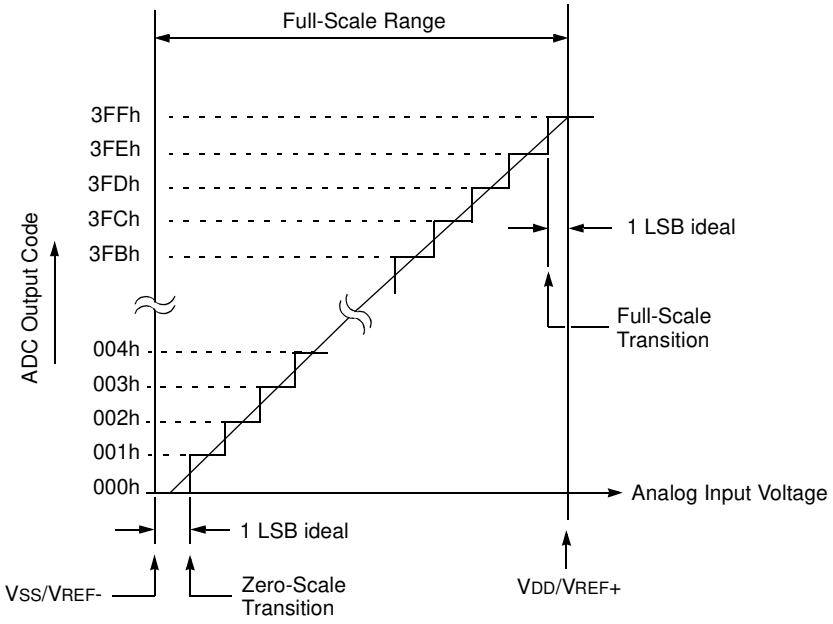


**TABLE 10-2: SUMMARY OF ASSOCIATED ADC REGISTERS**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| ADCON0(1) | ADFM | VCFG | — | CHS2 | CHS1 | CHS0 | GO/$\overline{\text{DONE}}$ | ADON | 00-0 0000 | 00-0 0000 |
| ANSEL | — | ADCS2(1) | ADCS1(1) | ADCS0(1) | ANS3 | ANS2(1) | ANS1 | ANS0 | -000 1111 | -000 1111 |
| ADRESH(1,2) | A/D Result Register High Byte | | | | | | | | xxxx xxxx | uuuu uuuu |
| ADRESL(1,2) | A/D Result Register Low Byte | | | | | | | | xxxx xxxx | uuuu uuuu |
| GPIO | — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | --x0 x000 | --x0 x000 |
| INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF | 0000 0000 | 0000 0000 |
| PIE1 | — | ADIE(1) | CCP1IE(1) | — | CMIE | — | TMR2IE(1) | TMR1IE | -00- 0-00 | -00- 0-00 |
| PIR1 | — | ADIF(1) | CCP1IF(1) | — | CMIF | — | TMR2IF(1) | TMR1IF | -00- 0-00 | -00- 0-00 |
| TRISIO | — | — | TRISIO5 | TRISIO4 | TRISIO3 | TRISIO2 | TRISIO1 | TRISIO0 | --11 1111 | --11 1111 |

**Legend:** x = unknown, u = unchanged, — = unimplemented read as '0'. Shaded cells are not used for ADC module.

**Note 1:** For PIC12F615/617/HV615 only.

**2:** Read Only Register.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## 11.0 ENHANCED CAPTURE/ COMPARE/PWM (WITH AUTO-SHUTDOWN AND DEAD BAND) MODULE (PIC12F615/617/ HV615 ONLY)

The Enhanced Capture/Compare/PWM module is a peripheral which allows the user to time and control different events. In Capture mode, the peripheral allows the timing of the duration of an event.The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate a Pulse-Width Modulated signal of varying frequency and duty cycle.

Table 11-1 shows the timer resources required by the ECCP module.

**TABLE 11-1: ECCP MODE – TIMER RESOURCES REQUIRED**

| ECCP Mode | Timer Resource |
|---|---|
| Capture | Timer1 |
| Compare | Timer1 |
| PWM | Timer2 |

**REGISTER 11-1: CCP1CON: ENHANCED CCP1 CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| P1M | — | DC1B1 | DC1B0 | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **P1M:** PWM Output Configuration bits
If CCP1M<3:2> = 00, 01, 10:
x = P1A assigned as Capture/Compare input; P1B assigned as port pins
If CCP1M<3:2> = 11:
0 = Single output; P1A modulated; P1B assigned as port pins
1 = Half-Bridge output; P1A, P1B modulated with dead-band control

bit 6 **Unimplemented:** Read as ‘0’

bit 5-4 **DC1B<1:0>:** PWM Duty Cycle Least Significant bits
Capture mode:
Unused.
Compare mode:
Unused.
PWM mode:
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR1L.

bit 3-0 **CCP1M<3:0>:** ECCP Mode Select bits
0000 =Capture/Compare/PWM off (resets ECCP module)
0001 =Unused (reserved)
0010 =Compare mode, toggle output on match (CCP1IF bit is set)
0011 =Unused (reserved)
0100 =Capture mode, every falling edge
0101 =Capture mode, every rising edge
0110 =Capture mode, every 4th rising edge
0111 =Capture mode, every 16th rising edge
1000 =Compare mode, set output on match (CCP1IF bit is set)
1001 =Compare mode, clear output on match (CCP1IF bit is set)
1010 =Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected)
1011 =Compare mode, trigger special event (CCP1IF bit is set; CCP1 resets TMR1 or TMR2 and starts an A/D conversion, if the ADC module is enabled)
1100 =PWM mode; P1A active-high; P1B active-high
1101 =PWM mode; P1A active-high; P1B active-low
1110 =PWM mode; P1A active-low; P1B active-high
1111 =PWM mode; P1A active-low; P1B active-low

## 11.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin CCP1. An event is defined as one of the following and is configured by the CCP1M<3:0> bits of the CCP1CON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

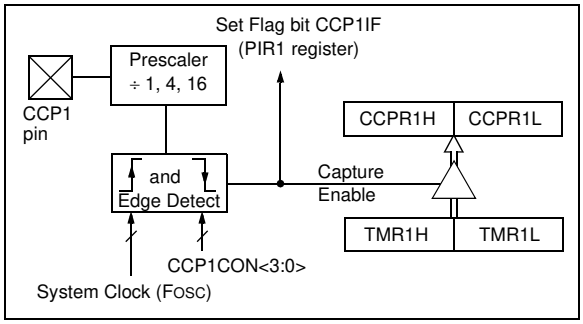
When a capture is made, the Interrupt Request Flag bit CCP1IF of the PIR1 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPR1H, CCPR1L register pair is read, the old captured value is overwritten by the new captured value (see Figure 11-1).

### 11.1.1 CCP1 PIN CONFIGURATION

In Capture mode, the CCP1 pin should be configured as an input by setting the associated TRIS control bit.

| **Note:** | If the CCP1 pin is configured as an output, a write to the port can cause a capture condition. |
|---|---|

**FIGURE 11-1: CAPTURE MODE OPERATION BLOCK DIAGRAM**




### 11.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

### 11.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCP1IE interrupt enable bit of the PIE1 register clear to avoid false interrupts. Additionally, the user should clear the CCP1IF interrupt flag bit of the PIR1 register following any change in operating mode.

### 11.1.4 CCP PRESCALER

There are four prescaler settings specified by the CCP1M<3:0> bits of the CCP1CON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCP1CON register before changing the prescaler (see Example 11-1).

**EXAMPLE 11-1: CHANGING BETWEEN CAPTURE PRESCALERS**

```
BANKSEL CCP1CON     ;Set Bank bits to point
                    ;to CCP1CON
CLRF    CCP1CON     ;Turn CCP module off
MOVLW   NEW_CAPT_PS ;Load the W reg with
                    ; the new prescaler
                    ; move value and CCP ON
MOVWF   CCP1CON     ;Load CCP1CON with this
                    ; value
```


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**TABLE 11-2: SUMMARY OF REGISTERS ASSOCIATED WITH CAPTURE**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| CCP1CON | P1M | — | DC1B1 | DC1B0 | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 | 0-00 0000 | 0-00 0000 |
| CCPR1L | Capture/Compare/PWM Register 1 Low Byte | | | | | | | | xxxx xxxx | uuuu uuuu |
| CCPR1H | Capture/Compare/PWM Register 1 High Byte | | | | | | | | xxxx xxxx | uuuu uuuu |
| INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF | 0000 0000 | 0000 0000 |
| PIE1 | — | ADIE(1) | CCP1IE(1) | — | CMIE | — | TMR2IE(1) | TMR1IE | -00- 0-00 | -00- 0-00 |
| PIR1 | — | ADIF(1) | CCP1IF(1) | — | CMIF | — | TMR2IF(1) | TMR1IF | -00- 0-00 | -00- 0-00 |
| T1CON | T1GINV | TMR1GE | T1CKPS1 | T1CKPS0 | T1OSCEN | $\overline{\text{T1SYNC}}$ | TMR1CS | TMR1ON | 0000 0000 | uuuu uuuu |
| TMR1L | Holding Register for the Least Significant Byte of the 16-bit TMR1 Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| TMR1H | Holding Register for the Most Significant Byte of the 16-bit TMR1 Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| TRISIO | — | — | TRISIO5 | TRISIO4 | TRISIO3 | TRISIO2 | TRISIO1 | TRISIO0 | --11 1111 | --11 1111 |

**Legend:** - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture.

**Note 1:** For PIC12F615/617/HV615 only.

## 11.2 Compare Mode

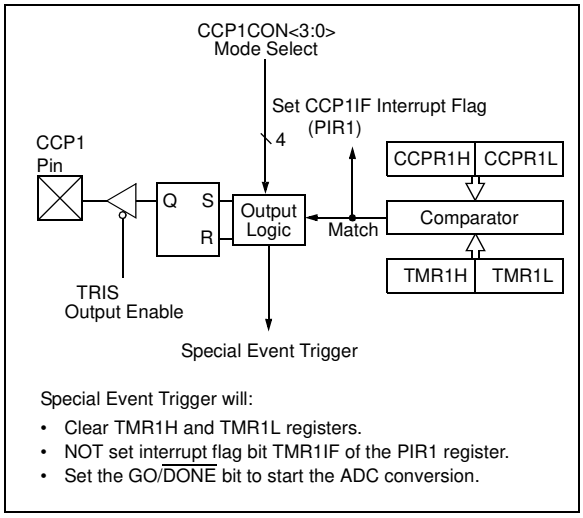
In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the CCP1 module may:

- Toggle the CCP1 output.
- Set the CCP1 output.
- Clear the CCP1 output.
- Generate a Special Event Trigger.
- Generate a Software Interrupt.

The action on the pin is based on the value of the CCP1M<3:0> control bits of the CCP1CON register.

All Compare modes can generate an interrupt.

**FIGURE 11-2: COMPARE MODE OPERATION BLOCK DIAGRAM**




### 11.2.1 CCP1 PIN CONFIGURATION

The user must configure the CCP1 pin as an output by clearing the associated TRIS bit.

> **Note:** Clearing the CCP1CON register will force the CCP1 compare output latch to the default low level. This is not the PORT I/O data latch.

### 11.2.2 TIMER1 MODE SELECTION

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

### 11.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen (CCP1M<3:0> = `1010`), the CCP1 module does not assert control of the CCP1 pin (see the CCP1CON register).

### 11.2.4 SPECIAL EVENT TRIGGER

When Special Event Trigger mode is chosen (CCP1M<3:0> = `1011`), the CCP1 module does the following:

- Resets Timer1
- Starts an ADC conversion if ADC is enabled

The CCP1 module does not assert control of the CCP1 pin in this mode (see the CCP1CON register).

The Special Event Trigger output of the CCP occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCPR1H, CCPR1L register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. This allows the CCPR1H, CCPR1L register pair to effectively provide a 16-bit programmable period register for Timer1.

> **Note 1:** The Special Event Trigger from the CCP module does not set interrupt flag bit TMRxIF of the PIR1 register.
>
> **2:** Removing the match condition by changing the contents of the CCPR1H and CCPR1L register pair, between the clock edge that generates the Special Event Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.


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**TABLE 11-3: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARE**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| CCP1CON | P1M | — | DC1B1 | DC1B0 | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 | 0-00 0000 | 0-00 0000 |
| CCPR1L | Capture/Compare/PWM Register 1 Low Byte | | | | | | | | xxxx xxxx | uuuu uuuu |
| CCPR1H | Capture/Compare/PWM Register 1 High Byte | | | | | | | | xxxx xxxx | uuuu uuuu |
| INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF | 0000 0000 | 0000 0000 |
| PIE1 | — | ADIE(1) | CCP1IE(1) | — | CMIE | — | TMR2IE(1) | TMR1IE | -00- 0-00 | -00- 0-00 |
| PIR1 | — | ADIF(1) | CCP1IF(1) | — | CMIF | — | TMR2IF(1) | TMR1IF | -00- 0-00 | -00- 0-00 |
| T1CON | T1GINV | TMR1GE | T1CKPS1 | T1CKPS0 | T1OSCEN | $\overline{\text{T1SYNC}}$ | TMR1CS | TMR1ON | 0000 0000 | uuuu uuuu |
| TMR1L | Holding Register for the Least Significant Byte of the 16-bit TMR1 Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| TMR1H | Holding Register for the Most Significant Byte of the 16-bit TMR1 Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| TMR2 | Timer2 Module Register | | | | | | | | 0000 0000 | 0000 0000 |
| TRISIO | — | — | TRISIO5 | TRISIO4 | TRISIO3 | TRISIO2 | TRISIO1 | TRISIO0 | --11 1111 | --11 1111 |

**Legend:** - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Compare.

**Note 1:** For PIC12F615/617/HV615 only.

## 11.3 PWM Mode

The PWM mode generates a Pulse-Width Modulated signal on the CCP1 pin. The duty cycle, period and resolution are determined by the following registers:

- PR2
- T2CON
- CCPR1L
- CCP1CON

In Pulse-Width Modulation (PWM) mode, the CCP module produces up to a 10-bit resolution PWM output on the CCP1 pin. Since the CCP1 pin is multiplexed with the PORT data latch, the TRIS for that pin must be cleared to enable the CCP1 pin output driver.

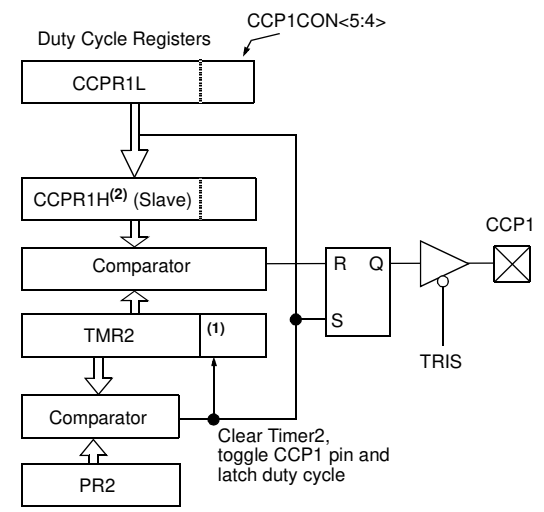
| **Note:** | Clearing the CCP1CON register will relinquish CCP1 control of the CCP1 pin. |
|---|---|

Figure 11-3 shows a simplified block diagram of PWM operation.

Figure 11-4 shows a typical waveform of the PWM signal.

For a step-by-step procedure on how to set up the CCP module for PWM operation, see **Section 11.3.7 "Setup for PWM Operation"**.

**FIGURE 11-3: SIMPLIFIED PWM BLOCK DIAGRAM**

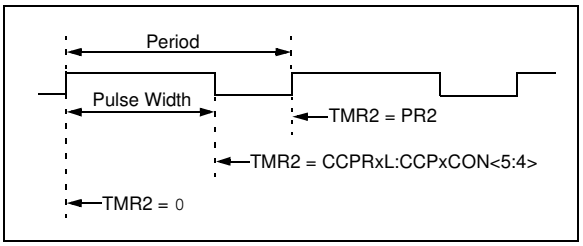



**Note 1:** The 8-bit timer TMR2 register is concatenated with the 2-bit internal system clock (FOSC), or 2 bits of the prescaler, to create the 10-bit time base.

**2:** In PWM mode, CCPR1H is a read-only register.

The PWM output (Figure 11-4) has a time base (period) and a time that the output stays high (duty cycle).

**FIGURE 11-4: CCP PWM OUTPUT**





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### 11.3.1 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 11-1.

**EQUATION 11-1: PWM PERIOD**

$$PWM\ Period = [(PR2) + 1] \bullet 4 \bullet T_{OSC} \bullet (TMR2\ Prescale\ Value)$$

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPR1L into CCPR1H.

| | |
|---|---|
| **Note:** | The Timer2 postscaler (see **Section 8.1 "Timer2 Operation"**) is not used in the determination of the PWM frequency. |

### 11.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPR1L register and DC1B<1:0> bits of the CCP1CON register. The CCPR1L contains the eight MSbs and the DC1B<1:0> bits of the CCP1CON register contain the two LSbs. CCPR1L and DC1B<1:0> bits of the CCP1CON register can be written to at any time. The duty cycle value is not latched into CCPR1H until after the period completes (i.e., a match between PR2 and TMR2 registers occurs). While using the PWM, the CCPR1H register is read-only.

Equation 11-2 is used to calculate the PWM pulse width.

Equation 11-3 is used to calculate the PWM duty cycle ratio.

**EQUATION 11-2: PULSE WIDTH**

$$Pulse\ Width = (CCPR1L{:}CCP1CON\langle 5{:}4\rangle) \bullet T_{OSC} \bullet (TMR2\ Prescale\ Value)$$

**EQUATION 11-3: DUTY CYCLE RATIO**

$$Duty\ Cycle\ Ratio = \frac{(CCPR1L{:}CCP1CON\langle 5{:}4\rangle)}{4(PR2 + 1)}$$

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (FOSC), or 2 bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPR1H and 2-bit latch, then the CCP1 pin is cleared (see Figure 11-3).

### 11.3.3 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 11-4.

**EQUATION 11-4: PWM RESOLUTION**

$$Resolution = \frac{\log[4(PR2 + 1)]}{\log(2)}\ bits$$

| | |
|---|---|
| Note: | If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged. |

**TABLE 11-4: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)**

| PWM Frequency | 1.22 kHz | 4.88 kHz | 19.53 kHz | 78.12 kHz | 156.3 kHz | 208.3 kHz |
|---|---|---|---|---|---|---|
| Timer Prescale (1, 4, 16) | 16 | 4 | 1 | 1 | 1 | 1 |
| PR2 Value | 0xFF | 0xFF | 0xFF | 0x3F | 0x1F | 0x17 |
| Maximum Resolution (bits) | 10 | 10 | 10 | 8 | 7 | 6.6 |

**TABLE 11-5: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 8 MHz)**

| PWM Frequency | 1.22 kHz | 4.90 kHz | 19.61 kHz | 76.92 kHz | 153.85 kHz | 200.0 kHz |
|---|---|---|---|---|---|---|
| Timer Prescale (1, 4, 16) | 16 | 4 | 1 | 1 | 1 | 1 |
| PR2 Value | 0x65 | 0x65 | 0x65 | 0x19 | 0x0C | 0x09 |
| Maximum Resolution (bits) | 8 | 8 | 8 | 6 | 5 | 5 |

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### 11.3.4 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCP1 pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

### 11.3.5 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See **Section 4.0 "Oscillator Module"** for additional details.

### 11.3.6 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

### 11.3.7 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Disable the PWM pin (CCP1) output drivers by setting the associated TRIS bit.
2. Set the PWM period by loading the PR2 register.
3. Configure the CCP module for the PWM mode by loading the CCP1CON register with the appropriate values.
4. Set the PWM duty cycle by loading the CCPR1L register and DC1B bits of the CCP1CON register.
5. Configure and start Timer2:
   - Clear the TMR2IF interrupt flag bit of the PIR1 register.
   - Set the Timer2 prescale value by loading the T2CKPS bits of the T2CON register.
   - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output after a new PWM cycle has started:
   - Wait until Timer2 overflows (TMR2IF bit of the PIR1 register is set).
   - Enable the CCP1 pin output driver by clearing the associated TRIS bit.


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## 11.4 PWM (Enhanced Mode)

The Enhanced PWM Mode can generate a PWM signal on up to four different output pins with up to 10-bits of resolution. It can do this through four different PWM output modes:

- Single PWM
- Half-Bridge PWM

To select an Enhanced PWM mode, the P1M bits of the CCP1CON register must be set appropriately.

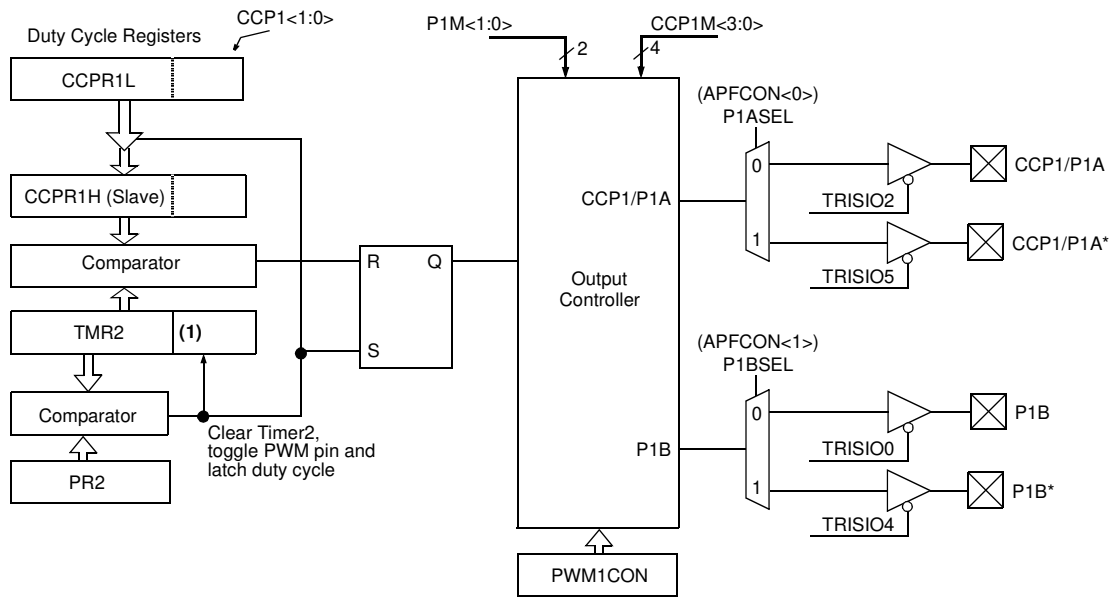
The PWM outputs are multiplexed with I/O pins and are designated P1A and P1B. The polarity of the PWM pins is configurable and is selected by setting the CCP1M bits in the CCP1CON register appropriately.

Table 11-6 shows the pin assignments for each Enhanced PWM mode.

Figure 11-5 shows an example of a simplified block diagram of the Enhanced PWM module.

**Note:** To prevent the generation of an incomplete waveform when the PWM is first enabled, the ECCP module waits until the start of a new PWM period before generating a PWM signal.

**FIGURE 11-5: EXAMPLE SIMPLIFIED BLOCK DIAGRAM OF THE ENHANCED PWM MODE**




* Alternate pin function.

**Note 1:** The 8-bit timer TMR2 register is concatenated with the 2-bit internal Q clock, or 2 bits of the prescaler to create the 10-bit time base.

**Note 1:** The TRIS register value for each PWM output must be configured appropriately.

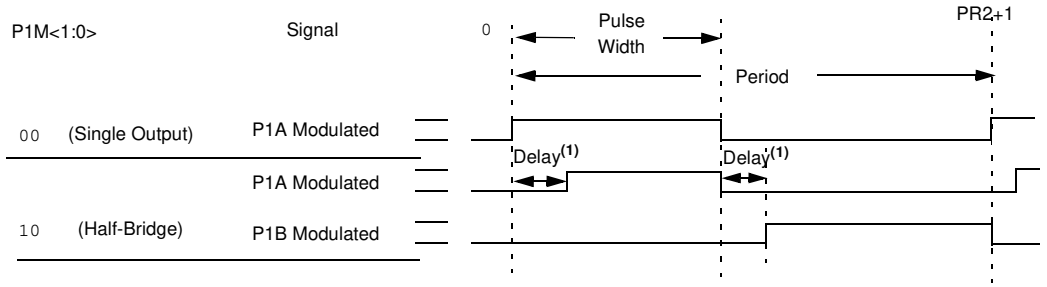
**2:** Clearing the CCP1CON register will relinquish ECCP control of all PWM output pins.

**3:** Any pin not used by an Enhanced PWM mode is available for alternate pin functions.

**TABLE 11-6: EXAMPLE PIN ASSIGNMENTS FOR VARIOUS PWM ENHANCED MODES**

| ECCP Mode | P1M<1:0> | CCP1/P1A | P1B |
|---|---|---|---|
| Single | 00 | Yes(1) | Yes(1) |
| Half-Bridge | 10 | Yes | Yes |

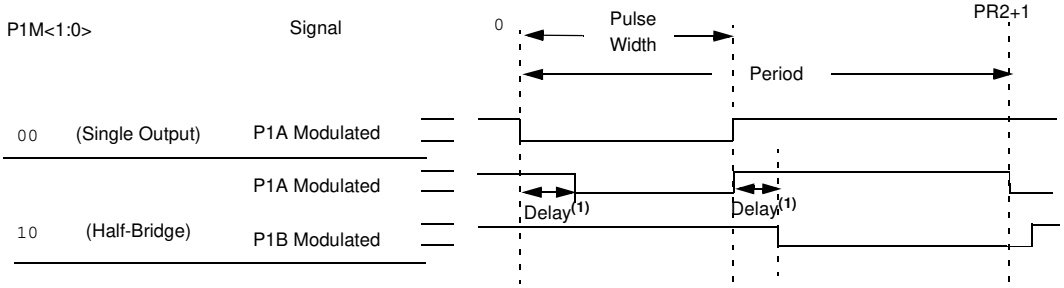
**FIGURE 11-6: EXAMPLE PWM (ENHANCED MODE) OUTPUT RELATIONSHIPS (ACTIVE-HIGH STATE)**




Relationships:
- Period = 4 * TOSC * (PR2 + 1) * (TMR2 Prescale Value)
- Pulse Width = TOSC * (CCPR1L<7:0>:CCP1CON<5:4>) * (TMR2 Prescale Value)
- Delay = 4 * TOSC * (PWM1CON<6:0>)

**Note 1:** Dead-band delay is programmed using the PWM1CON register (**Section 11.4.6 "Programmable Dead-Band Delay mode"**).

**FIGURE 11-7: EXAMPLE ENHANCED PWM OUTPUT RELATIONSHIPS (ACTIVE-LOW STATE)**




Relationships:
- Period = 4 * TOSC * (PR2 + 1) * (TMR2 Prescale Value)
- Pulse Width = TOSC * (CCPR1L<7:0>:CCP1CON<5:4>) * (TMR2 Prescale Value)
- Delay = 4 * TOSC * (PWM1CON<6:0>)

**Note 1:** Dead-band delay is programmed using the PWM1CON register (**Section 11.4.6 "Programmable Dead-Band Delay mode"**).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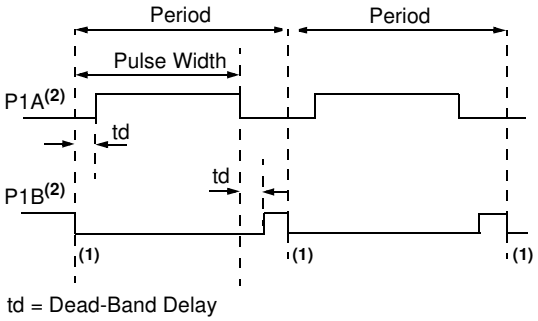
### 11.4.1 HALF-BRIDGE MODE

In Half-Bridge mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the CCP1/P1A pin, while the complementary PWM output signal is output on the P1B pin (see Figure 11-8). This mode can be used for Half-Bridge applications, as shown in Figure 11-9, or for Full-Bridge applications, where four power switches are being modulated with two PWM signals.

In Half-Bridge mode, the programmable dead-band delay can be used to prevent shoot-through current in Half-Bridge power devices. The value of the PDC<6:0> bits of the PWM1CON register sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. See **Section 11.4.6 "Programmable Dead-Band Delay mode"** for more details of the dead-band delay operations.

Since the P1A and P1B outputs are multiplexed with the PORT data latches, the associated TRIS bits must be cleared to configure P1A and P1B as outputs.

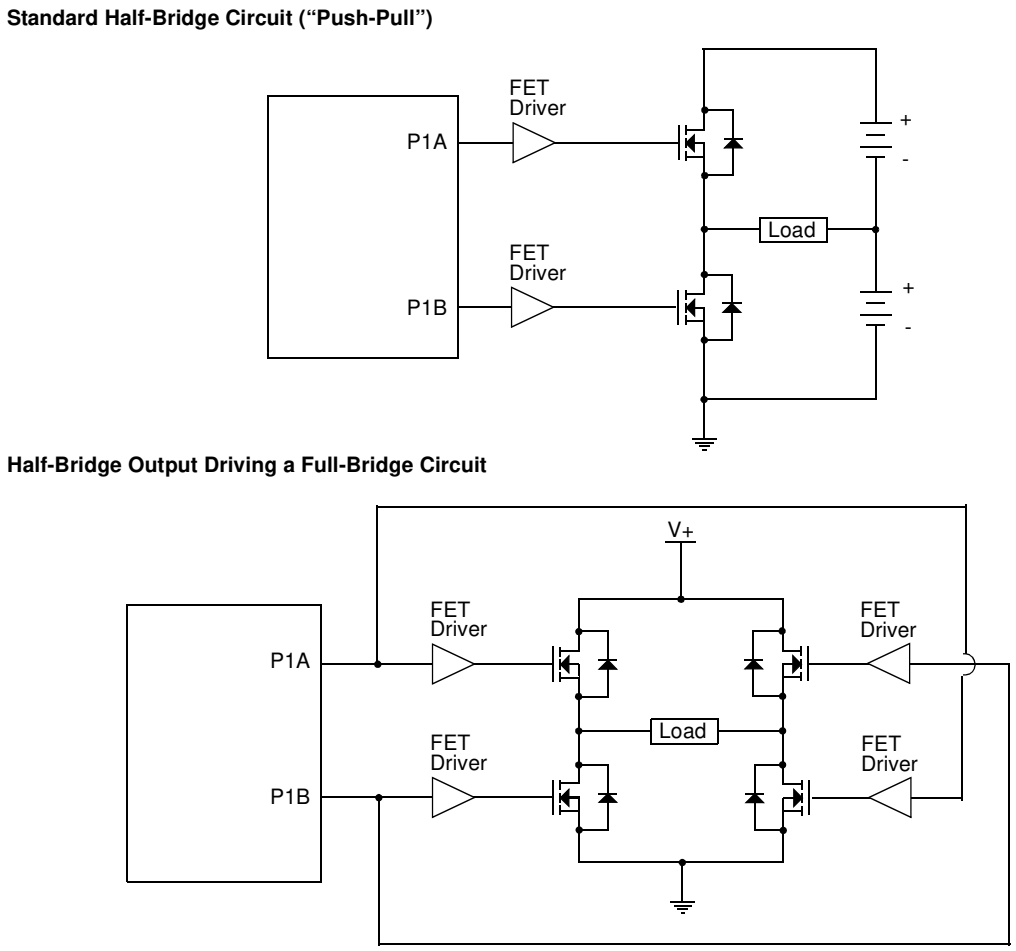
**FIGURE 11-8: EXAMPLE OF HALF-BRIDGE PWM OUTPUT**




**Note 1:** At this time, the TMR2 register is equal to the PR2 register.

**2:** Output signals are shown as active-high.

**FIGURE 11-9: EXAMPLE OF HALF-BRIDGE APPLICATIONS**



### 11.4.2 START-UP CONSIDERATIONS

When any PWM mode is used, the application hardware must use the proper external pull-up and/or pull-down resistors on the PWM output pins.

| | |
|---|---|
| **Note:** | When the microcontroller is released from Reset, all of the I/O pins are in the high-impedance state. The external circuits must keep the power switch devices in the OFF state until the microcontroller drives the I/O pins with the proper signal levels or activates the PWM output(s). |

The CCP1M<1:0> bits of the CCP1CON register allow the user to choose whether the PWM output signals are active-high or active-low for each PWM output pin (P1A and P1B). The PWM output polarities must be selected before the PWM pin output drivers are enabled. Changing the polarity configuration while the PWM pin output drivers are enable is not recommended since it may result in damage to the application circuits.

The P1A and P1B output latches may not be in the proper states when the PWM module is initialized. Enabling the PWM pin output drivers at the same time as the Enhanced PWM modes may cause damage to the application circuit. The Enhanced PWM modes must be enabled in the proper Output mode and complete a full PWM cycle before configuring the PWM pin output drivers. The completion of a full PWM cycle is indicated by the TMR2IF bit of the PIR1 register being set as the second PWM period begins.

### 11.4.3 OPERATION DURING SLEEP

When the device is placed in sleep, the allocated timer will not increment and the state of the module will not change. If the CCP1 pin is driving a value, it will continue to drive that value. When the device wakes up, it will continue from this state.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### 11.4.4 ENHANCED PWM AUTO-SHUTDOWN MODE

The PWM mode supports an Auto-Shutdown mode that will disable the PWM outputs when an external shutdown event occurs. Auto-Shutdown mode places the PWM output pins into a predetermined state. This mode is used to help prevent the PWM from damaging the application.

The auto-shutdown sources are selected using the ECCPASx bits of the ECCPAS register. A shutdown event may be generated by:

- A logic '0' on the INT pin
- Comparator
- Setting the ECCPASE bit in firmware

A shutdown condition is indicated by the ECCPASE (Auto-Shutdown Event Status) bit of the ECCPAS register. If the bit is a '0', the PWM pins are operating normally. If the bit is a '1', the PWM outputs are in the shutdown state. Refer to Figure 1.

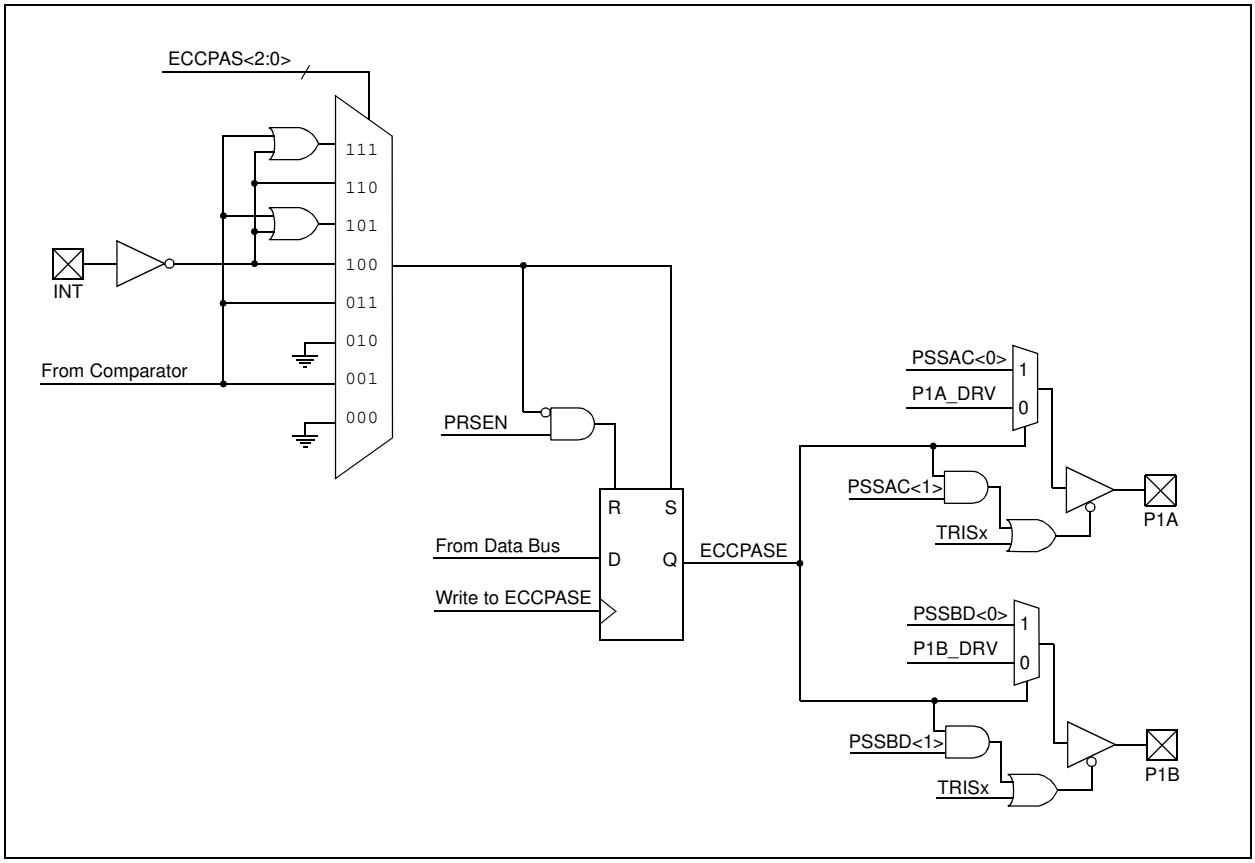
When a shutdown event occurs, two things happen:

The ECCPASE bit is set to '1'. The ECCPASE will remain set until cleared in firmware or an auto-restart occurs (see **Section 11.4.5 "Auto-Restart Mode"**).

The enabled PWM pins are asynchronously placed in their shutdown states. The state of P1A is determined by the PSSAC bit. The state of P1B is determined by the PSSBD bit. The PSSAC and PSSBD bits are located in the ECCPAS register. Each pin may be placed into one of three states:

- Drive logic '1'
- Drive logic '0'
- Tri-state (high-impedance)

**FIGURE 11-10: AUTO-SHUTDOWN BLOCK DIAGRAM**



**REGISTER 11-2: ECCPAS: ENHANCED CAPTURE/COMPARE/PWM AUTO-SHUTDOWN CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ECCPASE | ECCPAS2 | ECCPAS1 | ECCPAS0 | PSSAC1 | PSSAC0 | PSSBD1 | PSSBD0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **ECCPASE:** ECCP Auto-Shutdown Event Status bit
`1` = A shutdown event has occurred; ECCP outputs are in shutdown state
`0` = ECCP outputs are operating

bit 6-4 **ECCPAS<2:0>:** ECCP Auto-shutdown Source Select bits
`000` =Auto-Shutdown is disabled
`001` =Comparator output change
`010` =Auto-Shutdown is disabled
`011` =Comparator output change(1)
`100` =$V_{IL}$ on INT pin
`101` =$V_{IL}$ on INT pin or Comparator change
`110` =$V_{IL}$ on INT pin(1)
`111` =$V_{IL}$ on INT pin or Comparator change

bit 3-2 **PSSAC<1:0>:** Pin P1A Shutdown State Control bits
`00` = Drive pin P1A to ‘`0`’
`01` = Drive pin P1A to ‘`1`’
`1x` = Pin P1A tri-state

bit 1-0 **PSSBD<1:0>:** Pin P1B Shutdown State Control bits
`00` = Drive pin P1B to ‘`0`’
`01` = Drive pin P1B to ‘`1`’
`1x` = Pin P1B tri-state

**Note 1:** If CMSYNC is enabled, the shutdown will be delayed by Timer1.

**Note 1:** The auto-shutdown condition is a level-based signal, not an edge-based signal. As long as the level is present, the auto-shutdown will persist.

**2:** Writing to the ECCPASE bit is disabled while an auto-shutdown condition persists.

**3:** Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart) the PWM signal will always restart at the beginning of the next PWM period.


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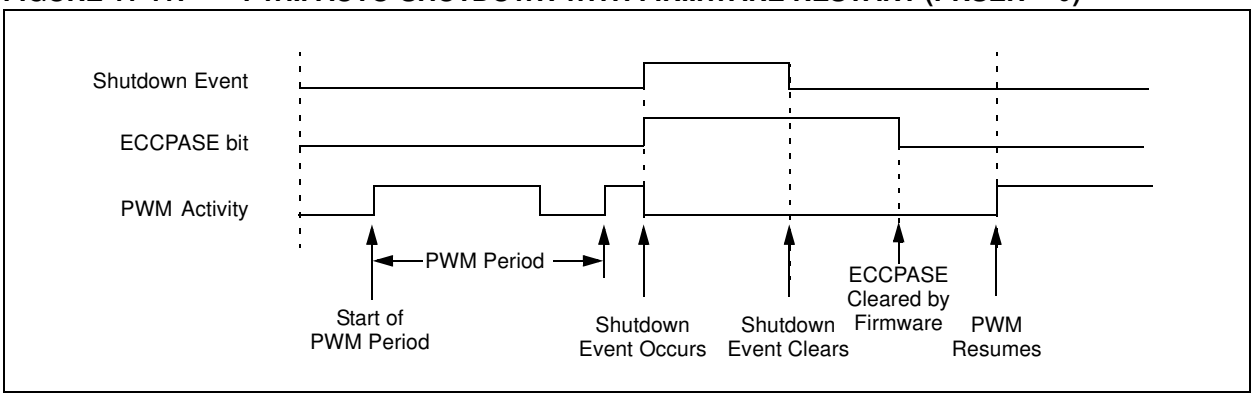
**FIGURE 11-11: PWM AUTO-SHUTDOWN WITH FIRMWARE RESTART (PRSEN = 0)**

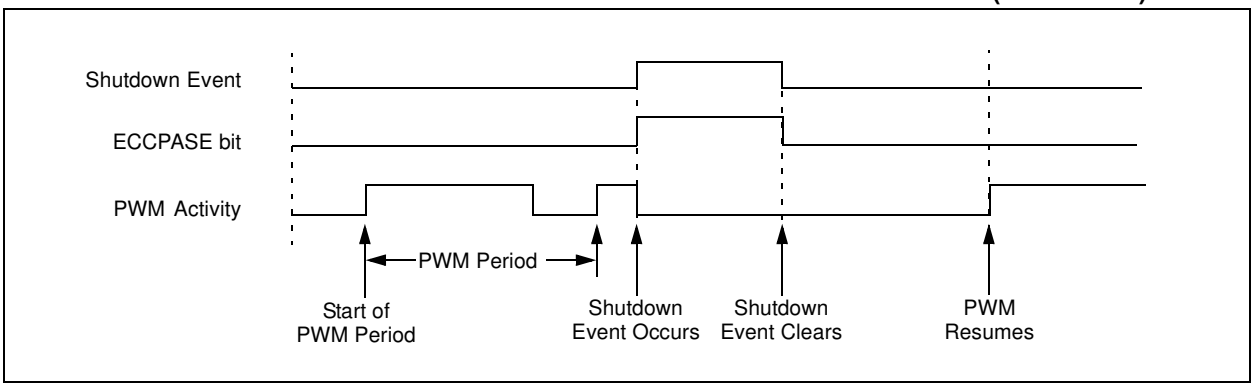



### 11.4.5 AUTO-RESTART MODE

The Enhanced PWM can be configured to automatically restart the PWM signal once the auto-shutdown condition has been removed. Auto-restart is enabled by setting the PRSEN bit in the PWM1CON register.

If auto-restart is enabled, the ECCPASE bit will remain set as long as the auto-shutdown condition is active. When the auto-shutdown condition is removed, the ECCPASE bit will be cleared via hardware and normal operation will resume.

**FIGURE 11-12: PWM AUTO-SHUTDOWN WITH AUTO-RESTART ENABLED (PRSEN = 1)**

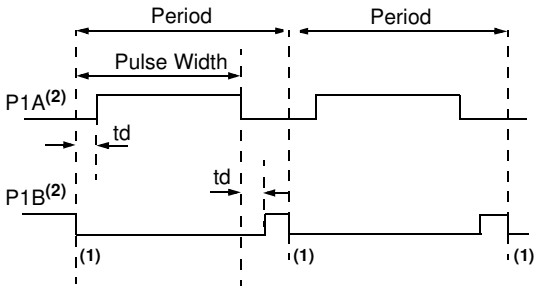


### 11.4.6 PROGRAMMABLE DEAD-BAND DELAY MODE

In Half-Bridge applications where all power switches are modulated at the PWM frequency, the power switches normally require more time to turn off than to turn on. If both the upper and lower power switches are switched at the same time (one turned on, and the other turned off), both switches may be on for a short period of time until one switch completely turns off. During this brief interval, a very high current (*shoot-through current*) will flow through both power switches, shorting the bridge supply. To avoid this potentially destructive shoot-through current from flowing during switching, turning on either of the power switches is normally delayed to allow the other switch to completely turn off.

In Half-Bridge mode, a digitally programmable dead-band delay is available to avoid shoot-through current from destroying the bridge power switches. The delay occurs at the signal transition from the non-active state to the active state. See Figure 11-13 for illustration. The lower seven bits of the associated PWMxCON register (Register 11-3) sets the delay period in terms of microcontroller instruction cycles (TCY or 4 TOSC).

**FIGURE 11-13: EXAMPLE OF HALF-BRIDGE PWM OUTPUT**

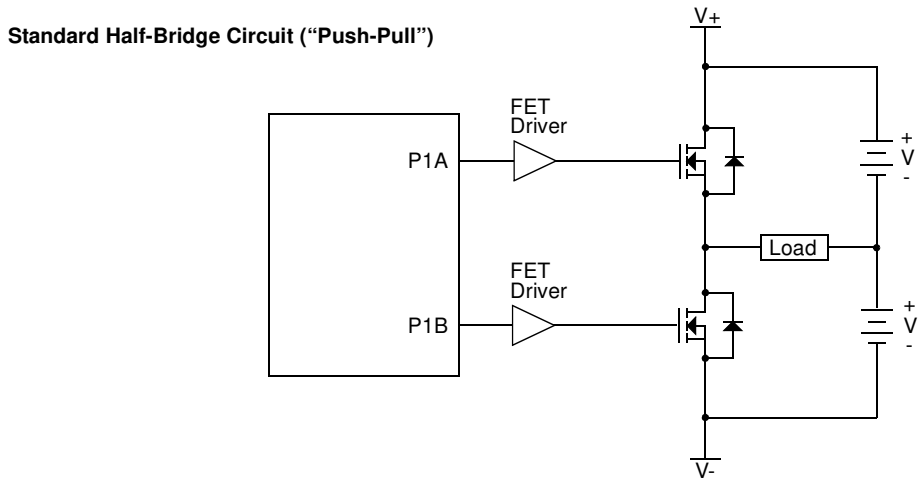



td = Dead-Band Delay

**Note 1:** At this time, the TMR2 register is equal to the PR2 register.

**2:** Output signals are shown as active-high.

**FIGURE 11-14: EXAMPLE OF HALF-BRIDGE APPLICATIONS**





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### REGISTER 11-3: PWM1CON: ENHANCED PWM CONTROL REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PRSEN | PDC6 | PDC5 | PDC4 | PDC3 | PDC2 | PDC1 | PDC0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **PRSEN:** PWM Restart Enable bit

1 = Upon auto-shutdown, the ECCPASE bit clears automatically once the shutdown event goes away; the PWM restarts automatically

0 = Upon auto-shutdown, ECCPASE must be cleared in software to restart the PWM

bit 6-0 **PDC<6:0>:** PWM Delay Count bits

PDCn =Number of FOSC/4 (4 * TOSC) cycles between the scheduled time when a PWM signal **should** transition active and the **actual** time it transitions active

### TABLE 11-7: SUMMARY OF REGISTERS ASSOCIATED WITH PWM

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| APFCON | — | — | — | T1GSEL | — | — | P1BSEL | P1ASEL | ---0 --00 | ---0 --00 |
| CCP1CON(1) | P1M | — | DC1B1 | DC1B0 | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 | 0-00 0000 | 0-00 0000 |
| CCPR1L(1) | Capture/Compare/PWM Register 1 Low Byte | | | | | | | | xxxx xxxx | uuuu uuuu |
| CCPR1H(1) | Capture/Compare/PWM Register 1 High Byte | | | | | | | | xxxx xxxx | uuuu uuuu |
| CMCON0 | CMON | COUT | CMOE | CMPOL | — | CMR | — | CMCH | 0000 -0-0 | 0000 -0-0 |
| CMCON1 | — | — | — | T1ACS | CMHYS | — | T1GSS | CMSYNC | ---0 0-10 | ---0 0-10 |
| ECCPAS(1) | ECCPASE | ECCPAS2 | ECCPAS1 | ECCPAS0 | PSSAC1 | PSSAC0 | PSSBD1 | PSSBD0 | 0000 0000 | 0000 0000 |
| PWM1CON | PRSEN | PDC6 | PDC5 | PDC4 | PDC3 | PDC2 | PDC1 | PDC0 | 0000 0000 | 0000 0000 |
| INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF | 0000 0000 | 0000 0000 |
| PIE1 | — | ADIE(1) | CCP1IE(1) | — | CMIE | — | TMR2IE(1) | TMR1IE | -00- 0-00 | -00- 0-00 |
| PIR1 | — | ADIF(1) | CCP1IF(1) | — | CMIF | — | TMR2IF(1) | TMR1IF | -00- 0-00 | -00- 0-00 |
| T2CON(1) | — | TOUTPS3 | TOUTPS2 | TOUTPS1 | TOUTPS0 | TMR2ON | T2CKPS1 | T2CKPS0 | -000 0000 | -000 0000 |
| TMR2(1) | Timer2 Module Register | | | | | | | | 0000 0000 | 0000 0000 |
| TRISIO | — | — | TRISIO5 | TRISIO4 | TRISIO3 | TRISIO2 | TRISIO1 | TRISIO0 | --11 1111 | --11 1111 |

**Legend:** – = Unimplemented locations, read as ‘0’, u = unchanged, x = unknown. Shaded cells are not used by the PWM.

**Note 1:** For PIC12F615/617/HV615 only.

**NOTES:**


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## 12.0 SPECIAL FEATURES OF THE CPU

The PIC12F609/615/617/12HV609/615 has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving features and offer code protection.

These features are:

- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Oscillator selection
- Sleep
- Code protection
- ID Locations
- In-Circuit Serial Programming

The PIC12F609/615/617/12HV609/615 has two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 64 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can use the Power-up Timer to provide at least a 64 ms Reset. With these three functions-on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-Down mode. The user can wake-up from Sleep through:

- External Reset
- Watchdog Timer Wake-up
- An interrupt

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost while the LP crystal option saves power. A set of Configuration bits are used to select various options (see Register 12-1).

### 12.1 Configuration Bits

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations as shown in Register 12-1. These bits are mapped in program memory location 2007h.

| | |
|---|---|
| **Note:** | Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See *Memory Programming Specification* (DS41204) for more information. |

### REGISTER 12-1: CONFIG: CONFIGURATION WORD REGISTER (ADDRESS: 2007h) FOR PIC12F609/615/HV609/615 ONLY

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| U-1 | U-1 | U-1 | U-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 |
| — | — | — | — | BOREN1(1) | BOREN0(1) | IOSCFS | $\overline{CP}$(2) | MCLRE(3) | $\overline{PWRTE}$ | WDTE | FOSC2 | FOSC1 | FOSC0 |
| bit 13 | | | | | | | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | P = Programmable | U = Unimplemented bit, read as ‘0’ |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 13-10 **Unimplemented**: Read as ‘1’

bit 9-8 **BOREN<1:0>:** Brown-out Reset Selection bits(1)
11 = BOR enabled
10 = BOR enabled during operation and disabled in Sleep
0x = BOR disabled

bit 7 **IOSCFS:** Internal Oscillator Frequency Select bit
1 = 8 MHz
0 = 4 MHz

bit 6 **$\overline{CP}$:** Code Protection bit(2)
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 5 **MCLRE:** $\overline{MCLR}$ Pin Function Select bit(3)
1 = $\overline{MCLR}$ pin function is $\overline{MCLR}$
0 = $\overline{MCLR}$ pin function is digital input, $\overline{MCLR}$ internally tied to $V_{DD}$

bit 4 **$\overline{PWRTE}$:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
111 =RC oscillator: CLKOUT function on GP4/OSC2/CLKOUT pin, RC on GP5/OSC1/CLKIN
110 =RCIO oscillator: I/O function on GP4/OSC2/CLKOUT pin, RC on GP5/OSC1/CLKIN
101 =INTOSC oscillator: CLKOUT function on GP4/OSC2/CLKOUT pin, I/O function on GP5/OSC1/CLKIN
100 = INTOSCIO oscillator: I/O function on GP4/OSC2/CLKOUT pin, I/O function on GP5/OSC1/CLKIN
011 =EC: I/O function on GP4/OSC2/CLKOUT pin, CLKIN on GP5/OSC1/CLKIN
010 =HS oscillator: High-speed crystal/resonator on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN
001 = XT oscillator: Crystal/resonator on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN
000 = LP oscillator: Low-power crystal on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN

**Note 1:** Enabling Brown-out Reset does not automatically enable Power-up Timer.
**2:** The entire program memory will be erased when the code protection is turned off.
**3:** When $\overline{MCLR}$ is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.


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### REGISTER 12-2: CONFIG – CONFIGURATION WORD (ADDRESS: 2007h) FOR PIC12F617 ONLY

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| U-1 | U-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 |
| — | — | WRT1 | WRT0 | BOREN1 | BOREN0 | IOSCFS | $\overline{CP}$ | MCLRE | $\overline{PWRTE}$ | WDTE | FOSC2 | F0SC1 | F0SC0 |
| bit 13 | | | | | | | | | | | | | bit 0 |

bit 13-12 **Unimplemented:** Read as '1'

bit 11-10 **WRT<1:0>:** Flash Program Memory Self Write Enable bits
11 = Write protection off
10 = 000h to 1FFh write protected, 200h to 7FFh may be modified by PMCON1 control
01 = 000h to 3FFh write protected, 400h to 7FFh may be modified by PMCON1 control
00 = 000h to 7FFh write protected, entire program memory is write protected.

bit 9-8 **BOREN<1:0>:** Brown-out Reset Enable bits
11 = BOR enabled
10 = BOR disabled during Sleep and enabled during operation
0X = BOR disabled

bit 7 **IOSCFS:** Internal Oscillator Frequency Select
1 = 8 MHz
0 = 4 MHz

bit 6 **$\overline{CP}$:** Code Protection
1 = Program memory is not code protected
0 = Program memory is external read and write protected

bit 5 **MCLRE:** $\overline{MCLR}$ Pin Function Select
1 = $\overline{MCLR}$ pin is $\overline{MCLR}$ function and weak internal pull-up is enabled
0 = $\overline{MCLR}$ pin is alternate function, $\overline{MCLR}$ function is internally disabled

bit 4 **$\overline{PWRTE}$:** Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
000 =LP oscillator: Low-power crystal on RA5/T1CKI/OSC1/CLKIN and RA4/AN3/$\overline{T1G}$/OSC2/CLKOUT
001 =XT oscillator: Crystal/resonator on RA5/T1CKI/OSC1/CLKIN and RA4/AN3/$\overline{T1G}$/OSC2/CLKOUT
010 =HS oscillator: High-speed crystal/resonator on RA5/T1CKI/OSC1/CLKIN and RA4/AN3/$\overline{T1G}$/OSC2/CLKOUT
011 =EC: I/O function on RA4/AN3/$\overline{T1G}$/OSC2/CLKOUT, CLKIN on RA5/T1CKI/OSC1/CLKIN
100 =INTOSCIO oscillator: I/O function on RA4/AN3/$\overline{T1G}$/OSC2/CLKOUT, I/O function on RA5/T1CKI/OSC1/CLKIN
101 =INTOSC oscillator: CLKOUT function on RA4/AN3/$\overline{T1G}$/OSC2/CLKOUT, I/O function on RA5/T1CKI/OSC1/CLKIN
110 =EXTRCIO oscillator: I/O function on RA4/AN3/$\overline{T1G}$/OSC2/CLKOUT, RC on RA5/T1CKI/OSC1/CLKIN
111 =EXTRC oscillator: CLKOUT function on RA4/AN3/$\overline{T1G}$/OSC2/CLKOUT, RC on RA5/T1CKI/OSC1/CLKIN

**Note 1:** Enabling Brown-out Reset does not automatically enable the Power-up Timer (PWRT).

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '1' | P = Programmable |
| -n = Value at POR | 1 = bit is set | 0 = bit is cleared | x = bit is unknown |

## 12.2 Calibration Bits

The 8 MHz internal oscillator is factory calibrated. These calibration values are stored in fuses located in the Calibration Word (2008h). The Calibration Word is not erased when using the specified bulk erase sequence in the *Memory Programming Specification* (DS41204) and thus, does not require reprogramming.

## 12.3 Reset

The PIC12F609/615/617/12HV609/615 device differentiates between various kinds of Reset:

a) Power-on Reset (POR)
b) WDT Reset during normal operation
c) WDT Reset during Sleep
d) $\overline{\text{MCLR}}$ Reset during normal operation
e) $\overline{\text{MCLR}}$ Reset during Sleep
f) Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

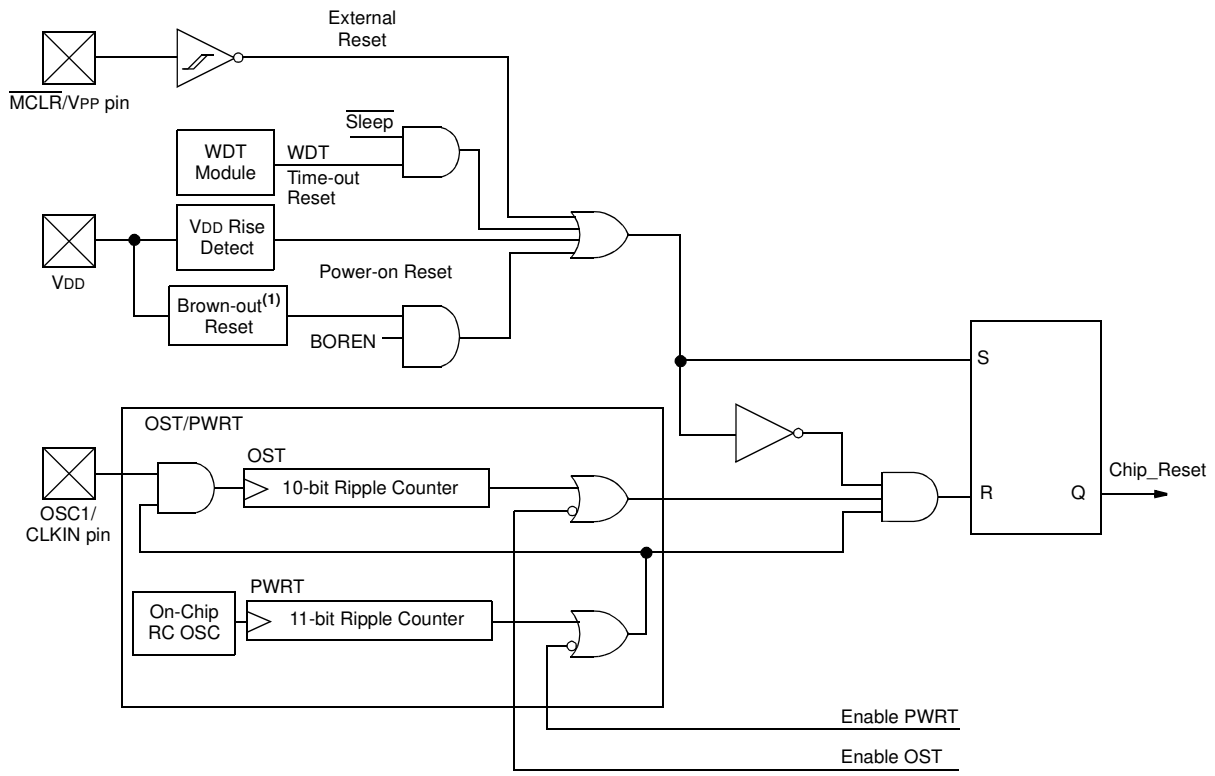
- Power-on Reset
- $\overline{\text{MCLR}}$ Reset
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

WDT wake-up does not cause register resets in the same manner as a WDT Reset since wake-up is viewed as the resumption of normal operation. $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different Reset situations, as indicated in Table 12-2. Software can use these bits to determine the nature of the Reset. See Table 12-5 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 12-1.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See **Section 16.0 "Electrical Specifications"** for pulse-width specifications.

**FIGURE 12-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**




**Note 1:** Refer to the Configuration Word register (Register 12-1).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### 12.3.1 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. To take advantage of the POR, simply connect the MCLR pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See **Section 16.0 "Electrical Specifications"** for details. If the BOR is enabled, the maximum rise time specification does not apply. The BOR circuitry will keep the device in Reset until VDD reaches VBOR (see **Section 12.3.4 "Brown-out Reset (BOR)"**).

| | |
|---|---|
| **Note:** | The POR circuit does not produce an internal Reset when VDD declines. To re-enable the POR, VDD must reach Vss for a minimum of 100 μs. |

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure proper operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Note AN607, *"Power-up Trouble Shooting"* (DS00607).

### 12.3.2 MCLR

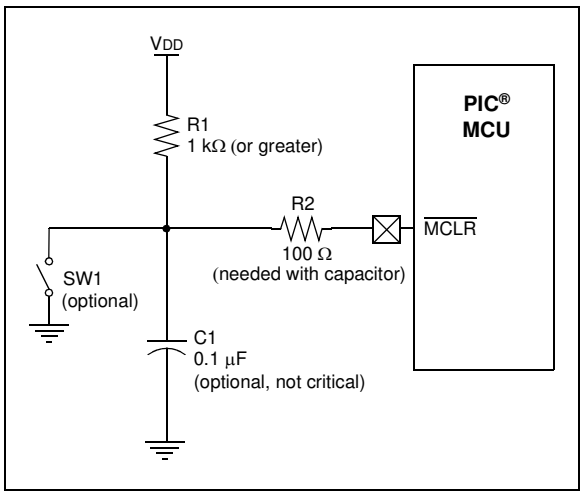
PIC12F609/615/617/12HV609/615 has a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive MCLR pin low.

Voltages applied to the MCLR pin that exceed its specification can result in both MCLR Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the MCLR pin no longer be tied directly to VDD. The use of an RC network, as shown in Figure 12-2, is suggested.

An internal MCLR option is enabled by clearing the MCLRE bit in the Configuration Word register. When MCLRE = 0, the Reset signal to the chip is generated internally. When the MCLRE = 1, the GP3/MCLR pin becomes an external Reset input. In this mode, the GP3/MCLR pin has a weak pull-up to VDD.

**FIGURE 12-2: RECOMMENDED MCLR CIRCUIT**




### 12.3.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates from an internal RC oscillator. For more information, see **Section 4.4 "Internal Clock Modes"**. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A Configuration bit, PWRTE, can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should be enabled when Brown-out Reset is enabled, although it is not required.

The Power-up Timer delay will vary from chip-to-chip due to:

- VDD variation
- Temperature variation
- Process variation

See DC parameters for details (**Section 16.0 "Electrical Specifications"**).

| | |
|---|---|
| **Note:** | Voltage spikes below VSS at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the MCLR pin, rather than pulling this pin directly to VSS. |

### 12.3.4 BROWN-OUT RESET (BOR)

The BOREN0 and BOREN1 bits in the Configuration Word register select one of three BOR modes. One mode has been added to allow control of the BOR enable for lower current during Sleep. By selecting BOREN<1:0> = 10, the BOR is automatically disabled in Sleep to conserve power and enabled on wake-up. See Register 12-1 for the Configuration Word definition.

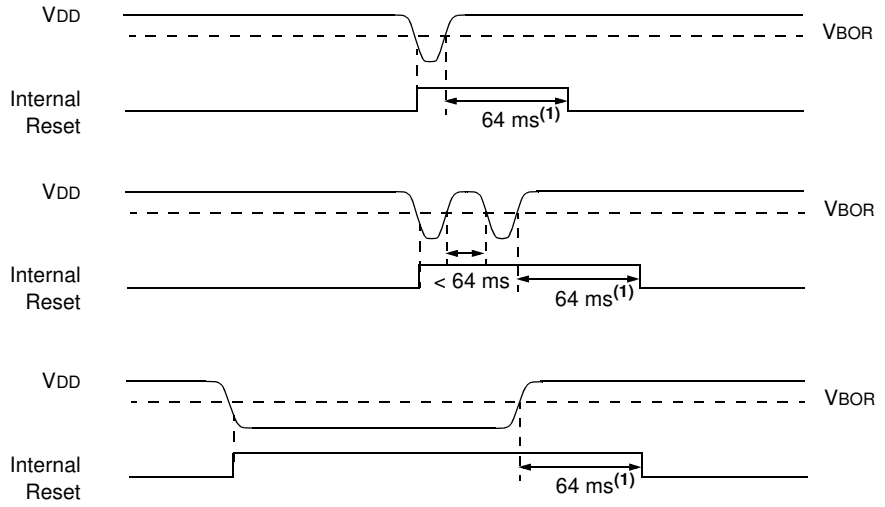
A brown-out occurs when $V_{DD}$ falls below $V_{BOR}$ for greater than parameter $T_{BOR}$ (see **Section 16.0 "Electrical Specifications"**). The brown-out condition will reset the device. This will occur regardless of $V_{DD}$ slew rate. A Brown-out Reset may not occur if $V_{DD}$ falls below $V_{BOR}$ for less than parameter $T_{BOR}$.

On any Reset (Power-on, Brown-out Reset, Watchdog timer, etc.), the chip will remain in Reset until $V_{DD}$ rises above $V_{BOR}$ (see Figure 12-3). If enabled, the Power-up Timer will be invoked by the Reset and keep the chip in Reset an additional 64 ms.

| | |
|---|---|
| **Note:** | The Power-up Timer is enabled by the $\overline{\text{PWRTE}}$ bit in the Configuration Word register. |

If $V_{DD}$ drops below $V_{BOR}$ while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once $V_{DD}$ rises above $V_{BOR}$, the Power-up Timer will execute a 64 ms Reset.

**FIGURE 12-3: BROWN-OUT SITUATIONS**




**Note 1:** 64 ms delay only if $\overline{\text{PWRTE}}$ bit is programmed to '0'.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### 12.3.5 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows:

- PWRT time-out is invoked after POR has expired.
- OST is activated after the PWRT time-out has expired.

The total time-out will vary based on oscillator configuration and $\overline{\text{PWRTE}}$ bit status. For example, in EC mode with $\overline{\text{PWRTE}}$ bit erased (PWRT disabled), there will be no time-out at all. Figure 12-4, Figure 12-5 and Figure 12-6 depict time-out sequences.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then, bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 12-5). This is useful for testing purposes or to synchronize more than one PIC12F609/615/617/12HV609/615 device operating in parallel.

Table 12-6 shows the Reset conditions for some special registers, while Table 12-5 shows the Reset conditions for all the registers.

### 12.3.6 POWER CONTROL (PCON) REGISTER

The Power Control register PCON (address 8Eh) has two Status bits to indicate what type of Reset occurred last.

Bit 0 is $\overline{\text{BOR}}$ (Brown-out). $\overline{\text{BOR}}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if $\overline{\text{BOR}}$ = 0, indicating that a Brown-out has occurred. The $\overline{\text{BOR}}$ Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (BOREN<1:0> = 00 in the Configuration Word register).

Bit 1 is $\overline{\text{POR}}$ (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if $\overline{\text{POR}}$ is '0', it will indicate that a Power-on Reset has occurred (i.e., VDD may have gone too low).

For more information, see **Section 12.3.4 "Brown-out Reset (BOR)"**.

**TABLE 12-1: TIME-OUT IN VARIOUS SITUATIONS**

| Oscillator Configuration | Power-up | | Brown-out Reset | | Wake-up from Sleep |
|---|---|---|---|---|---|
| | $\overline{\text{PWRTE}}$ = 0 | $\overline{\text{PWRTE}}$ = 1 | $\overline{\text{PWRTE}}$ = 0 | $\overline{\text{PWRTE}}$ = 1 | |
| XT, HS, LP | TPWRT + 1024 • TOSC | 1024 • TOSC | TPWRT + 1024 • TOSC | 1024 • TOSC | 1024 • TOSC |
| RC, EC, INTOSC | TPWRT | — | TPWRT | — | — |

**TABLE 12-2: STATUS/PCON BITS AND THEIR SIGNIFICANCE**

| $\overline{\text{POR}}$ | $\overline{\text{BOR}}$ | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ | Condition |
|---|---|---|---|---|
| 0 | x | 1 | 1 | Power-on Reset |
| u | 0 | 1 | 1 | Brown-out Reset |
| u | u | 0 | u | WDT Reset |
| u | u | 0 | 0 | WDT Wake-up |
| u | u | u | u | $\overline{\text{MCLR}}$ Reset during normal operation |
| u | u | 1 | 0 | $\overline{\text{MCLR}}$ Reset during Sleep |

**Legend:** u = unchanged, x = unknown

**TABLE 12-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT RESET**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets(1) |
|---|---|---|---|---|---|---|---|---|---|---|
| PCON | — | — | — | — | — | — | $\overline{\text{POR}}$ | $\overline{\text{BOR}}$ | ---- --qq | ---- --uu |
| STATUS | IRP | RP1 | RP0 | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ | Z | DC | C | 0001 1xxx | 000q quuu |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by BOR.

**Note 1:** Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

**FIGURE 12-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$): CASE 1**

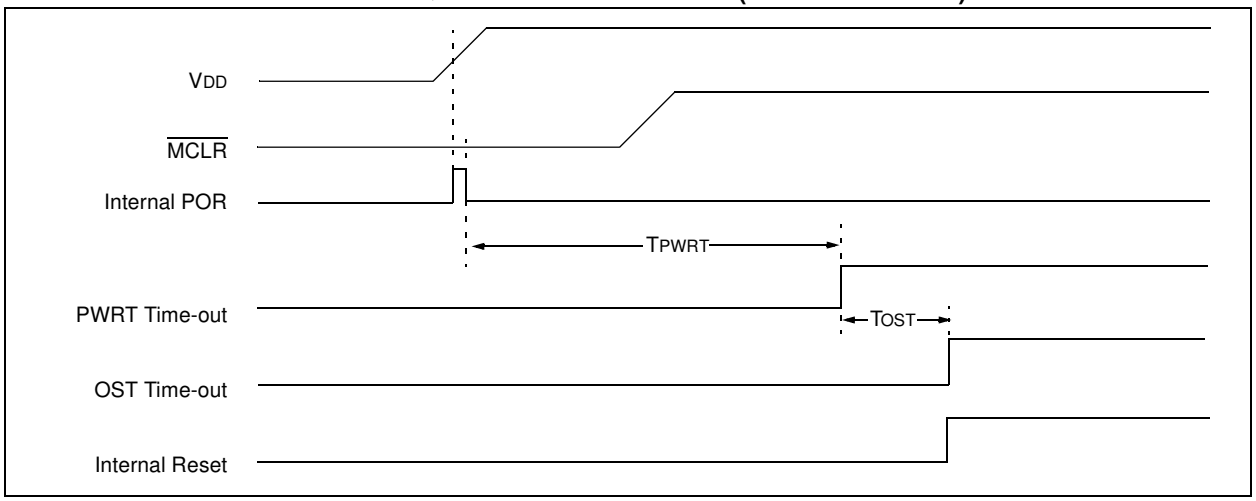


**FIGURE 12-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$): CASE 2**

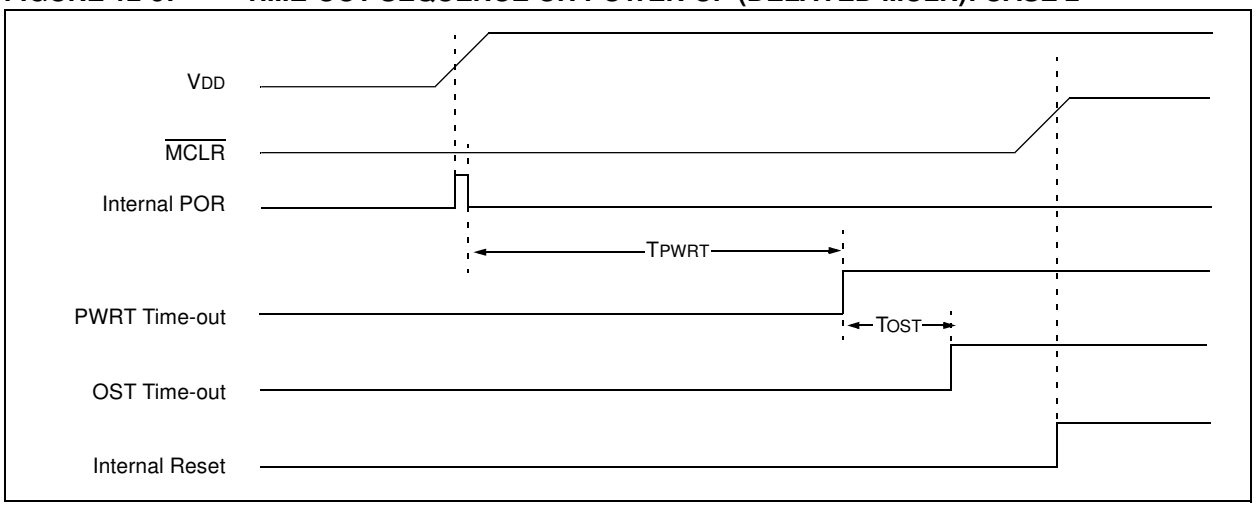


**FIGURE 12-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ WITH VDD)**

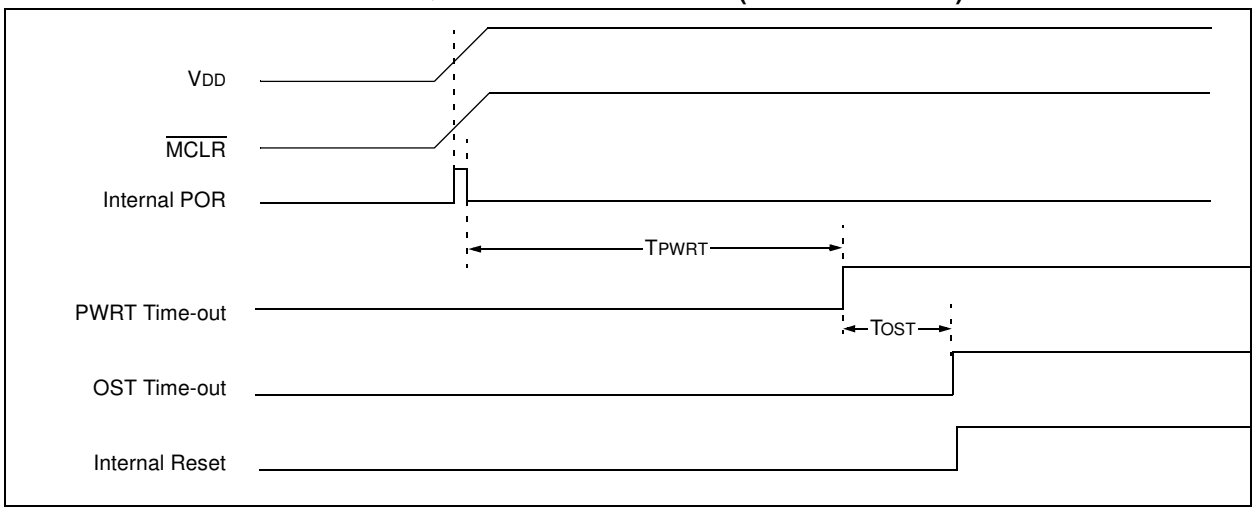



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**TABLE 12-4: INITIALIZATION CONDITION FOR REGISTERS (PIC12F609/HV609)**

| Register | Address | Power-on Reset | $\overline{\text{MCLR}}$ Reset<br>WDT Reset<br>Brown-out Reset(1) | Wake-up from Sleep through Interrupt<br>Wake-up from Sleep through WDT Time-out |
|---|---|---|---|---|
| W | — | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| INDF | 00h/80h | xxxx xxxx | xxxx xxxx | uuuu uuuu |
| TMR0 | 01h | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PCL | 02h/82h | 0000 0000 | 0000 0000 | PC + 1(3) |
| STATUS | 03h/83h | 0001 1xxx | 000q quuu(4) | uuuq quuu(4) |
| FSR | 04h/84h | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| GPIO | 05h | --x0 x000 | --u0 u000 | --uu uuuu |
| PCLATH | 0Ah/8Ah | ---0 0000 | ---0 0000 | ---u uuuu |
| INTCON | 0Bh/8Bh | 0000 0000 | 0000 0000 | uuuu uuuu(2) |
| PIR1 | 0Ch | ----- 0--0 | ---- 0--0 | ---- u--u(2) |
| TMR1L | 0Eh | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| TMR1H | 0Fh | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| T1CON | 10h | 0000 0000 | uuuu uuuu | -uuu uuuu |
| VRCON | 19h | 0-00 0000 | 0-00 0000 | u-uu uuuu |
| CMCON0 | 1Ah | 0000 -0-0 | 0000 -0-0 | uuuu -u-u |
| CMCON1 | 1Ch | ---0 0-10 | ---0 0-10 | ---u u-qu |
| OPTION_REG | 81h | 1111 1111 | 1111 1111 | uuuu uuuu |
| TRISIO | 85h | --11 1111 | --11 1111 | --uu uuuu |
| PIE1 | 8Ch | ----- 0--0 | ---- 0--0 | ---- u--u |
| PCON | 8Eh | ---- --0x | ---- --uu(1, 5) | ---- --uu |
| OSCTUNE | 90h | ---0 0000 | ---u uuuu | ---u uuuu |
| WPU | 95h | --11 -111 | --11 -111 | --uu -uuu |
| IOC | 96h | --00 0000 | --00 0000 | --uu uuuu |
| ANSEL | 9Fh | ---- 1-11 | ---- 1-11 | ---- q-qq |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition.

**Note 1:** If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

**2:** One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

**3:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**4:** See Table 12-6 for Reset value for specific condition.

**5:** If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

### TABLE 12-5: INITIALIZATION CONDITION FOR REGISTERS (PIC12F615/617/HV615)

| Register | Address | Power-on Reset | $\overline{\text{MCLR}}$ Reset<br>WDT Reset<br>Brown-out Reset(1) | Wake-up from Sleep through Interrupt<br>Wake-up from Sleep through WDT Time-out |
|---|---|---|---|---|
| W | — | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| INDF | 00h/80h | xxxx xxxx | xxxx xxxx | uuuu uuuu |
| TMR0 | 01h | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PCL | 02h/82h | 0000 0000 | 0000 0000 | PC + 1(3) |
| STATUS | 03h/83h | 0001 1xxx | 000q quuu(4) | uuuq quuu(4) |
| FSR | 04h/84h | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| GPIO | 05h | --x0 x000 | --u0 u000 | --uu uuuu |
| PCLATH | 0Ah/8Ah | ---0 0000 | ---0 0000 | ---u uuuu |
| INTCON | 0Bh/8Bh | 0000 0000 | 0000 0000 | uuuu uuuu(2) |
| PIR1 | 0Ch | -000 0-00 | -000 0-00 | -uuu u-uu(2) |
| TMR1L | 0Eh | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| TMR1H | 0Fh | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| T1CON | 10h | 0000 0000 | uuuu uuuu | -uuu uuuu |
| TMR2(1) | 11h | 0000 0000 | 0000 0000 | uuuu uuuu |
| T2CON(1) | 12h | -000 0000 | -000 0000 | -uuu uuuu |
| CCPR1L(1) | 13h | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| CCPR1H(1) | 14h | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| CCP1CON(1) | 15h | 0-00 0000 | 0-00 0000 | u-uu uuuu |
| PWM1CON(1) | 16h | 0000 0000 | 0000 0000 | uuuu uuuu |
| ECCPAS(1) | 17h | 0000 0000 | 0000 0000 | uuuu uuuu |
| VRCON | 19h | 0-00 0000 | 0-00 0000 | u-uu uuuu |
| CMCON0 | 1Ah | 0000 -0-0 | 0000 -0-0 | uuuu -u-u |
| CMCON1 | 1Ch | ---0 0-10 | ---0 0-10 | ---u u-qu |
| ADRESH(1) | 1Eh | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| ADCON0(1) | 1Fh | 00-0 0000 | 00-0 0000 | uu-u uuuu |
| OPTION_REG | 81h | 1111 1111 | 1111 1111 | uuuu uuuu |
| TRISIO | 85h | --11 1111 | --11 1111 | --uu uuuu |
| PIE1 | 8Ch | -00- 0-00 | -00- 0-00 | -uu- u-uu |
| PCON | 8Eh | ---- --0x | ---- --uu(1, 5) | ---- --uu |
| OSCTUNE | 90h | ---0 0000 | ---u uuuu | ---u uuuu |
| PR2 | 92h | 1111 1111 | 1111 1111 | 1111 1111 |
| APFCON | 93h | ---0 --00 | ---0 --00 | ---u --uu |
| WPU | 95h | --11 -111 | --11 -111 | --uu -uuu |
| IOC | 96h | --00 0000 | --00 0000 | --uu uuuu |
| PMCON1(6) | 98h | ---- -000 | ---- -000 | ---- -uuu |
| PMCON2(6) | 99h | ---- ---- | ---- ---- | ---- ---- |
| PMADRL(6) | 9Ah | 0000 0000 | 0000 0000 | uuuu uuuu |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition.

**Note 1:** If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

**2:** One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

**3:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**4:** See Table 12-6 for Reset value for specific condition.

**5:** If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

**6:** For PIC12F617 only.


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**TABLE 12-5: INITIALIZATION CONDITION FOR REGISTERS (CONTINUED)(PIC12F615/617/HV615)**

| Register | Address | Power-on Reset | $\overline{\text{MCLR}}$ Reset<br>WDT Reset (Continued)<br>Brown-out Reset(1) | Wake-up from Sleep through Interrupt<br>Wake-up from Sleep through WDT Time-out (Continued) |
|---|---|---|---|---|
| PMADRH(6) | 9Bh | ---- -000 | ---- -000 | ---- -uuu |
| PMDATL(6) | 9Ch | 0000 0000 | 0000 0000 | uuuu uuuu |
| PMDATH(6) | 9Dh | --00 0000 | --00 0000 | --uu uuuu |
| ADRESL(1) | 9Eh | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| ANSEL | 9Fh | -000 1111 | -000 1111 | -uuu qqqq |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition.

**Note 1:** If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

**2:** One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

**3:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**4:** See Table 12-6 for Reset value for specific condition.

**5:** If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

**6:** For PIC12F617 only.

**TABLE 12-6: INITIALIZATION CONDITION FOR SPECIAL REGISTERS**

| Condition | Program Counter | Status Register | PCON Register |
|---|---|---|---|
| Power-on Reset | 000h | 0001 1xxx | ---- --0x |
| $\overline{\text{MCLR}}$ Reset during normal operation | 000h | 000u uuuu | ---- --uu |
| $\overline{\text{MCLR}}$ Reset during Sleep | 000h | 0001 0uuu | ---- --uu |
| WDT Reset | 000h | 0000 uuuu | ---- --uu |
| WDT Wake-up | PC + 1 | uuu0 0uuu | ---- --uu |
| Brown-out Reset | 000h | 0001 1uuu | ---- --10 |
| Interrupt Wake-up from Sleep | PC + 1(1) | uuu1 0uuu | ---- --uu |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, reads as '0'.

**Note 1:** When the wake-up is due to an interrupt and Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

## 12.4 Interrupts

The PIC12F609/615/617/12HV609/615 has 8 sources of interrupt:

- External Interrupt GP2/INT
- Timer0 Overflow Interrupt
- GPIO Change Interrupts
- Comparator Interrupt
- A/D Interrupt (PIC12F615/617/HV615 only)
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt (PIC12F615/617/HV615 only)
- Enhanced CCP Interrupt (PIC12F615/617/HV615 only)
- Flash Memory Self Write (PIC12F617 only)

The Interrupt Control register (INTCON) and Peripheral Interrupt Request Register 1 (PIR1) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

The Global Interrupt Enable bit, GIE of the INTCON register, enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register and PIE1 register. GIE is cleared on Reset.

When an interrupt is serviced, the following actions occur automatically:

- The GIE is cleared to disable any further interrupt.
- The return address is pushed onto the stack.
- The PC is loaded with 0004h.

The Return from Interrupt instruction, `RETFIE`, exits the interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- GPIO Change Interrupt
- Timer0 Overflow Interrupt

The peripheral interrupt flags are contained in the special register, PIR1. The corresponding interrupt enable bit is contained in special register, PIE1.

The following interrupt flags are contained in the PIR1 register:

- A/D Interrupt
- Comparator Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- Enhanced CCP Interrupt

For external interrupt events, such as the INT pin or GPIO change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 12-8). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

| | |
|---|---|
| **Note 1:** | Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit. |
| **2:** | When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again. |

For additional information on Timer1, Timer2, comparators, ADC, Enhanced CCP modules, refer to the respective peripheral section.

### 12.4.1 GP2/INT INTERRUPT

The external interrupt on the GP2/INT pin is edge-triggered; either on the rising edge if the INTEDG bit of the OPTION register is set, or the falling edge, if the INTEDG bit is clear. When a valid edge appears on the GP2/INT pin, the INTF bit of the INTCON register is set. This interrupt can be disabled by clearing the INTE control bit of the INTCON register. The INTF bit must be cleared by software in the Interrupt Service Routine before re-enabling this interrupt. The GP2/INT interrupt can wake-up the processor from Sleep, if the INTE bit was set prior to going into Sleep. See **Section 12.7 “Power-Down Mode (Sleep)”** for details on Sleep and Figure 12-9 for timing of wake-up from Sleep through GP2/INT interrupt.

| | |
|---|---|
| **Note:** | The ANSEL register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read ‘0’ and cannot generate an interrupt. |


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### 12.4.2 TIMER0 INTERRUPT

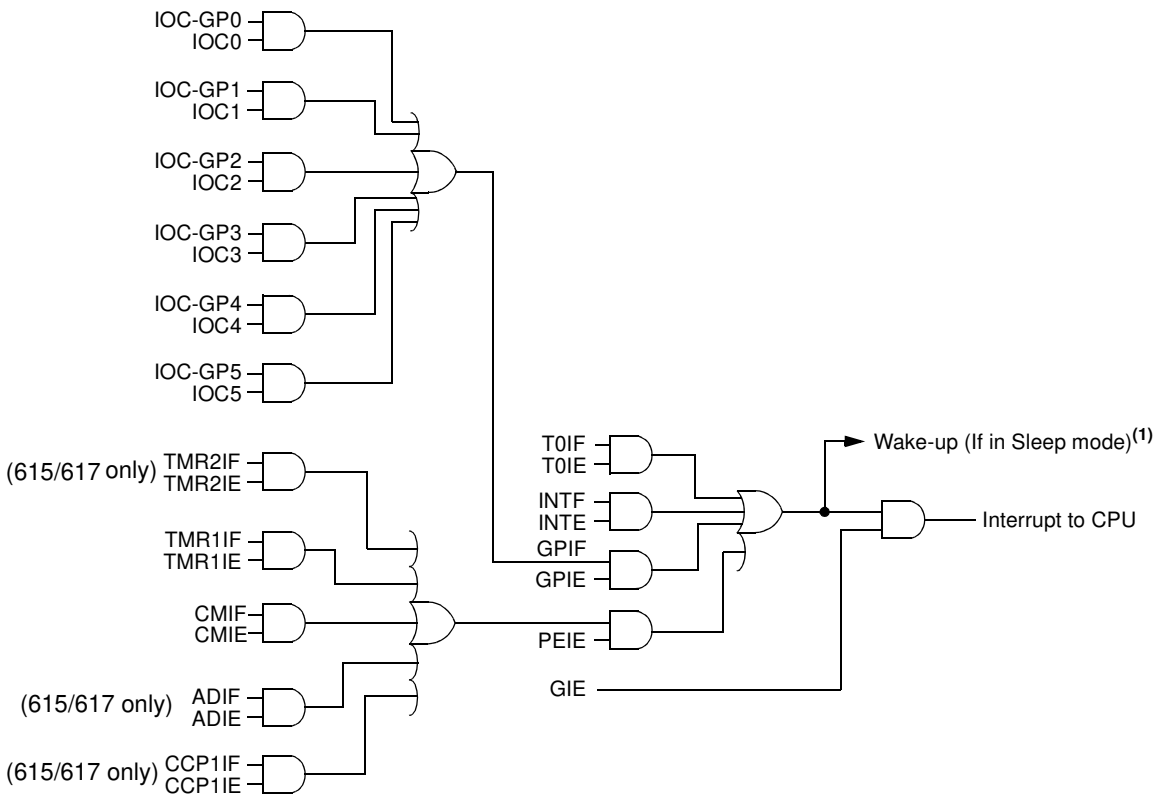
An overflow (FFh → 00h) in the TMR0 register will set the T0IF bit of the INTCON register. The interrupt can be enabled/disabled by setting/clearing T0IE bit of the INTCON register. See **Section 6.0 "Timer0 Module"** for operation of the Timer0 module.

### 12.4.3 GPIO INTERRUPT-ON-CHANGE

An input change on GPIO sets the GPIF bit of the INTCON register. The interrupt can be enabled/disabled by setting/clearing the GPIE bit of the INTCON register. Plus, individual pins can be configured through the IOC register.

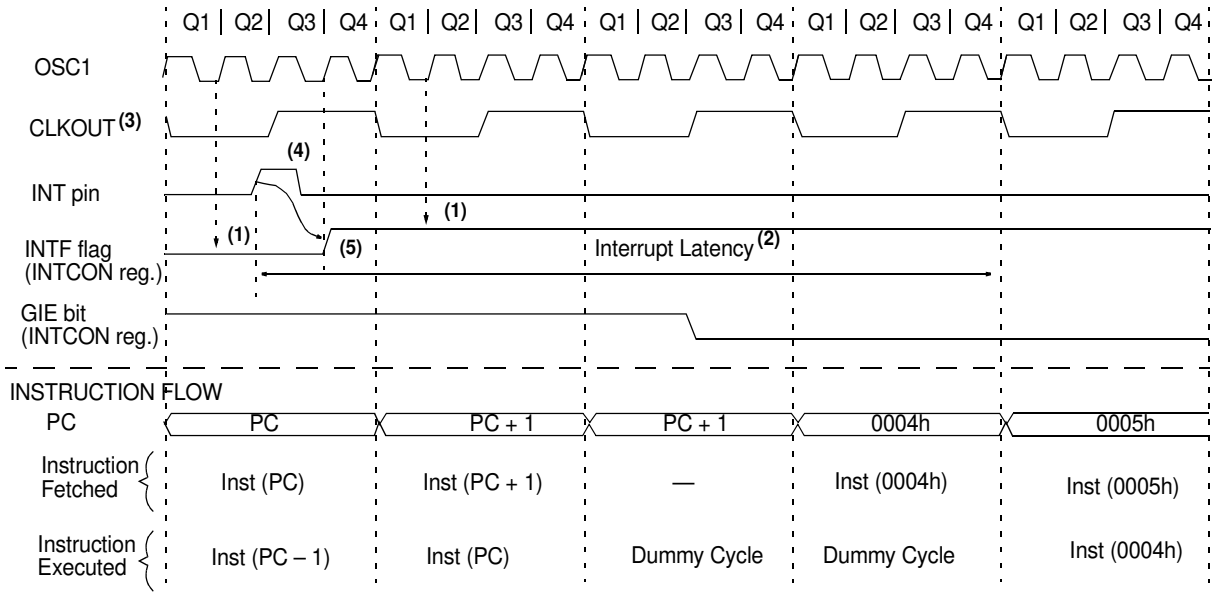
| | |
|---|---|
| **Note:** | If a change on the I/O pin should occur when any GPIO operation is being executed, then the GPIF interrupt flag may not get set. |

**FIGURE 12-7: INTERRUPT LOGIC**




**Note 1:** Some peripherals depend upon the system clock for operation. Since the system clock is suspended during Sleep, only those peripherals which do not depend upon the system clock will wake the part from Sleep. See **Section 12.7.1 "Wake-up from Sleep"**.

**FIGURE 12-8: INT PIN INTERRUPT TIMING**




**Note 1:** INTF flag is sampled here (every Q1).

**2:** Asynchronous interrupt latency = 3-4 TCY. Synchronous latency = 3 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

**3:** CLKOUT is available only in INTOSC and RC Oscillator modes.

**4:** For minimum width of INT pulse, refer to AC specifications in **Section 16.0 "Electrical Specifications"**.

**5:** INTF is enabled to be set any time during the Q4-Q1 cycles.

**TABLE 12-7: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF | 0000 0000 | 0000 0000 |
| IOC | — | — | IOC5 | IOC4 | IOC3 | IOC2 | IOC1 | IOC0 | --00 0000 | --00 0000 |
| PIR1 | — | ADIF(1) | CCP1IF(1) | — | CMIF | — | TMR2IF(1) | TMR1IF | -00- 0-00 | -000 0-00 |
| PIE1 | — | ADIE(1) | CCP1IE(1) | — | CMIE | — | TMR2IE(1) | TMR1IE | -00- 0-00 | -000 0-00 |

**Legend:** x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by the interrupt module.

**Note 1:** PIC12F615/617/HV615 only.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## 12.5 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Temporary holding registers W_TEMP and STATUS_TEMP should be placed in the last 16 bytes of GPR (see Figure 2-3). These 16 locations are common to all banks and do not require banking. This makes context save and restore operations simpler. The code shown in Example 12-1 can be used to:

- Store the W register
- Store the STATUS register
- Execute the ISR code
- Restore the Status (and Bank Select Bit register)
- Restore the W register

**Note:** The PIC12F609/615/617/12HV609/615 does not require saving the PCLATH. However, if computed GOTOs are used in both the ISR and the main code, the PCLATH must be saved and restored in the ISR.

**EXAMPLE 12-1: SAVING STATUS AND W REGISTERS IN RAM**

```
MOVWF   W_TEMP              ;Copy W to TEMP register
SWAPF   STATUS,W            ;Swap status to be saved into W
                            ;Swaps are used because they do not affect the status bits
MOVWF   STATUS_TEMP         ;Save status to bank zero STATUS_TEMP register
:
:(ISR)                      ;Insert user code here
:
SWAPF   STATUS_TEMP,W       ;Swap STATUS_TEMP register into W
                            ;(sets bank to original state)
MOVWF   STATUS              ;Move W into STATUS register
SWAPF   W_TEMP,F            ;Swap W_TEMP
SWAPF   W_TEMP,W            ;Swap W_TEMP into W
```

## 12.6 Watchdog Timer (WDT)

The Watchdog Timer is a free running, on-chip RC oscillator, which requires no external components. This RC oscillator is separate from the external RC oscillator of the CLKIN pin and INTOSC. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped (for example, by execution of a SLEEP instruction). During normal operation, a WDT time out generates a device Reset. If the device is in Sleep mode, a WDT time out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the Configuration bit, WDTE, as clear (**Section 12.1 “Configuration Bits”**).

### 12.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms (with no prescaler). The time-out periods vary with temperature, $V_{DD}$ and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

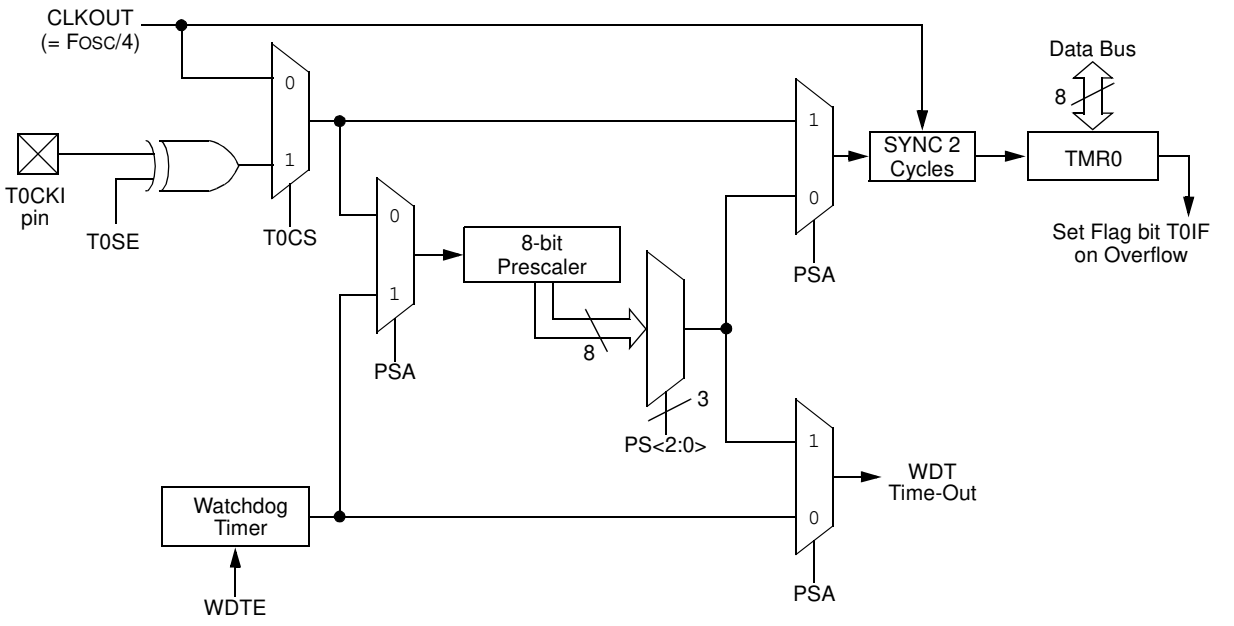
The CLRWDT and SLEEP instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device Reset.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer time out.

### 12.6.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst-case conditions (i.e., VDD = Min., Temperature = Max., Max. WDT prescaler) it may take several seconds before a WDT time out occurs.

**FIGURE 12-2: WATCHDOG TIMER BLOCK DIAGRAM**




**Note 1:** T0SE, T0CS, PSA, PS<2:0> are bits in the OPTION register.

**TABLE 12-8: WDT STATUS**

| Conditions | WDT |
|---|---|
| WDTE = 0 | Cleared |
| CLRWDT Command | |
| Oscillator Fail Detected | |
| Exit Sleep + System Clock = T1OSC, EXTRC, INTRC, EXTCLK | |
| Exit Sleep + System Clock = XT, HS, LP | Cleared until the end of OST |

**TABLE 12-9: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| OPTION_REG | $\overline{\text{GPPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| CONFIG | IOSCFS | $\overline{\text{CP}}$ | MCLRE | $\overline{\text{PWRTE}}$ | WDTE | FOSC2 | FOSC1 | FOSC0 | — | — |

**Legend:** Shaded cells are not used by the Watchdog Timer.
**Note 1:** See Register 12-1 for operation of all Configuration Word register bits.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## 12.7 Power-Down Mode (Sleep)

The Power-Down mode is entered by executing a SLEEP instruction.

If the Watchdog Timer is enabled:

- WDT will be cleared but keeps running.
- $\overline{PD}$ bit in the STATUS register is cleared.
- $\overline{TO}$ bit is set.
- Oscillator driver is turned off.
- I/O ports maintain the status they had before SLEEP was executed (driving high, low or high-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD or VSS, with no external circuitry drawing current from the I/O pin and the comparators and CVREF should be disabled. I/O pins that are high-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on GPIO should be considered.

The $\overline{MCLR}$ pin must be at a logic high level.

| | |
|---|---|
| **Note:** | It should be noted that a Reset generated by a WDT time-out does not drive $\overline{MCLR}$ pin low. |

### 12.7.1 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

1. External Reset input on $\overline{MCLR}$ pin.
2. Watchdog Timer wake-up (if WDT was enabled).
3. Interrupt from GP2/INT pin, GPIO change or a peripheral interrupt.

The first event will cause a device Reset. The two latter events are considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device Reset. The $\overline{PD}$ bit, which is set on power-up, is cleared when Sleep is invoked. $\overline{TO}$ bit is cleared if WDT wake-up occurred.

The following peripheral interrupts can wake the device from Sleep:

1. Timer1 interrupt. Timer1 must be operating as an asynchronous counter.
2. ECCP Capture mode interrupt.
3. A/D conversion (when A/D clock source is RC).
4. Comparator output changes state.
5. Interrupt-on-change.
6. External Interrupt from INT pin.

Other peripherals cannot generate interrupts since during Sleep, no on-chip clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction, then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

| | |
|---|---|
| **Note:** | If the global interrupts are disabled (GIE is cleared) and any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from Sleep. |

The WDT is cleared when the device wakes up from Sleep, regardless of the source of wake-up.

### 12.7.2 WAKE-UP USING INTERRUPTS

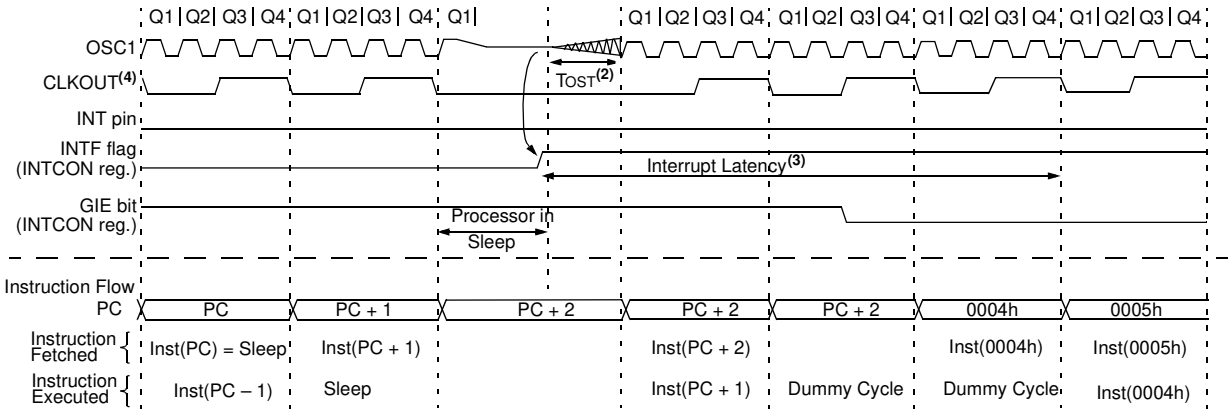
When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will not be cleared, the $\overline{TO}$ bit will not be set and the $\overline{PD}$ bit will not be cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will Immediately wake-up from Sleep. The SLEEP instruction is executed. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will be cleared, the $\overline{TO}$ bit will be set and the $\overline{PD}$ bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction. See Figure 12-9 for more details.

**FIGURE 12-9: WAKE-UP FROM SLEEP THROUGH INTERRUPT**




**Note 1:** XT, HS or LP Oscillator mode assumed.

**2:** TOST = 1024 TOSC (drawing not to scale). This delay does not apply to EC, INTOSC and RC Oscillator modes.

**3:** GIE = '1' assumed. In this case after wake-up, the processor jumps to 0004h. If GIE = '0', execution will continue in-line.

**4:** CLKOUT is not available in XT, HS, LP or EC Oscillator modes, but shown here for timing reference.

## 12.8 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP™ for verification purposes.

| | |
|---|---|
| **Note:** | The entire Flash program memory will be erased when the code protection is turned off. See the *MemoryProgramming Specification* (DS41204) for more information. |

## 12.9 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable during Program/Verify mode. Only the Least Significant 7 bits of the ID locations are used.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## 12.10 In-Circuit Serial Programming™

ThePIC12F609/615/617/12HV609/615 microcontrollers can be serially programmed while in the end application circuit. This is simply done with five connections for:

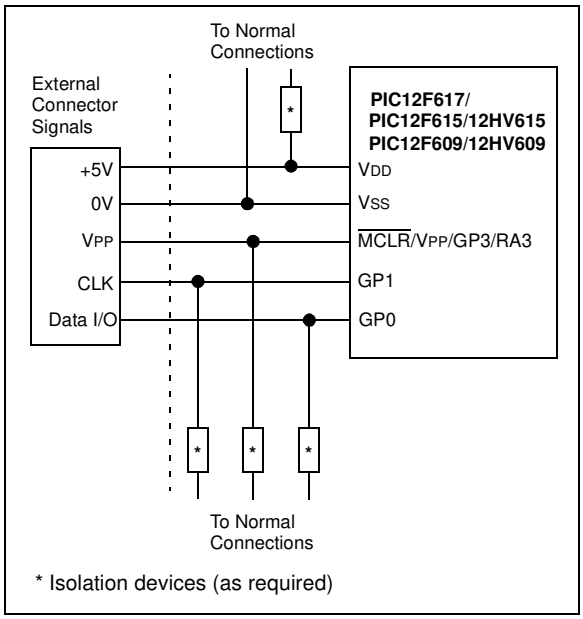
- clock
- data
- power
- ground
- programming voltage

This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a Program/Verify mode by holding the GP0 and GP1 pins low, while raising the $\overline{\text{MCLR}}$ (VPP) pin from VIL to VIHH. See the *Memory Programming Specification* (DS41284) for more information. GP0 becomes the programming data and GP1 becomes the programming clock. Both GP0 and GP1 are Schmitt Trigger inputs in Program/Verify mode.

A typical In-Circuit Serial Programming connection is shown in Figure 12-10.

**FIGURE 12-10: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION**




**Note:** To erase the device VDD must be above the Bulk Erase VDD minimum given in the *Memory Programming Specification* (DS41284)

## 12.11 In-Circuit Debugger

Since in-circuit debugging requires access to three pins, MPLAB® ICD 2 development with an 14-pin device is not practical. A special 28-pin PIC12F609/615/617/12HV609/615 ICD device is used with MPLAB ICD 2 to provide separate clock, data and $\overline{\text{MCLR}}$ pins and frees all normally available pins to the user.

A special debugging adapter allows the ICD device to be used in place of a PIC12F609/615/617/12HV609/615 device. The debugging adapter is the only source of the ICD device.

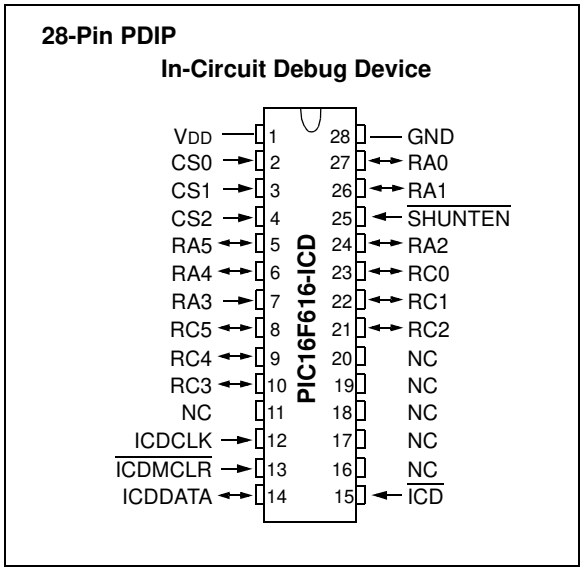
When the $\overline{\text{ICD}}$ pin on the PIC12F609/615/617/12HV609/615 ICD device is held low, the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB ICD 2. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 12-10 shows which features are consumed by the background debugger.

**TABLE 12-10: DEBUGGER RESOURCES**

| Resource | Description |
|---|---|
| I/O pins | ICDCLK, ICDDATA |
| Stack | 1 level |
| Program Memory | Address 0h must be NOP<br>700h-7FFh |

For more information, see "*MPLAB® ICD 2 In-Circuit Debugger User's Guide*" (DS51331), available on Microchip's web site (www.microchip.com).

**FIGURE 12-11: 28 PIN ICD PINOUT**



**NOTES:**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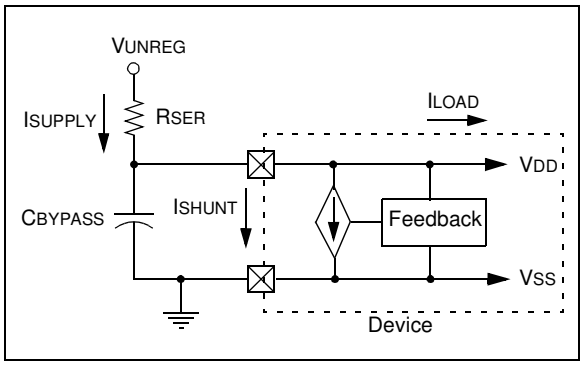
## 13.0 VOLTAGE REGULATOR

The PIC12HV609/HV615 devices include a permanent internal 5 volt (nominal) shunt regulator in parallel with the VDD pin. This eliminates the need for an external voltage regulator in systems sourced by an unregulated supply. All external devices connected directly to the VDD pin will share the regulated supply voltage and contribute to the total VDD supply current (ILOAD).

### 13.1 Regulator Operation

A shunt regulator generates a specific supply voltage by creating a voltage drop across a pass resistor RSER. The voltage at the VDD pin of the microcontroller is monitored and compared to an internal voltage reference. The current through the resistor is then adjusted, based on the result of the comparison, to produce a voltage drop equal to the difference between the supply voltage VUNREG and the VDD of the microcontroller. See Figure 13-1 for voltage regulator schematic.

**FIGURE 13-1: VOLTAGE REGULATOR**




An external current limiting resistor, RSER, located between the unregulated supply, VUNREG, and the VDD pin, drops the difference in voltage between VUNREG and VDD. RSER must be between RMAX and RMIN as defined by Equation 13-1.

**EQUATION 13-1: RSER LIMITING RESISTOR**

$$R_{MAX} = \frac{(VU_{MIN} - 5V)}{1.05 \bullet (4\ mA + I_{LOAD})}$$

$$R_{MIN} = \frac{(VU_{MAX} - 5V)}{0.95 \bullet (50\ mA)}$$

Where:

RMAX = maximum value of RSER (ohms)

RMIN = minimum value of RSER (ohms)

VUMIN = minimum value of VUNREG

VUMAX = maximum value of VUNREG

VDD = regulated voltage (5V nominal)

ILOAD = maximum expected load current in mA including I/O pin currents and external circuits connected to VDD.

1.05 = compensation for +5% tolerance of RSER

0.95 = compensation for -5% tolerance of RSER

### 13.2 Regulator Considerations

The supply voltage VUNREG and load current are not constant. Therefore, the current range of the regulator is limited. Selecting a value for RSER must take these three factors into consideration.

Since the regulator uses the band gap voltage as the regulated voltage reference, this voltage reference is permanently enabled in the PIC12HV609/HV615 devices.

The shunt regulator will still consume current when below operating voltage range for the shunt regulator.

### 13.3 Design Considerations

For more information on using the shunt regulator and managing current load, see Application Note AN1035, "*Designing with HV Microcontrollers*" (DS01035).

**NOTES:**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## 14.0 INSTRUCTION SET SUMMARY

The PIC12F609/615/617/12HV609/615 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode,** which specifies the instruction type and one or more **operands,** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 14-1, while the various opcode fields are summarized in Table 14-1.

Table 14-2 lists the instructions recognized by the MPASM™ assembler.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 μs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a `NOP`.

All instruction examples use the format '`0xhh`' to represent a hexadecimal number, where '`h`' signifies a hexadecimal digit.

### 14.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (RMW) operation. The register is read, the data is modified, and the result is stored according to either the instruction or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

For example, a `CLRF GPIO` instruction will read GPIO, clear all the data bits, then write the result back to GPIO. This example would have the unintended consequence of clearing the condition that set the GPIF flag.

**TABLE 14-1: OPCODE FIELD DESCRIPTIONS**

| Field | Description |
|---|---|
| f | Register file address (0x00 to 0x7F) |
| W | Working register (accumulator) |
| b | Bit address within an 8-bit file register |
| k | Literal field, constant data or label |
| x | Don't care location (= `0` or `1`).<br>The assembler will generate code with x = `0`.<br>It is the recommended form of use for compatibility with all Microchip software tools. |
| d | Destination select; d = `0`: store result in W,<br>d = `1`: store result in file register f.<br>Default is d = `1`. |
| PC | Program Counter |
| $\overline{TO}$ | Time-out bit |
| C | Carry bit |
| DC | Digit carry bit |
| Z | Zero bit |
| $\overline{PD}$ | Power-down bit |

**FIGURE 14-1: GENERAL FORMAT FOR INSTRUCTIONS**

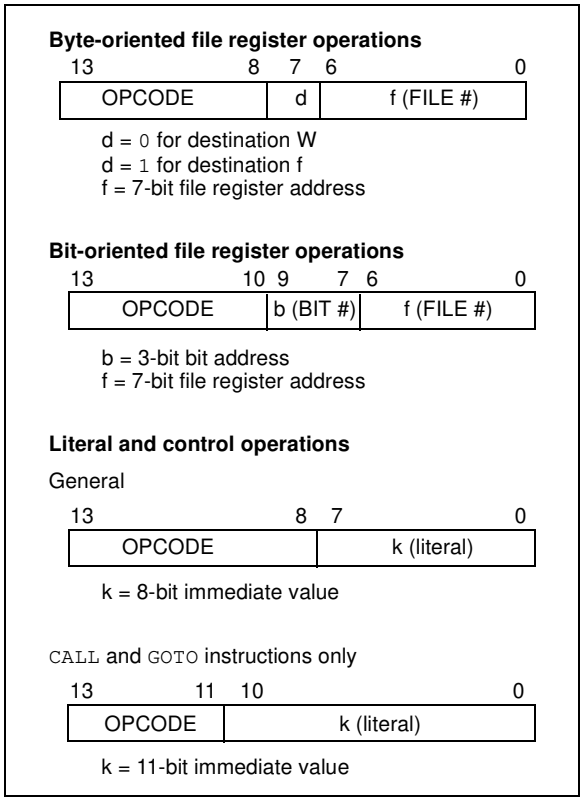

**TABLE 14-2: PIC12F609/615/617/12HV609/615 INSTRUCTION SET**

| Mnemonic, Operands | | Description | Cycles | 14-Bit Opcode MSb | | | LSb | Status Affected | Notes |
|---|---|---|---|---|---|---|---|---|---|
| **BYTE-ORIENTED FILE REGISTER OPERATIONS** | | | | | | | | | |
| ADDWF | f, d | Add W and f | 1 | 00 | 0111 | dfff | ffff | C, DC, Z | **1, 2** |
| ANDWF | f, d | AND W with f | 1 | 00 | 0101 | dfff | ffff | Z | **1, 2** |
| CLRF | f | Clear f | 1 | 00 | 0001 | 1fff | ffff | Z | **2** |
| CLRW | – | Clear W | 1 | 00 | 0001 | 0xxx | xxxx | Z | |
| COMF | f, d | Complement f | 1 | 00 | 1001 | dfff | ffff | Z | **1, 2** |
| DECF | f, d | Decrement f | 1 | 00 | 0011 | dfff | ffff | Z | **1, 2** |
| DECFSZ | f, d | Decrement f, Skip if 0 | 1**(2)** | 00 | 1011 | dfff | ffff | | **1, 2, 3** |
| INCF | f, d | Increment f | 1 | 00 | 1010 | dfff | ffff | Z | **1, 2** |
| INCFSZ | f, d | Increment f, Skip if 0 | 1**(2)** | 00 | 1111 | dfff | ffff | | **1, 2, 3** |
| IORWF | f, d | Inclusive OR W with f | 1 | 00 | 0100 | dfff | ffff | Z | **1, 2** |
| MOVF | f, d | Move f | 1 | 00 | 1000 | dfff | ffff | Z | **1, 2** |
| MOVWF | f | Move W to f | 1 | 00 | 0000 | 1fff | ffff | | |
| NOP | – | No Operation | 1 | 00 | 0000 | 0xx0 | 0000 | | |
| RLF | f, d | Rotate Left f through Carry | 1 | 00 | 1101 | dfff | ffff | C | **1, 2** |
| RRF | f, d | Rotate Right f through Carry | 1 | 00 | 1100 | dfff | ffff | C | **1, 2** |
| SUBWF | f, d | Subtract W from f | 1 | 00 | 0010 | dfff | ffff | C, DC, Z | **1, 2** |
| SWAPF | f, d | Swap nibbles in f | 1 | 00 | 1110 | dfff | ffff | | **1, 2** |
| XORWF | f, d | Exclusive OR W with f | 1 | 00 | 0110 | dfff | ffff | Z | **1, 2** |
| **BIT-ORIENTED FILE REGISTER OPERATIONS** | | | | | | | | | |
| BCF | f, b | Bit Clear f | 1 | 01 | 00bb | bfff | ffff | | **1, 2** |
| BSF | f, b | Bit Set f | 1 | 01 | 01bb | bfff | ffff | | **1, 2** |
| BTFSC | f, b | Bit Test f, Skip if Clear | 1 **(2)** | 01 | 10bb | bfff | ffff | | **3** |
| BTFSS | f, b | Bit Test f, Skip if Set | 1 **(2)** | 01 | 11bb | bfff | ffff | | **3** |
| **LITERAL AND CONTROL OPERATIONS** | | | | | | | | | |
| ADDLW | k | Add literal and W | 1 | 11 | 111x | kkkk | kkkk | C, DC, Z | |
| ANDLW | k | AND literal with W | 1 | 11 | 1001 | kkkk | kkkk | Z | |
| CALL | k | Call Subroutine | 2 | 10 | 0kkk | kkkk | kkkk | | |
| CLRWDT | – | Clear Watchdog Timer | 1 | 00 | 0000 | 0110 | 0100 | $\overline{TO}$, $\overline{PD}$ | |
| GOTO | k | Go to address | 2 | 10 | 1kkk | kkkk | kkkk | | |
| IORLW | k | Inclusive OR literal with W | 1 | 11 | 1000 | kkkk | kkkk | Z | |
| MOVLW | k | Move literal to W | 1 | 11 | 00xx | kkkk | kkkk | | |
| RETFIE | – | Return from interrupt | 2 | 00 | 0000 | 0000 | 1001 | | |
| RETLW | k | Return with literal in W | 2 | 11 | 01xx | kkkk | kkkk | | |
| RETURN | – | Return from Subroutine | 2 | 00 | 0000 | 0000 | 1000 | | |
| SLEEP | – | Go into Standby mode | 1 | 00 | 0000 | 0110 | 0011 | $\overline{TO}$, $\overline{PD}$ | |
| SUBLW | k | Subtract W from literal | 1 | 11 | 110x | kkkk | kkkk | C, DC, Z | |
| XORLW | k | Exclusive OR literal with W | 1 | 11 | 1010 | kkkk | kkkk | Z | |

**Note 1:** When an I/O register is modified as a function of itself (e.g., `MOVF GPIO, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

**2:** If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

**3:** If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.


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## 14.2 Instruction Descriptions

| ADDLW | Add literal and W |
|---|---|
| Syntax: | [ *label* ] ADDLW k |
| Operands: | $0 \le k \le 255$ |
| Operation: | (W) + k → (W) |
| Status Affected: | C, DC, Z |
| Description: | The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register. |

| ADDWF | Add W and f |
|---|---|
| Syntax: | [ *label* ] ADDWF f,d |
| Operands: | $0 \le f \le 127$<br>$d \in [0,1]$ |
| Operation: | (W) + (f) → (destination) |
| Status Affected: | C, DC, Z |
| Description: | Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'. |

| ANDLW | AND literal with W |
|---|---|
| Syntax: | [ *label* ] ANDLW k |
| Operands: | $0 \le k \le 255$ |
| Operation: | (W) .AND. (k) → (W) |
| Status Affected: | Z |
| Description: | The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register. |

| ANDWF | AND W with f |
|---|---|
| Syntax: | [ *label* ] ANDWF f,d |
| Operands: | $0 \le f \le 127$<br>$d \in [0,1]$ |
| Operation: | (W) .AND. (f) → (destination) |
| Status Affected: | Z |
| Description: | AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'. |

| BCF | Bit Clear f |
|---|---|
| Syntax: | [ *label* ] BCF f,b |
| Operands: | $0 \le f \le 127$<br>$0 \le b \le 7$ |
| Operation: | 0 → (f<b>) |
| Status Affected: | None |
| Description: | Bit 'b' in register 'f' is cleared. |

| BSF | Bit Set f |
|---|---|
| Syntax: | [ *label* ] BSF f,b |
| Operands: | $0 \le f \le 127$<br>$0 \le b \le 7$ |
| Operation: | 1 → (f<b>) |
| Status Affected: | None |
| Description: | Bit 'b' in register 'f' is set. |

| BTFSC | Bit Test f, Skip if Clear |
|---|---|
| Syntax: | [ *label* ] BTFSC f,b |
| Operands: | $0 \le f \le 127$<br>$0 \le b \le 7$ |
| Operation: | skip if (f<b>) = 0 |
| Status Affected: | None |
| Description: | If bit 'b' in register 'f' is '1', the next instruction is executed.<br>If bit 'b' in register 'f' is '0', the next instruction is discarded, and a NOP is executed instead, making this a two-cycle instruction. |

| BTFSS | Bit Test f, Skip if Set |
|---|---|
| Syntax: | [ *label* ] BTFSS f,b |
| Operands: | $0 \le f \le 127$<br>$0 \le b < 7$ |
| Operation: | skip if (f<b>) = 1 |
| Status Affected: | None |
| Description: | If bit 'b' in register 'f' is '0', the next instruction is executed.<br>If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. |

| CALL | Call Subroutine |
|---|---|
| Syntax: | [ *label* ] CALL k |
| Operands: | $0 \le k \le 2047$ |
| Operation: | (PC)+ 1→ TOS,<br>k → PC<10:0>,<br>(PCLATH<4:3>) → PC<12:11> |
| Status Affected: | None |
| Description: | Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction. |

| CLRF | Clear f |
|---|---|
| Syntax: | [ *label* ] CLRF f |
| Operands: | $0 \le f \le 127$ |
| Operation: | 00h → (f)<br>1 → Z |
| Status Affected: | Z |
| Description: | The contents of register 'f' are cleared and the Z bit is set. |

| CLRW | Clear W |
|---|---|
| Syntax: | [ *label* ] CLRW |
| Operands: | None |
| Operation: | 00h → (W)<br>1 → Z |
| Status Affected: | Z |
| Description: | W register is cleared. Zero bit (Z) is set. |

| CLRWDT | Clear Watchdog Timer |
|---|---|
| Syntax: | [ *label* ] CLRWDT |
| Operands: | None |
| Operation: | 00h → WDT<br>0 → WDT prescaler,<br>1 → $\overline{TO}$<br>1 → $\overline{PD}$ |
| Status Affected: | $\overline{TO}$, $\overline{PD}$ |
| Description: | CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT.<br>Status bits $\overline{TO}$ and $\overline{PD}$ are set. |

| COMF | Complement f |
|---|---|
| Syntax: | [ *label* ] COMF f,d |
| Operands: | $0 \le f \le 127$<br>$d \in [0,1]$ |
| Operation: | ($\bar{f}$) → (destination) |
| Status Affected: | Z |
| Description: | The contents of register 'f' are complemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'. |

| DECF | Decrement f |
|---|---|
| Syntax: | [ *label* ] DECF f,d |
| Operands: | $0 \le f \le 127$<br>$d \in [0,1]$ |
| Operation: | (f) - 1 → (destination) |
| Status Affected: | Z |
| Description: | Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'. |


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| DECFSZ | Decrement f, Skip if 0 |
|---|---|
| Syntax: | [ *label* ] DECFSZ f,d |
| Operands: | $0 \le f \le 127$<br>$d \in [0,1]$ |
| Operation: | (f) - 1 → (destination);<br>skip if result = 0 |
| Status Affected: | None |
| Description: | The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.<br>If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a two-cycle instruction. |

| INCFSZ | Increment f, Skip if 0 |
|---|---|
| Syntax: | [ *label* ] INCFSZ f,d |
| Operands: | $0 \le f \le 127$<br>$d \in [0,1]$ |
| Operation: | (f) + 1 → (destination),<br>skip if result = 0 |
| Status Affected: | None |
| Description: | The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.<br>If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a two-cycle instruction. |

| GOTO | Unconditional Branch |
|---|---|
| Syntax: | [ *label* ] GOTO k |
| Operands: | $0 \le k \le 2047$ |
| Operation: | k → PC<10:0><br>PCLATH<4:3> → PC<12:11> |
| Status Affected: | None |
| Description: | GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction. |

| IORLW | Inclusive OR literal with W |
|---|---|
| Syntax: | [ *label* ] IORLW k |
| Operands: | $0 \le k \le 255$ |
| Operation: | (W) .OR. k → (W) |
| Status Affected: | Z |
| Description: | The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register. |

| INCF | Increment f |
|---|---|
| Syntax: | [ *label* ] INCF f,d |
| Operands: | $0 \le f \le 127$<br>$d \in [0,1]$ |
| Operation: | (f) + 1 → (destination) |
| Status Affected: | Z |
| Description: | The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. |

| IORWF | Inclusive OR W with f |
|---|---|
| Syntax: | [ *label* ] IORWF f,d |
| Operands: | $0 \le f \le 127$<br>$d \in [0,1]$ |
| Operation: | (W) .OR. (f) → (destination) |
| Status Affected: | Z |
| Description: | Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. |

| MOVF | Move f |
|---|---|
| Syntax: | [ *label* ] MOVF f,d |
| Operands: | $0 \le f \le 127$<br>$d \in [0,1]$ |
| Operation: | (f) → (dest) |
| Status Affected: | Z |
| Description: | The contents of register 'f' is moved to a destination dependent upon the status of 'd'. If d = 0, destination is W register. If d = 1, the destination is file register 'f' itself. d = 1 is useful to test a file register since Status flag Z is affected. |
| Words: | 1 |
| Cycles: | 1 |
| Example: | `MOVF FSR, 0`<br>After Instruction<br>W = value in FSR register<br>Z = 1 |

| MOVWF | Move W to f |
|---|---|
| Syntax: | [ *label* ] MOVWF f |
| Operands: | $0 \le f \le 127$ |
| Operation: | (W) → (f) |
| Status Affected: | None |
| Description: | Move data from W register to register 'f'. |
| Words: | 1 |
| Cycles: | 1 |
| Example: | `MOVW OPTION F`<br>Before Instruction<br>OPTION = 0xFF<br>W = 0x4F<br>After Instruction<br>OPTION = 0x4F<br>W = 0x4F |

| MOVLW | Move literal to W |
|---|---|
| Syntax: | [ *label* ] MOVLW k |
| Operands: | $0 \le k \le 255$ |
| Operation: | k → (W) |
| Status Affected: | None |
| Description: | The eight-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's. |
| Words: | 1 |
| Cycles: | 1 |
| Example: | `MOVLW 0x5A`<br>After Instruction<br>W = 0x5A |

| NOP | No Operation |
|---|---|
| Syntax: | [ *label* ] NOP |
| Operands: | None |
| Operation: | No operation |
| Status Affected: | None |
| Description: | No operation. |
| Words: | 1 |
| Cycles: | 1 |
| Example: | `NOP` |


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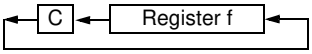
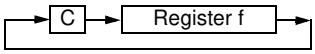
| RETFIE | Return from Interrupt |
|---|---|
| Syntax: | [ *label* ] RETFIE |
| Operands: | None |
| Operation: | TOS → PC,<br>1 → GIE |
| Status Affected: | None |
| Description: | Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INT-CON<7>). This is a two-cycle instruction. |
| Words: | 1 |
| Cycles: | 2 |
| Example: | `RETFIE`<br>After Interrupt<br>PC = TOS<br>GIE = 1 |

| RETLW | Return with literal in W |
|---|---|
| Syntax: | [ *label* ] RETLW k |
| Operands: | $0 \le k \le 255$ |
| Operation: | k → (W);<br>TOS → PC |
| Status Affected: | None |
| Description: | The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction. |
| Words: | 1 |
| Cycles: | 2 |
| Example: | `CALL TABLE;W contains`<br>`;table offset`<br>`;value`<br>`GOTO DONE`<br>`TABLE` •<br>•<br>`ADDWF PC ;W = offset`<br>`RETLW k1 ;Begin table`<br>`RETLW k2 ;`<br>•<br>•<br>•<br>`RETLW kn ;End of table`<br>`DONE`<br>Before Instruction<br>W = 0x07<br>After Instruction<br>W = value of k8 |

| RETURN | Return from Subroutine |
|---|---|
| Syntax: | [ *label* ] RETURN |
| Operands: | None |
| Operation: | TOS → PC |
| Status Affected: | None |
| Description: | Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction. |

| RLF | Rotate Left f through Carry |
|---|---|
| Syntax: | [ *label* ] RLF f,d |
| Operands: | $0 \le f \le 127$<br>$d \in [0,1]$ |
| Operation: | See description below |
| Status Affected: | C |
| Description: | The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.<br>  |
| Words: | 1 |
| Cycles: | 1 |
| Example: | `RLF REG1,0`<br>Before Instruction<br>`REG1 = 1110 0110`<br>`C = 0`<br>After Instruction<br>`REG1 = 1110 0110`<br>`W = 1100 1100`<br>`C = 1` |

| RRF | Rotate Right f through Carry |
|---|---|
| Syntax: | [ *label* ] RRF f,d |
| Operands: | $0 \le f \le 127$<br>$d \in [0,1]$ |
| Operation: | See description below |
| Status Affected: | C |
| Description: | The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.<br>  |

| SLEEP | Enter Sleep mode |
|---|---|
| Syntax: | [ *label* ] SLEEP |
| Operands: | None |
| Operation: | 00h → WDT,<br>0 → WDT prescaler,<br>1 → $\overline{TO}$,<br>0 → $\overline{PD}$ |
| Status Affected: | $\overline{TO}$, $\overline{PD}$ |
| Description: | The power-down Status bit, $\overline{PD}$ is cleared. Time-out Status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.<br>The processor is put into Sleep mode with the oscillator stopped. |

| SUBLW | Subtract W from literal |
|---|---|
| Syntax: | [ *label* ] SUBLW k |
| Operands: | $0 \le k \le 255$ |
| Operation: | k - (W) → (W) |
| Status Affected: | C, DC, Z |
| Description: | The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register. |

| Result | Condition |
|---|---|
| C = 0 | W > k |
| C = 1 | W ≤ k |
| DC = 0 | W<3:0> > k<3:0> |
| DC = 1 | W<3:0> ≤ k<3:0> |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| SUBWF | Subtract W from f |
|---|---|
| Syntax: | [ *label* ] SUBWF f,d |
| Operands: | $0 \le f \le 127$<br>$d \in [0,1]$ |
| Operation: | (f) - (W) → (destination) |
| Status Affected: | C, DC, Z |
| Description: | Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'. |

| | |
|---|---|
| C = 0 | W > f |
| C = 1 | W ≤ f |
| DC = 0 | W<3:0> > f<3:0> |
| DC = 1 | W<3:0> ≤ f<3:0> |

| SWAPF | Swap Nibbles in f |
|---|---|
| Syntax: | [ *label* ] SWAPF f,d |
| Operands: | $0 \le f \le 127$<br>$d \in [0,1]$ |
| Operation: | (f<3:0>) → (destination<7:4>),<br>(f<7:4>) → (destination<3:0>) |
| Status Affected: | None |
| Description: | The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'. |

| XORLW | Exclusive OR literal with W |
|---|---|
| Syntax: | [ *label* ] XORLW k |
| Operands: | $0 \le k \le 255$ |
| Operation: | (W) .XOR. k → (W) |
| Status Affected: | Z |
| Description: | The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register. |

| XORWF | Exclusive OR W with f |
|---|---|
| Syntax: | [ *label* ] XORWF f,d |
| Operands: | $0 \le f \le 127$<br>$d \in [0,1]$ |
| Operation: | (W) .XOR. (f) → (destination) |
| Status Affected: | Z |
| Description: | Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'. |

**NOTES:**


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## 15.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB C Compiler for Various Device Families
  - HI-TECH C for Various Device Families
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
  - MPLAB ICD 3
  - PICkit™ 3 Debug Express
- Device Programmers
  - PICkit™ 2 Programmer
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

### 15.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - In-Circuit Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (C or assembly)
  - Mixed C and assembly
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

## 15.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

## 15.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

## 15.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

## 15.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

## 15.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility


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## 15.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

## 15.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

## 15.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

## 15.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

## 15.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

## 15.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at $V_{DDMIN}$ and $V_{DDMAX}$ for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

## 15.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.


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# 16.0 ELECTRICAL SPECIFICATIONS

## Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40° to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.3V to +6.5V

Voltage on $\overline{MCLR}$ with respect to Vss ..... -0.3V to +13.5V

Voltage on all other pins with respect to $V_{SS}$ ..... -0.3V to ($V_{DD}$ + 0.3V)

Total power dissipation(1) ..... 800 mW

Maximum current out of $V_{SS}$ pin ..... 95 mA

Maximum current into $V_{DD}$ pin ..... 95 mA

Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) ..... ± 20 mA

Output clamp current, $I_{OK}$ (Vo < 0 or Vo >$V_{DD}$) ..... ± 20 mA

Maximum output current sunk by any I/O pin ..... 25 mA

Maximum output current sourced by any I/O pin ..... 25 mA

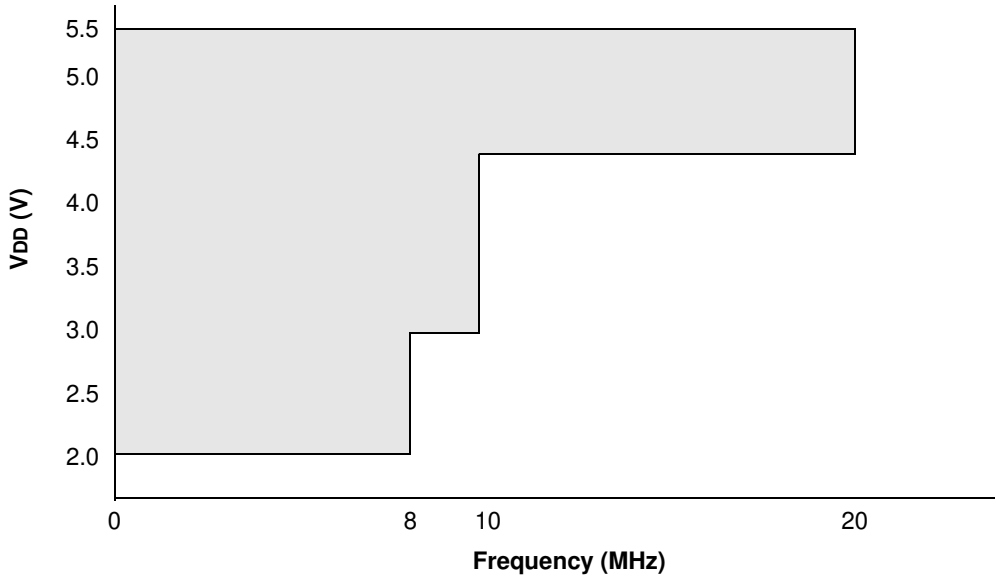
Maximum current sunk by GPIO ..... 90 mA

Maximum current sourced GPIO ..... 90 mA

**Note 1:** Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$.

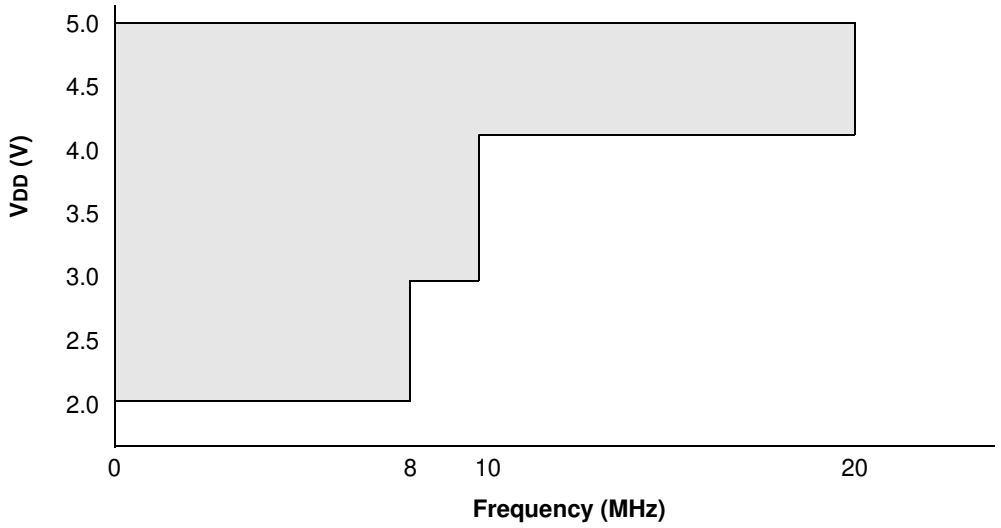
† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

**FIGURE 16-1: PIC12F609/615/617 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C**




**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.

**FIGURE 16-2: PIC12HV609/615 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C**




**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.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## 16.1 DC Characteristics: PIC12F609/615/617/12HV609/615-I (Industrial) PIC12F609/615/617/12HV609/615-E (Extended)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial<br>-40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | VDD | **Supply Voltage** | | | | | |
| D001 | | PIC12F609/615/617 | 2.0 | — | 5.5 | V | FOSC < = 4 MHz |
| D001 | | PIC12HV609/615 | 2.0 | — | —(2) | V | FOSC < = 4 MHz |
| D001B | | PIC12F609/615/617 | 2.0 | — | 5.5 | V | FOSC < = 8 MHz |
| D001B | | PIC12HV609/615 | 2.0 | — | —(2) | V | FOSC < = 8 MHz |
| D001C | | PIC12F609/615/617 | 3.0 | — | 5.5 | V | FOSC < = 10 MHz |
| D001C | | PIC12HV609/615 | 3.0 | — | —(2) | V | FOSC < = 10 MHz |
| D001D | | PIC12F609/615/617 | 4.5 | — | 5.5 | V | FOSC < = 20 MHz |
| D001D | | PIC12HV609/615 | 4.5 | — | —(2) | V | FOSC < = 20 MHz |
| D002* | VDR | **RAM Data Retention Voltage(1)** | 1.5 | — | — | V | Device in Sleep mode |
| D003 | VPOR | **VDD Start Voltage** to ensure internal Power-on Reset signal | — | VSS | — | V | See **Section 12.3.1 "Power-on Reset (POR)"** for details. |
| D004* | SVDD | **VDD Rise Rate** to ensure internal Power-on Reset signal | 0.05 | — | — | V/ms | See **Section 12.3.1 "Power-on Reset (POR)"** for details. |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

**2:** User defined. Voltage across the shunt regulator should not exceed 5V.

## 16.2 DC Characteristics: PIC12F609/615/617-I (Industrial) PIC12F609/615/617-E (Extended)

| DC CHARACTERISTICS | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial<br>-40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Device Characteristics** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** | |
| | | | | | | **VDD** | **Note** |
| D010 | **Supply Current (IDD)(1, 2)**<br>PIC12F609/615/617 | — | 13 | 25 | μA | 2.0 | FOSC = 32 kHz<br>LP Oscillator mode |
| | | — | 19 | 29 | μA | 3.0 | |
| | | — | 32 | 51 | μA | 5.0 | |
| D011* | | — | 135 | 225 | μA | 2.0 | FOSC = 1 MHz<br>XT Oscillator mode |
| | | — | 185 | 285 | μA | 3.0 | |
| | | — | 300 | 405 | μA | 5.0 | |
| D012 | | — | 240 | 360 | μA | 2.0 | FOSC = 4 MHz<br>XT Oscillator mode |
| | | — | 360 | 505 | μA | 3.0 | |
| | | — | 0.66 | 1.0 | mA | 5.0 | |
| D013* | | — | 75 | 110 | μA | 2.0 | FOSC = 1 MHz<br>EC Oscillator mode |
| | | — | 155 | 255 | μA | 3.0 | |
| | | — | 345 | 530 | μA | 5.0 | |
| D014 | | — | 185 | 255 | μA | 2.0 | FOSC = 4 MHz<br>EC Oscillator mode |
| | | — | 325 | 475 | μA | 3.0 | |
| | | — | 0.665 | 1.0 | mA | 5.0 | |
| D016* | | — | 245 | 340 | μA | 2.0 | FOSC = 4 MHz<br>INTOSC mode |
| | | — | 360 | 485 | μA | 3.0 | |
| | | — | 0.620 | 0.845 | mA | 5.0 | |
| D017 | | — | 395 | 550 | μA | 2.0 | FOSC = 8 MHz<br>INTOSC mode |
| | | — | 0.620 | 0.850 | mA | 3.0 | |
| | | — | 1.2 | 1.6 | mA | 5.0 | |
| D018 | | — | 175 | 235 | μA | 2.0 | FOSC = 4 MHz<br>EXTRC mode(3) |
| | | — | 285 | 390 | μA | 3.0 | |
| | | — | 530 | 750 | μA | 5.0 | |
| D019 | | — | 2.2 | 3.1 | mA | 4.5 | FOSC = 20 MHz<br>HS Oscillator mode |
| | | — | 2.8 | 3.35 | mA | 5.0 | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

**3:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in KOhms (KΩ).


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## 16.3 DC Characteristics: PIC12HV609/615-I (Industrial) PIC12HV609/615-E (Extended)

| DC CHARACTERISTICS | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial<br>-40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Device Characteristics** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** | |
| | | | | | | **VDD** | **Note** |
| D010 | **Supply Current (IDD)(1, 2)**<br>PIC12HV609/615 | — | 160 | 230 | μA | 2.0 | FOSC = 32 kHz<br>LP Oscillator mode |
| | | — | 240 | 310 | μA | 3.0 | |
| | | — | 280 | 400 | μA | 4.5 | |
| D011* | | — | 270 | 380 | μA | 2.0 | FOSC = 1 MHz<br>XT Oscillator mode |
| | | — | 400 | 560 | μA | 3.0 | |
| | | — | 520 | 780 | μA | 4.5 | |
| D012 | | — | 380 | 540 | μA | 2.0 | FOSC = 4 MHz<br>XT Oscillator mode |
| | | — | 575 | 810 | μA | 3.0 | |
| | | — | 0.875 | 1.3 | mA | 4.5 | |
| D013* | | — | 215 | 310 | μA | 2.0 | FOSC = 1 MHz<br>EC Oscillator mode |
| | | — | 375 | 565 | μA | 3.0 | |
| | | — | 570 | 870 | μA | 4.5 | |
| D014 | | — | 330 | 475 | μA | 2.0 | FOSC = 4 MHz<br>EC Oscillator mode |
| | | — | 550 | 800 | μA | 3.0 | |
| | | — | 0.85 | 1.2 | mA | 4.5 | |
| D016* | | — | 310 | 435 | μA | 2.0 | FOSC = 4 MHz<br>INTOSC mode |
| | | — | 500 | 700 | μA | 3.0 | |
| | | — | 0.74 | 1.1 | mA | 4.5 | |
| D017 | | — | 460 | 650 | μA | 2.0 | FOSC = 8 MHz<br>INTOSC mode |
| | | — | 0.75 | 1.1 | mA | 3.0 | |
| | | — | 1.2 | 1.6 | mA | 4.5 | |
| D018 | | — | 320 | 465 | μA | 2.0 | FOSC = 4 MHz<br>EXTRC mode(3) |
| | | — | 510 | 750 | μA | 3.0 | |
| | | — | 0.770 | 1.0 | mA | 4.5 | |
| D019 | | — | 2.5 | 3.4 | mA | 4.5 | FOSC = 20 MHz<br>HS Oscillator mode |

* These parameters are characterized but not tested.

† Data in “Typ” column is at 4.5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

**3:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

## 16.4 DC Characteristics: PIC12F609/615/617 - I (Industrial)

| DC CHARACTERISTICS | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Device Characteristics** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** | |
| | | | | | | **VDD** | **Note** |
| D020 | **Power-down Base Current (IPD)(2)** | — | 0.05 | 0.9 | μA | 2.0 | WDT, BOR, Comparator, VREF and T1OSC disabled |
| | | — | 0.15 | 1.2 | μA | 3.0 | |
| | PIC12F609/615/617 | — | 0.35 | 1.5 | μA | 5.0 | |
| | | | 150 | 500 | nA | 3.0 | -40°C ≤ TA ≤ +25°C for industrial |
| D021 | | — | 0.5 | 1.5 | μA | 2.0 | WDT Current(1) |
| | | — | 2.5 | 4.0 | μA | 3.0 | |
| | | — | 9.5 | 17 | μA | 5.0 | |
| D022 | | — | 5.0 | 9 | μA | 3.0 | BOR Current(1) |
| | | — | 6.0 | 12 | μA | 5.0 | |
| D023 | | — | 50 | 60 | μA | 2.0 | Comparator Current(1), single comparator enabled |
| | | — | 55 | 65 | μA | 3.0 | |
| | | — | 60 | 75 | μA | 5.0 | |
| D024 | | — | 30 | 40 | μA | 2.0 | CVREF Current(1) (high range) |
| | | — | 45 | 60 | μA | 3.0 | |
| | | — | 75 | 105 | μA | 5.0 | |
| D025* | | — | 39 | 50 | μA | 2.0 | CVREF Current(1) (low range) |
| | | — | 59 | 80 | μA | 3.0 | |
| | | — | 98 | 130 | μA | 5.0 | |
| D026 | | — | 5.5 | 10 | μA | 2.0 | T1OSC Current(1), 32.768 kHz |
| | | — | 7.0 | 12 | μA | 3.0 | |
| | | — | 8.5 | 14 | μA | 5.0 | |
| D027 | | — | 0.2 | 1.6 | μA | 3.0 | A/D Current(1), no conversion in progress |
| | | — | 0.36 | 1.9 | μA | 5.0 | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

**2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.


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## 16.5 DC Characteristics: PIC12F609/615/617 - E (Extended)

| DC CHARACTERISTICS | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Device Characteristics** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** | |
| | | | | | | **VDD** | **Note** |
| D020E | **Power-down Base Current (IPD)(2)**<br>PIC12F609/615/617 | — | 0.05 | 4.0 | μA | 2.0 | WDT, BOR, Comparator, VREF and T1OSC disabled |
| | | — | 0.15 | 5.0 | μA | 3.0 | |
| | | — | 0.35 | 8.5 | μA | 5.0 | |
| D021E | | — | 0.5 | 5.0 | μA | 2.0 | WDT Current(1) |
| | | — | 2.5 | 8.0 | μA | 3.0 | |
| | | — | 9.5 | 19 | μA | 5.0 | |
| D022E | | — | 5.0 | 15 | μA | 3.0 | BOR Current(1) |
| | | — | 6.0 | 19 | μA | 5.0 | |
| D023E | | — | 50 | 70 | μA | 2.0 | Comparator Current(1), single comparator enabled |
| | | — | 55 | 75 | μA | 3.0 | |
| | | — | 60 | 80 | μA | 5.0 | |
| D024E | | — | 30 | 40 | μA | 2.0 | CVREF Current(1) (high range) |
| | | — | 45 | 60 | μA | 3.0 | |
| | | — | 75 | 105 | μA | 5.0 | |
| D025E* | | — | 39 | 50 | μA | 2.0 | CVREF Current(1) (low range) |
| | | — | 59 | 80 | μA | 3.0 | |
| | | — | 98 | 130 | μA | 5.0 | |
| D026E | | — | 5.5 | 16 | μA | 2.0 | T1OSC Current(1), 32.768 kHz |
| | | — | 7.0 | 18 | μA | 3.0 | |
| | | — | 8.5 | 22 | μA | 5.0 | |
| D027E | | — | 0.2 | 6.5 | μA | 3.0 | A/D Current(1), no conversion in progress |
| | | — | 0.36 | 10 | μA | 5.0 | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

**2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

## 16.6 DC Characteristics: PIC12HV609/615 - I (Industrial)

| DC CHARACTERISTICS | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Device Characteristics** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** | |
| | | | | | | **VDD** | **Note** |
| D020 | **Power-down Base Current (IPD)(2,3)** | — | 135 | 200 | μA | 2.0 | WDT, BOR, Comparator, VREF and T1OSC disabled |
| | | — | 210 | 280 | μA | 3.0 | |
| | PIC12HV609/615 | — | 260 | 350 | μA | 4.5 | |
| D021 | | — | 135 | 200 | μA | 2.0 | WDT Current(1) |
| | | — | 210 | 285 | μA | 3.0 | |
| | | — | 265 | 360 | μA | 4.5 | |
| D022 | | — | 215 | 285 | μA | 3.0 | BOR Current(1) |
| | | — | 265 | 360 | μA | 4.5 | |
| D023 | | — | 185 | 270 | μA | 2.0 | Comparator Current(1), single comparator enabled |
| | | — | 265 | 350 | μA | 3.0 | |
| | | — | 320 | 430 | μA | 4.5 | |
| D024 | | — | 165 | 235 | μA | 2.0 | CVREF Current(1) (high range) |
| | | — | 255 | 330 | μA | 3.0 | |
| | | — | 330 | 430 | μA | 4.5 | |
| D025* | | — | 175 | 245 | μA | 2.0 | CVREF Current(1) (low range) |
| | | — | 275 | 350 | μA | 3.0 | |
| | | — | 355 | 450 | μA | 4.5 | |
| D026 | | — | 140 | 205 | μA | 2.0 | T1OSC Current(1), 32.768 kHz |
| | | — | 220 | 290 | μA | 3.0 | |
| | | — | 270 | 360 | μA | 4.5 | |
| D027 | | — | 210 | 280 | μA | 3.0 | A/D Current(1), no conversion in progress |
| | | — | 260 | 350 | μA | 4.5 | |

* These parameters are characterized but not tested.

† Data in “Typ” column is at 4.5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

**2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

**3:** Shunt regulator is always on and always draws operating current.


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## 16.7 DC Characteristics: PIC12HV609/615-E (Extended)

| DC CHARACTERISTICS | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Device Characteristics** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** | |
| | | | | | | **VDD** | **Note** |
| D020E | **Power-down Base Current (IPD)(2,3)**<br>PIC12HV609/615 | — | 135 | 200 | μA | 2.0 | WDT, BOR, Comparator, VREF and T1OSC disabled |
| | | — | 210 | 280 | μA | 3.0 | |
| | | — | 260 | 350 | μA | 4.5 | |
| D021E | | — | 135 | 200 | μA | 2.0 | WDT Current(1) |
| | | — | 210 | 285 | μA | 3.0 | |
| | | — | 265 | 360 | μA | 4.5 | |
| D022E | | — | 215 | 285 | μA | 3.0 | BOR Current(1) |
| | | — | 265 | 360 | μA | 4.5 | |
| D023E | | — | 185 | 280 | μA | 2.0 | Comparator Current(1), single comparator enabled |
| | | — | 265 | 360 | μA | 3.0 | |
| | | — | 320 | 430 | μA | 4.5 | |
| D024E | | — | 165 | 235 | μA | 2.0 | CVREF Current(1) (high range) |
| | | — | 255 | 330 | μA | 3.0 | |
| | | — | 330 | 430 | μA | 4.5 | |
| D025E* | | — | 175 | 245 | μA | 2.0 | CVREF Current(1) (low range) |
| | | — | 275 | 350 | μA | 3.0 | |
| | | — | 355 | 450 | μA | 4.5 | |
| D026E | | — | 140 | 205 | μA | 2.0 | T1OSC Current(1), 32.768 kHz |
| | | — | 220 | 290 | μA | 3.0 | |
| | | — | 270 | 360 | μA | 4.5 | |
| D027E | | — | 210 | 280 | μA | 3.0 | A/D Current(1), no conversion in progress |
| | | — | 260 | 350 | μA | 4.5 | |

* These parameters are characterized but not tested.

† Data in “Typ” column is at 4.5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

**2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

**3:** Shunt regulator is always on and always draws operating current.

## 16.8 DC Characteristics: PIC12F609/615/617/12HV609/615-I (Industrial) PIC12F609/615/617/12HV609/615-E (Extended)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial<br>-40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | VIL | **Input Low Voltage** | | | | | |
| | | I/O port: | | | | | |
| D030 | | with TTL buffer | Vss | — | 0.8 | V | 4.5V ≤ VDD ≤ 5.5V |
| D030A | | | Vss | — | 0.15 VDD | V | 2.0V ≤ VDD ≤ 4.5V |
| D031 | | with Schmitt Trigger buffer | Vss | — | 0.2 VDD | V | 2.0V ≤ VDD ≤ 5.5V |
| D032 | | $\overline{\text{MCLR}}$, OSC1 (RC mode) | VSS | — | 0.2 VDD | V | **(NOTE 1)** |
| D033 | | OSC1 (XT and LP modes) | VSS | — | 0.3 | V | |
| D033A | | OSC1 (HS mode) | VSS | — | 0.3 VDD | V | |
| | VIH | **Input High Voltage** | | | | | |
| | | I/O ports: | | — | | | |
| D040 | | with TTL buffer | 2.0 | — | VDD | V | 4.5V ≤ VDD ≤ 5.5V |
| D040A | | | 0.25 VDD + 0.8 | — | VDD | V | 2.0V ≤ VDD ≤ 4.5V |
| D041 | | with Schmitt Trigger buffer | 0.8 VDD | — | VDD | V | 2.0V ≤ VDD ≤ 5.5V |
| D042 | | $\overline{\text{MCLR}}$ | 0.8 VDD | — | VDD | V | |
| D043 | | OSC1 (XT and LP modes) | 1.6 | — | VDD | V | |
| D043A | | OSC1 (HS mode) | 0.7 VDD | — | VDD | V | |
| D043B | | OSC1 (RC mode) | 0.9 VDD | — | VDD | V | **(NOTE 1)** |
| | IIL | **Input Leakage Current(2,3)** | | | | | |
| D060 | | I/O ports | — | ± 0.1 | ± 1 | μA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance |
| D061 | | GP3/$\overline{\text{MCLR}}$(3,4) | — | ± 0.7 | ± 5 | μA | VSS ≤ VPIN ≤ VDD |
| D063 | | OSC1 | — | ± 0.1 | ± 5 | μA | VSS ≤ VPIN ≤ VDD, XT, HS and LP oscillator configuration |
| D070* | IPUR | **GPIO Weak Pull-up Current(5)** | 50 | 250 | 400 | μA | VDD = 5.0V, VPIN = VSS |
| | VOL | **Output Low Voltage** | — | — | 0.6 | V | IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C |
| D080 | | I/O ports | — | — | 0.6 | V | IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C |
| | VOH | **Output High Voltage** | VDD – 0.7 | — | — | V | IOH = -2.5mA, VDD = 4.5V, -40°C to +125°C |
| D090 | | I/O ports(2) | VDD – 0.7 | — | — | V | IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

**2:** Negative current is defined as current sourced by the pin.

**3:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**4:** This specification applies to GP3/$\overline{\text{MCLR}}$ configured as GP3 with the internal weak pull-up disabled.

**5:** This specification applies to all weak pull-up pins, including the weak pull-up found on GP3/$\overline{\text{MCLR}}$. When GP3/$\overline{\text{MCLR}}$ is configured as $\overline{\text{MCLR}}$ reset pin, the weak pull-up is always enabled.

**6:** Applies to PIC12F617 only.


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## 16.8 DC Characteristics: PIC12F609/615/617/12HV609/615-I (Industrial) PIC12F609/615/617/12HV609/615-E (Extended) (Continued)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial<br>-40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D101* | COSC2 | **Capacitive Loading Specs on Output Pins**<br>OSC2 pin | — | — | 15 | pF | In XT, HS and LP modes when external clock is used to drive OSC1 |
| D101A* | CIO | All I/O pins | — | — | 50 | pF | |
| | | **Program Flash Memory** | | | | | |
| D130 | EP | Cell Endurance | 10K | 100K | — | E/W | -40°C ≤ TA ≤ +85°C |
| D130A | ED | Cell Endurance | 1K | 10K | — | E/W | +85°C ≤ TA ≤ +125°C |
| D131 | VPR | VDD for Read | VMIN | — | 5.5 | V | VMIN = Minimum operating voltage |
| D132 | VPEW | VDD for Bulk Erase/Write | 4.5 | — | 5.5 | V | |
| D132A | VPEW | VDD for Row Erase/Write(6) | VMIN | — | 5.5 | V | |
| D133 | TPEW | Erase/Write cycle time | — | 2 | 2.5 | ms | |
| D134 | TRETD | Characteristic Retention | 40 | — | — | Year | Provided no other specifications are violated |

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

**2:** Negative current is defined as current sourced by the pin.

**3:** The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**4:** This specification applies to GP3/$\overline{MCLR}$ configured as GP3 with the internal weak pull-up disabled.

**5:** This specification applies to all weak pull-up pins, including the weak pull-up found on GP3/$\overline{MCLR}$. When GP3/$\overline{MCLR}$ is configured as $\overline{MCLR}$ reset pin, the weak pull-up is always enabled.

**6:** Applies to PIC12F617 only.

## 16.9 Thermal Considerations

| Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +125°C | | | | | |
|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | **Typ** | **Units** | **Conditions** |
| TH01 | $\theta_{JA}$ | Thermal Resistance Junction to Ambient | 84.6* | C/W | 8-pin PDIP package |
| | | | 149.5* | C/W | 8-pin SOIC package |
| | | | 211* | C/W | 8-pin MSOP package |
| | | | 60* | C/W | 8-pin DFN 3x3mm package |
| | | | 44* | C/W | 8-pin DFN 4x4mm package |
| TH02 | $\theta_{JC}$ | Thermal Resistance Junction to Case | 41.2* | C/W | 8-pin PDIP package |
| | | | 39.9* | C/W | 8-pin SOIC package |
| | | | 39* | C/W | 8-pin MSOP package |
| | | | 9* | C/W | 8-pin DFN 3x3mm package |
| | | | 3.0* | C/W | 8-pin DFN 4x4mm package |
| TH03 | $T_{DIE}$ | Die Temperature | 150* | C | |
| TH04 | PD | Power Dissipation | — | W | PD = $P_{INTERNAL}$ + $P_{I/O}$ |
| TH05 | $P_{INTERNAL}$ | Internal Power Dissipation | — | W | $P_{INTERNAL}$ = $I_{DD}$ x $V_{DD}$ **(NOTE 1)** |
| TH06 | $P_{I/O}$ | I/O Power Dissipation | — | W | $P_{I/O}$ = Σ ($I_{OL}$ * $V_{OL}$) + Σ ($I_{OH}$ * ($V_{DD}$ - $V_{OH}$)) |
| TH07 | $P_{DER}$ | Derated Power | — | W | $P_{DER}$ = $PD_{MAX}$ ($T_{DIE}$ - $T_A$)/$\theta_{JA}$ **(NOTE 2)** |

* These parameters are characterized but not tested.

**Note 1:** $I_{DD}$ is current to run the chip alone without driving any load on the output pins.

**2:** $T_A$ = Ambient temperature.


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## 16.10 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

| **T** | | | |
|---|---|---|---|
| F | Frequency | T | Time |

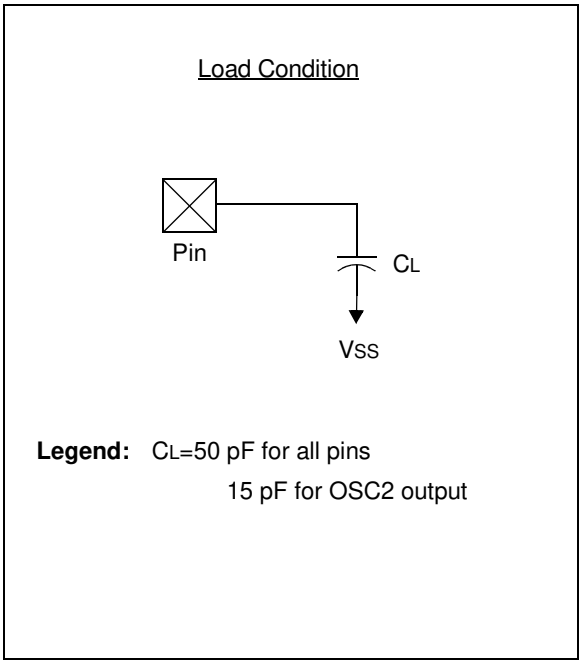
Lowercase letters (pp) and their meanings:

| **pp** | | | |
|---|---|---|---|
| cc | CCP1 | osc | OSC1 |
| ck | CLKOUT | rd | $\overline{RD}$ |
| cs | $\overline{CS}$ | rw | $\overline{RD}$ or $\overline{WR}$ |
| di | SDI | sc | SCK |
| do | SDO | ss | $\overline{SS}$ |
| dt | Data in | t0 | T0CKI |
| io | I/O Port | t1 | T1CKI |
| mc | $\overline{MCLR}$ | wr | $\overline{WR}$ |

Uppercase letters and their meanings:

| **S** | | | |
|---|---|---|---|
| F | Fall | P | Period |
| H | High | R | Rise |
| I | Invalid (High-impedance) | V | Valid |
| L | Low | Z | High-impedance |

**FIGURE 16-3: LOAD CONDITIONS**



## 16.11 AC Characteristics: PIC12F609/615/617/12HV609/615 (Industrial, Extended)

**FIGURE 16-4: CLOCK TIMING**

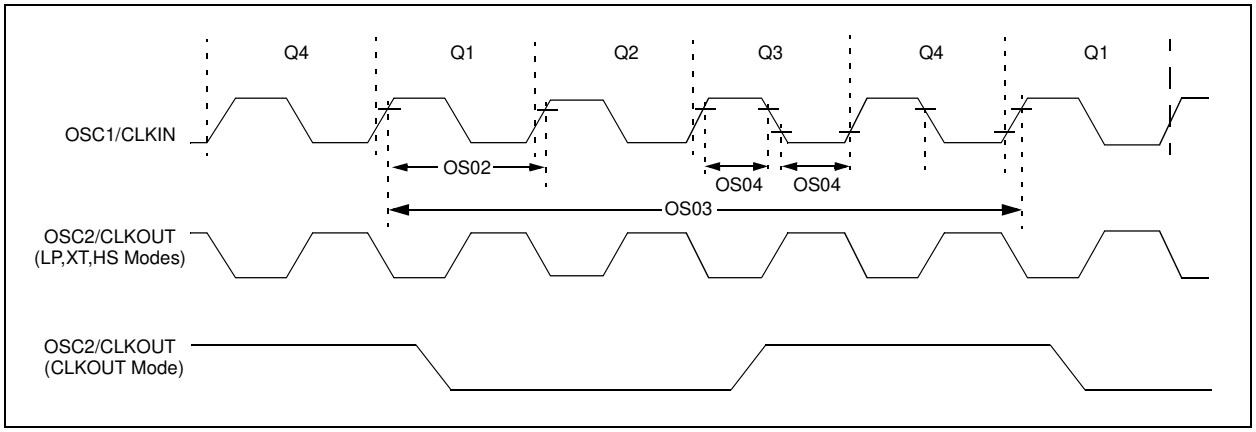



**TABLE 16-1: CLOCK OSCILLATOR TIMING REQUIREMENTS**

**Standard Operating Conditions (unless otherwise stated)**
Operating temperature -40°C ≤ TA ≤ +125°C

| Param No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| OS01 | FOSC | External CLKIN Frequency(1) | DC | — | 37 | kHz | LP Oscillator mode |
| | | | DC | — | 4 | MHz | XT Oscillator mode |
| | | | DC | — | 20 | MHz | HS Oscillator mode |
| | | | DC | — | 20 | MHz | EC Oscillator mode |
| | | Oscillator Frequency(1) | — | 32.768 | — | kHz | LP Oscillator mode |
| | | | 0.1 | — | 4 | MHz | XT Oscillator mode |
| | | | 1 | — | 20 | MHz | HS Oscillator mode |
| | | | DC | — | 4 | MHz | RC Oscillator mode |
| OS02 | TOSC | External CLKIN Period(1) | 27 | — | ∞ | μs | LP Oscillator mode |
| | | | 250 | — | ∞ | ns | XT Oscillator mode |
| | | | 50 | — | ∞ | ns | HS Oscillator mode |
| | | | 50 | — | ∞ | ns | EC Oscillator mode |
| | | Oscillator Period(1) | — | 30.5 | — | μs | LP Oscillator mode |
| | | | 250 | — | 10,000 | ns | XT Oscillator mode |
| | | | 50 | — | 1,000 | ns | HS Oscillator mode |
| | | | 250 | — | — | ns | RC Oscillator mode |
| OS03 | TCY | Instruction Cycle Time(1) | 200 | TCY | DC | ns | TCY = 4/FOSC |
| OS04* | TOSH, TOSL | External CLKIN High, External CLKIN Low | 2 | — | — | μs | LP oscillator |
| | | | 100 | — | — | ns | XT oscillator |
| | | | 20 | — | — | ns | HS oscillator |
| OS05* | TOSR, TOSF | External CLKIN Rise, External CLKIN Fall | 0 | — | ∞ | ns | LP oscillator |
| | | | 0 | — | ∞ | ns | XT oscillator |
| | | | 0 | — | ∞ | ns | HS oscillator |

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min” values with an external clock applied to OSC1 pin. When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.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### TABLE 16-2: OSCILLATOR PARAMETERS

**Standard Operating Conditions (unless otherwise stated)**
Operating Temperature -40°C ≤ TA ≤ +125°C

| Param No. | Sym | Characteristic | Freq. Tolerance | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| OS06 | TWARM | Internal Oscillator Switch when running(3) | — | — | — | 2 | TOSC | Slowest clock |
| OS07 | INTOSC | Internal Calibrated INTOSC Frequency(2) (4MHz) | ±1% | 3.96 | 4.0 | 4.04 | MHz | VDD = 3.5V, $T_A$ = 25°C |
| | | | ±2% | 3.92 | 4.0 | 4.08 | MHz | 2.5V ≤ VDD ≤ 5.5V, 0°C ≤ TA ≤ +85°C |
| | | | ±5% | 3.80 | 4.0 | 4.2 | MHz | 2.0V ≤ VDD ≤ 5.5V, -40°C ≤ TA ≤ +85°C (Ind.), -40°C ≤ TA ≤ +125°C (Ext.) |
| OS08 | INTOSC | Internal Calibrated INTOSC Frequency(2) (8MHz) | ±1% | 7.92 | 8.0 | 8.08 | MHz | VDD = 3.5V, $T_A$ = 25°C |
| | | | ±2% | 7.84 | 8.0 | 8.16 | MHz | 2.5V ≤ VDD ≤ 5.5V, 0°C ≤ TA ≤ +85°C |
| | | | ±5% | 7.60 | 8.0 | 8.40 | MHz | 2.0V ≤ VDD ≤ 5.5V, -40°C ≤ TA ≤ +85°C (Ind.), -40°C ≤ TA ≤ +125°C (Ext.) |
| OS10* | TIOSC ST | INTOSC Oscillator Wake-up from Sleep Start-up Time | — | 5.5 | 12 | 24 | μs | VDD = 2.0V, -40°C to +85°C |
| | | | — | 3.5 | 7 | 14 | μs | VDD = 3.0V, -40°C to +85°C |
| | | | — | 3 | 6 | 11 | μs | VDD = 5.0V, -40°C to +85°C |

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

**2:** To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

**3:** By design.

**FIGURE 16-5: CLKOUT AND I/O TIMING**

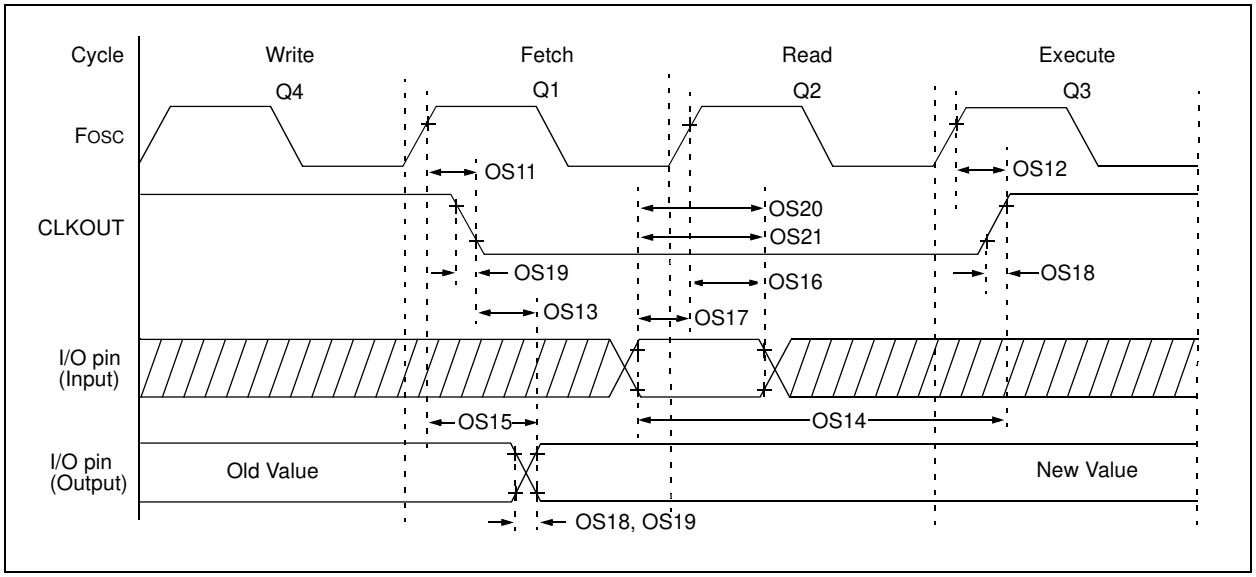


**TABLE 16-3: CLKOUT AND I/O TIMING PARAMETERS**

**Standard Operating Conditions (unless otherwise stated)**
Operating Temperature -40°C ≤ TA ≤ +125°C

| Param No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| OS11 | TOSH2CKL | FOSC↑ to CLKOUT↓ (1) | — | — | 70 | ns | VDD = 5.0V |
| OS12 | TOSH2CKH | FOSC↑ to CLKOUT↑ (1) | — | — | 72 | ns | VDD = 5.0V |
| OS13 | TCKL2IOV | CLKOUT↓ to Port out valid(1) | — | — | 20 | ns | |
| OS14 | TIOV2CKH | Port input valid before CLKOUT↑(1) | TOSC + 200 ns | — | — | ns | |
| OS15 | TOSH2IOV | FOSC↑ (Q1 cycle) to Port out valid | — | 50 | 70* | ns | VDD = 5.0V |
| OS16 | TOSH2IOI | FOSC↑ (Q2 cycle) to Port input invalid (I/O in hold time) | 50 | — | — | ns | VDD = 5.0V |
| OS17 | TIOV2OSH | Port input valid to FOSC↑ (Q2 cycle) (I/O in setup time) | 20 | — | — | ns | |
| OS18 | TIOR | Port output rise time(2) | —<br>— | 15<br>40 | 72<br>32 | ns | VDD = 2.0V<br>VDD = 5.0V |
| OS19 | TIOF | Port output fall time(2) | —<br>— | 28<br>15 | 55<br>30 | ns | VDD = 2.0V<br>VDD = 5.0V |
| OS20* | TINP | INT pin input high or low time | 25 | — | — | ns | |
| OS21* | TRAP | GPIO interrupt-on-change new input level time | TCY | — | — | ns | |

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated.

**Note 1:** Measurements are taken in RC mode where CLKOUT output is 4 x TOSC.

**2:** Includes OSC2 in CLKOUT mode.


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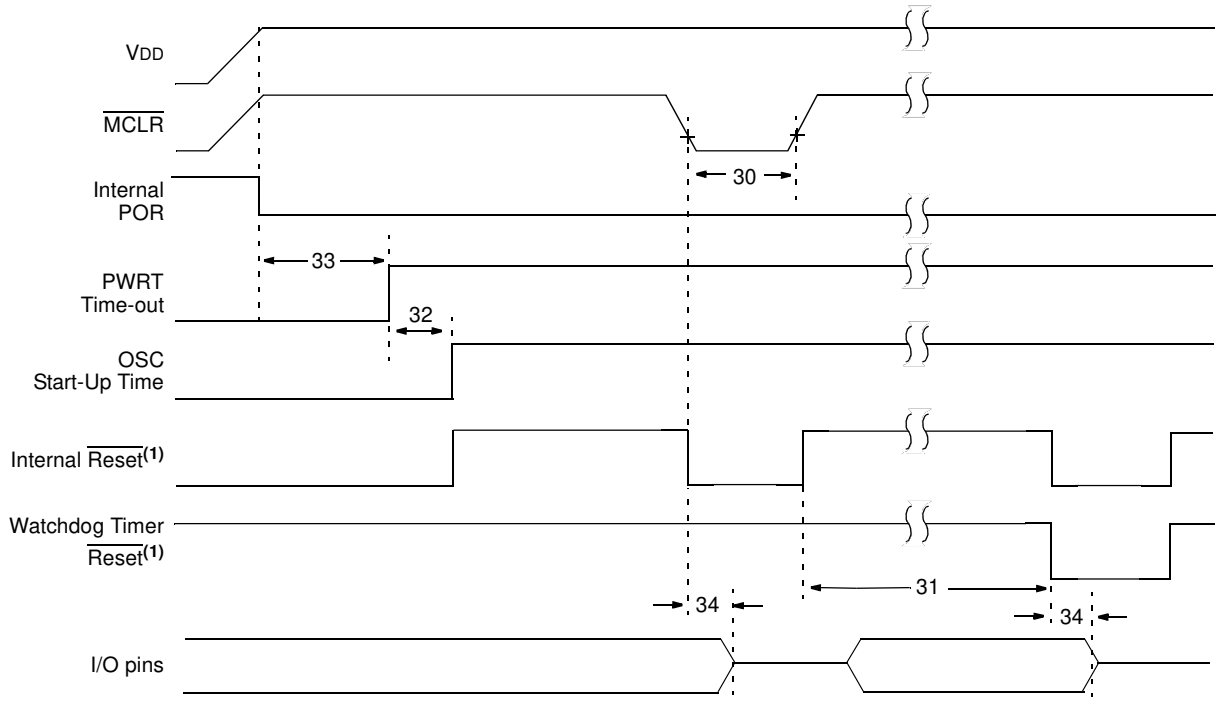
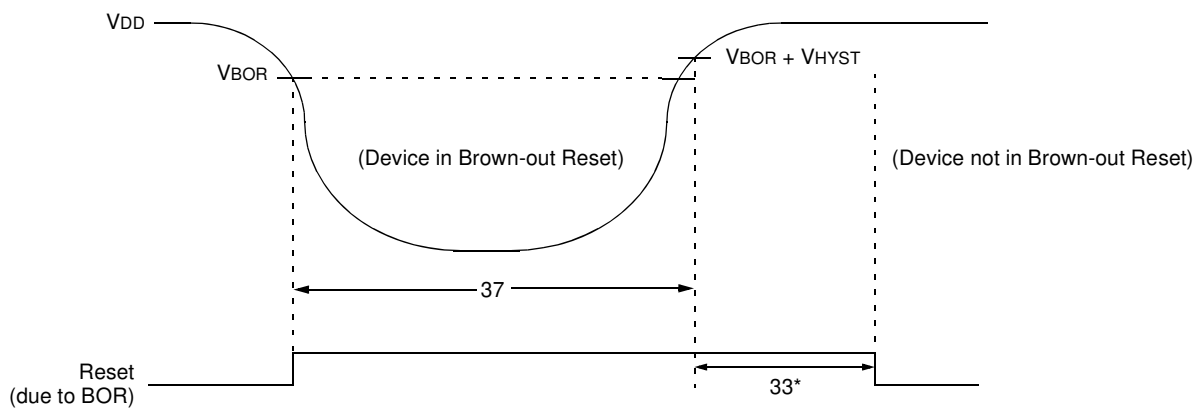
**FIGURE 16-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**




**Note 1:** Asserted low.

**FIGURE 16-7: BROWN-OUT RESET TIMING AND CHARACTERISTICS**




* 64 ms delay only if $\overline{\text{PWRTE}}$ bit in the Configuration Word register is programmed to '0'.

**TABLE 16-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS**

| **Standard Operating Conditions (unless otherwise stated)**<br>Operating Temperature -40°C ≤ TA ≤ +125°C | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 30 | TMCL | $\overline{\text{MCLR}}$ Pulse Width (low) | 2<br>5 | —<br>— | —<br>— | μs<br>μs | VDD = 5V, -40°C to +85°C<br>VDD = 5V, -40°C to +125°C |
| 31* | TWDT | Watchdog Timer Time-out Period (No Prescaler) | 10<br>10 | 20<br>20 | 30<br>35 | ms<br>ms | VDD = 5V, -40°C to +85°C<br>VDD = 5V, -40°C to +125°C |
| 32 | TOST | Oscillation Start-up Timer Period(1, 2) | — | 1024 | — | TOSC | **(NOTE 3)** |
| 33* | TPWRT | Power-up Timer Period | 40 | 65 | 140 | ms | |
| 34* | TIOZ | I/O High-impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset | — | — | 2.0 | μs | |
| 35 | VBOR | Brown-out Reset Voltage | 2.0 | 2.15 | 2.3 | V | **(NOTE 4)** |
| 36* | VHYST | Brown-out Reset Hysteresis | — | 100 | — | mV | |
| 37* | TBOR | Brown-out Reset Minimum Detection Period | 100 | — | — | μs | VDD ≤ VBOR |

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

**2:** By design.

**3:** Period of the slower clock.

**4:** To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.


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**FIGURE 16-8: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS**

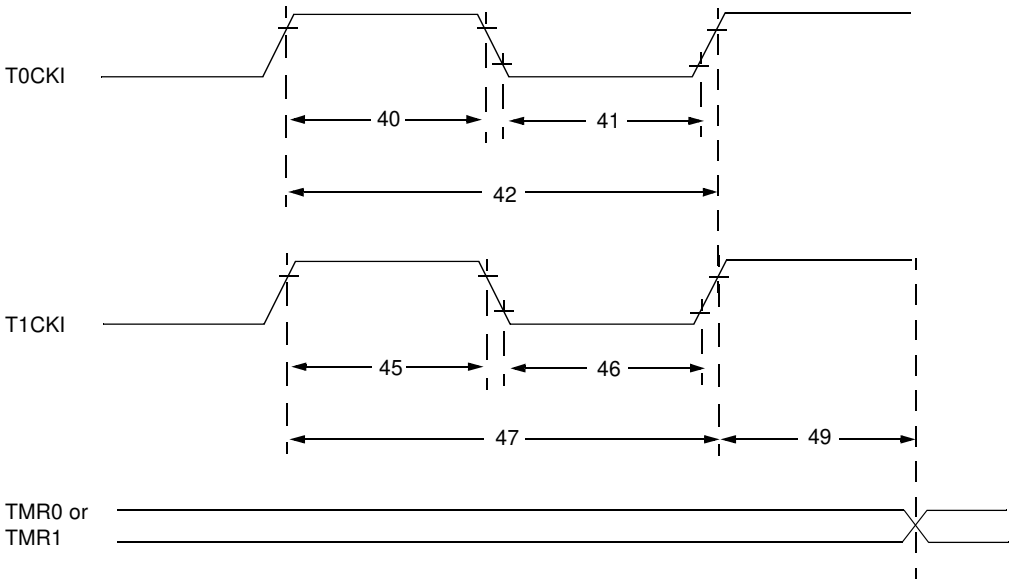



**TABLE 16-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS**

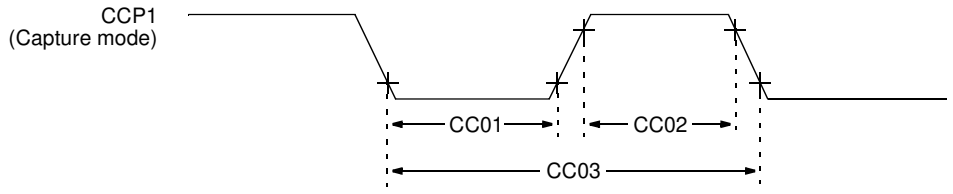
**Standard Operating Conditions (unless otherwise stated)**
Operating Temperature -40°C ≤ TA ≤ +125°C

| Param No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 40* | TT0H | T0CKI High Pulse Width | No Prescaler | 0.5 TCY + 20 | — | — | ns | |
| | | | With Prescaler | 10 | — | — | ns | |
| 41* | TT0L | T0CKI Low Pulse Width | No Prescaler | 0.5 TCY + 20 | — | — | ns | |
| | | | With Prescaler | 10 | — | — | ns | |
| 42* | TT0P | T0CKI Period | | Greater of: 20 or TCY + 40 / N | — | — | ns | N = prescale value (2, 4, ..., 256) |
| 45* | TT1H | T1CKI High Time | Synchronous, No Prescaler | 0.5 TCY + 20 | — | — | ns | |
| | | | Synchronous, with Prescaler | 15 | — | — | ns | |
| | | | Asynchronous | 30 | — | — | ns | |
| 46* | TT1L | T1CKI Low Time | Synchronous, No Prescaler | 0.5 TCY + 20 | — | — | ns | |
| | | | Synchronous, with Prescaler | 15 | — | — | ns | |
| | | | Asynchronous | 30 | — | — | ns | |
| 47* | TT1P | T1CKI Input Period | Synchronous | Greater of: 30 or TCY + 40 / N | — | — | ns | N = prescale value (1, 2, 4, 8) |
| | | | Asynchronous | 60 | — | — | ns | |
| 48 | FT1 | Timer1 Oscillator Input Frequency Range (oscillator enabled by setting bit T1OSCEN) | | — | 32.768 | — | kHz | |
| 49* | TCKEZTMR1 | Delay from External Clock Edge to Timer Increment | | 2 TOSC | — | 7 TOSC | — | Timers in Sync mode |

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 16-9: PIC12F615/617/HV615 CAPTURE/COMPARE/PWM TIMINGS (ECCP)**




**Note:** Refer to Figure 16-3 for load conditions.

**TABLE 16-6: PIC12F615/617/HV615 CAPTURE/COMPARE/PWM REQUIREMENTS (ECCP)**

**Standard Operating Conditions (unless otherwise stated)**
Operating Temperature -40°C ≤ TA ≤ +125°C

| Param No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| CC01* | TccL | CCP1 Input Low Time | No Prescaler | 0.5TCY + 20 | — | — | ns | |
| | | | With Prescaler | 20 | — | — | ns | |
| CC02* | TccH | CCP1 Input High Time | No Prescaler | 0.5TCY + 20 | — | — | ns | |
| | | | With Prescaler | 20 | — | — | ns | |
| CC03* | TccP | CCP1 Input Period | | $\frac{3T_{CY} + 40}{N}$ | — | — | ns | N = prescale value (1, 4 or 16) |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**TABLE 16-7: COMPARATOR SPECIFICATIONS**

**Standard Operating Conditions (unless otherwise stated)**
Operating Temperature -40°C ≤ TA ≤ +125°C

| Param No. | Sym | Characteristics | | Min | Typ† | Max | Units | Comments |
|---|---|---|---|---|---|---|---|---|
| CM01 | VOS | Input Offset Voltage(2) | | — | ± 5.0 | ± 10 | mV | |
| CM02 | VCM | Input Common Mode Voltage | | 0 | — | VDD – 1.5 | V | |
| CM03* | CMRR | Common Mode Rejection Ratio | | +55 | — | — | dB | |
| CM04* | TRT | Response Time(1) | Falling | — | 150 | 600 | ns | |
| | | | Rising | — | 200 | 1000 | ns | |
| CM05* | TMC2COV | Comparator Mode Change to Output Valid | | — | — | 10 | μs | |
| CM06* | VHYS | Input Hysteresis Voltage | | — | 45 | 60 | mV | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Response time is measured with one comparator input at (VDD - 1.5)/2 - 100 mV to (VDD - 1.5)/2 + 20 mV. The other input is at (VDD -1.5)/2.

**2:** Input offset voltage is measured with one comparator input at (VDD - 1.5V)/2.


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**TABLE 16-8: COMPARATOR VOLTAGE REFERENCE (CVREF) SPECIFICATIONS**

| Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +125°C | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristics** | **Min** | **Typ†** | **Max** | **Units** | **Comments** |
| CV01* | CLSB | Step Size(2) | —<br>— | VDD/24<br>VDD/32 | —<br>— | V<br>V | Low Range (VRR = 1)<br>High Range (VRR = 0) |
| CV02* | CACC | Absolute Accuracy(3) | —<br>— | —<br>— | ± 1/2<br>± 1/2 | LSb<br>LSb | Low Range (VRR = 1)<br>High Range (VRR = 0) |
| CV03* | CR | Unit Resistor Value (R) | — | 2k | — | Ω | |
| CV04* | CST | Settling Time(1) | — | — | 10 | μs | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Settling time measured while VRR = 1 and VR<3:0> transitions from '0000' to '1111'.

**2:** See **Section 9.10 "Comparator Voltage Reference"** for more information.

**3:** Absolute Accuracy when CVREF output is ≤ (VDD -1.5).

**TABLE 16-9: VOLTAGE REFERENCE SPECIFICATIONS**

| VR Voltage Reference Specifications | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +125°C | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristics** | **Min** | **Typ** | **Max** | **Units** | **Comments** |
| VR01 | VP6OUT | VP6 voltage output | 0.5 | 0.6 | 0.7 | V | |
| VR02 | V1P2OUT | V1P2 voltage output | 1.05 | 1.20 | 1.35 | V | |
| VR03* | TSTABLE | Settling Time | — | 10 | — | μs | |

* These parameters are characterized but not tested.

**TABLE 16-10: SHUNT REGULATOR SPECIFICATIONS (PIC12HV609/615 only)**

| SHUNT REGULATOR CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +125°C | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristics** | **Min** | **Typ** | **Max** | **Units** | **Comments** |
| SR01 | VSHUNT | Shunt Voltage | 4.75 | 5 | 5.4 | V | |
| SR02 | ISHUNT | Shunt Current | 4 | — | 50 | mA | |
| SR03* | TSETTLE | Settling Time | — | — | 150 | ns | To 1% of final value |
| SR04 | CLOAD | Load Capacitance | 0.01 | — | 10 | μF | Bypass capacitor on VDD pin |
| SR05 | ΔISNT | Regulator operating current | — | 180 | — | μA | Includes band gap reference current |

* These parameters are characterized but not tested.

**TABLE 16-11: PIC12F615/617/HV615 A/D CONVERTER (ADC) CHARACTERISTICS:**

| **Standard Operating Conditions (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +125°C | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| AD01 | NR | Resolution | — | — | 10 bits | bit | |
| AD02 | EIL | Integral Error | — | — | ±1 | LSb | VREF = 5.12V(5) |
| AD03 | EDL | Differential Error | — | — | ±1 | LSb | No missing codes to 10 bits<br>VREF = 5.12V(5) |
| AD04 | EOFF | Offset Error | — | +1.5 | +2.0 | LSb | VREF = 5.12V(5) |
| AD07 | EGN | Gain Error | — | — | ±1 | LSb | VREF = 5.12V(5) |
| AD06<br>AD06A | VREF | Reference Voltage(3) | 2.2<br>2.5 | — | —<br>VDD | V | <br>Absolute minimum to ensure 1 LSb accuracy |
| AD07 | VAIN | Full-Scale Range | VSS | — | VREF | V | |
| AD08 | ZAIN | Recommended Impedance of Analog Voltage Source | — | — | 10 | kΩ | |
| AD09* | IREF | VREF Input Current(3) | 10 | — | 1000 | μA | During VAIN acquisition.<br>Based on differential of VHOLD to VAIN. |
| | | | — | — | 50 | μA | During A/D conversion cycle. |

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Total Absolute Error includes integral, differential, offset and gain errors.

**2:** The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

**3:** ADC VREF is from external VREF or VDD pin, whichever is selected as reference input.

**4:** When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module.

**5:** VREF = 5V for PIC12HV615.


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**TABLE 16-12: PIC12F615/617/HV615 A/D CONVERSION REQUIREMENTS**

**Standard Operating Conditions (unless otherwise stated)**
Operating temperature -40°C ≤ TA ≤ +125°C

| Param No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| AD130* | TAD | A/D Clock Period | 1.6 | — | 9.0 | μs | TOSC-based, VREF ≥ 3.0V |
| | | | 3.0 | — | 9.0 | μs | TOSC-based, VREF full range(3) |
| | | A/D Internal RC Oscillator Period | 3.0 | 6.0 | 9.0 | μs | ADCS<1:0> = 11 (ADRC mode) At VDD = 2.5V |
| | | | 1.6 | 4.0 | 6.0 | μs | At VDD = 5.0V |
| AD131 | TCNV | Conversion Time (not including Acquisition Time)(1) | — | 11 | — | TAD | Set GO/$\overline{\text{DONE}}$ bit to new data in A/D Result register |
| AD132* | TACQ | Acquisition Time | | 11.5 | — | μs | |
| AD133* | TAMP | Amplifier Settling Time | — | — | 5 | μs | |
| AD134 | TGO | Q4 to A/D Clock Start | — | TOSC/2 | — | — | |
| | | | — | TOSC/2 + TCY | — | — | If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed. |

* These parameters are characterized but not tested.

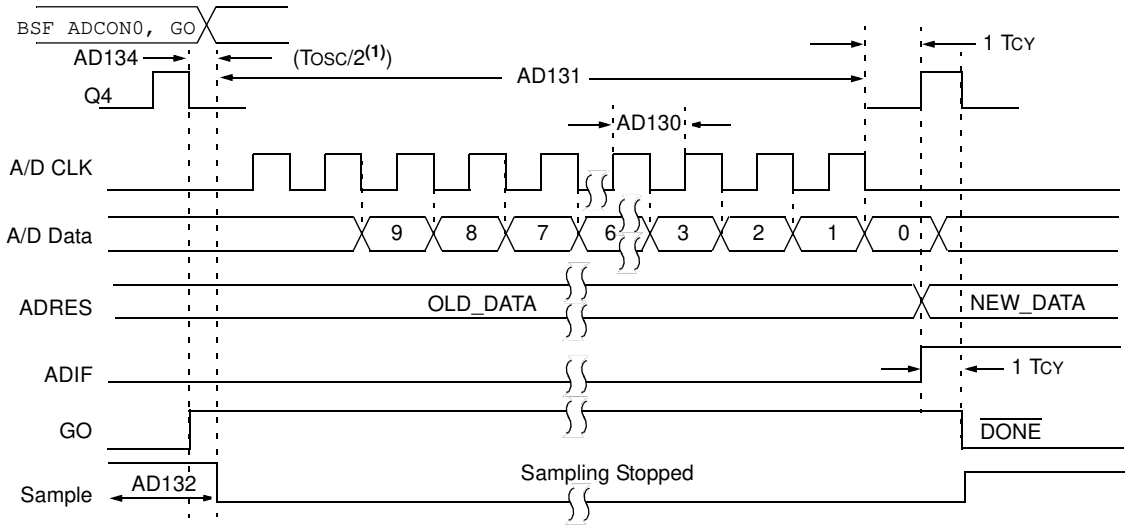
† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** ADRESH and ADRESL registers may be read on the following TCY cycle.

**2:** See **Section 10.3 "A/D Acquisition Requirements"** for minimum conditions.

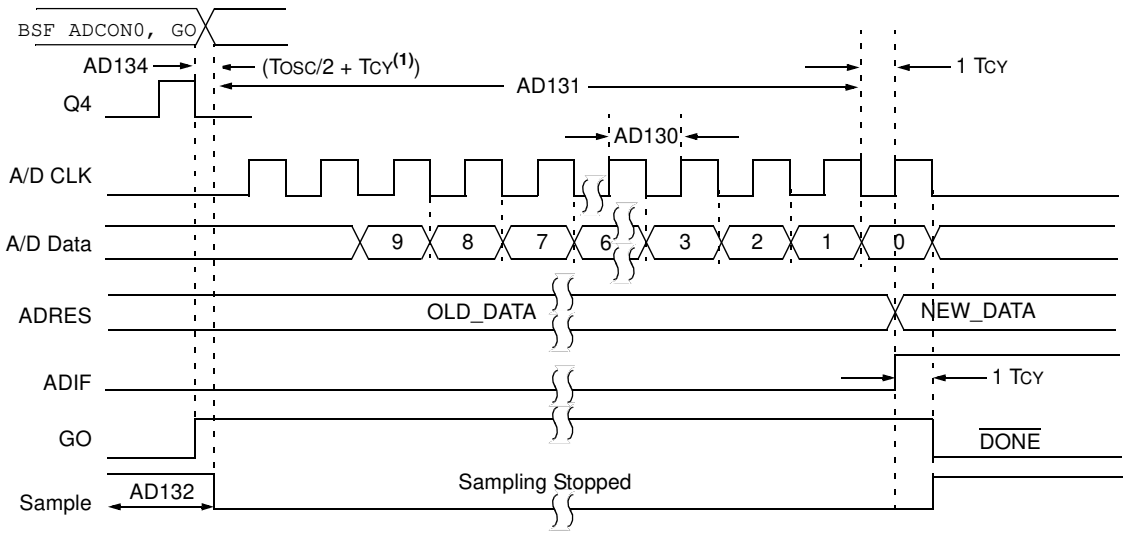
**3:** Full range for PIC12HV609/HV615 powered by the shunt regulator is the 5V regulated voltage.

**FIGURE 16-10: PIC12F615/617/HV615 A/D CONVERSION TIMING (NORMAL MODE)**




**Note 1:** If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

**FIGURE 16-11: PIC12F615/617/HV615 A/D CONVERSION TIMING (SLEEP MODE)**




**Note 1:** If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.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## 16.12 High Temperature Operation

This section outlines the specifications for the PIC12F615 device operating in a temperature range between -40°C and 150°C.(4) The specifications between -40°C and 150°C(4) are identical to those shown in DS41288 and DS80329.

**Note 1:** Writes are **not allowed** for Flash Program Memory above 125°C.

**2:** All AC timing specifications are increased by 30%. This derating factor will include parameters such as TPWRT.

**3:** The temperature range indicator in the part number is "H" for -40°C to 150°C.(4)

Example: PIC12F615T-H/ST indicates the device is shipped in a TAPE and reel configuration, in the MSOP package, and is rated for operation from -40°C to 150°C.(4)

**4:** AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

**TABLE 16-13: ABSOLUTE MAXIMUM RATINGS**

| Parameter | Source/Sink | Value | Units |
|---|---|---|---|
| Max. Current: VDD | Source | 20 | mA |
| Max. Current: VSS | Sink | 50 | mA |
| Max. Current: PIN | Source | 5 | mA |
| Max. Current: PIN | Sink | 10 | mA |
| Pin Current: at VOH | Source | 3 | mA |
| Pin Current: at VOL | Sink | 8.5 | mA |
| Port Current: GPIO | Source | 20 | mA |
| Port Current: GPIO | Sink | 50 | mA |
| Maximum Junction Temperature | | 155 | °C |

**Note:** Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

**TABLE 16-14: DC CHARACTERISTICS FOR IDD SPECIFICATIONS FOR PIC12F615-H (High Temp.)**

| Param No. | Device Characteristics | Units | Min | Typ | Max | Condition | |
|---|---|---|---|---|---|---|---|
| | | | | | | VDD | Note |
| D010 | Supply Current (IDD) | μA | — | 13 | 58 | 2.0 | IDD LP OSC (32 kHz) |
| | | | — | 19 | 67 | 3.0 | |
| | | | — | 32 | 92 | 5.0 | |
| D011 | | μA | — | 135 | 316 | 2.0 | IDD XT OSC (1 MHz) |
| | | | — | 185 | 400 | 3.0 | |
| | | | — | 300 | 537 | 5.0 | |
| D012 | | μA | — | 240 | 495 | 2.0 | IDD XT OSC (4 MHz) |
| | | | — | 360 | 680 | 3.0 | |
| | | mA | — | 0.660 | 1.20 | 5.0 | |
| D013 | | μA | — | 75 | 158 | 2.0 | IDD EC OSC (1 MHz) |
| | | | — | 155 | 338 | 3.0 | |
| | | | — | 345 | 792 | 5.0 | |
| D014 | | μA | — | 185 | 357 | 2.0 | IDD EC OSC (4 MHz) |
| | | | — | 325 | 625 | 3.0 | |
| | | mA | — | 0.665 | 1.30 | 5.0 | |
| D016 | | μA | — | 245 | 476 | 2.0 | IDD INTOSC (4 MHz) |
| | | | — | 360 | 672 | 3.0 | |
| | | | — | 620 | 1.10 | 5.0 | |
| D017 | | μA | — | 395 | 757 | 2.0 | IDD INTOSC (8 MHz) |
| | | mA | — | 0.620 | 1.20 | 3.0 | |
| | | | — | 1.20 | 2.20 | 5.0 | |
| D018 | | μA | — | 175 | 332 | 2.0 | IDD EXTRC (4 MHz) |
| | | | — | 285 | 518 | 3.0 | |
| | | | — | 530 | 972 | 5.0 | |
| D019 | | mA | — | 2.20 | 4.10 | 4.5 | IDD HS OSC (20 MHz) |
| | | | — | 2.80 | 4.80 | 5.0 | |


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**TABLE 16-15: DC CHARACTERISTICS FOR IPD SPECIFICATIONS FOR PIC12F615-H (High Temp.)**

| Param No. | Device Characteristics | Units | Min | Typ | Max | Condition | |
|---|---|---|---|---|---|---|---|
| | | | | | | VDD | Note |
| D020E | Power Down Base Current | μA | — | 0.05 | 12 | 2.0 | IPD Base |
| | | | — | 0.15 | 13 | 3.0 | |
| | | | — | 0.35 | 14 | 5.0 | |
| D021E | | μA | — | 0.5 | 20 | 2.0 | WDT Current |
| | | | — | 2.5 | 25 | 3.0 | |
| | | | — | 9.5 | 36 | 5.0 | |
| D022E | | μA | — | 5.0 | 28 | 3.0 | BOR Current |
| | | | — | 6.0 | 36 | 5.0 | |
| D023E | | μA | — | 105 | 195 | 2.0 | IPD Current (Both Comparators Enabled) |
| | | | — | 110 | 210 | 3.0 | |
| | | | — | 116 | 220 | 5.0 | |
| | | μA | — | 50 | 105 | 2.0 | IPD Current (One Comparator Enabled) |
| | | | — | 55 | 110 | 3.0 | |
| | | | — | 60 | 125 | 5.0 | |
| D024E | | μA | — | 30 | 58 | 2.0 | IPD (CVREF, High Range) |
| | | | — | 45 | 85 | 3.0 | |
| | | | — | 75 | 142 | 5.0 | |
| D025E | | μA | — | 39 | 76 | 2.0 | IPD (CVREF, Low Range) |
| | | | — | 59 | 114 | 3.0 | |
| | | | — | 98 | 190 | 5.0 | |
| D026E | | μA | — | 5.5 | 30 | 2.0 | IPD (T1 OSC, 32 kHz) |
| | | | — | 7.0 | 35 | 3.0 | |
| | | | — | 8.5 | 45 | 5.0 | |
| D027E | | μA | — | 0.2 | 12 | 3.0 | IPD (A2D on, not converting) |
| | | | — | 0.3 | 15 | 5.0 | |

**TABLE 16-16: WATCHDOG TIMER SPECIFICATIONS FOR PIC12F615-H (High Temp.)**

| Param No. | Sym | Characteristic | Units | Min | Typ | Max | Conditions |
|---|---|---|---|---|---|---|---|
| 31 | TWDT | Watchdog Timer Time-out Period (No Prescaler) | ms | 6 | 20 | 70 | 150°C Temperature |

**TABLE 16-17: LEAKAGE CURRENT SPECIFICATIONS FOR PIC12F615-H (High Temp.)**

| Param No. | Sym | Characteristic | Units | Min | Typ | Max | Conditions |
|---|---|---|---|---|---|---|---|
| D061 | IIL | Input Leakage Current(1) (GP3/RA3/$\overline{\text{MCLR}}$) | μA | — | ±0.5 | ±5.0 | VSS ≤ VPIN ≤ VDD |
| D062 | IIL | Input Leakage Current(2) (GP3/RA3/$\overline{\text{MCLR}}$) | μA | 50 | 250 | 400 | VDD = 5.0V |

**Note 1:** This specification applies when GP3/RA3/$\overline{\text{MCLR}}$ is configured as an input with the pull-up disabled. The leakage current for the GP3/RA3/$\overline{\text{MCLR}}$ pin is higher than for the standard I/O port pins.

**2:** This specification applies when GP3/RA3/$\overline{\text{MCLR}}$ is configured as the $\overline{\text{MCLR}}$ reset pin function with the weak pull-up enabled.

**TABLE 16-18: OSCILLATOR PARAMETERS FOR PIC12F615-H (High Temp.)**

| Param No. | Sym | Characteristic | Frequency Tolerance | Units | Min | Typ | Max | Conditions |
|---|---|---|---|---|---|---|---|---|
| OS08 | INTOSC | Int. Calibrated INTOSC Freq.(1) | ±10% | MHz | 7.2 | 8.0 | 8.8 | 2.0V ≤ VDD ≤ 5.5V<br>-40°C ≤ TA ≤ 150°C |

**Note 1:** To ensure these oscillator frequency tolerances, Vdd and Vss must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

**TABLE 16-19: COMPARATOR SPECIFICATIONS FOR PIC12F615-H (High Temp.)**

| Param No. | Sym | Characteristic | Units | Min | Typ | Max | Conditions |
|---|---|---|---|---|---|---|---|
| CM01 | VOS | Input Offset Voltage | mV | — | ±5 | ±20 | (VDD - 1.5)/2 |


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## 17.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

| | |
|---|---|
| **Note:** | The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range. |

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where s is a standard deviation, over each temperature range.

**FIGURE 17-1: PIC12F609/615/617 IDD LP (32 kHz) vs. VDD**

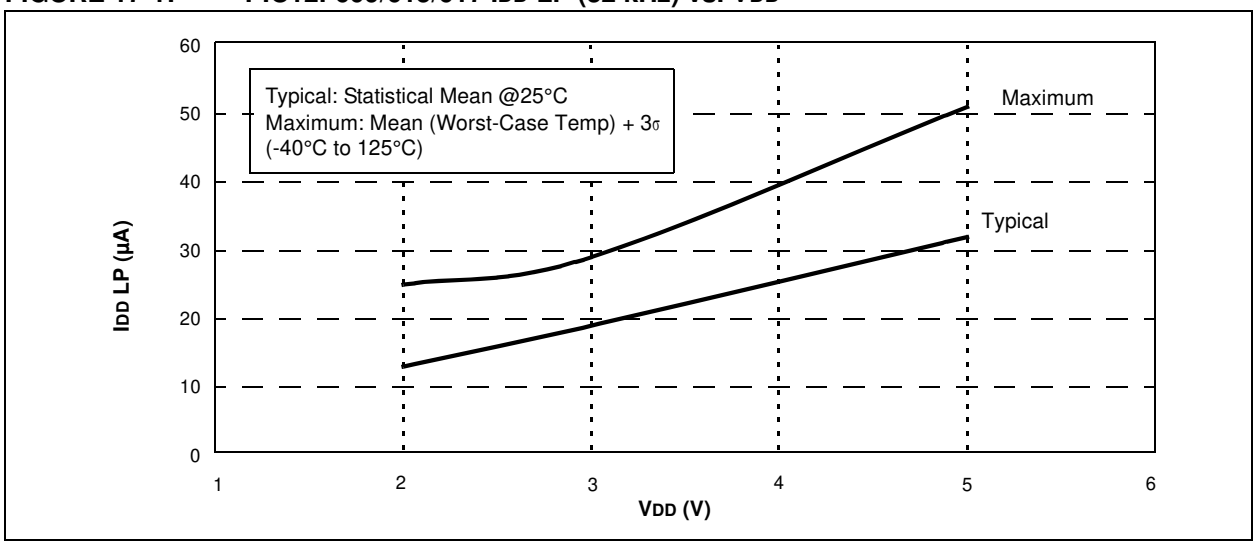


**FIGURE 17-2: PIC12F609/615/617 IDD EC (1 MHz) vs. VDD**

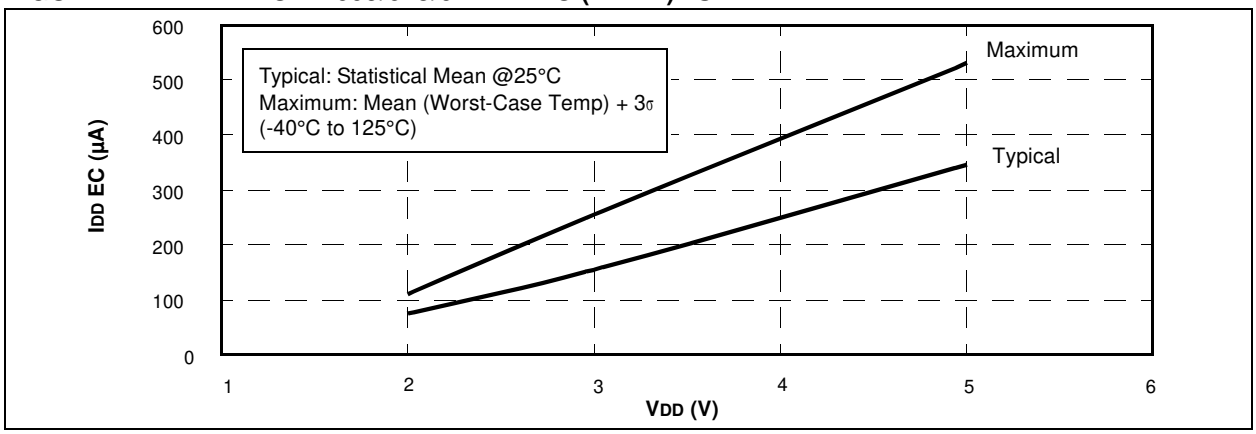

**FIGURE 17-3: PIC12F609/615/617 IDD EC (4 MHz) vs. VDD**

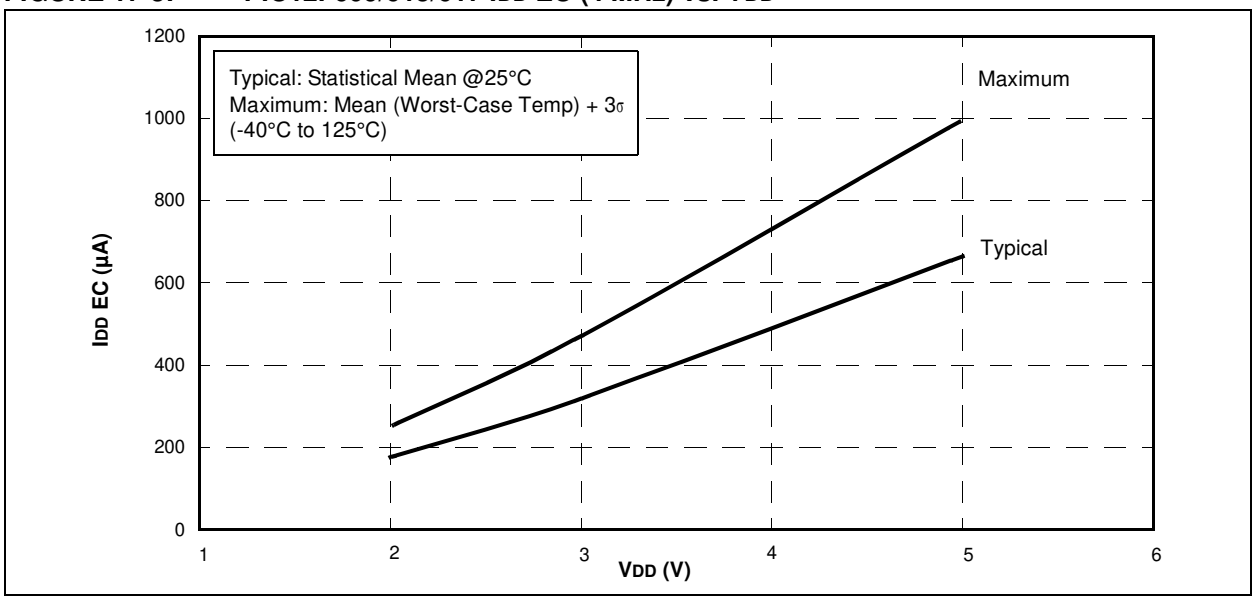


**FIGURE 17-4: PIC12F609/615/617 IDD XT (1 MHz) vs. VDD**

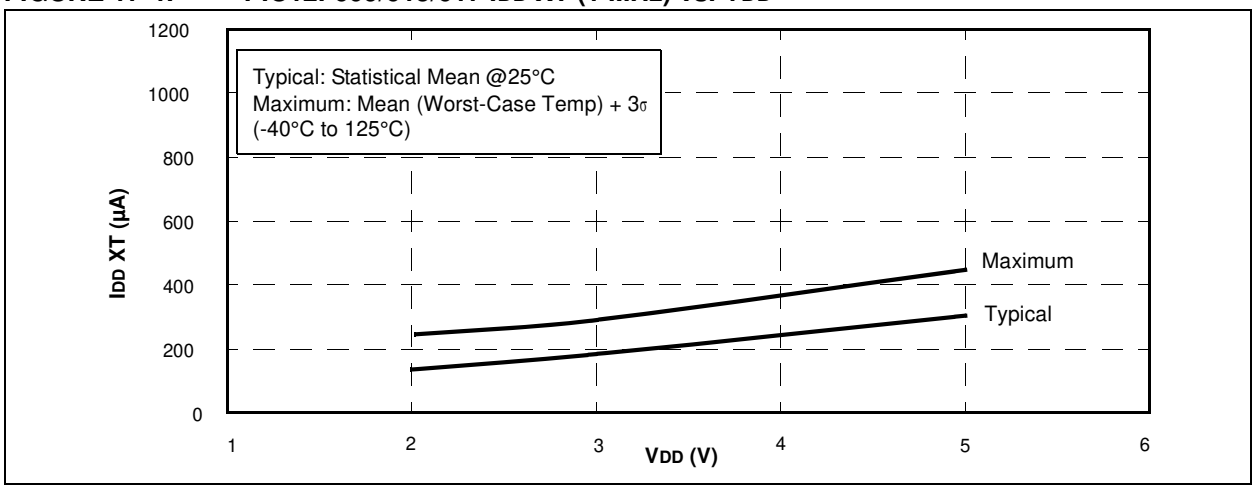


**FIGURE 17-5: PIC12F609/615/617 IDD XT (4 MHz) vs. VDD**

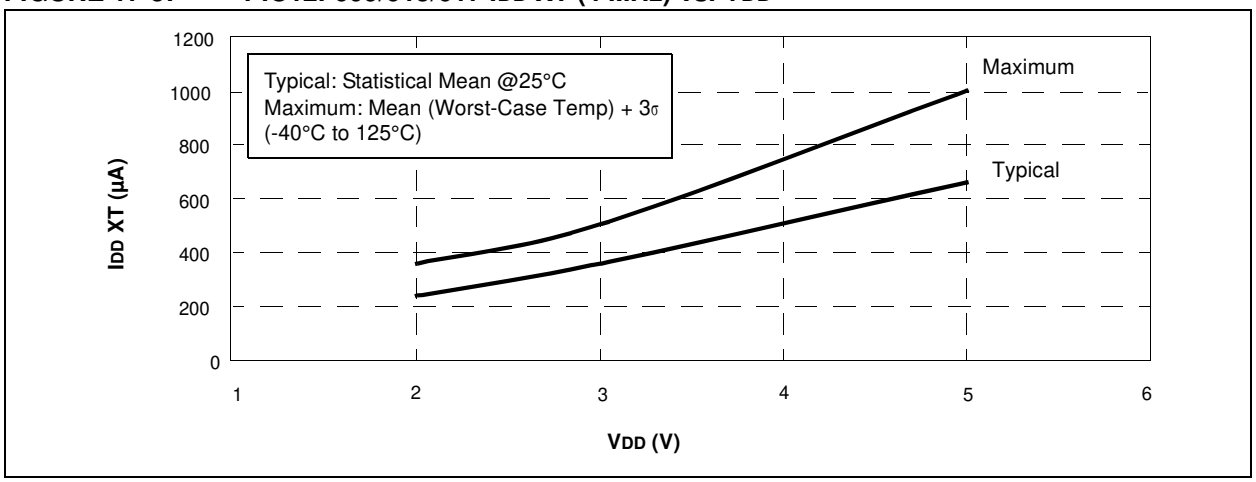



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**FIGURE 17-6: PIC12F609/615/617 IDD INTOSC (4 MHz) vs. VDD**

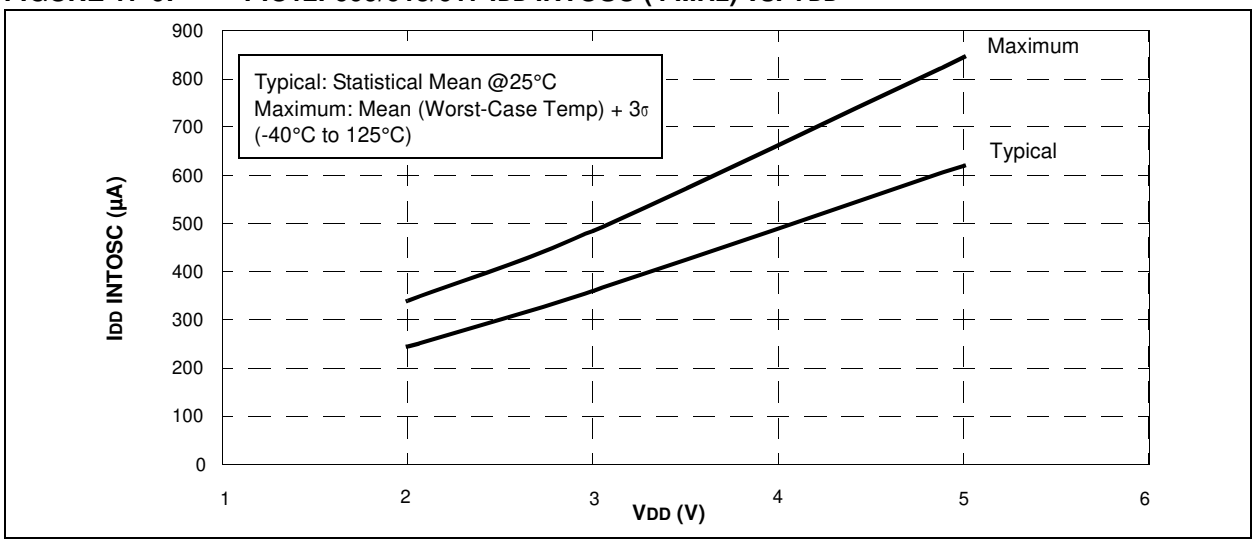


**FIGURE 17-7: PIC12F609/615/617 IDD INTOSC (8 MHz) vs. VDD**

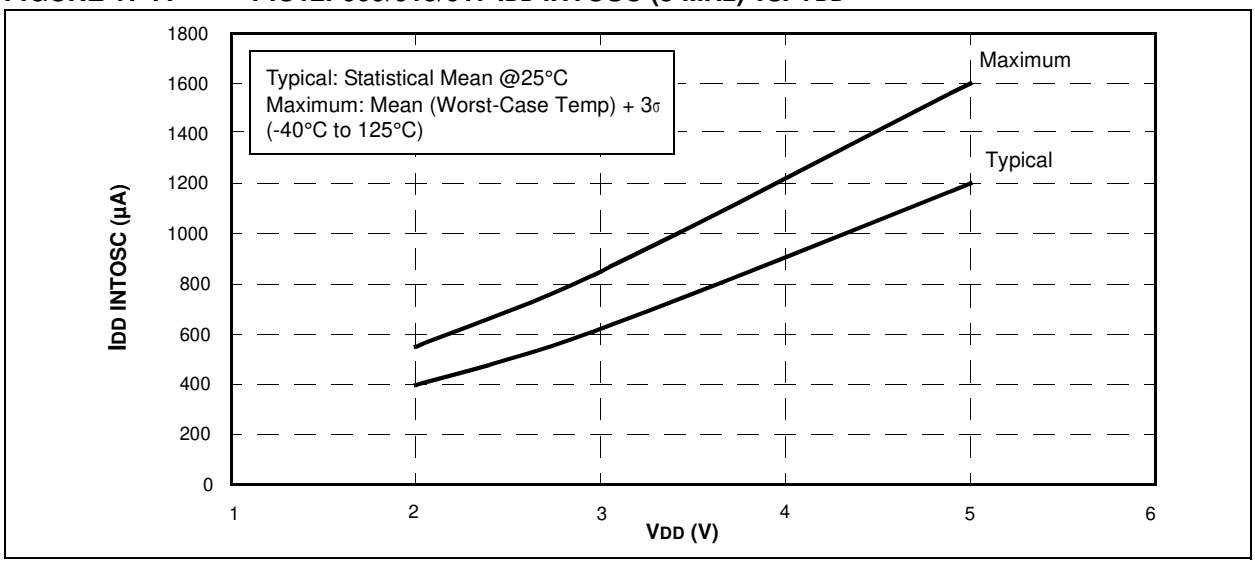

**FIGURE 17-8: PIC12F609/615617 IDD EXTRC (4 MHz) vs. VDD**

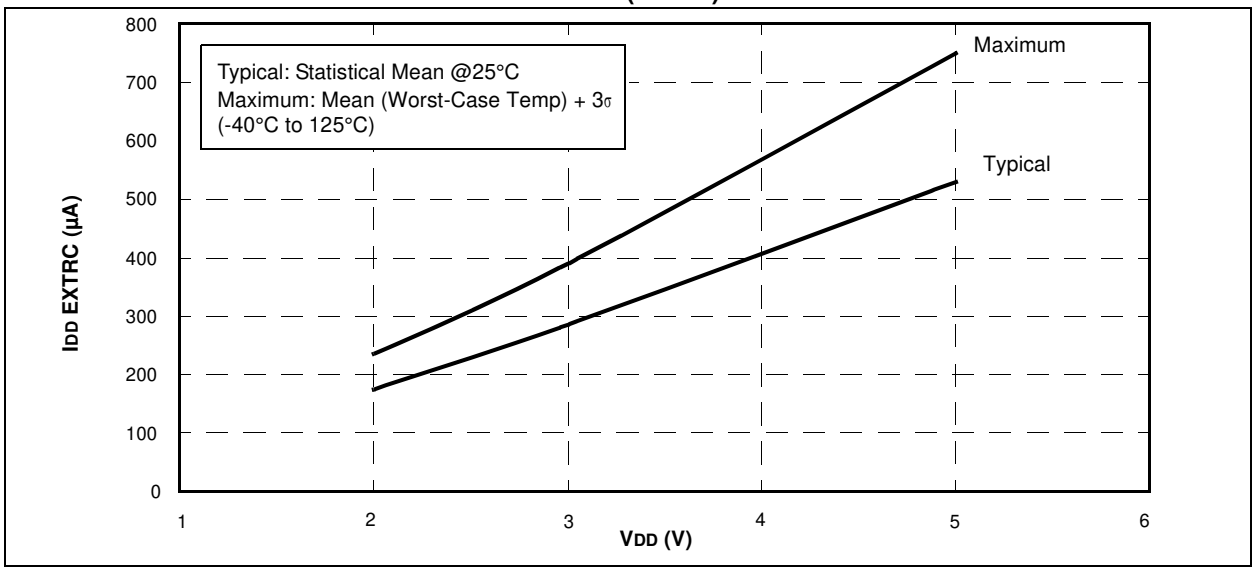


**FIGURE 17-9: PIC12F609/615/617 IDD HS (20 MHz) vs. VDD**

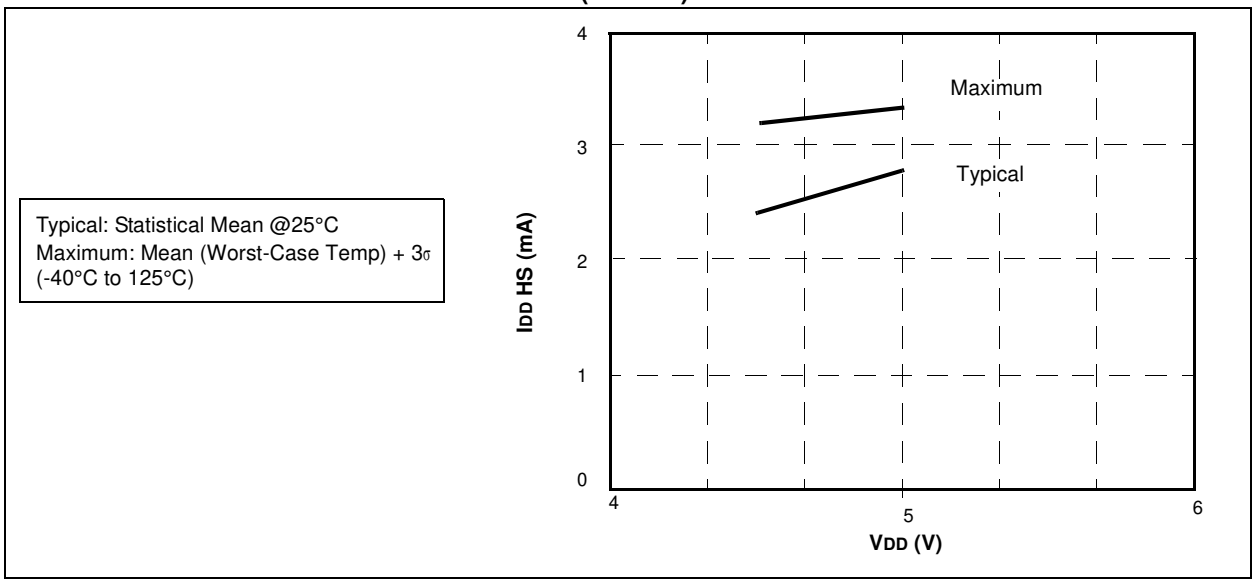



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**FIGURE 17-10: PIC12F609/615/617 IPD BASE vs. VDD**

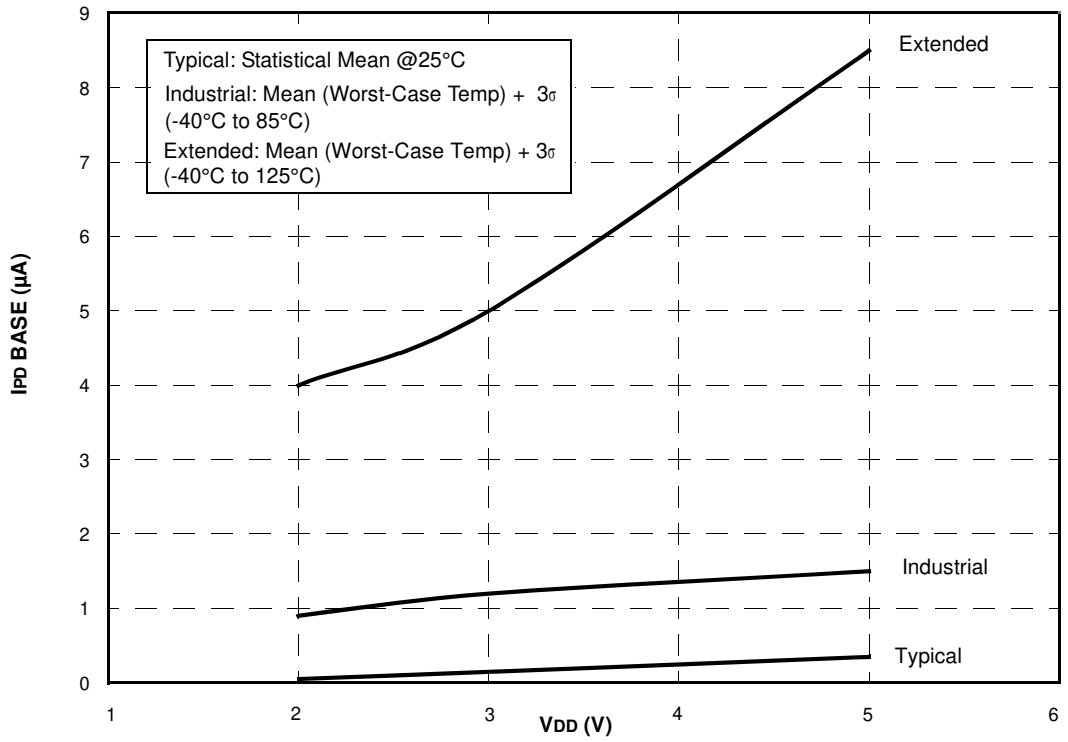


**FIGURE 17-11: PIC12F609/615/617 IPD COMPARATOR (SINGLE ON) vs. VDD**

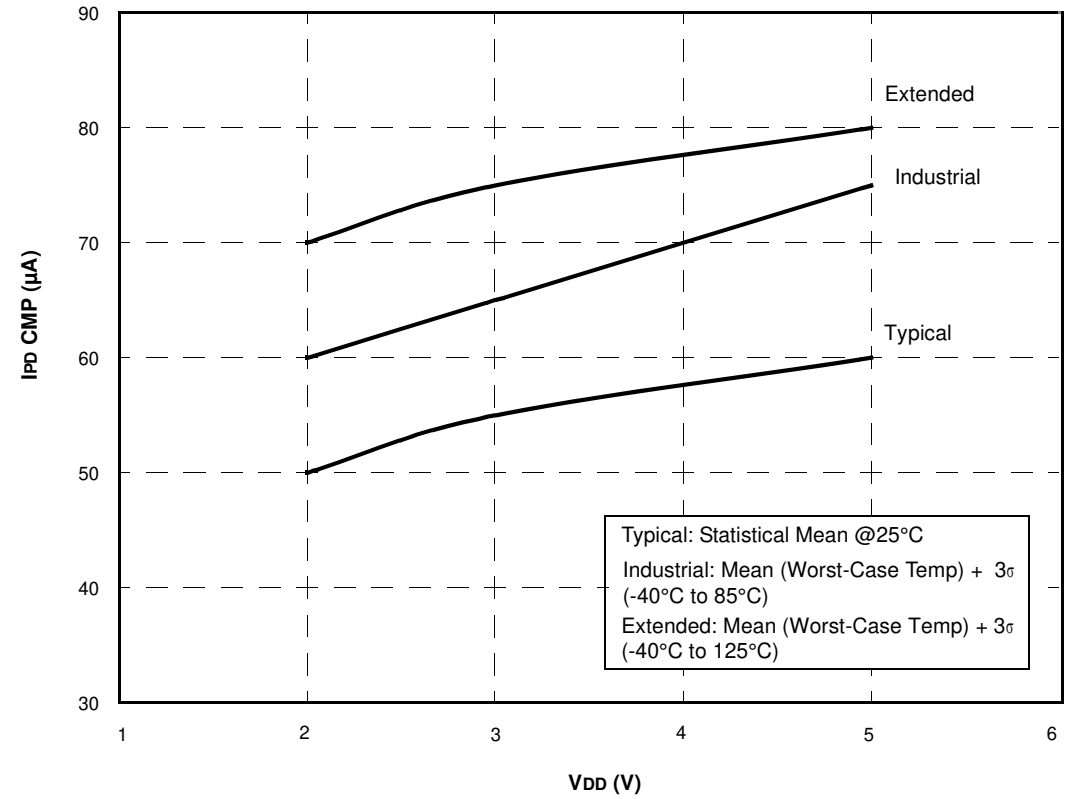

**FIGURE 17-12: PIC12F609/615/617 IPD WDT vs. VDD**

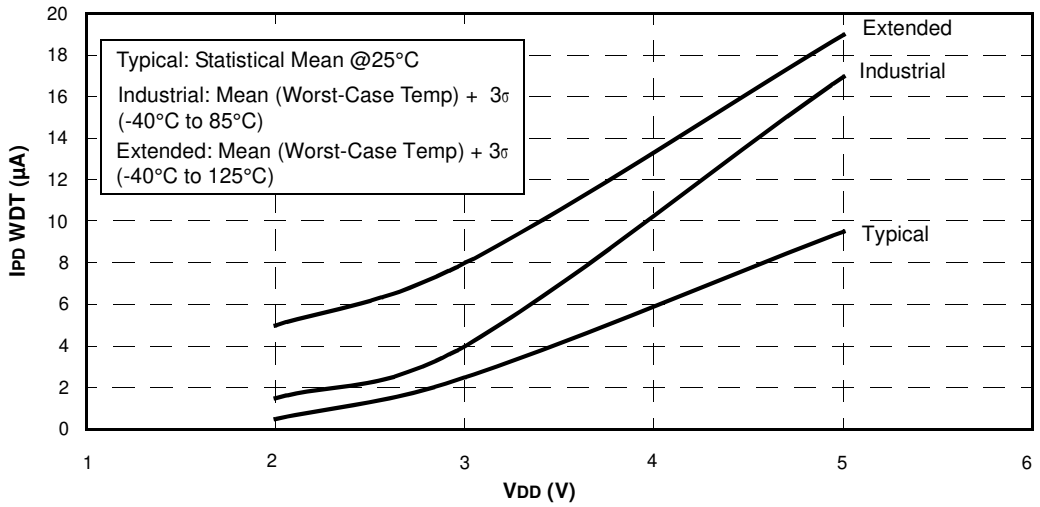


**FIGURE 17-13: PIC12F609/615/617 IPD BOR vs. VDD**

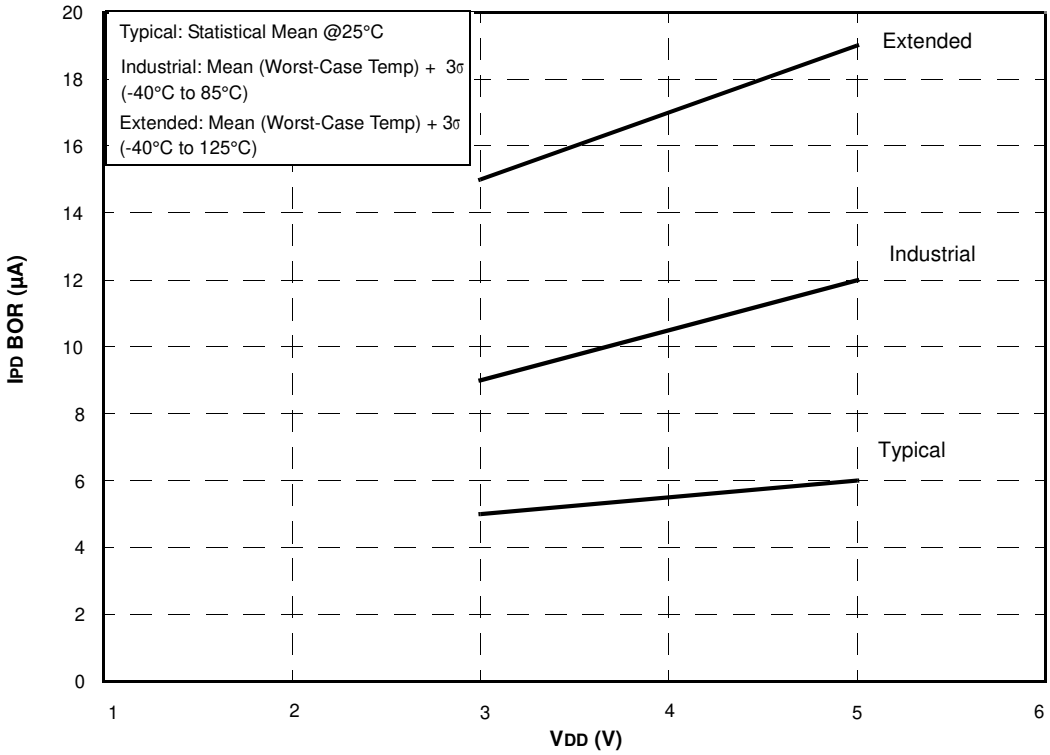



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**FIGURE 17-14: PIC12F609/615/617 IPD CVREF (LOW RANGE) vs. VDD**

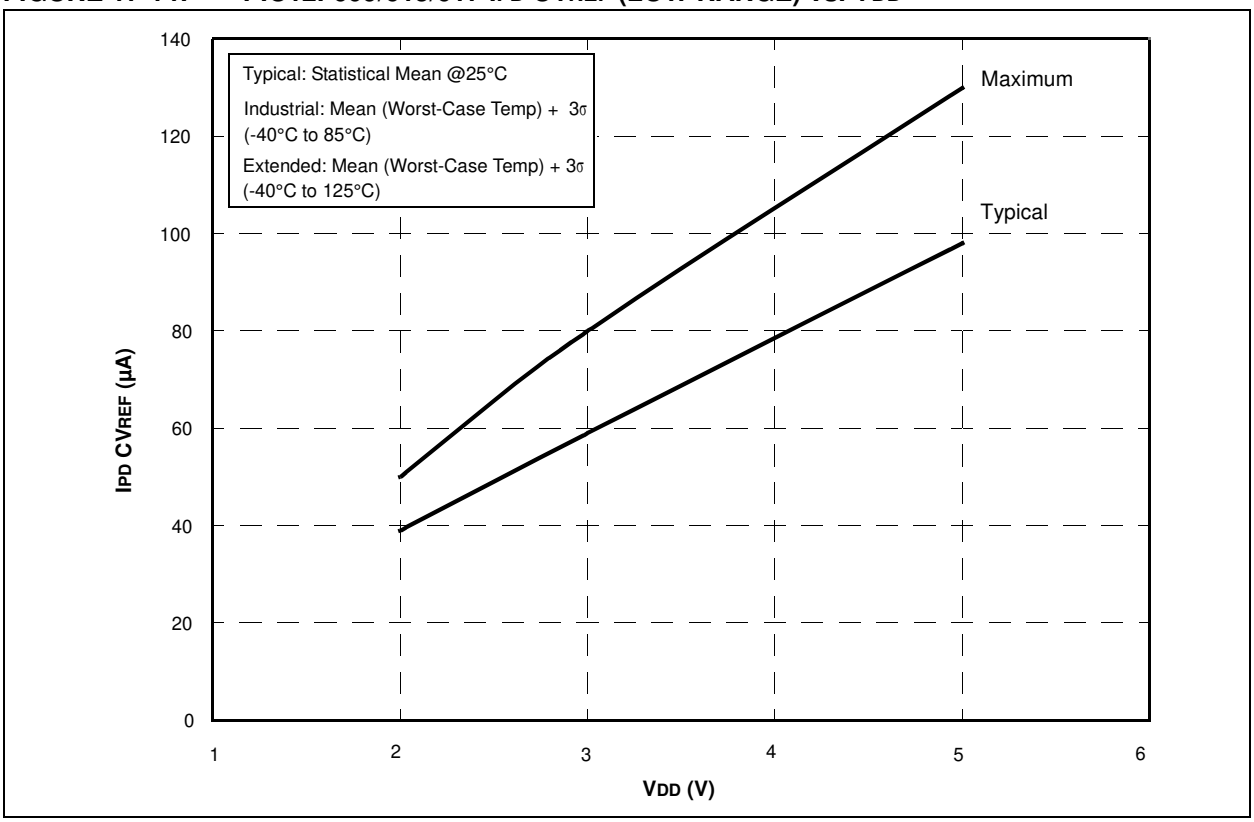


**FIGURE 17-15: PIC12F609/615/617 IPD CVREF (HI RANGE) vs. VDD**

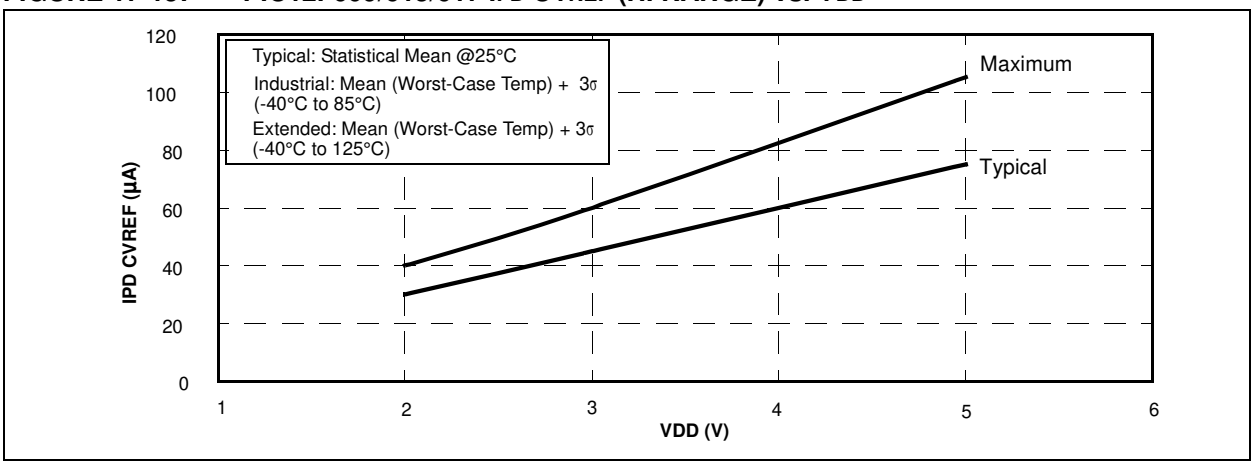

**FIGURE 17-16: PIC12F609/615/617 IPD T1OSC vs. VDD**

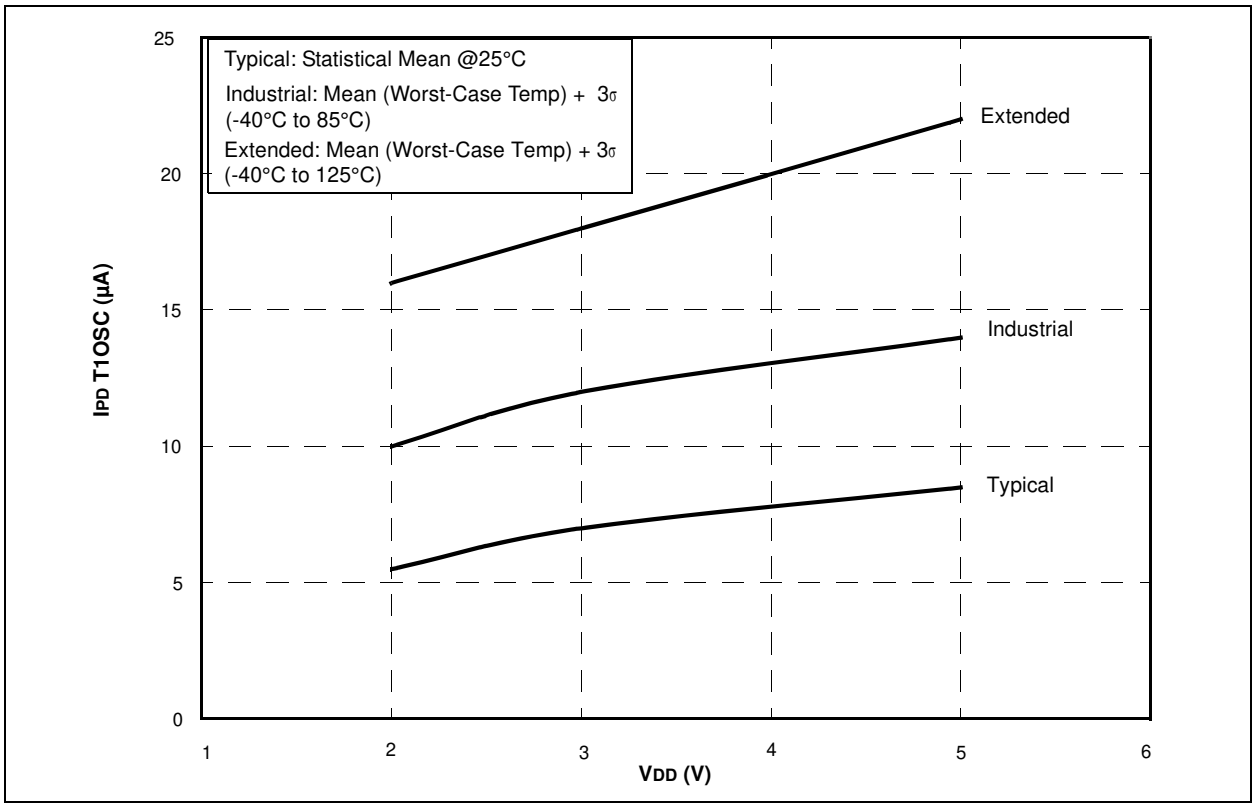


**FIGURE 17-17: PIC12F615/617 IPD A/D vs. VDD**

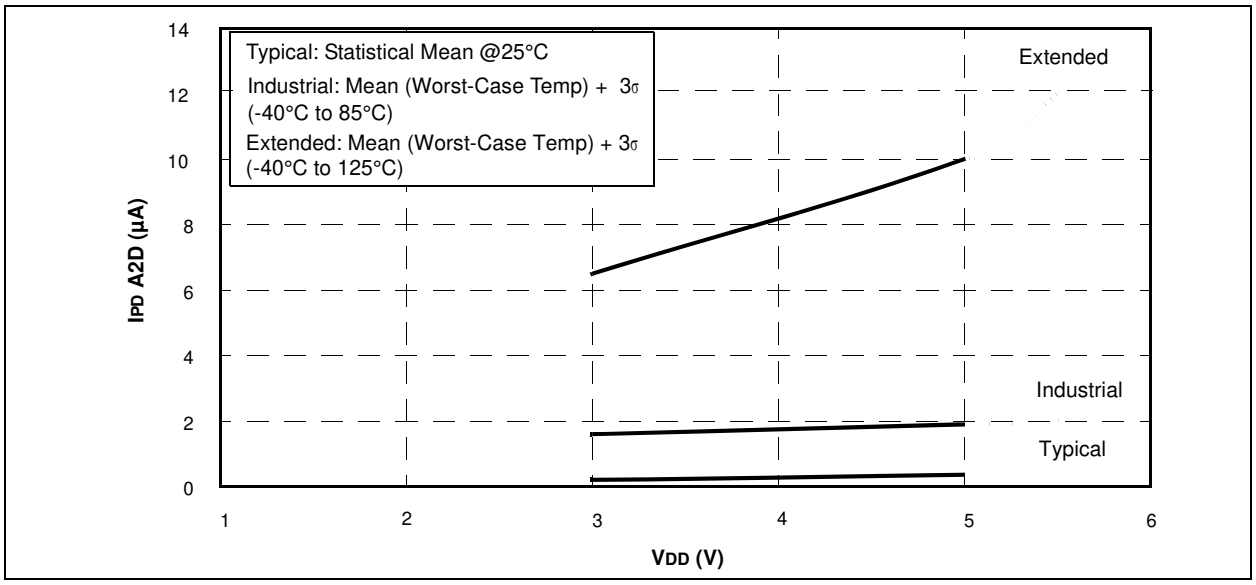



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**FIGURE 17-18: PIC12HV609/615 IDD LP (32 kHz) vs. VDD**

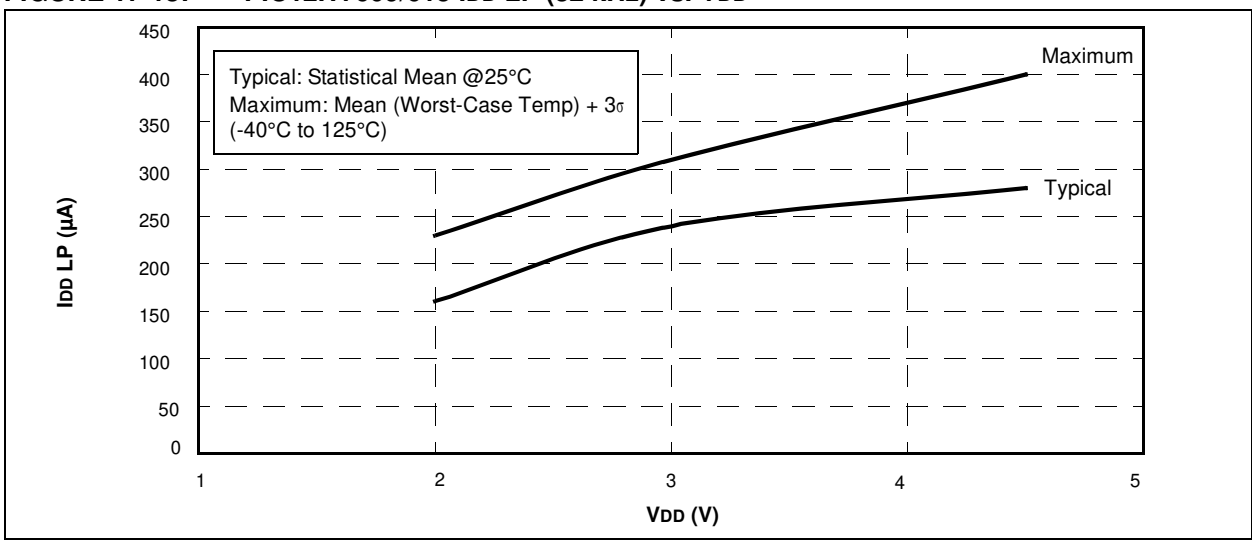


**FIGURE 17-19: PIC12HV609/615 IDD EC (1 MHz) vs. VDD**

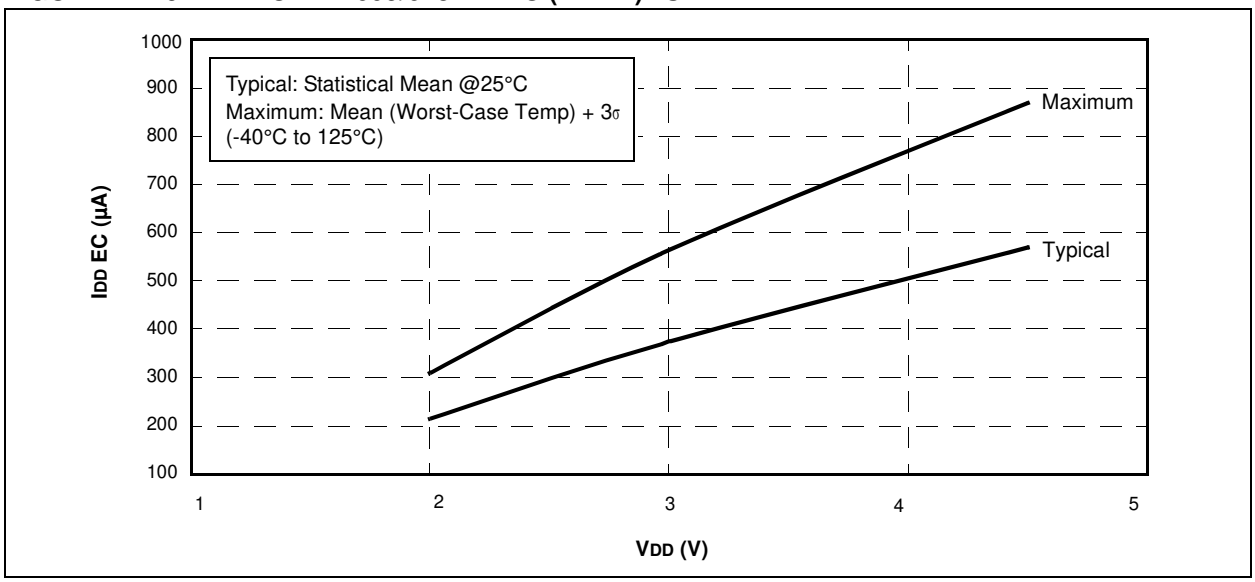


**FIGURE 17-20: PIC12HV609/615 IDD EC (4 MHz) vs. VDD**

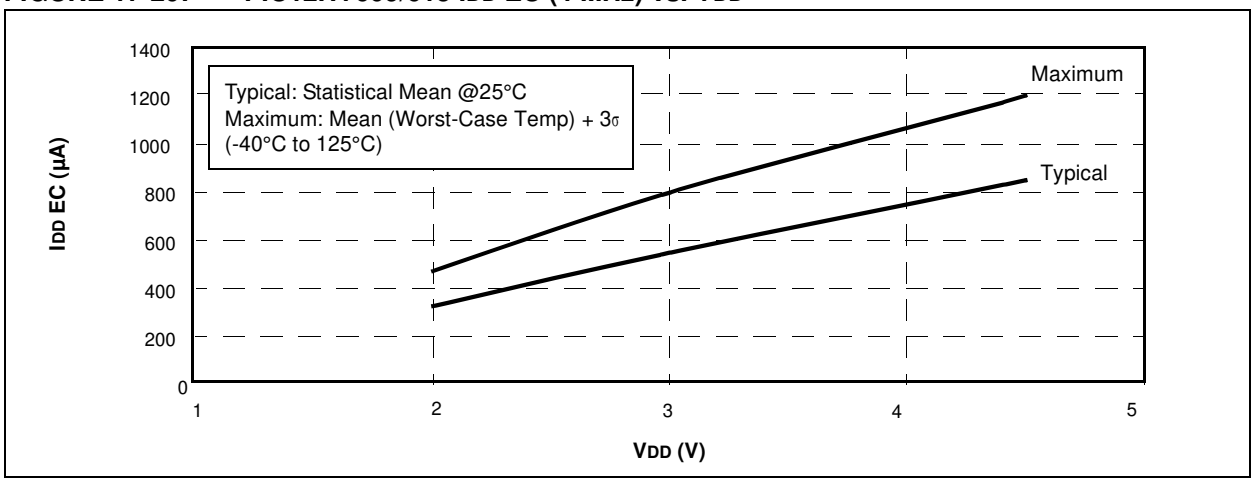

**FIGURE 17-21: PIC12HV609/615 IDD XT (1 MHz) vs. VDD**

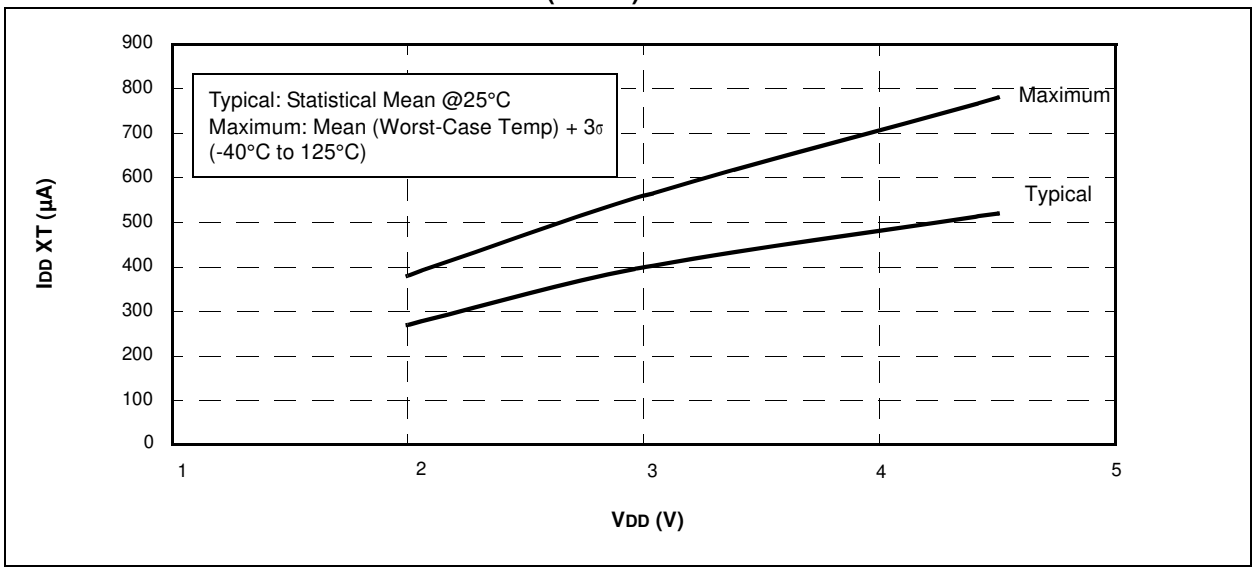


**FIGURE 17-22: PIC12HV609/615 IDD XT (4 MHz) vs. VDD**

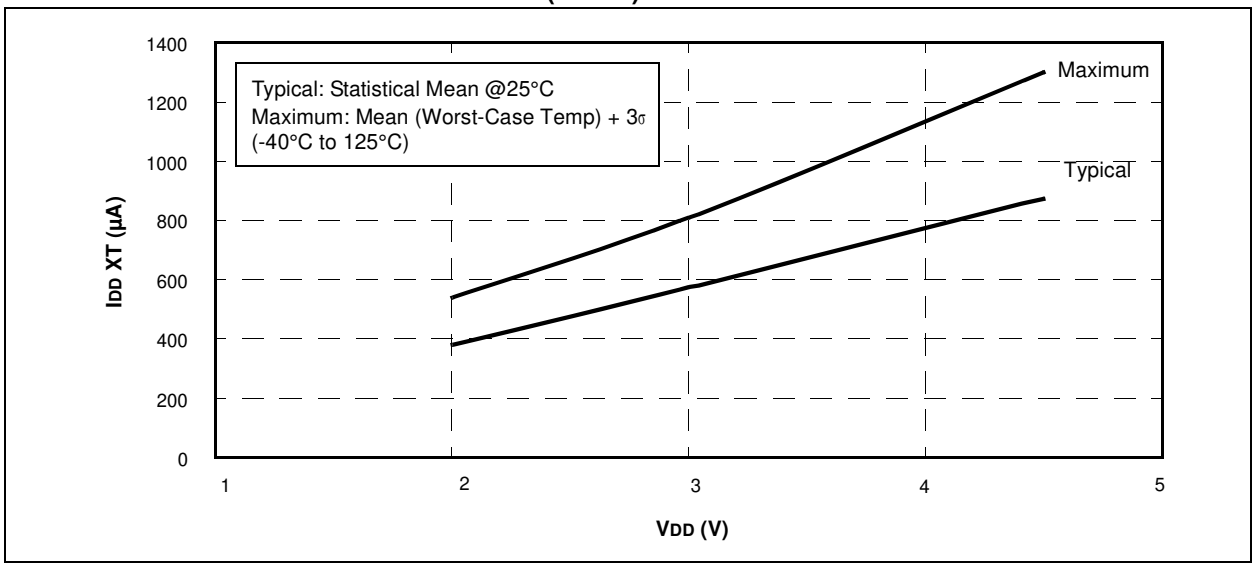


**FIGURE 17-23: PIC12HV609/615 IDD INTOSC (4 MHz) vs. VDD**

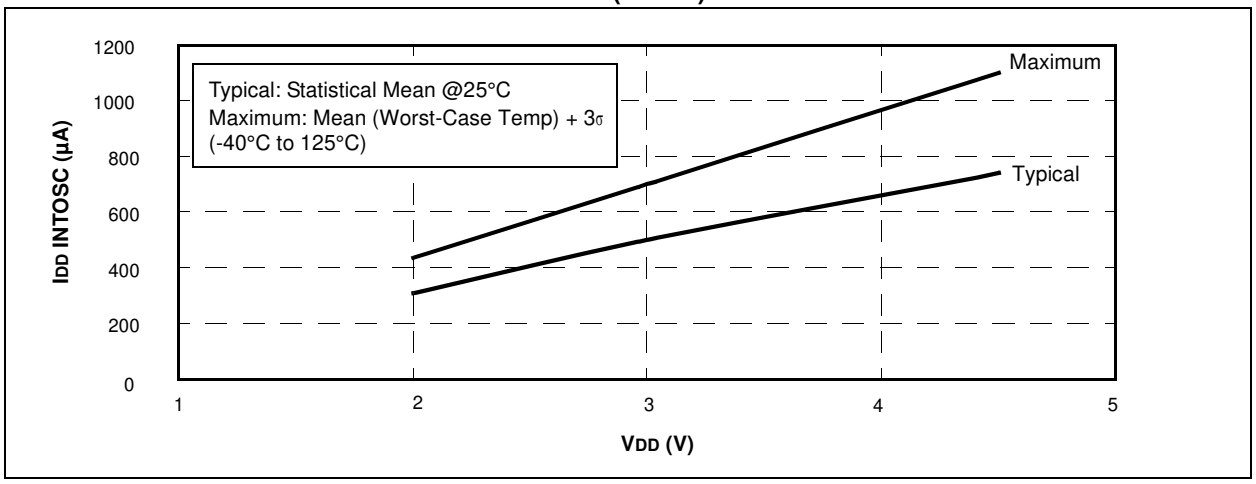



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**FIGURE 17-24: PIC12HV609/615 IDD INTOSC (8 MHz) vs. VDD**

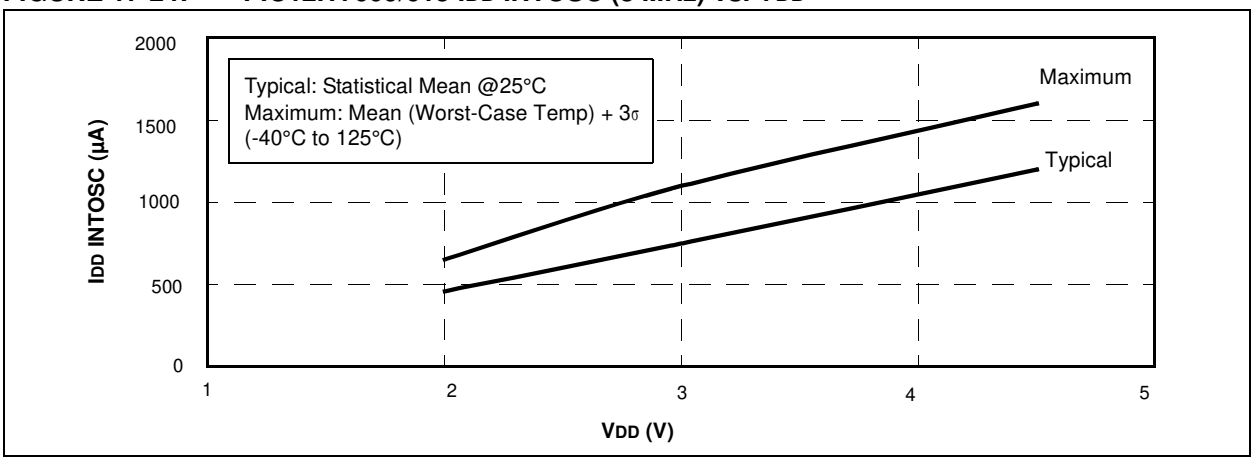


**FIGURE 17-25: PIC12HV609/615 IDD EXTRC (4 MHz) vs. VDD**

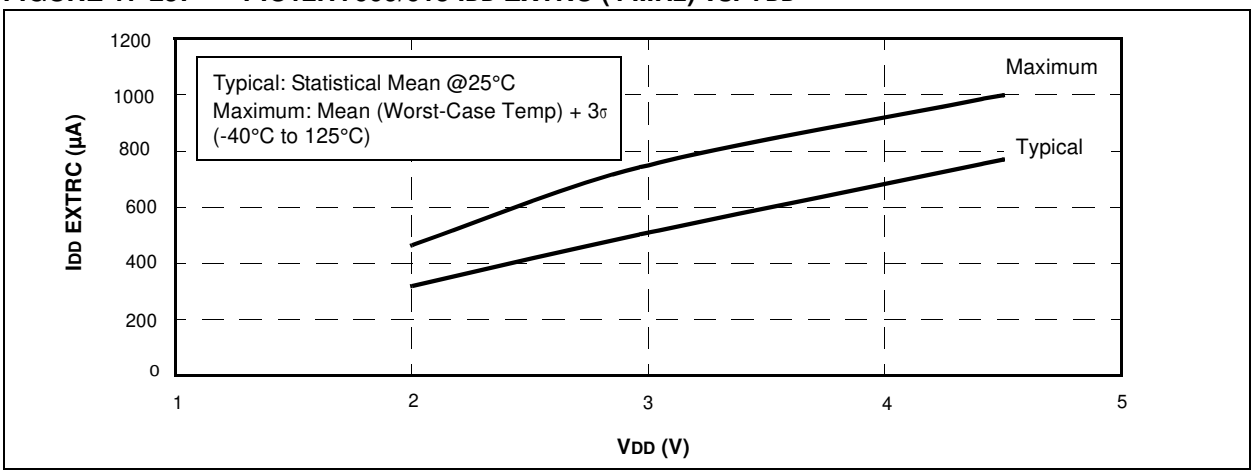


**FIGURE 17-26: PIC12HV609/615 IPD BASE vs. VDD**

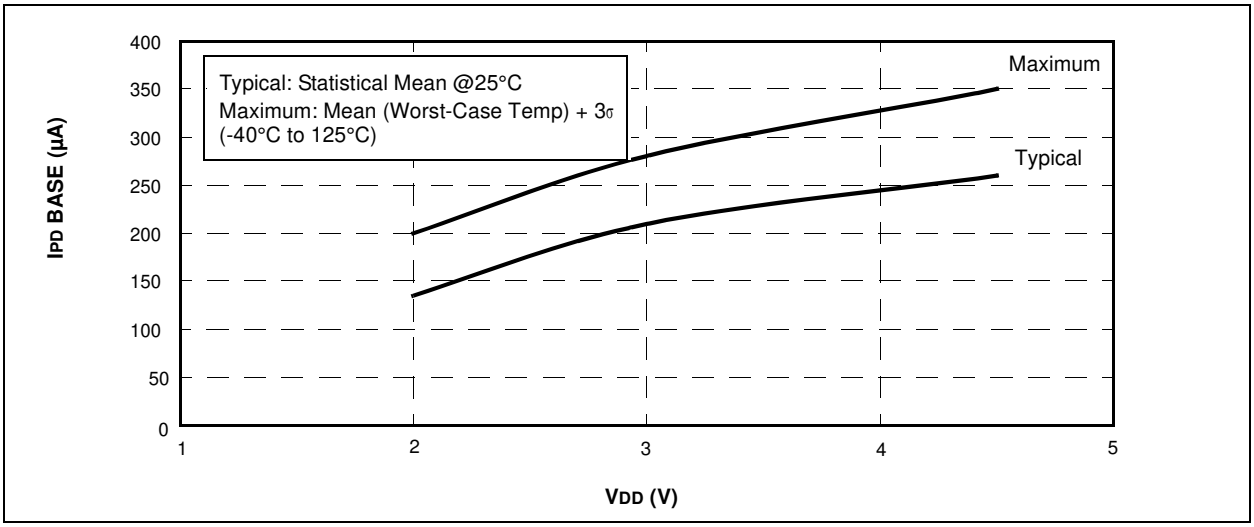

**FIGURE 17-27: PIC12HV609/615 IPD COMPARATOR (SINGLE ON) vs. VDD**

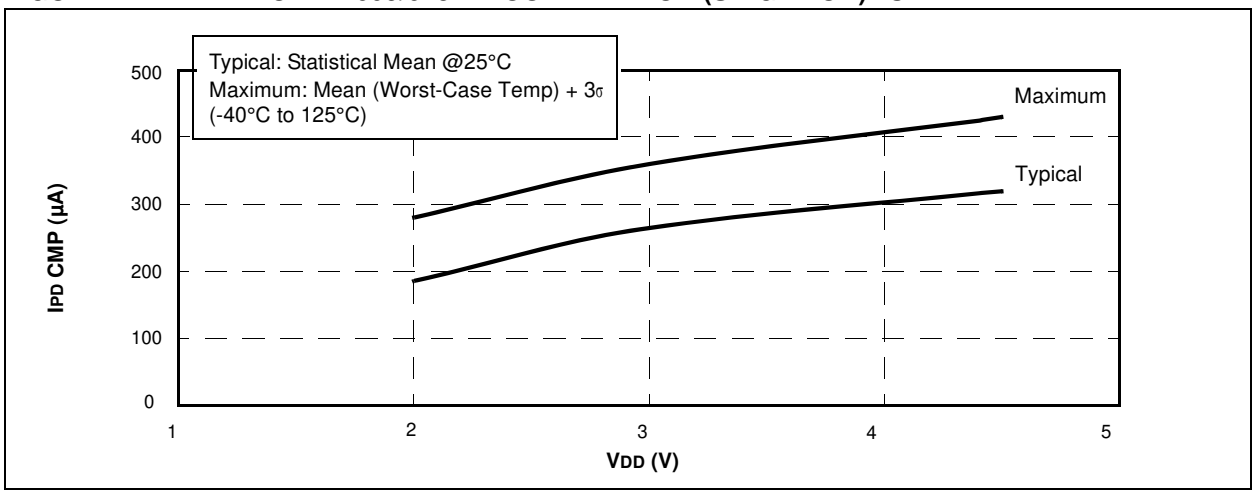


**FIGURE 17-28: PIC12HV609/615 IPD WDT vs. VDD**

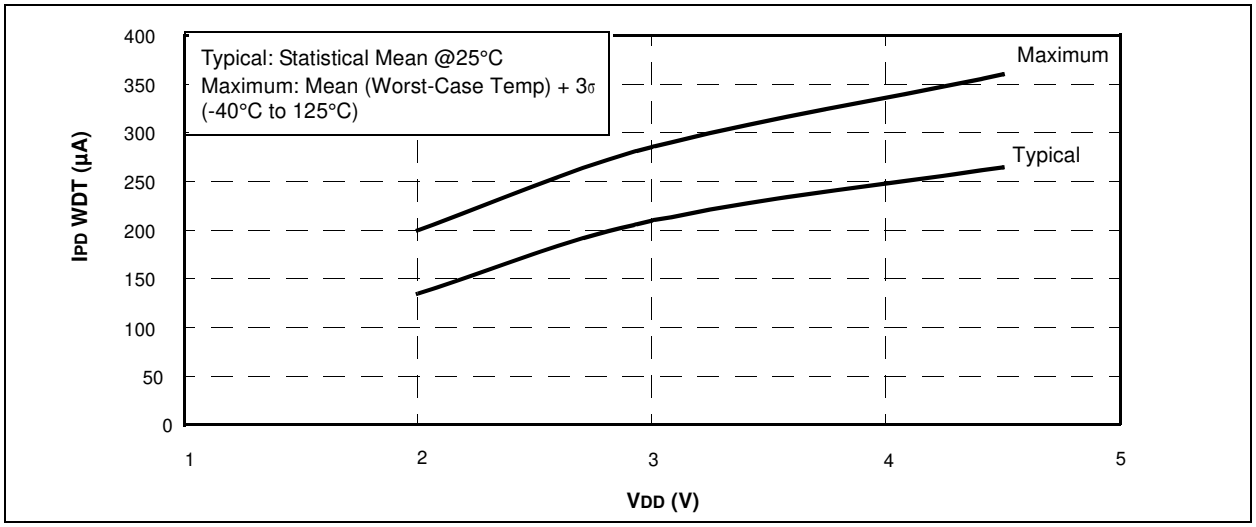


**FIGURE 17-29: PIC12HV609/615 IPD BOR vs. VDD**

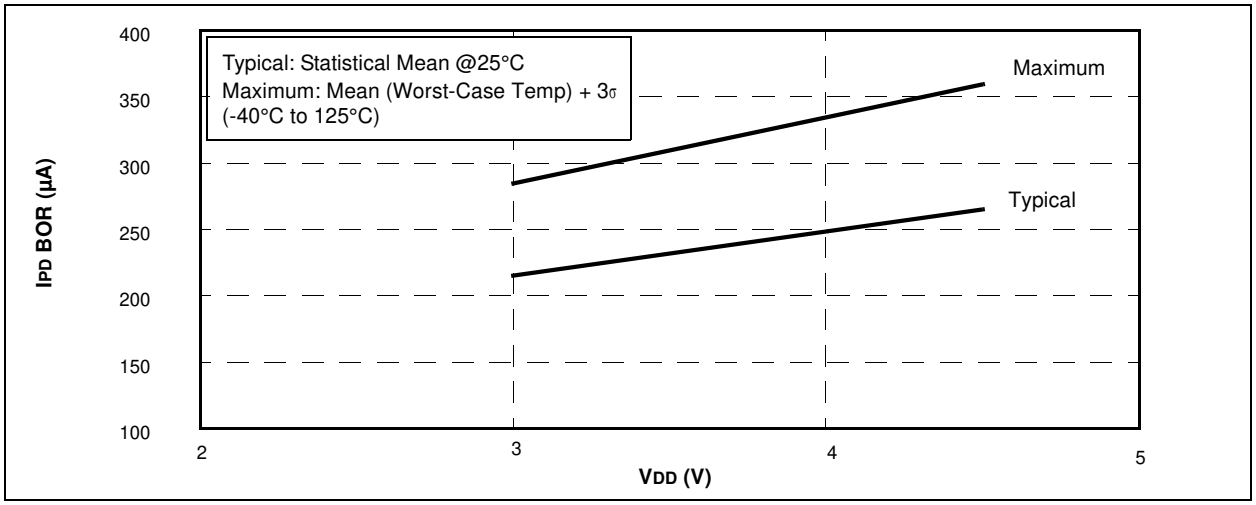



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**FIGURE 17-30: PIC12HV609/615 IPD CVREF (LOW RANGE) vs. VDD**

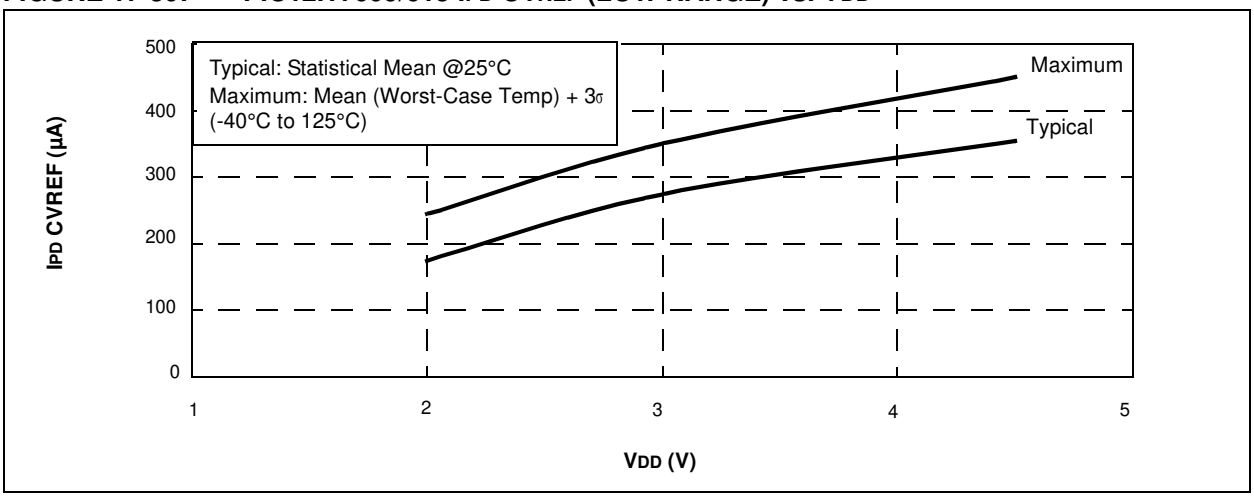


**FIGURE 17-31: PIC12HV609/615 IPD CVREF (HI RANGE) vs. VDD**

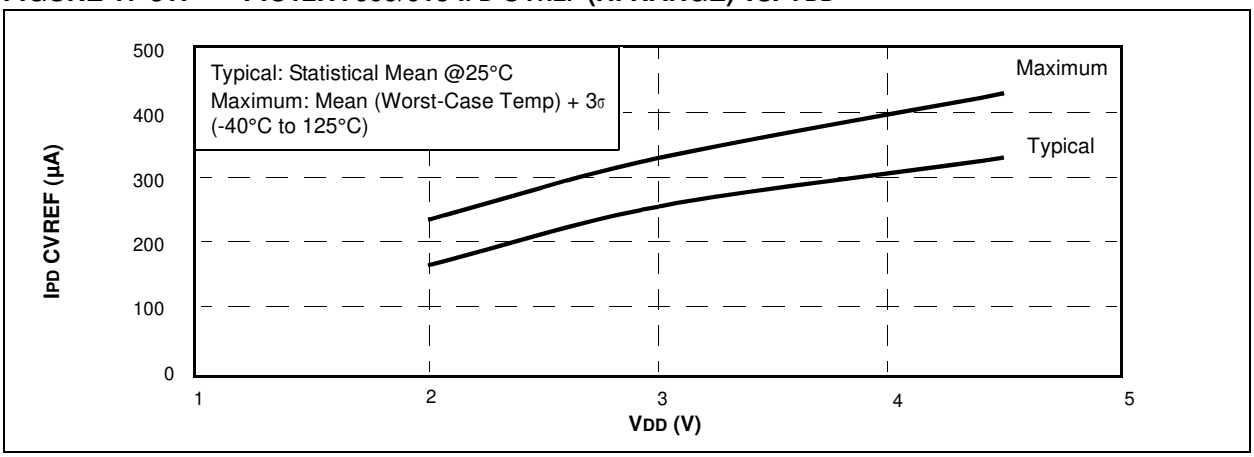


**FIGURE 17-32: PIC12HV609/615 IPD T1OSC vs. VDD**

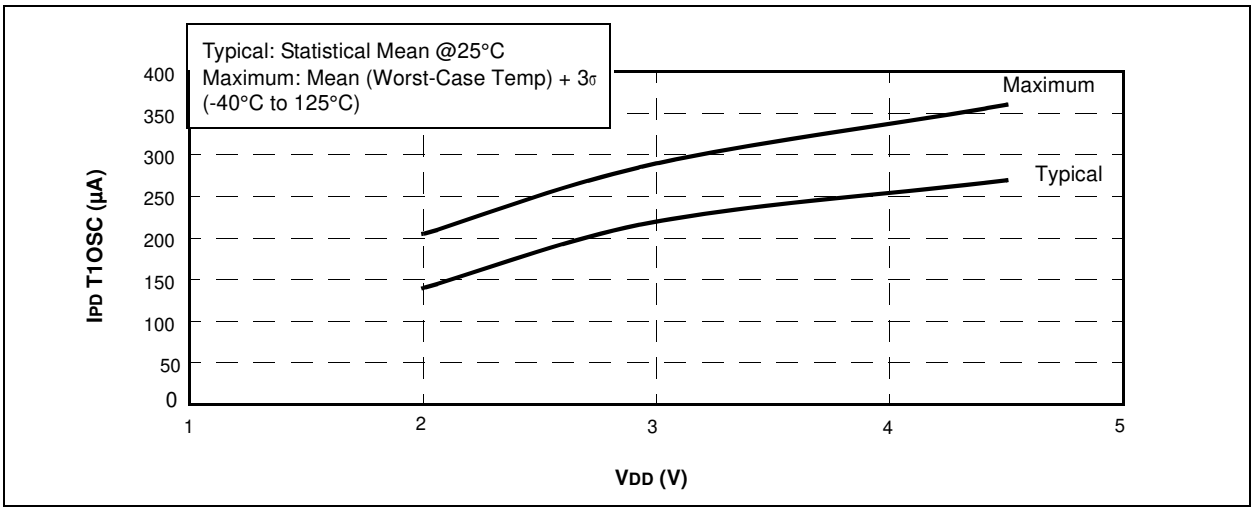

**FIGURE 17-33: PIC12HV615 IPD A/D vs. VDD**

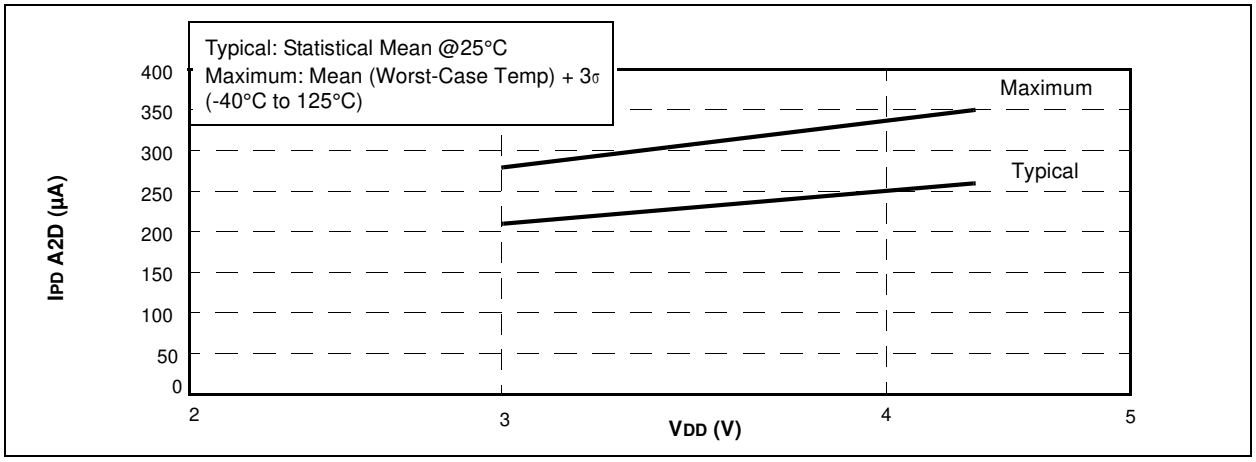


**FIGURE 17-34: VOL vs. IOL OVER TEMPERATURE (VDD = 3.0V)**

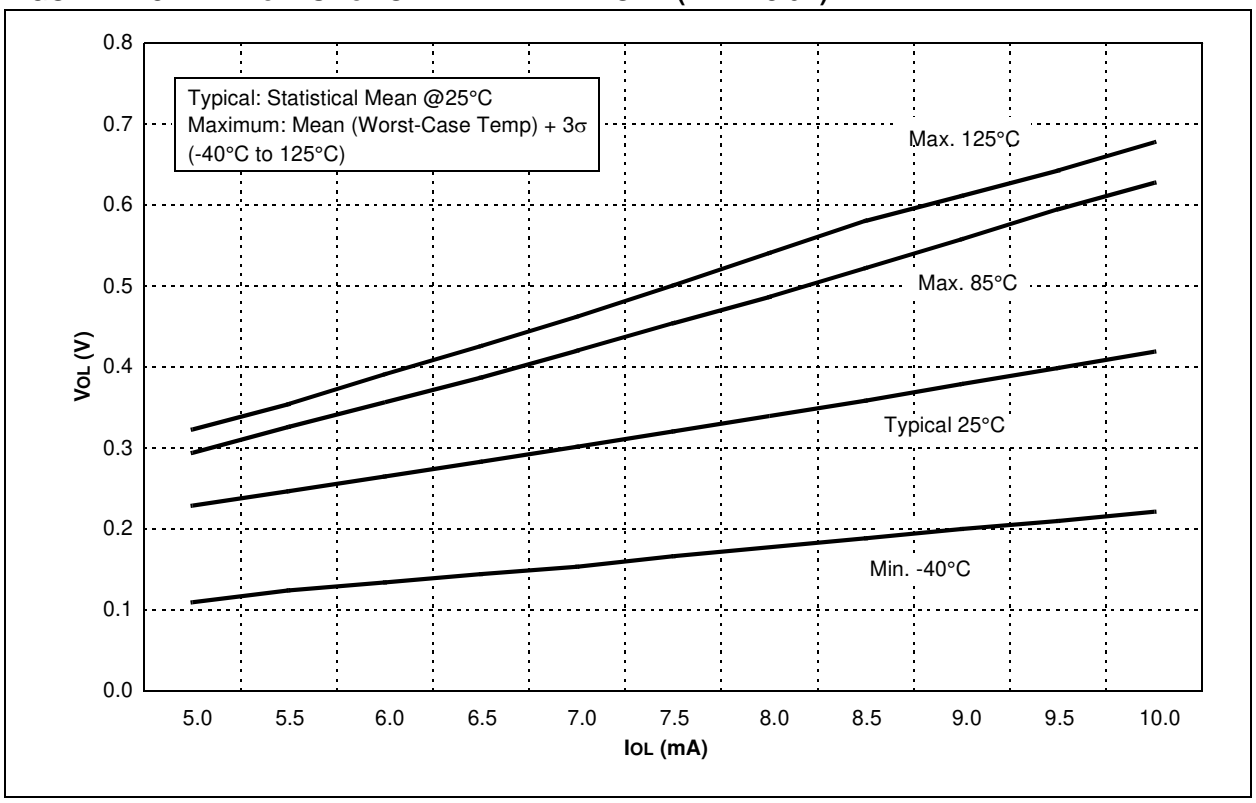



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**FIGURE 17-35: VOL vs. IOL OVER TEMPERATURE (VDD = 5.0V)**

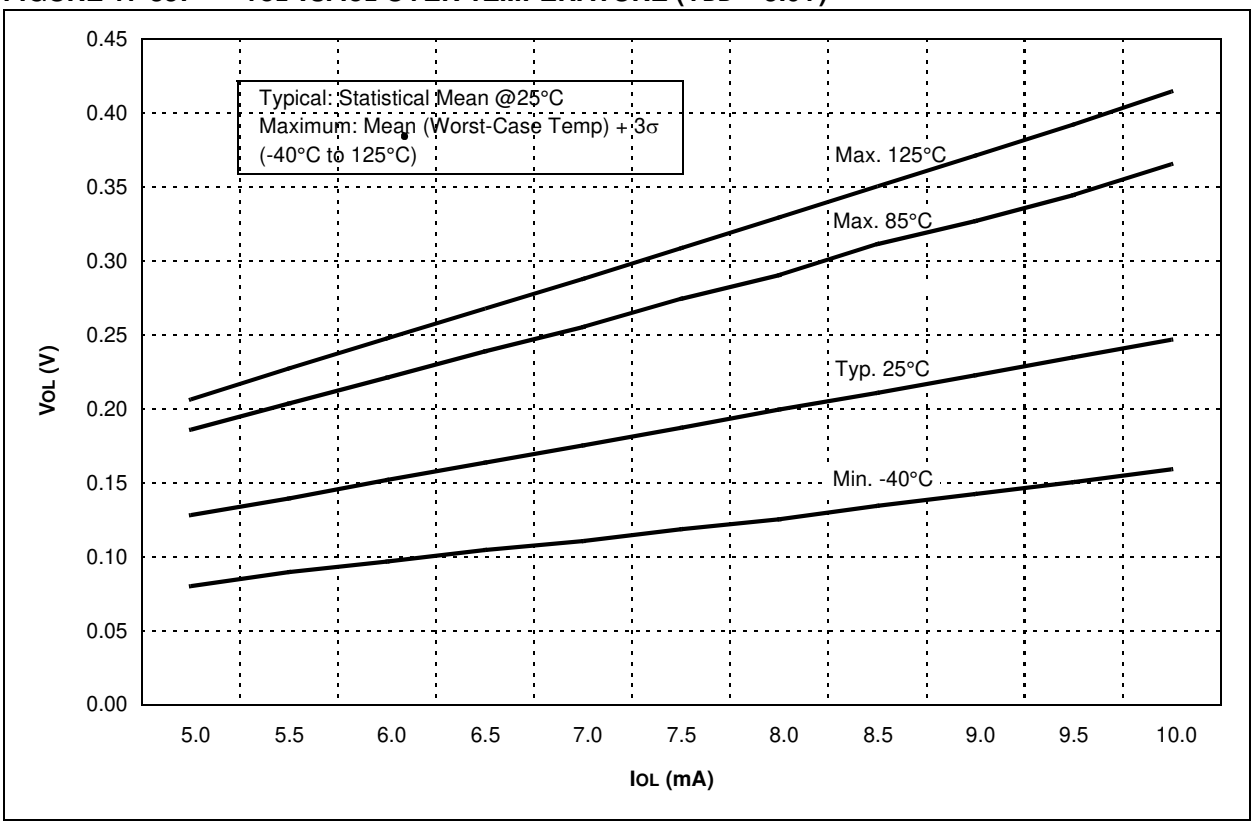


**FIGURE 17-36: VOH vs. IOH OVER TEMPERATURE (VDD = 3.0V)**

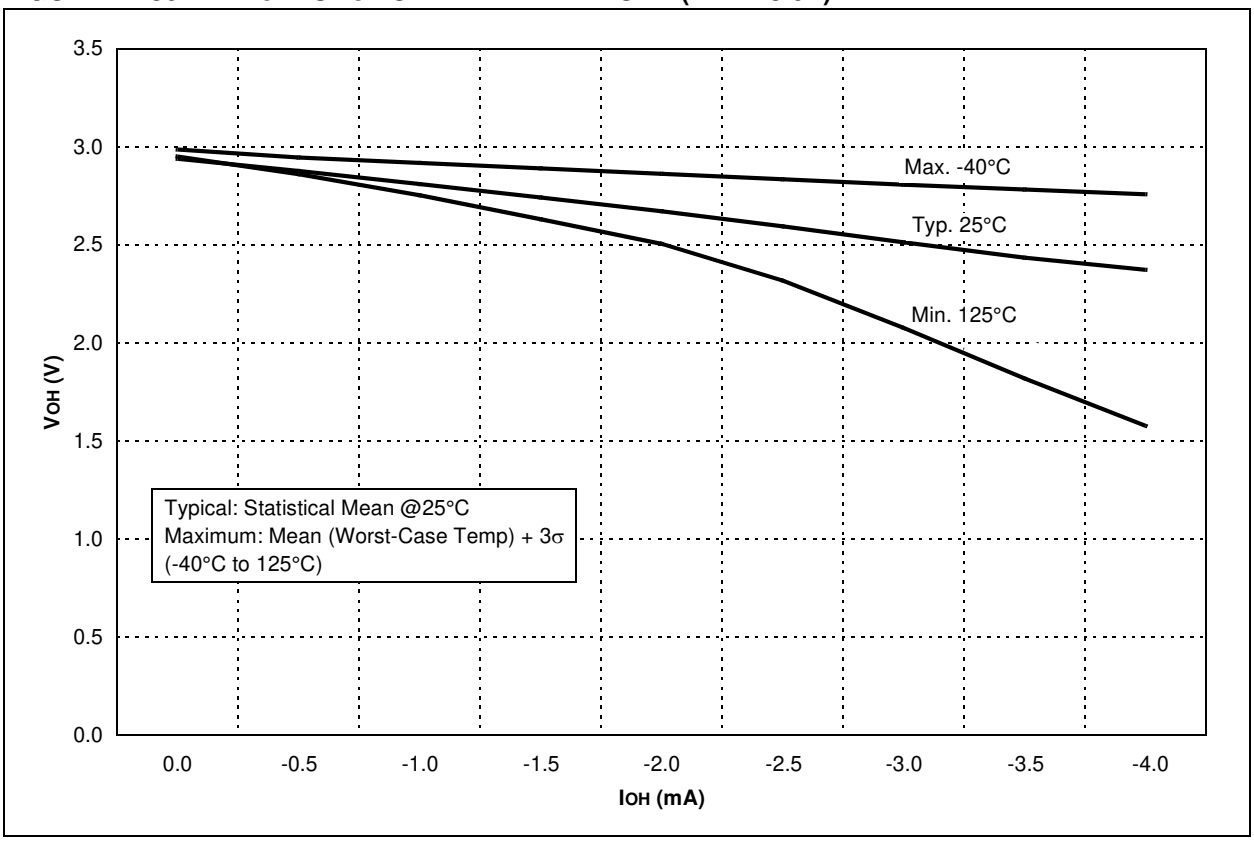

**FIGURE 17-37: VOH vs. IOH OVER TEMPERATURE (VDD = 5.0V)**

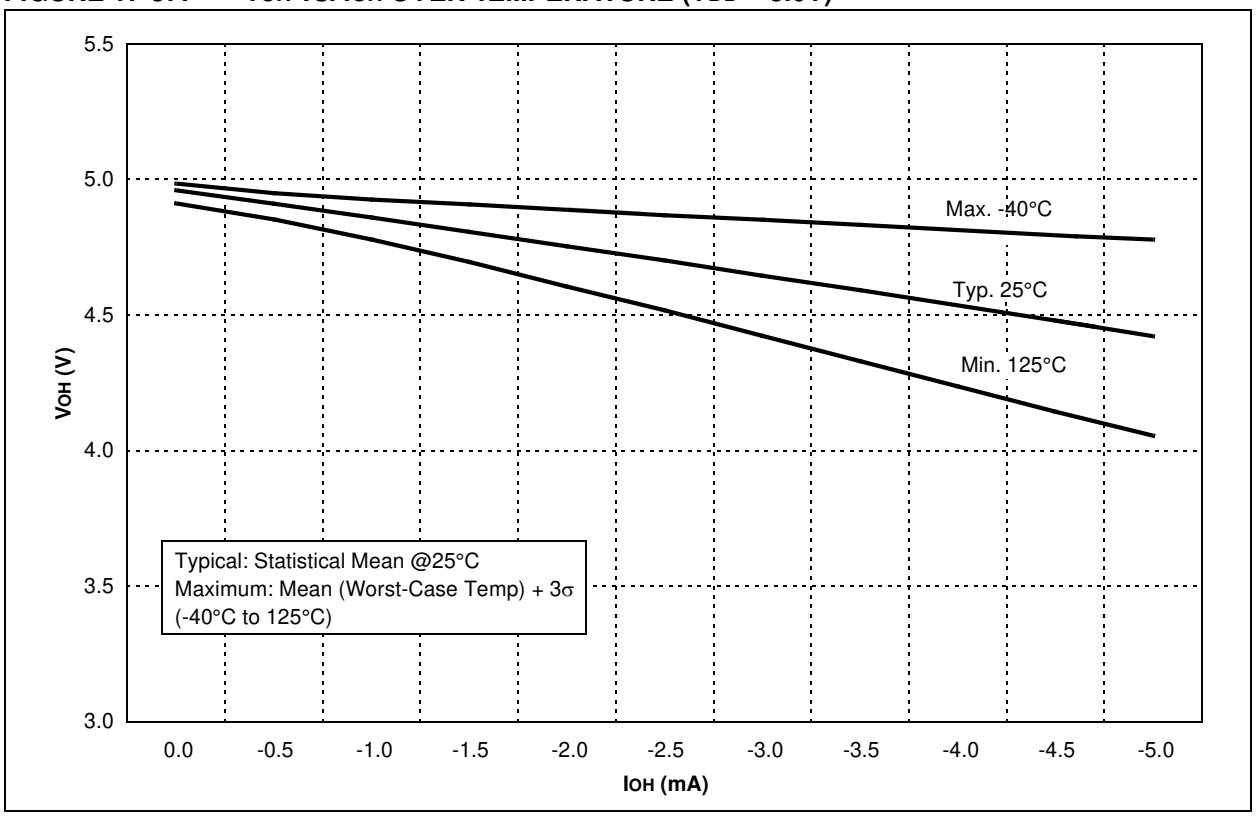


**FIGURE 17-38: TTL INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE**

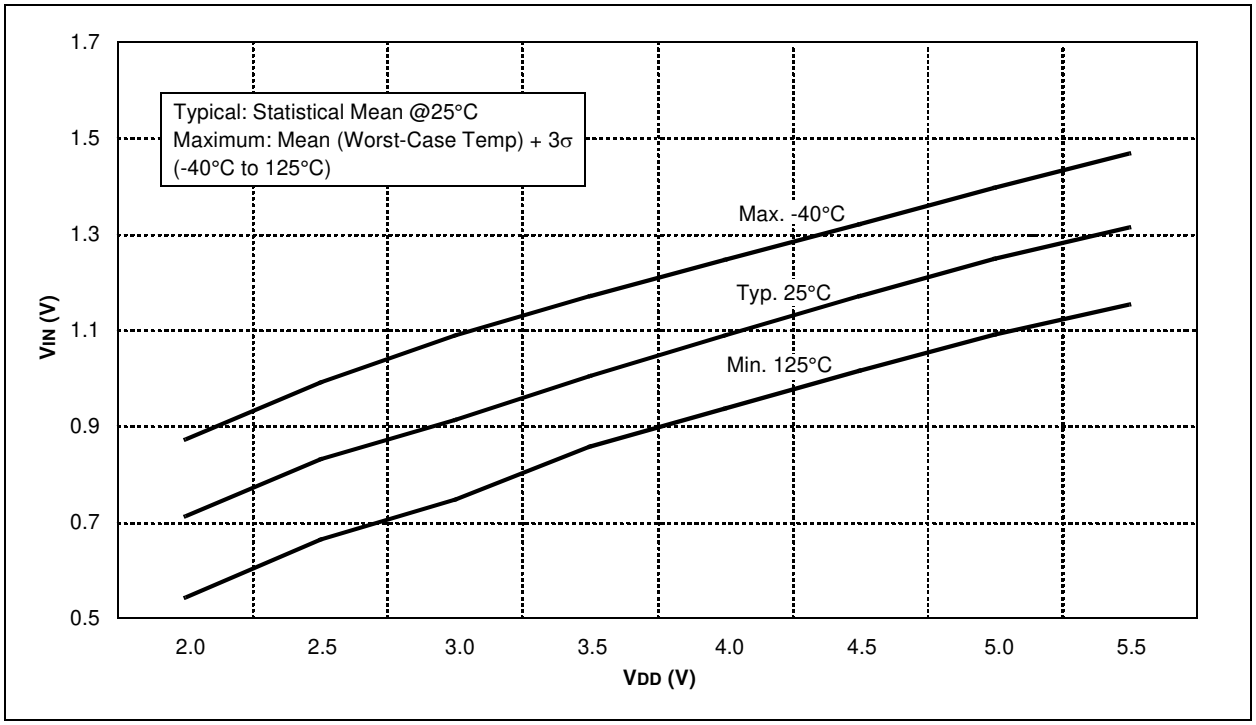



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**FIGURE 17-39: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE**

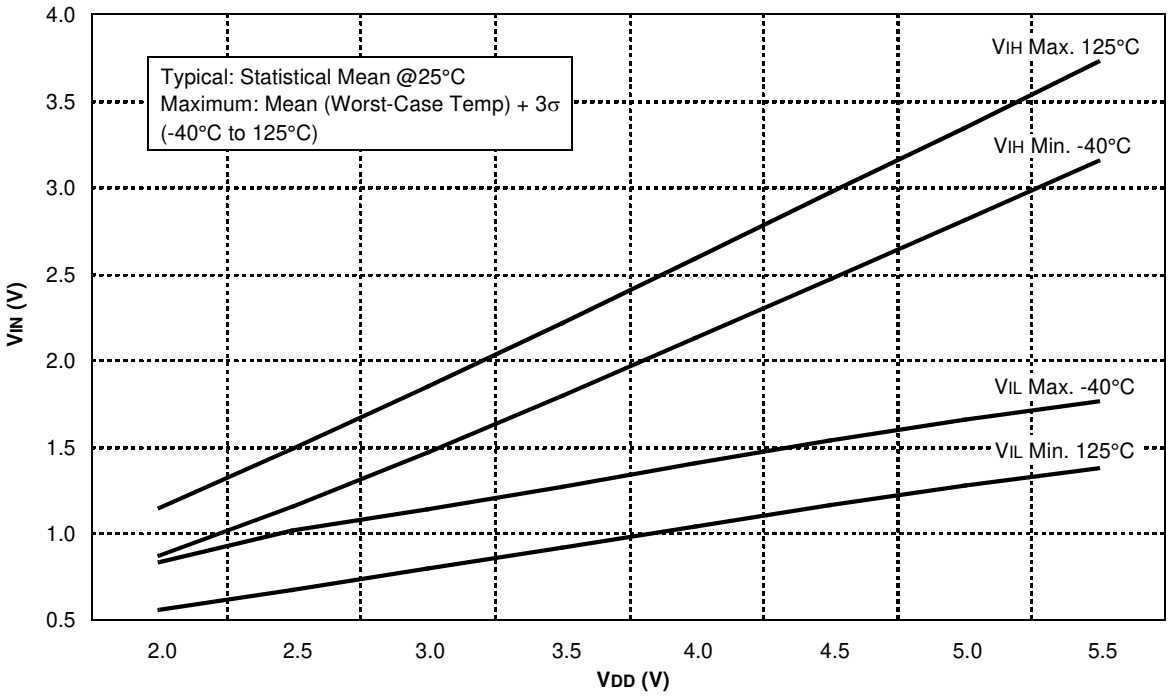


**FIGURE 17-40: TYPICAL HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE**

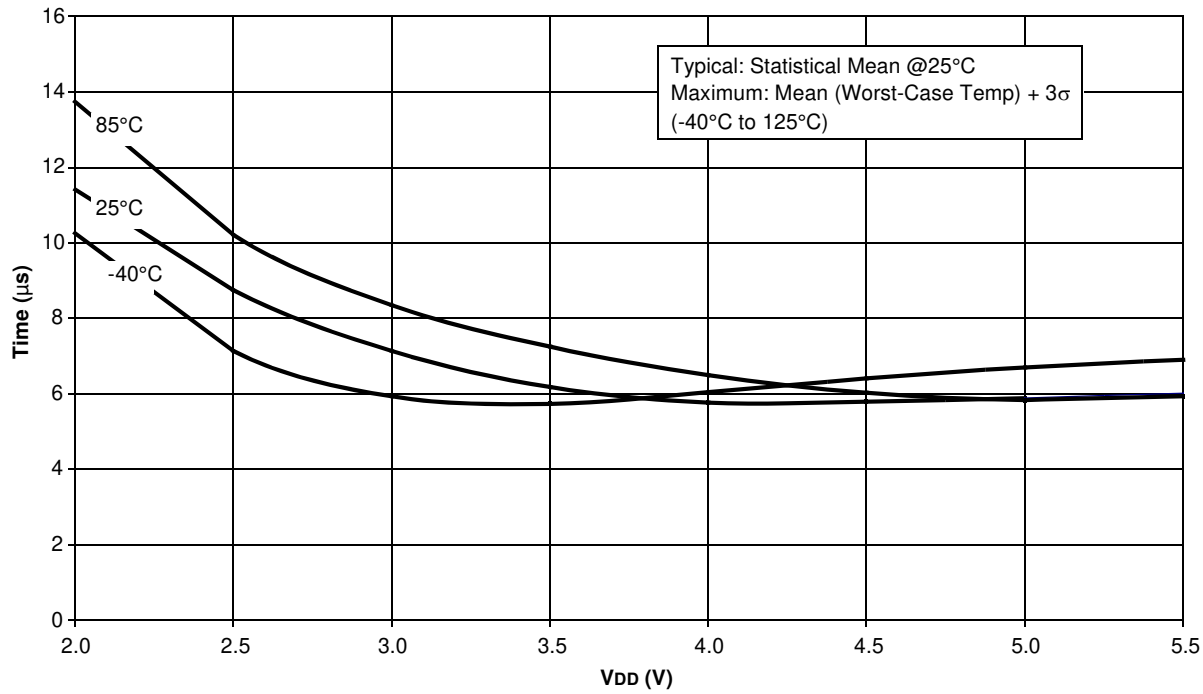

**FIGURE 17-41: MAXIMUM HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE**

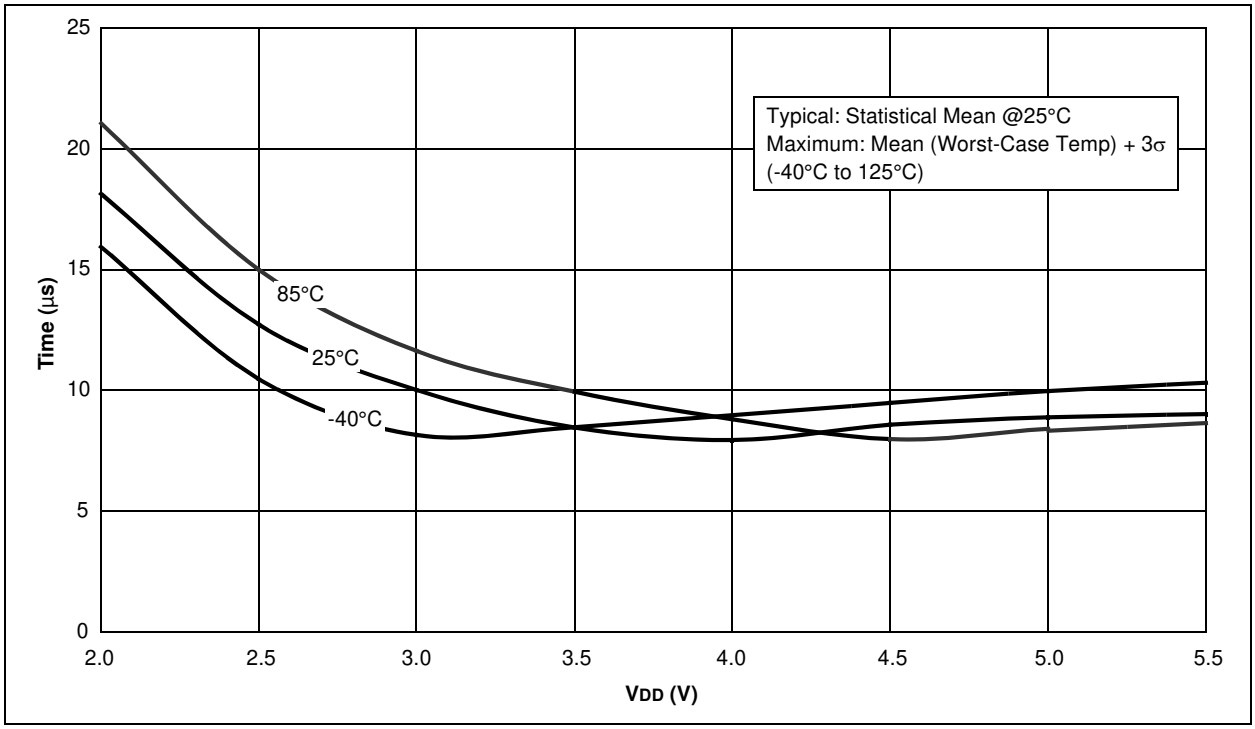


**FIGURE 17-42: MINIMUM HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE**

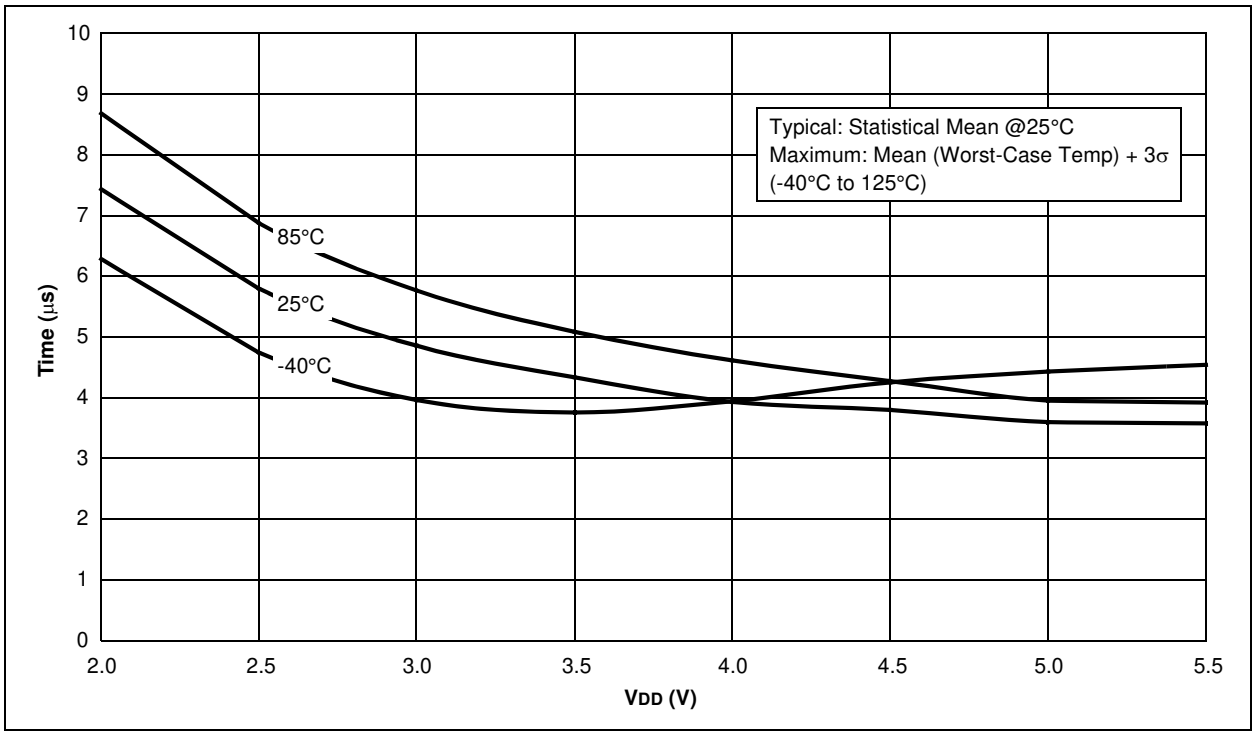



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**FIGURE 17-43: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (25°C)**

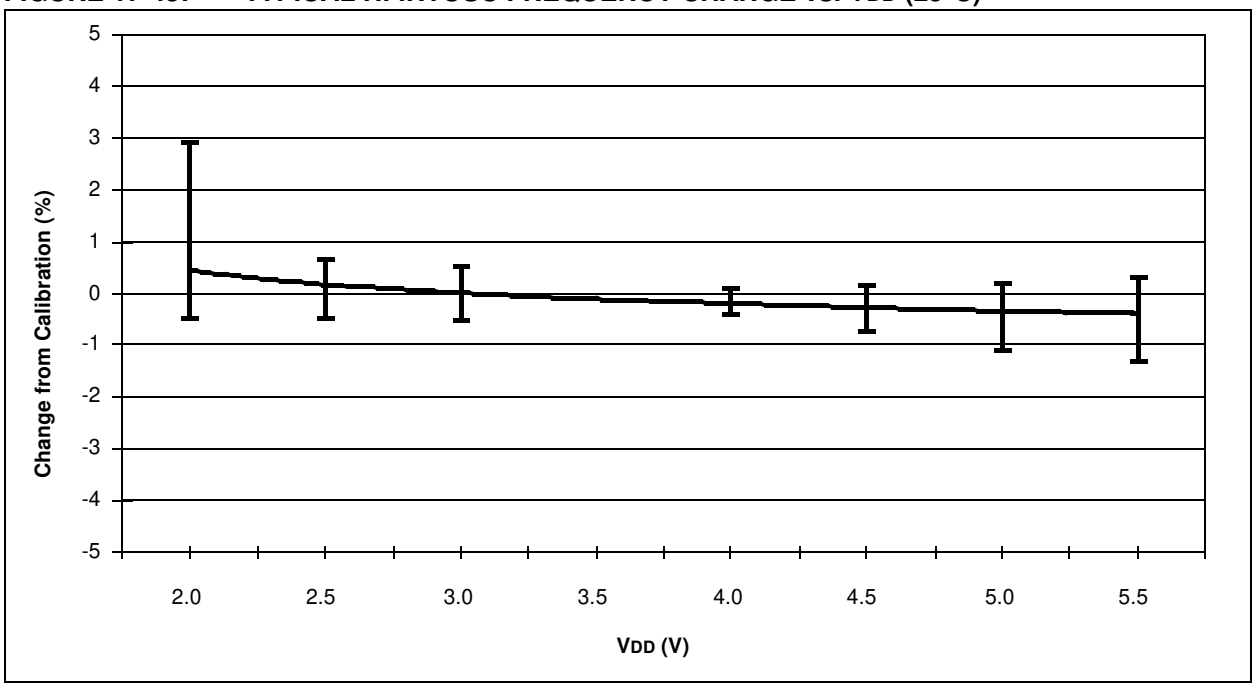


**FIGURE 17-44: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (85°C)**

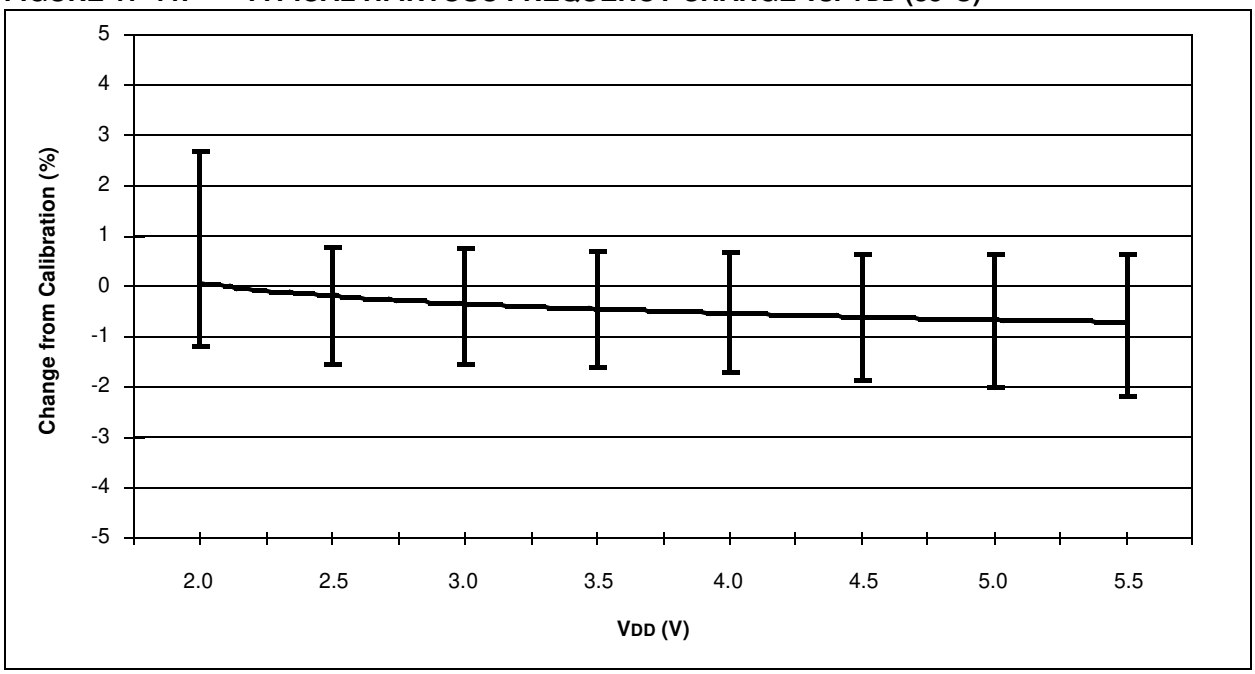

**FIGURE 17-45: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (125°C)**

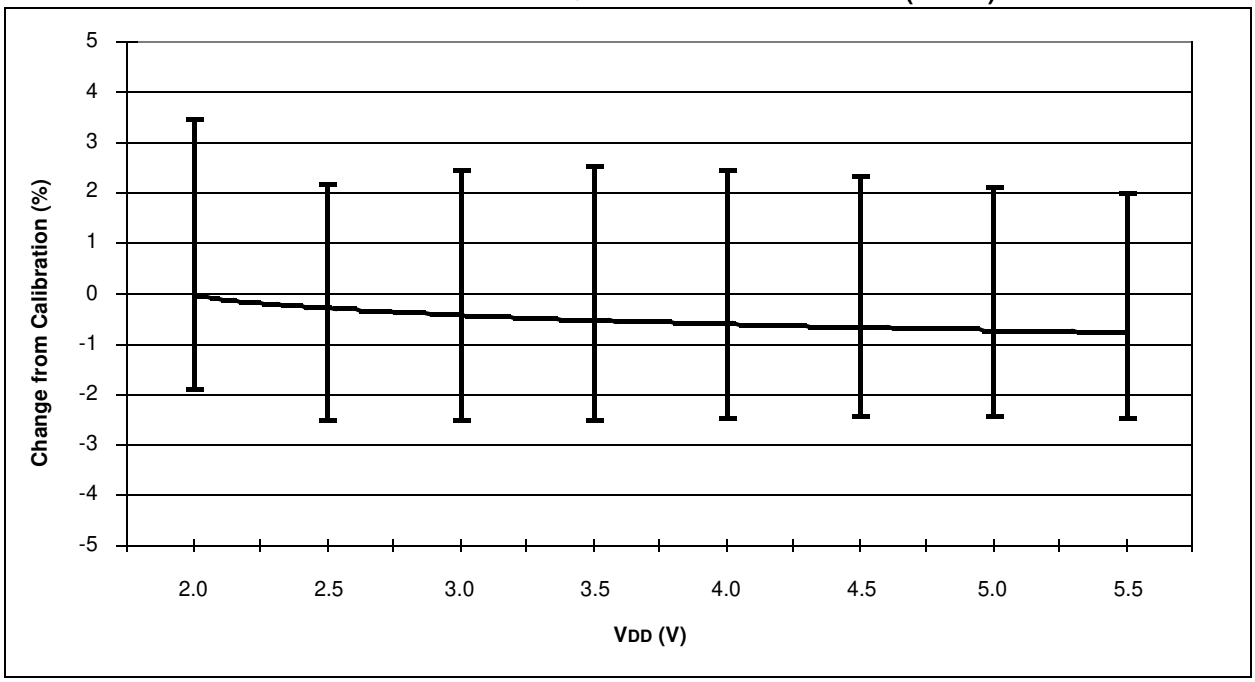


**FIGURE 17-46: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (-40°C)**

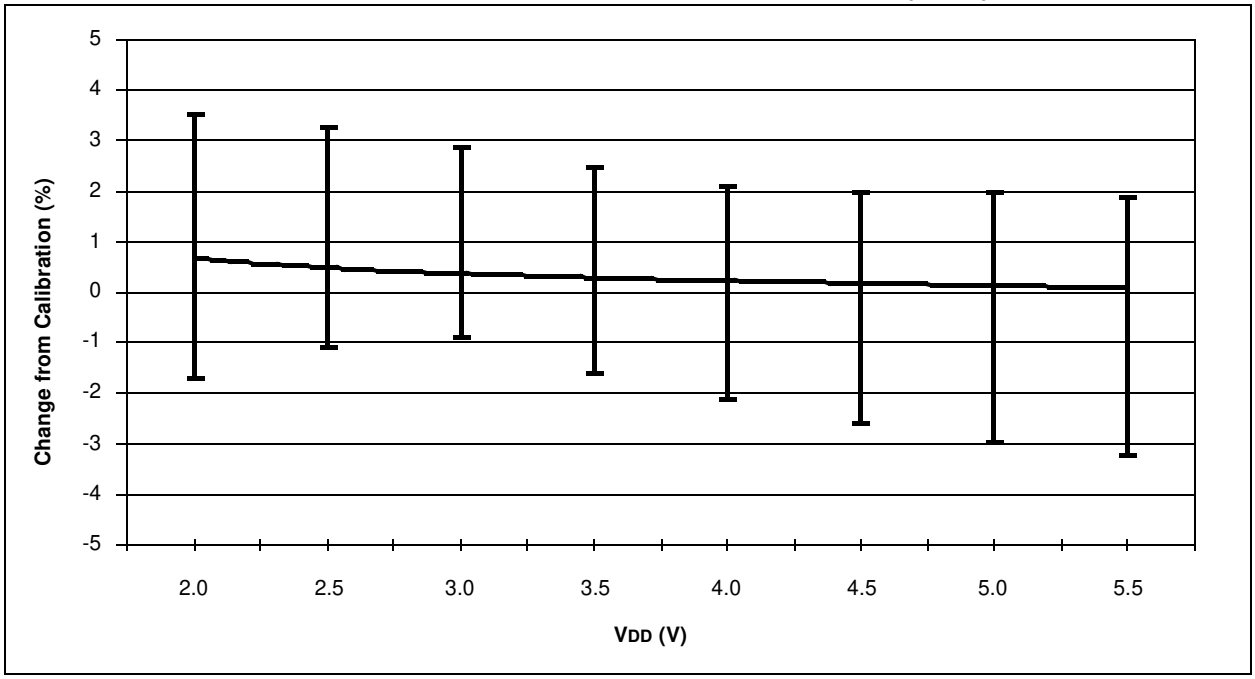



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**FIGURE 17-47: 0.6V REFERENCE VOLTAGE vs. TEMP (TYPICAL)**

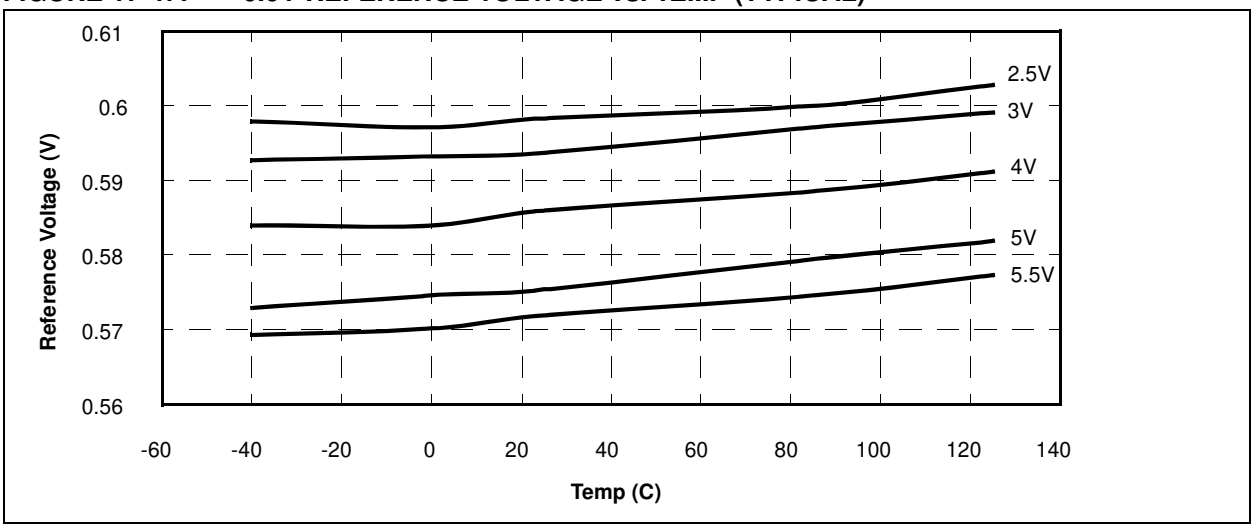


**FIGURE 17-48: 1.2V REFERENCE VOLTAGE vs. TEMP (TYPICAL)**

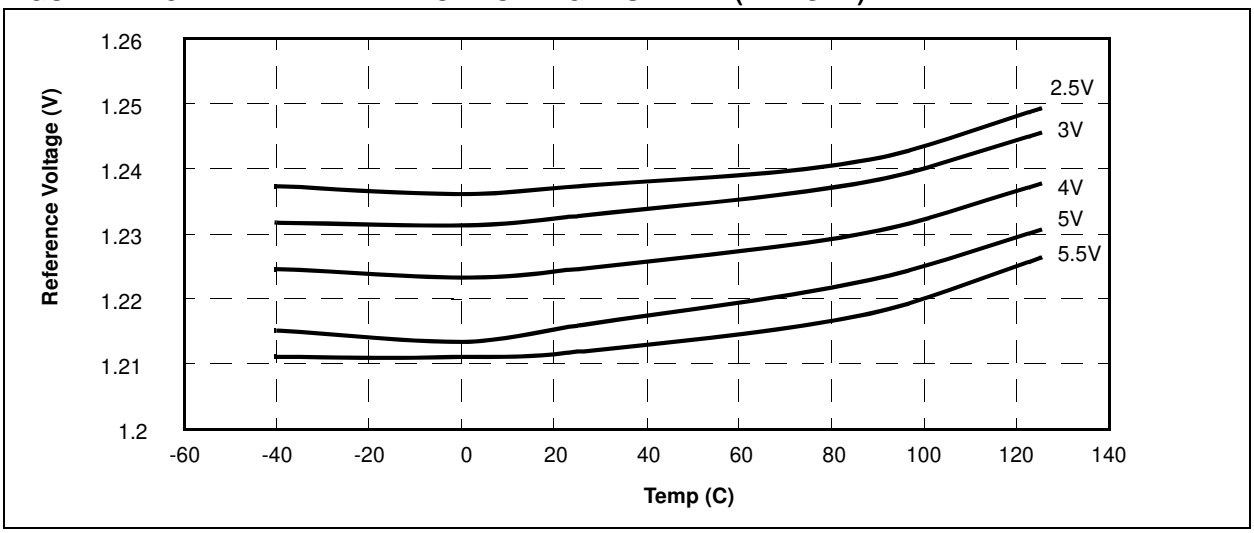


**FIGURE 17-49: SHUNT REGULATOR VOLTAGE vs. INPUT CURRENT (TYPICAL)**

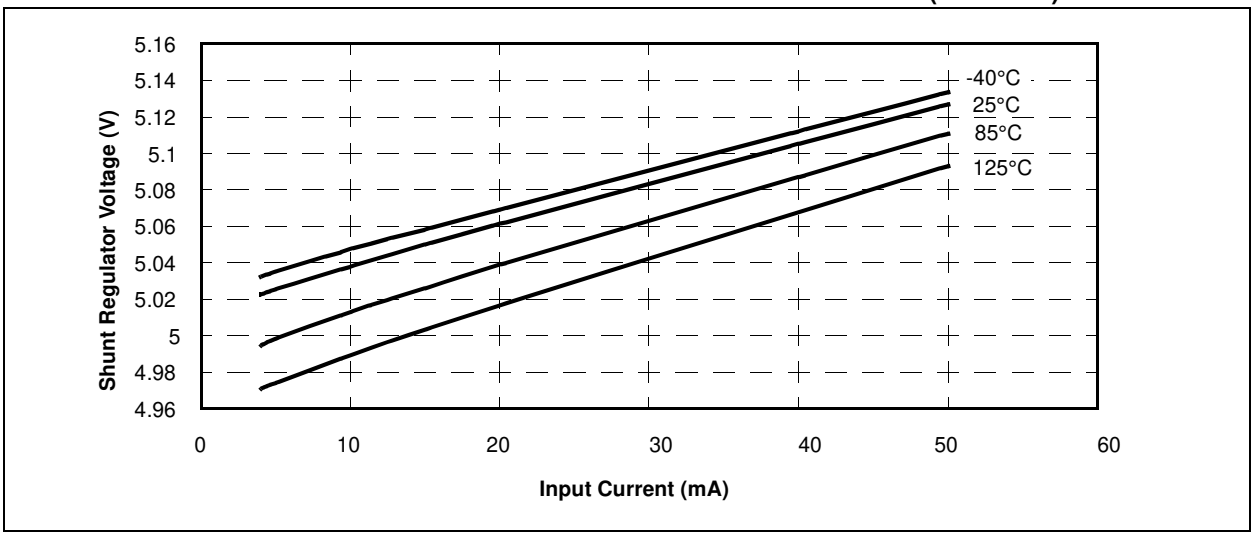

**FIGURE 17-50: SHUNT REGULATOR VOLTAGE vs. TEMP (TYPICAL)**

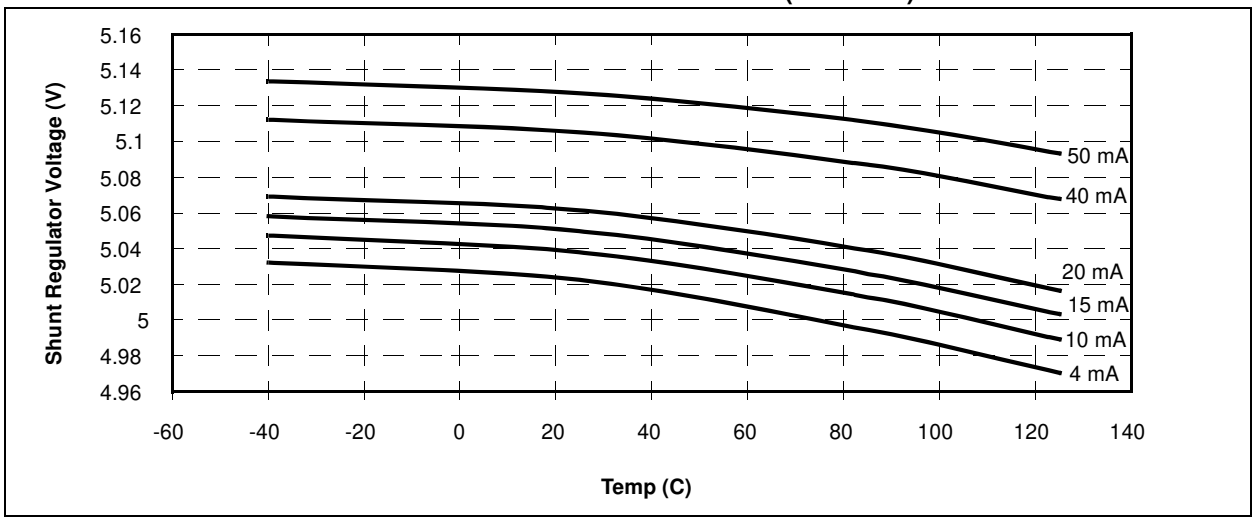


**FIGURE 17-51: COMPARATOR RESPONSE TIME (RISING EDGE)**

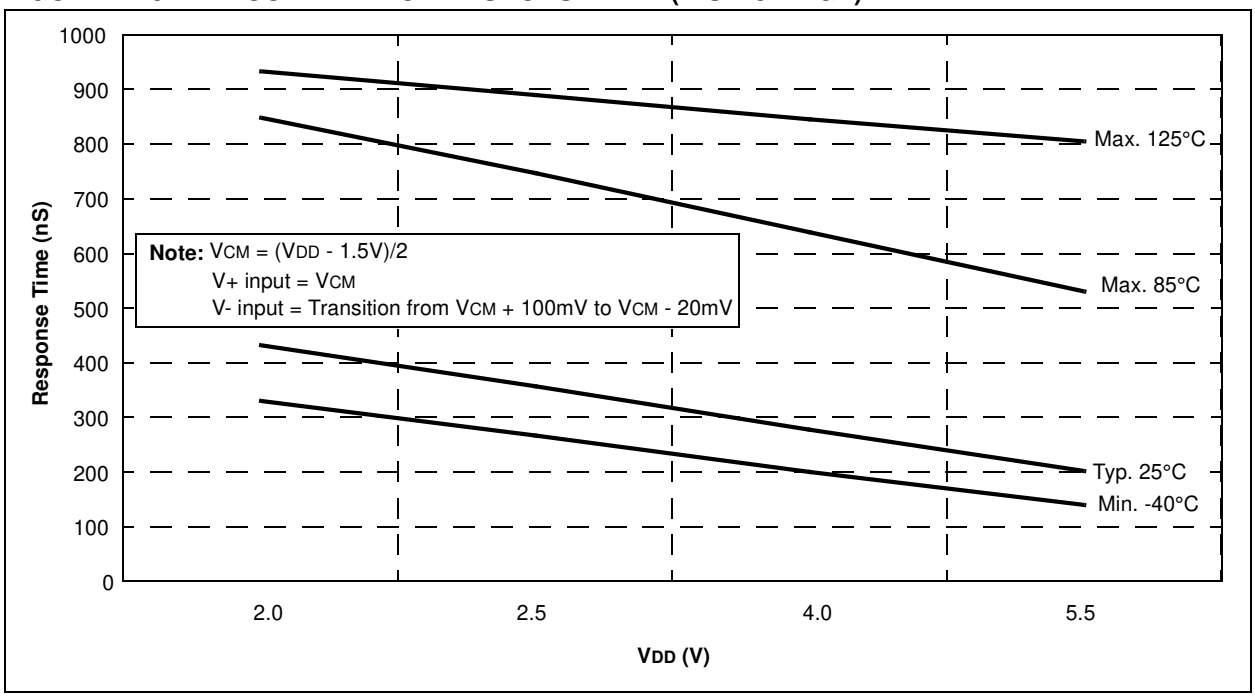



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**FIGURE 17-52: COMPARATOR RESPONSE TIME (FALLING EDGE)**

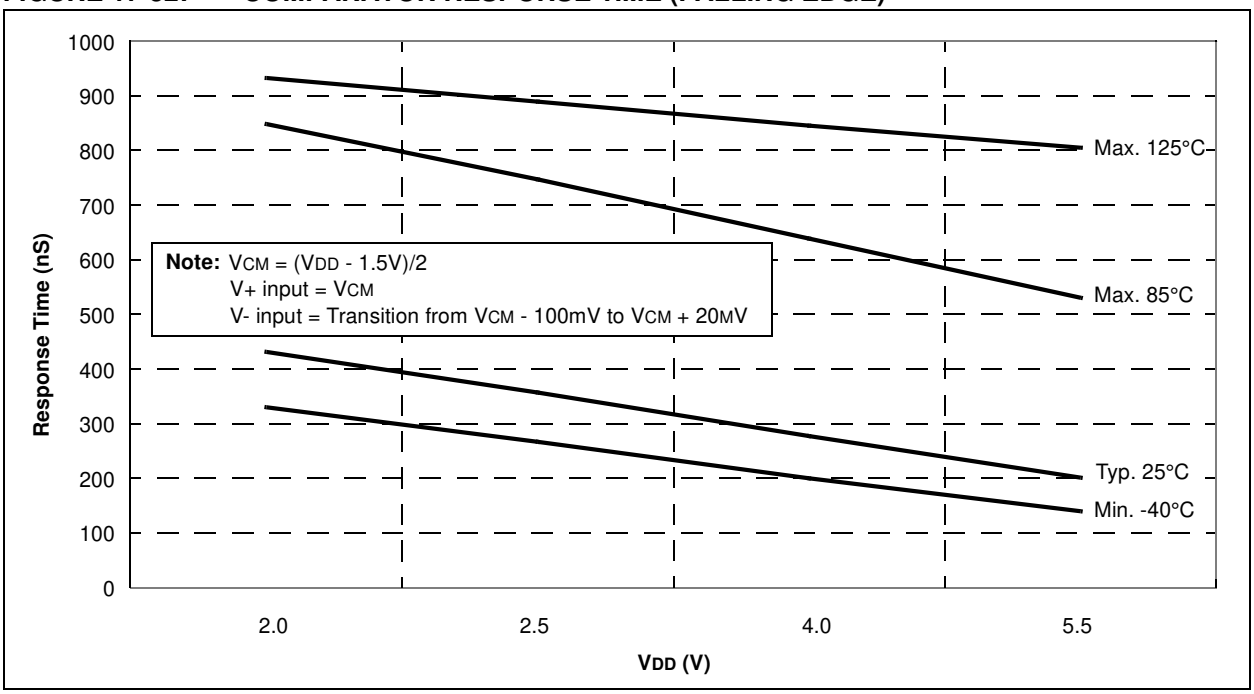
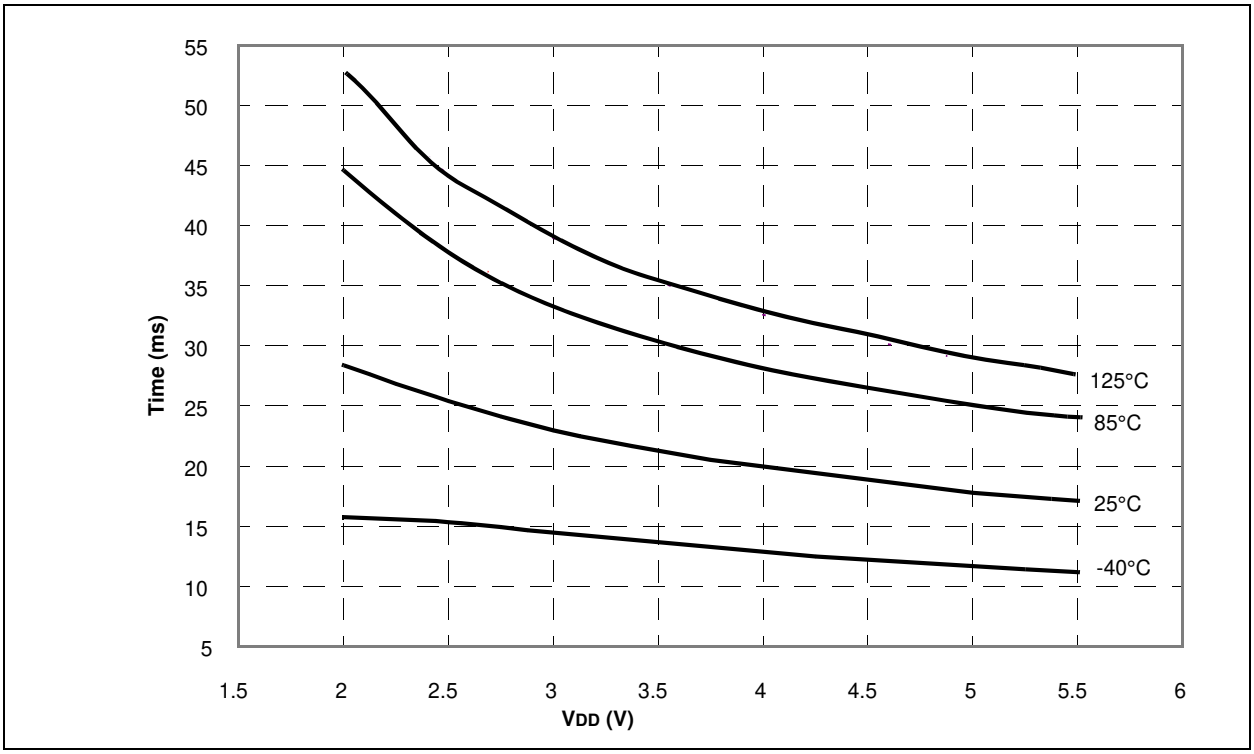



**FIGURE 17-53: WDT TIME-OUT PERIOD vs. VDD OVER TEMPERATURE**



**NOTES:**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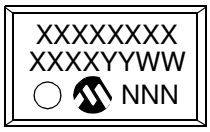
## 18.0 PACKAGING INFORMATION

### 18.1 Package Marking Information

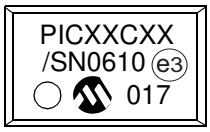
8-Lead PDIP (.300”)

Example

8-Lead SOIC (.150”)



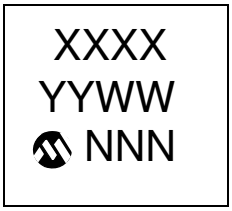

Example



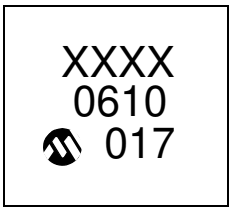

8-Lead MSOP

Example

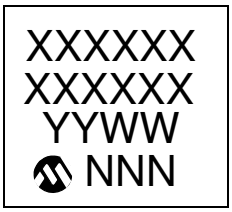
8-Lead DFN (3x3 mm)



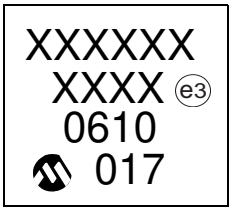

Example




8-Lead DFN (4x4 mm) (for PIC12F609/615/HV609/615 devices only)




Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | e3 | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ( e3 ) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

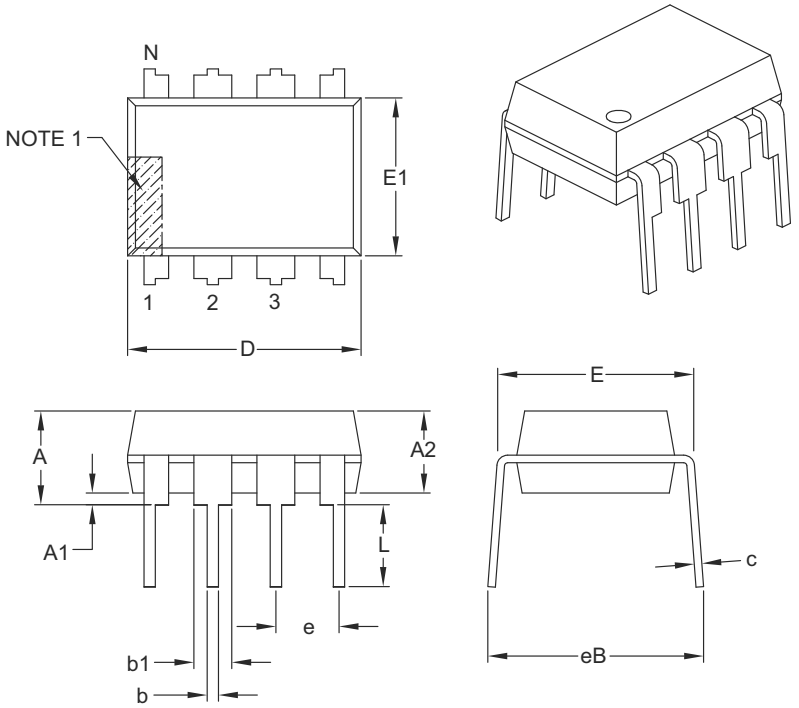
* Standard PIC device marking consists of Microchip part number, year code, week code, and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

## 18.2 Package Details

The following sections give the technical details of the packages.

### 8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | .100 BSC | | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B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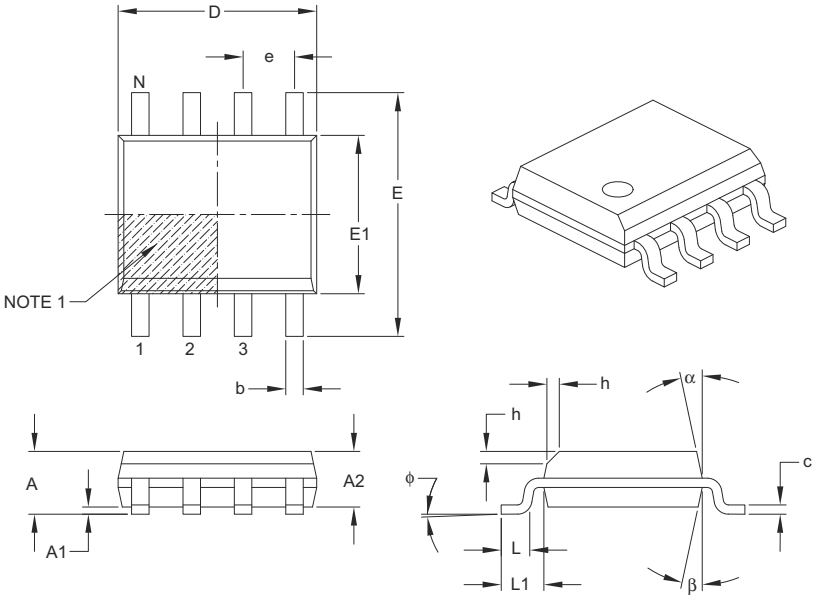
## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | – |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | 6.00 BSC | | |
| Molded Package Width | E1 | 3.90 BSC | | |
| Overall Length | D | 4.90 BSC | | |
| Chamfer (optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | 1.04 REF | | |
| Foot Angle | φ | 0° | – | 8° |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

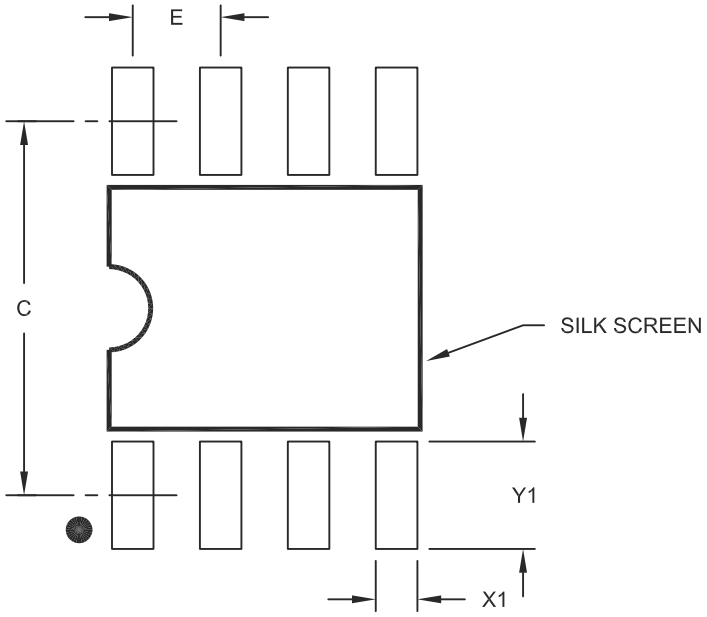
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

### 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A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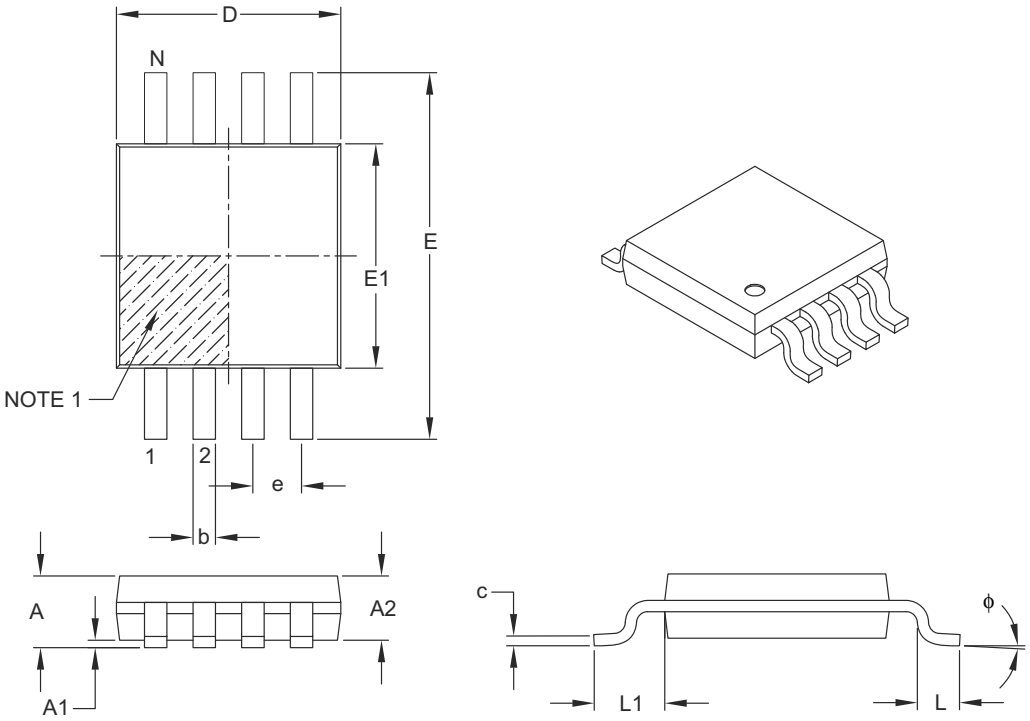
## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | – | – | 1.10 |
| Molded Package Thickness | A2 | 0.75 | 0.85 | 0.95 |
| Standoff | A1 | 0.00 | – | 0.15 |
| Overall Width | E | 4.90 BSC | | |
| Molded Package Width | E1 | 3.00 BSC | | |
| Overall Length | D | 3.00 BSC | | |
| Foot Length | L | 0.40 | 0.60 | 0.80 |
| Footprint | L1 | 0.95 REF | | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.08 | – | 0.23 |
| Lead Width | b | 0.22 | – | 0.40 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

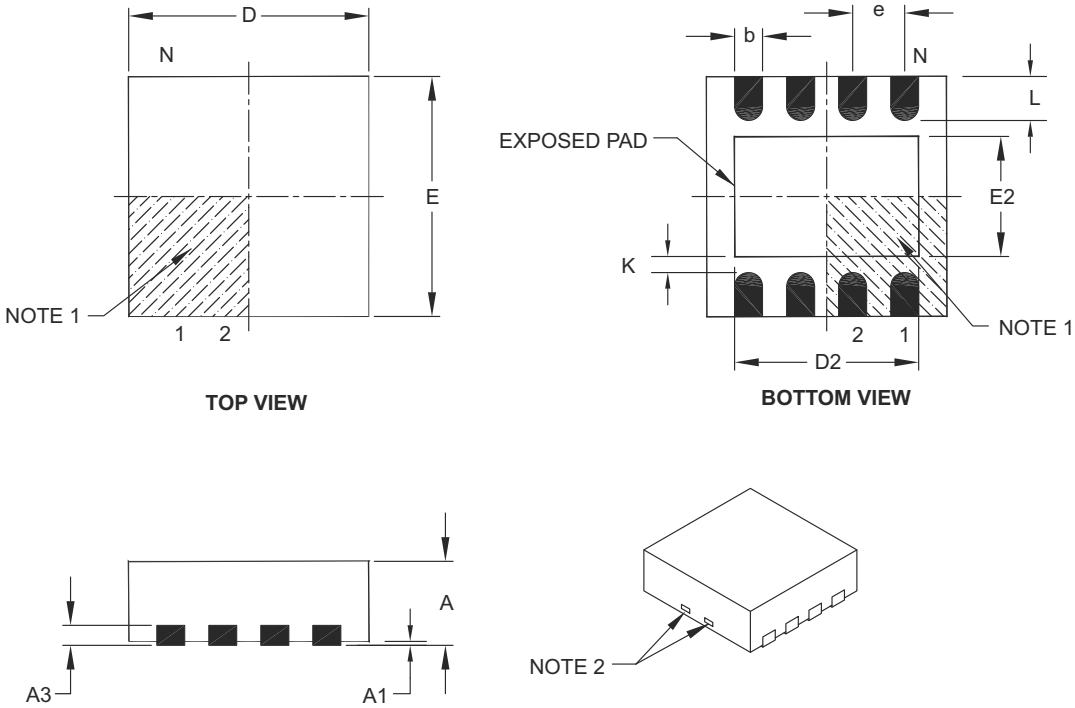
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

### 8-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | 0.20 REF | | |
| Overall Length | D | 3.00 BSC | | |
| Exposed Pad Width | E2 | 0.00 | – | 1.60 |
| Overall Width | E | 3.00 BSC | | |
| Exposed Pad Length | D2 | 0.00 | – | 2.40 |
| Contact Width | b | 0.25 | 0.30 | 0.35 |
| Contact Length | L | 0.20 | 0.30 | 0.55 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-062B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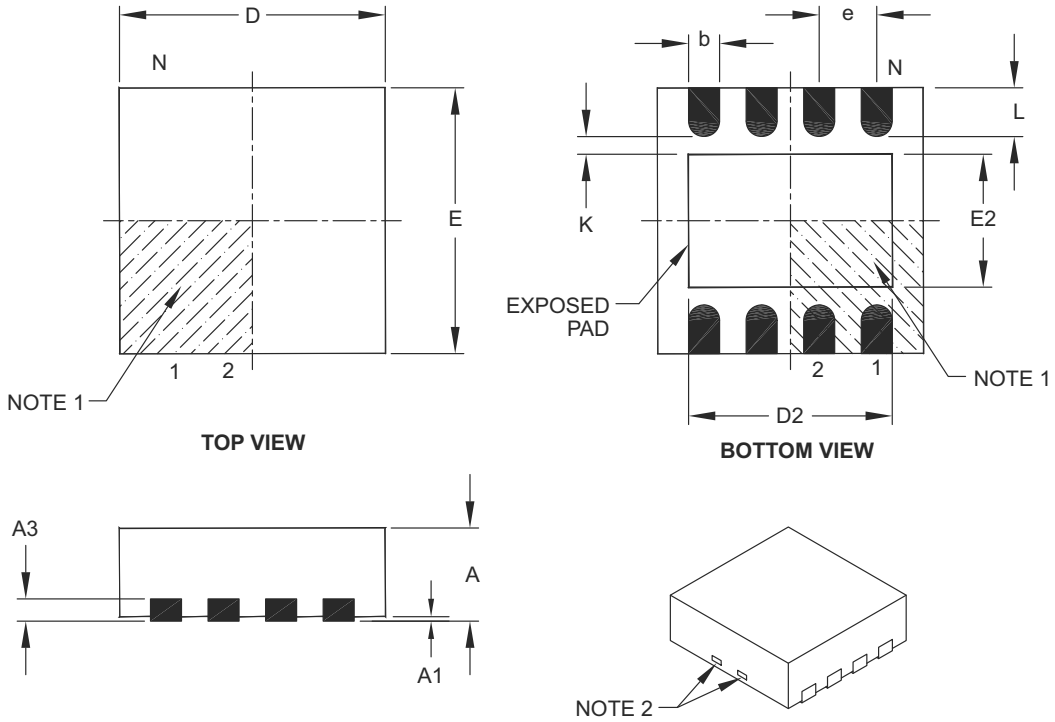
## 8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 0.80 BSC | | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | 0.20 REF | | |
| Overall Length | D | 4.00 BSC | | |
| Exposed Pad Width | E2 | 0.00 | 2.20 | 2.80 |
| Overall Width | E | 4.00 BSC | | |
| Exposed Pad Length | D2 | 0.00 | 3.00 | 3.60 |
| Contact Width | b | 0.25 | 0.30 | 0.35 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

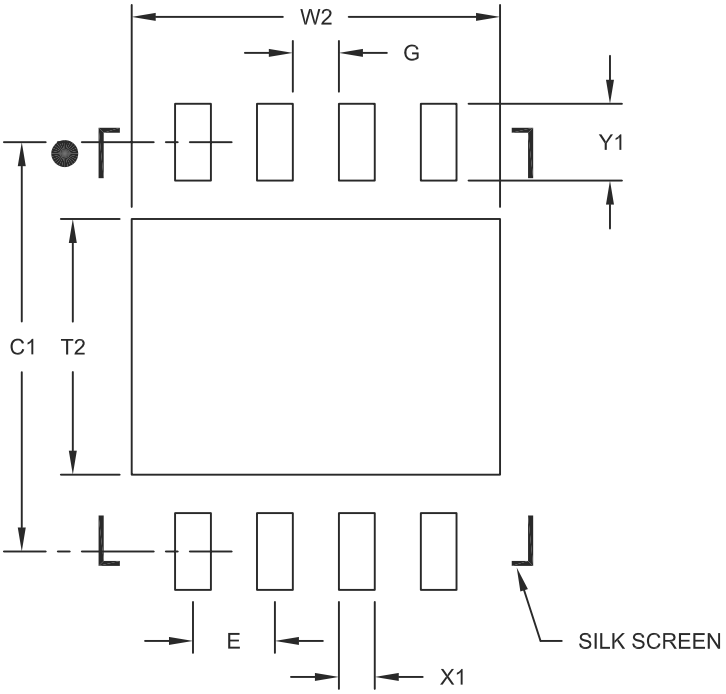
**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131D

### 8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.80 BSC | | |
| Optional Center Pad Width | W2 | | | 3.60 |
| Optional Center Pad Length | T2 | | | 2.50 |
| Contact Pad Spacing | C1 | | 4.00 | |
| Contact Pad Width (X8) | X1 | | | 0.35 |
| Contact Pad Length (X8) | Y1 | | | 0.75 |
| Distance Between Pads | G | 0.45 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2131B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# APPENDIX A: DATA SHEET REVISION HISTORY

## Revision A

This is a new data sheet.

## Revision B (05/2008)

Added Graphs. Revised 28-Pin ICD Pinout, Electrical Specifications Section, Package Details.

## Revision C (09/2009)

Updated adding the PIC12F617 device throughout the entire data sheet; Added Figure 2-2 to Memory Organization section; Added section 3 ”FLASH PROGRAM MEMORY SELF READ/SELF WRITE CONTROL (FOR PIC12F617 ONLY)”; Updated Register 12-1; Updated Table12-5 adding PMCON1, PMCON2, PMADRL, PMADRH, PMDATL, PMDATH; Added section 16-12 in the Electrical Specification section; Other minor edits.

## Revision D (01/2010)

Updated Figure 17-50; Revised 16.8 DC Characteristics; Removed Preliminary Status.

# APPENDIX B: MIGRATING FROM OTHER PIC® DEVICES

This discusses some of the issues in migrating from other PIC devices to the PIC12F6XX Family of devices.

## B.1 PIC12F675 to PIC12F609/615/ 12HV609/615

**TABLE B-1: FEATURE COMPARISON**

| Feature | PIC12F675 | PIC12F609/ 615/ 12HV609/615 |
|---|---|---|
| Max Operating Speed | 20 MHz | 20 MHz |
| Max Program Memory (Words) | 1024 | 1024 |
| SRAM (bytes) | 64 | 64 |
| A/D Resolution | 10-bit | 10-bit (615 only) |
| Timers (8/16-bit) | 1/1 | 2/1 (615)<br>1/1 (609) |
| Oscillator Modes | 8 | 8 |
| Brown-out Reset | Y | Y |
| Internal Pull-ups | RA0/1/2/4/5 | GP0/1/2/4/5, $\overline{\text{MCLR}}$ |
| Interrupt-on-change | RA0/1/2/3/4/5 | GP0/1/2/3/4/5 |
| Comparator | 1 | 1 |
| ECCP | N | Y (615) |
| INTOSC Frequencies | 4 MHz | 4/8 MHz |
| Internal Shunt Regulator | N | Y (PIC12HV609/ 615) |

**Note:** This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

**NOTES:**


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Device: PIC12F609/615/617/12HV609/615 Literature Number: DS41302D

Questions:

1. What are the best features of this document?

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2. How does this document meet your hardware and software development needs?

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3. Do you find the organization of this document easy to follow? If not, why?

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4. What additions to the document do you think would enhance the structure and subject?

_____

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5. What deletions from the document could be made without affecting the overall usefulness?

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6. Is there any incorrect or misleading information (what and where)?

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7. How would you improve this document?

_____

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## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | /XX | XXX |
|---|---|---|---|
| Device | Temperature Range | Package | Pattern |

| | | | | |
|---|---|---|---|---|
| **Device:** | PIC12F609, PIC12F609T(1), PIC12HV609, PIC12HV609T(1), PIC12F615, PIC12F615T(1), PIC12HV615, PIC12HV615T(1), PIC12F617, PIC12F617T(1) | | | |
| **Temperature Range:** | H | = | -40°C to +150°C | (High Temp)(3) |
| | I | = | -40°C to +85°C | (Industrial) |
| | E | = | -40°C to +125°C | (Extended) |
| **Package:** | P | = | Plastic DIP (PDIP) | |
| | SN | = | 8-lead Small Outline (150 mil) (SOIC) | |
| | MS | = | Micro Small Outline (MSOP) | |
| | MF | = | 8-lead Plastic Dual Flat, No Lead (3x3) (DFN) | |
| | MD | = | 8-lead Plastic Dual Flat, No Lead (4x4)(DFN)(1,2) | |
| **Pattern:** | QTP, SQTP or ROM Code; Special Requirements (blank otherwise) | | | |

**Examples:**

a) PIC12F615-E/P 301 = Extended Temp., PDIP package, 20 MHz, QTP pattern #301
b) PIC12F615-I/SN = Industrial Temp., SOIC package, 20 MHz
c) PIC12F615T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
d) PIC12F609T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
e) PIC12HV615T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
f) PIC12HV609T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
g) PIC12F617T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
h) PIC12F617-I/P = Industrial Temp., PDIP package, 20 MHz
i) PIC12F615-H/SN = High Temp., SOIC package, 20 MHz

**Note 1:** T = in tape and reel for MSOP, SOIC and DFN packages only.
**2:** Not available for PIC12F617.
**3:** High Temp. available for PIC12F615 only.

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