EN: This Datasheet/Document is presented by the manufacturer.

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24AA01/24LC01B

1K I²C™ Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
24AA01	1.8-5.5	400 kHz(1)	I
24LC01B	2.5-5.5	400 kHz	I, E

Note 1: 100 kHz for VCC <2.5V

Features

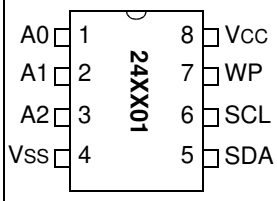
- Single-supply with operation down to 1.8V
- Low-power CMOS technology
  - 1 mA active current typical
  - 1 μA standby current typical (I-temp)
- Organized as 1 block of 128 bytes (1 x 128 x 8)
- 2-wire serial interface bus, I²C™ compatible
- Schmitt Trigger inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (24AA01) and 400 kHz (24LC01B) compatibility
- Self-timed write cycle (including auto-erase)
- Page write buffer for up to 8 bytes
- 2 ms typical write cycle time for page write
- Hardware write-protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 erase/write cycles
- Data retention > 200 years
- 8-lead PDIP, SOIC, TSSOP and MSOP packages
- 5-lead SOT-23 package
- Standard and Pb-free finishes
- Available for extended temperature ranges:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

Description

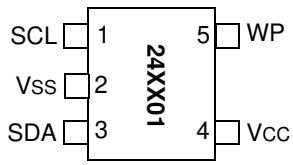
The Microchip Technology Inc. 24AA01/24LC01B (24XX01*) is a 1 Kbit Electrically Erasable PROM. The device is organized as one block of 128 x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 1.8V with standby and active currents of only 1 μA and 1 mA, respectively. The 24XX01 also has a page write capability for up to 8 bytes of data. The 24XX01 is available in the standard 8-pin PDIP, surface mount SOIC, TSSOP and MSOP packages and is also available in the 5-lead SOT-23 package.

Package Types

PDIP/SOIC/TSSOP/MSOP

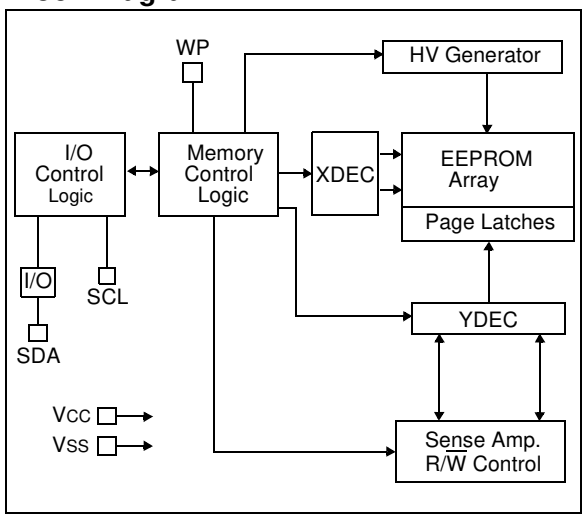


SOT-23-5



Note: Pins A0, A1 and A2 are not used by the 24XX01 (no internal connections).

Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

V_{CC}.....6.5V

All inputs and outputs w.r.t. V_{SS} ..... -0.3V to V_{CC} +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-65°C to +125°C

ESD protection on all pins .....≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			V_{CC} = +1.8V to +5.5V Industrial (I): T_A = -40°C to +85°C Automotive (E): T_A = -40°C to +125°C				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D1	V_{IH}	**WP, SCL and SDA pins**	—	—	—	—	—
D2	—	High-level input voltage	0.7 V_{CC}	—	—	V	—
D3	V_{IL}	Low-level input voltage	—	—	0.3 V_{CC}	V	—
D4	V_{HYS}	Hysteresis of Schmitt Trigger inputs	0.05 V_{CC}	—	—	V	**(Note)**
D5	V_{OL}	Low-level output voltage	—	—	0.40	V	I_{OL} = 3.0 mA, V_{CC} = 2.5V
D6	I_{LI}	**Input leakage current**	—	—	±1	µA	V_{IN} =.1V to V_{CC}
D7	I_{LO}	**Output leakage current**	—	—	±1	µA	V_{OUT} =.1V to V_{CC}
D8	C_{IN}, C_{OUT}	Pin capacitance (all inputs/outputs)	—	—	10	pF	V_{CC} = 5.0V **(Note)** T_A = 25°C, F_{CLK} = 1 MHz
D9	I_{CC} write	**Operating current**	—	0.1	3	mA	V_{CC} = 5.5V, SCL = 400 kHz
D10	I_{CC} read		—	0.05	1	mA	—
D11	I_{CCS}	**Standby current**	— —	0.01 —	1 5	µA µA	Industrial Automotive SDA = SCL = V_{CC} WP = V_{SS}

Note: This parameter is periodically sampled and not 100% tested.

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TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			V_{CC} = +1.8V to +5.5V Industrial (I): T_A = -40°C to +85°C Automotive (E): T_A = -40°C to +125°C				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
1	F_{CLK}	Clock frequency	— —	— —	400 100	kHz	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA01)**
2	T_{HIGH}	Clock high time	600 4000	— —	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} <2.5V **(24AA01)**
3	T_{LOW}	Clock low time	1300 4700	— —	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA01)**
4	T_R	SDA and SCL rise time **(Note 1)**	— —	— —	300 1000	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA01)**
5	T_F	SDA and SCL fall time	—	— —	300	ns	**(Note 1)**
6	$T_{HD:STA}$	Start condition hold time	600 4000	— —	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA01)**
7	$T_{SU:STA}$	Start condition setup time	600 4700	— —	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA01)**
8	$T_{HD:DAT}$	Data input hold time	0	— —	—	ns	**(Note 2)**
9	$T_{SU:DAT}$	Data input setup time	100 250	— —	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA01)**
10	$T_{SU:STO}$	Stop condition setup time	600 4000	— —	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA01)**
11	T_{AA}	Output valid from clock **(Note 2)**	— —	— —	900 3500	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA01)**
12	T_{BUF}	Bus free-time: Time the bus must be free before a new transmission can start	1300 4700	— —	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA01)**
13	T_{OF}	Output fall time from V_{IH} minimum to V_{IL} maximum	20+0.1C_B —	— —	250 250	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA01)**
14	T_{SP}	Input filter spike suppression (SDA and SCL pins)	—	—	50	ns	**(Notes 1 and 3)**
15	T_{WC}	Write cycle time (byte or page)	—	—	5	ms	—
16	—	Endurance	1M	—	—	cycles	25°C, **(Note 4)**

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined T_{SP} and V_{HYS} specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a T_I specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site: www.microchip.com.

FIGURE 1-1: BUS TIMING DATA

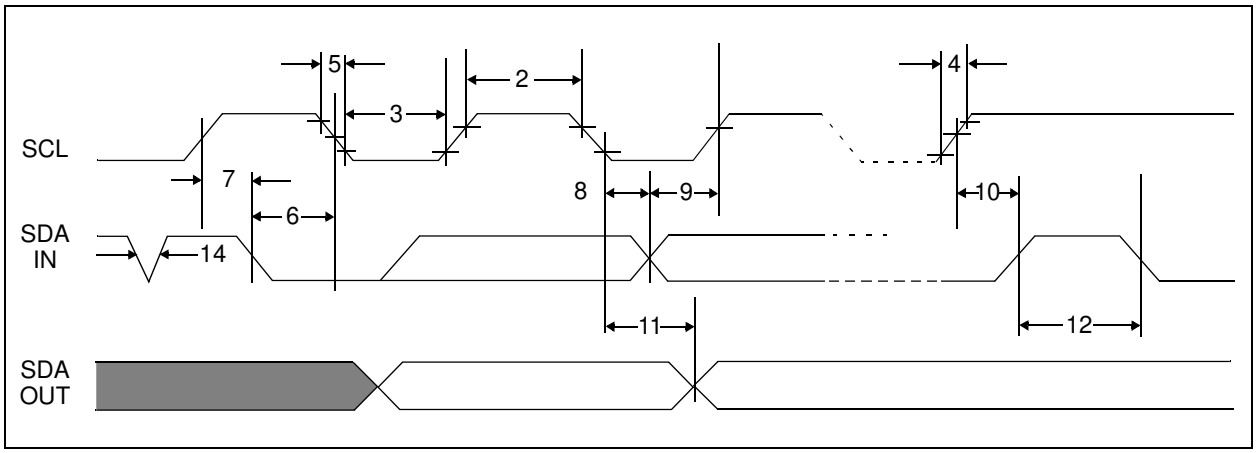
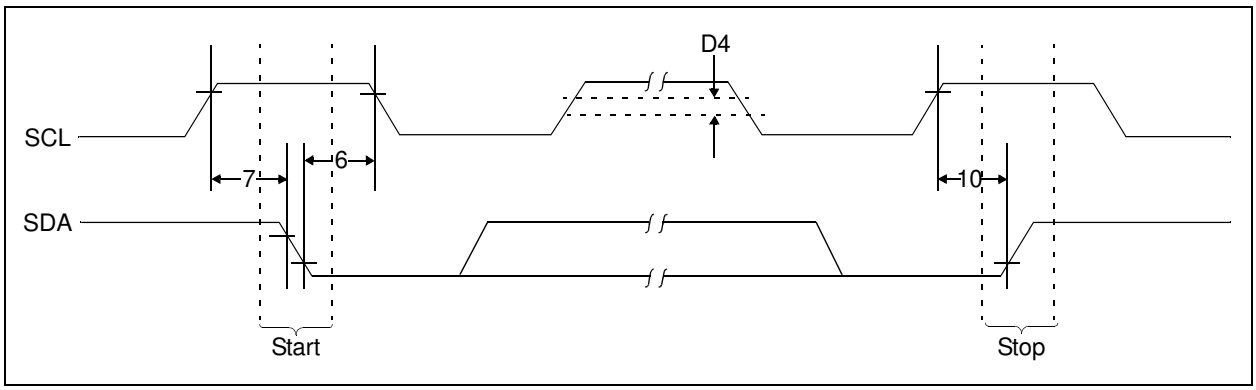


FIGURE 1-2: BUS TIMING START/STOP



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2.0 FUNCTIONAL DESCRIPTION

The 24XX01 supports a bidirectional, 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, while defining a device receiving data as a receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24XX01 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain high.

3.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

3.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between the Start and Stop conditions is determined by the master device and is, theoretically, unlimited (although only the last sixteen will be stored when doing a write operation). When an overwrite does occur, it will replace data in a first-in first-out (FIFO) fashion.

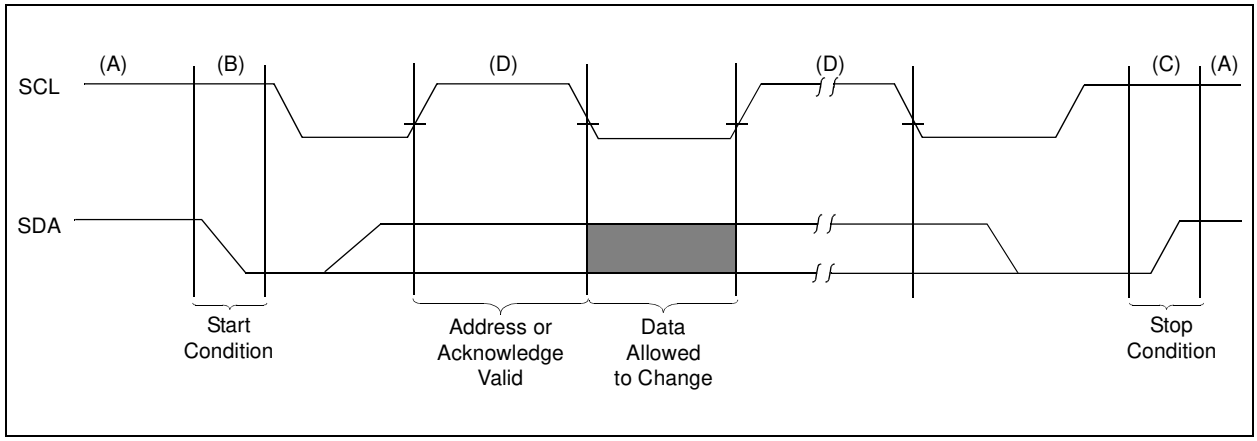
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The 24XX01 does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24XX01) will leave the data line high to enable the master to generate the Stop condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



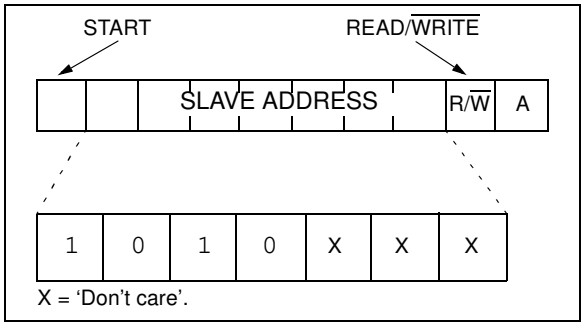
3.6 Device Addressing

A control byte is the first byte received following the Start condition from the master device. The control byte consists of a four-bit control code. For the 24XX01, this is set as '1010' binary for read and write operations. The next three bits of the control byte are 'don't care's' for the 24XX01.

The last bit of the control byte defines the operation to be performed. When set to '1', a read operation is selected. When set to '0', a write operation is selected. Following the Start condition, the 24XX01 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a '1010' code, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24XX01 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



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4.0 WRITE OPERATION

4.1 Byte Write

Following the Start condition from the master, the device code (4 bits), the block address (3 bits, don't cares) and the R/$\overline{W}$ bit, which is a logic low, is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24XX01. After receiving another Acknowledge signal from the 24XX01, the master device will transmit the data word to be written into the addressed memory location. The 24XX01 acknowledges again and the master generates a Stop condition. This initiates the internal write cycle, and, during this time, the 24XX01 will not generate Acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and first data byte are transmitted to the 24XX01 in the same way as in a byte write. However, instead of generating a Stop condition, the master transmits up to 8 data bytes to the 24XX01, which are temporarily stored in the on-chip page buffer and will be written into the memory once the master has transmitted a Stop condition. Upon receipt of each word, the four lower-order address pointer bits are internally incremented by '1'. The higher-order 7 bits of the word address remain constant. If the master should transmit more than 8 words prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 4-2).

Note:	Page write operations are limited to writing bytes within a single physical page **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size - 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 4-1: BYTE WRITE

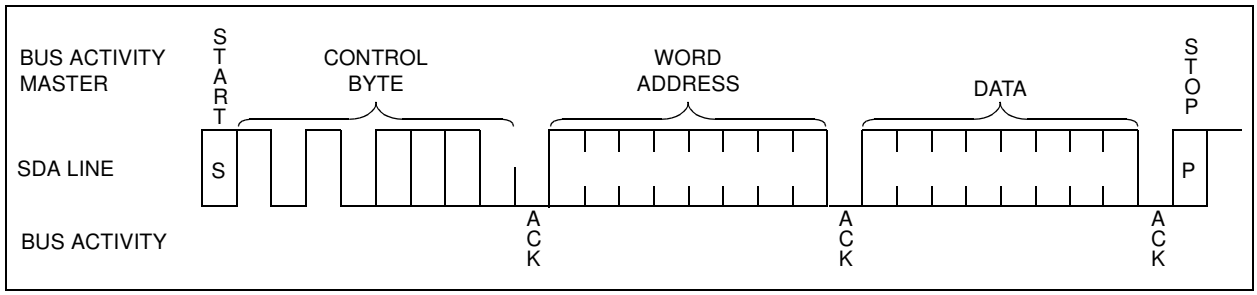
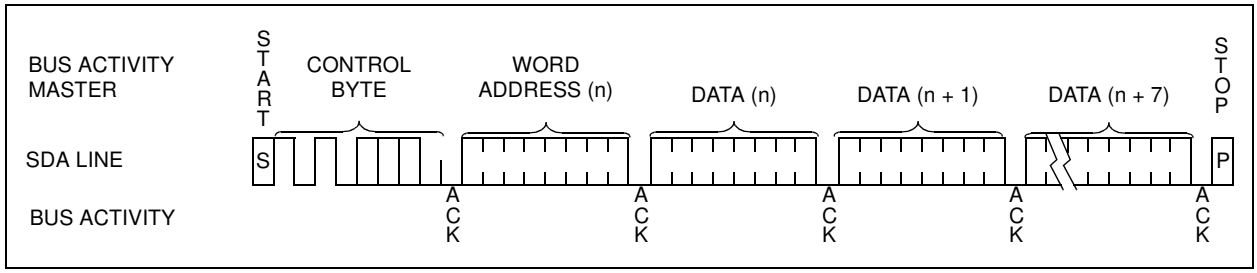


FIGURE 4-2: PAGE WRITE

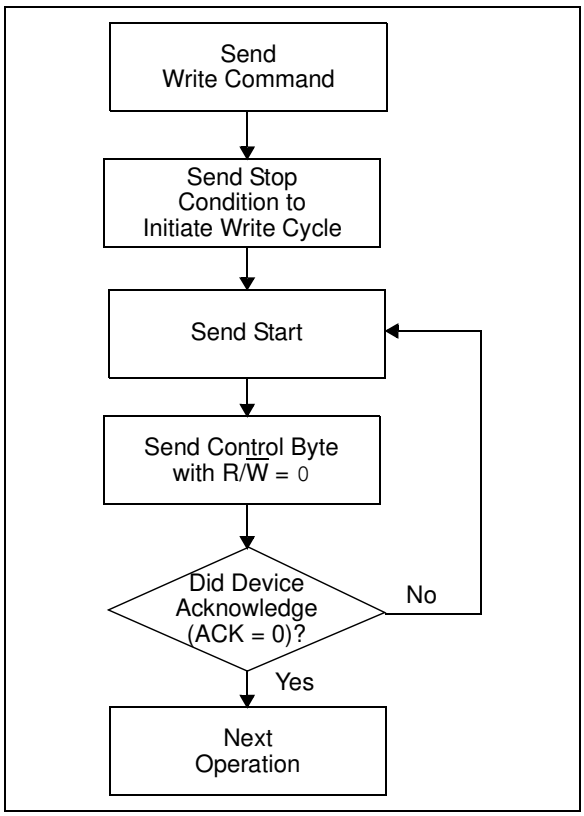


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5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally-timed write cycle. ACK polling can then be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, no ACK will be returned. If the cycle is complete, the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 5-1 for a flow diagram of this operation.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE-PROTECTION

The 24XX01 can be used as a serial ROM when the WP pin is connected to VCC. Programming will be inhibited and the entire memory will be write-protected.

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7.0 READ OPERATION

Read operations are initiated in the same way as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

7.1 Current Address Read

The 24XX01 contains an address counter that maintains the address of the last word accessed, internally incremented by '1'. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to '1', the 24XX01 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the 24XX01 discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is accomplished by sending the word address to the 24XX01 as part of a write operation. Once the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. The master then issues the control byte again, but with the R/$\overline{W}$ bit set to a '1'. The 24XX01 will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the 24XX01 discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read, except that once the 24XX01 transmits the first data byte, the master issues an acknowledge (as opposed to a Stop condition in a random read). This directs the 24XX01 to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24XX01 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24XX01 employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below 1.5V at nominal conditions.

The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

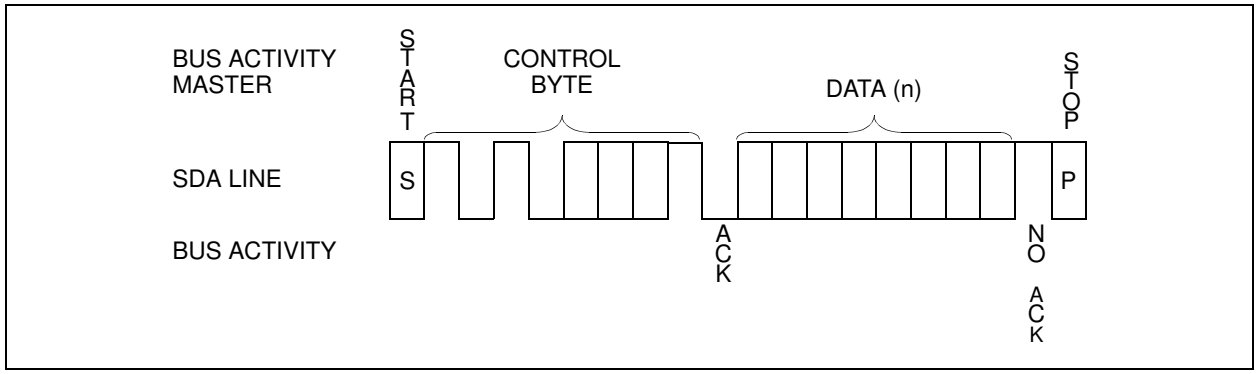


FIGURE 7-2: RANDOM READ

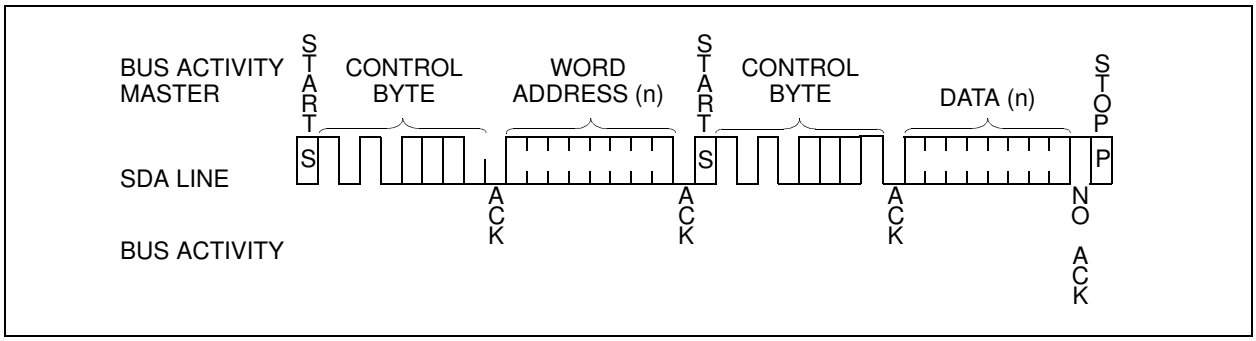
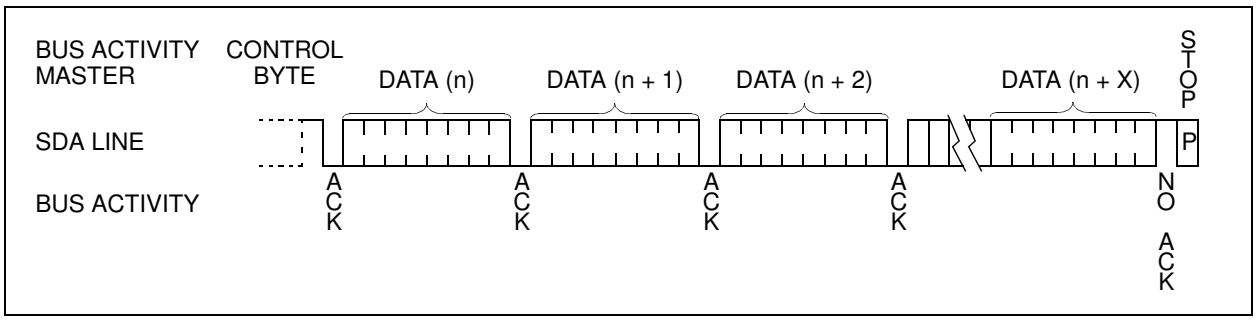


FIGURE 7-3: SEQUENTIAL READ



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8.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 8-1.

TABLE 8-1: PIN FUNCTION TABLE

Name	PDIP	SOIC	TSSOP	MSOP	SOT23	Description
A0	1	1	1	1	—	Not Connected
A1	2	2	2	2	—	Not Connected
A2	3	3	3	3	—	Not Connected
VSS	4	4	4	4	2	Ground
SDA	5	5	5	5	3	Serial Address/Data I/O
SCL	6	6	6	6	1	Serial Clock
WP	7	7	7	7	5	Write-Protect Input
VCC	8	8	8	8	4	+1.8V to 5.5V Power Supply

8.1 A0, A1, A2

The A0, A1 and A2 pins are not used by the 24XX01. They may be left floating or tied to either VSS or VCC.

8.2 Serial Address/Data Input/Output (SDA)

The SDA input is a bidirectional pin used to transfer addresses and data into and out of the device. Since it is an open-drain terminal, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating Start and Stop conditions.

8.3 Serial Clock (SCL)

The SCL input is used to synchronize the data transfer to and from the device.

8.4 Write-Protect (WP)

This pin must be connected to either VSS or VCC.

If tied to VSS normal memory operation is enabled (read/write the entire memory 00-7F).

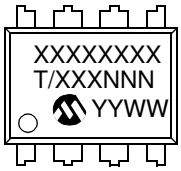
If tied to VCC, write operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24XX01 as a serial ROM when WP is enabled (tied to VCC).

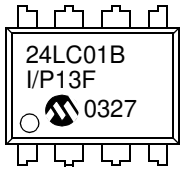
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

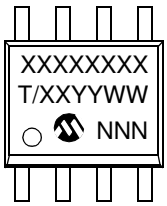
8-Lead PDIP (300 mil)



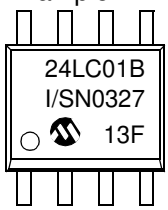
Example:



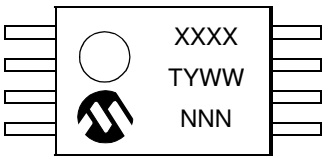
8-Lead SOIC (150 mil)



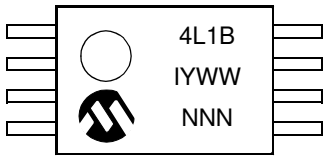
Example:



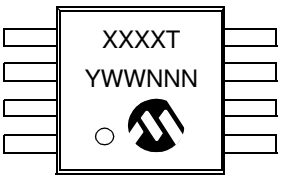
8-Lead TSSOP



Example:

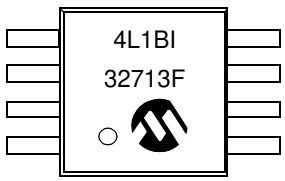


8-Lead MSOP

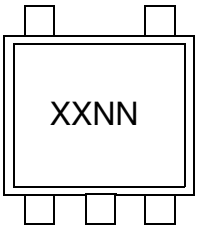


Part Number	TSSOP/MSOP Marking Code	
	STD	Pb-Free
24AA01	4A01	G4A1
24LC01B	4L01	G4L1

Example:



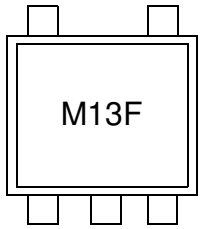
5-Lead SOT-23



Part Number	SOT-23 Marking Code	
	STD	Pb-Free
24AA01	B1	B1
24LC01B-I	M1	M1
24LC01B-E	N1	N1

Note: Pb-free part number using "G" suffix is marked on carton.

Example:



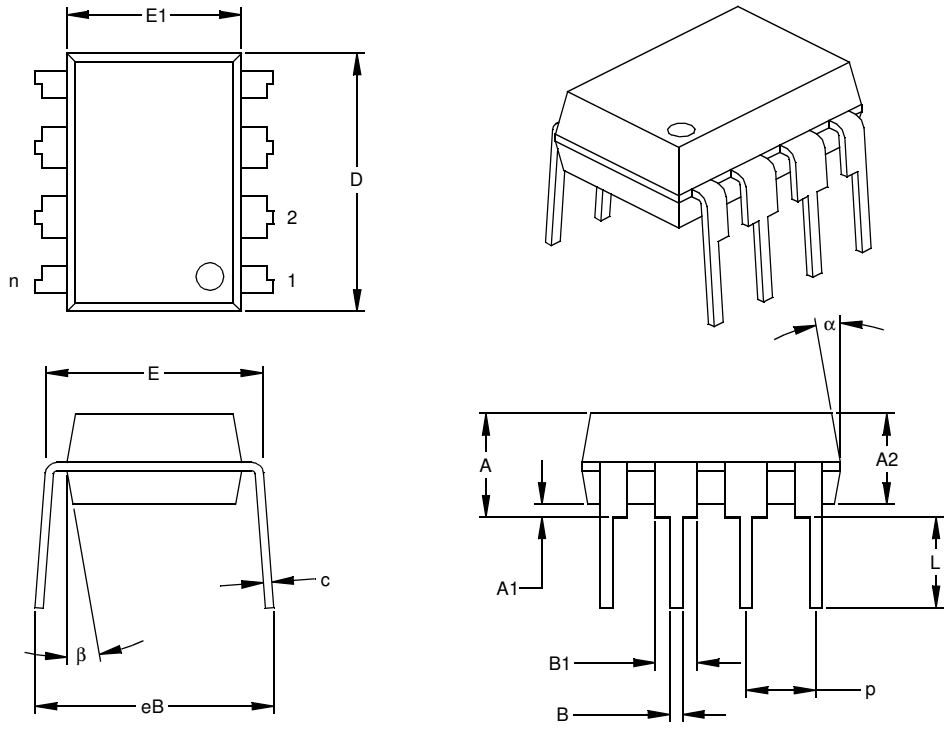
Legend:	XX...X	Customer specific information*
	T	Temperature grade (I,E)
	YY	Year code (last 2 digits of calendar year)
	Y	Year code (last digit of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard QTP marking consists of Microchip part number, year code, week code, and traceability code.

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8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

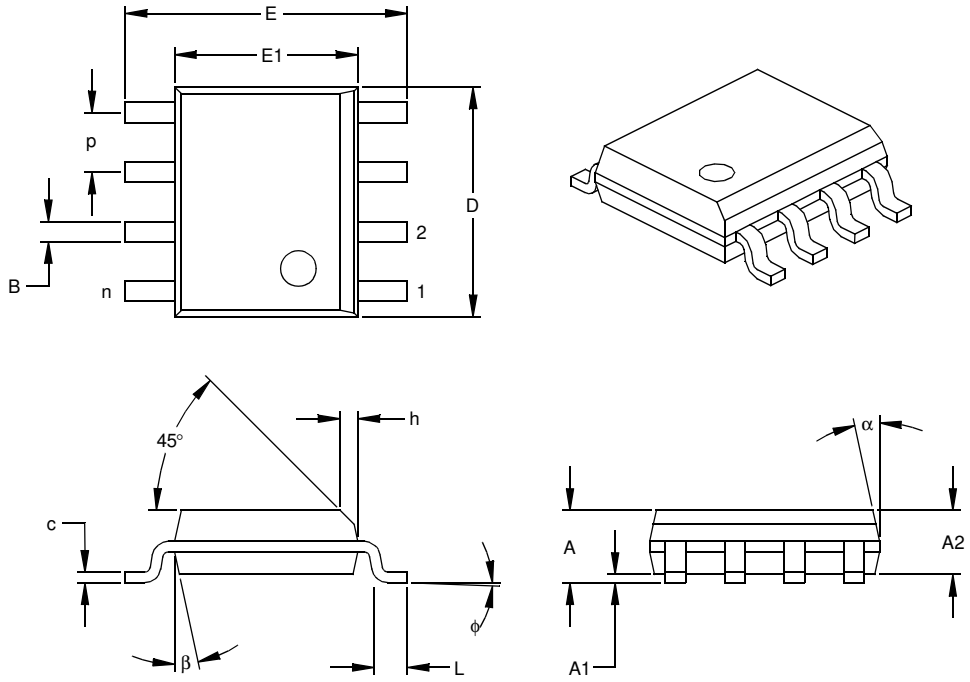


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



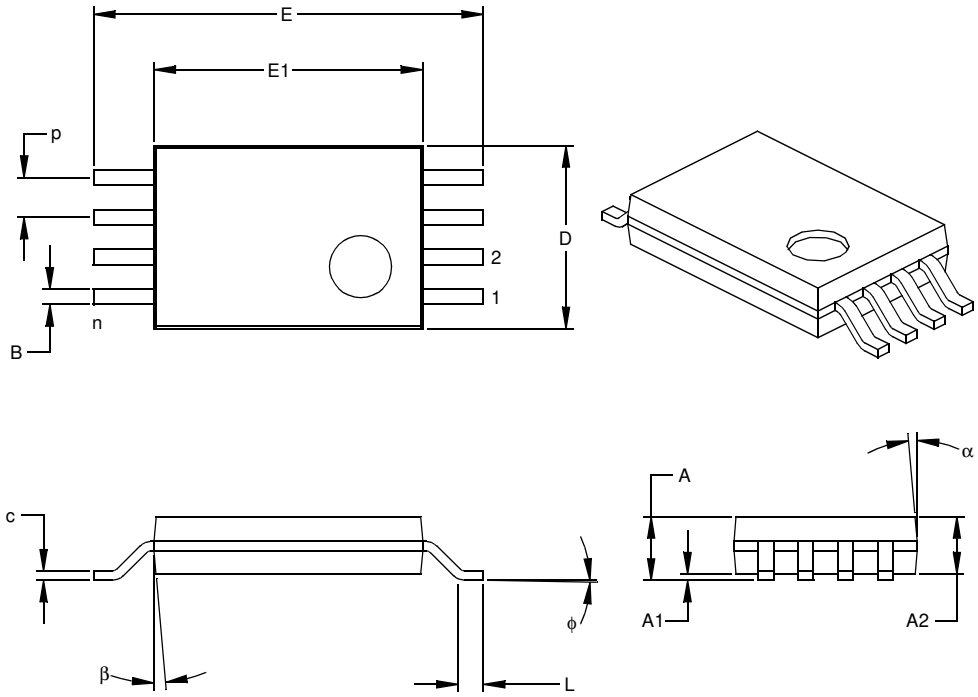
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

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8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)

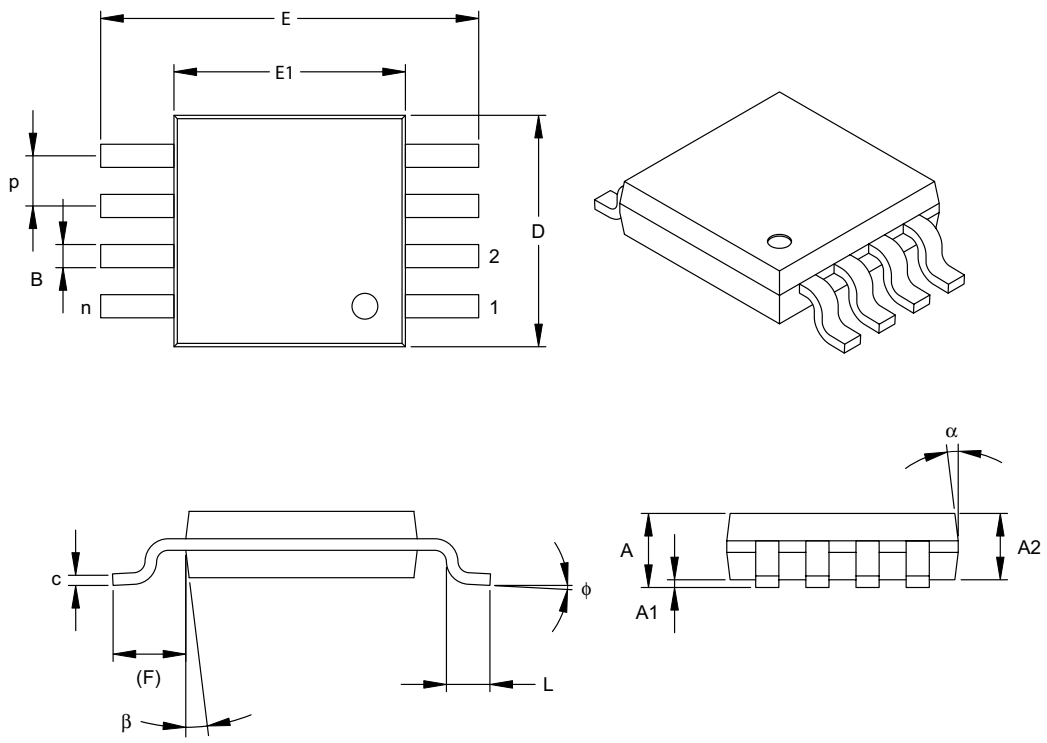


Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-086

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	φ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

Notes:

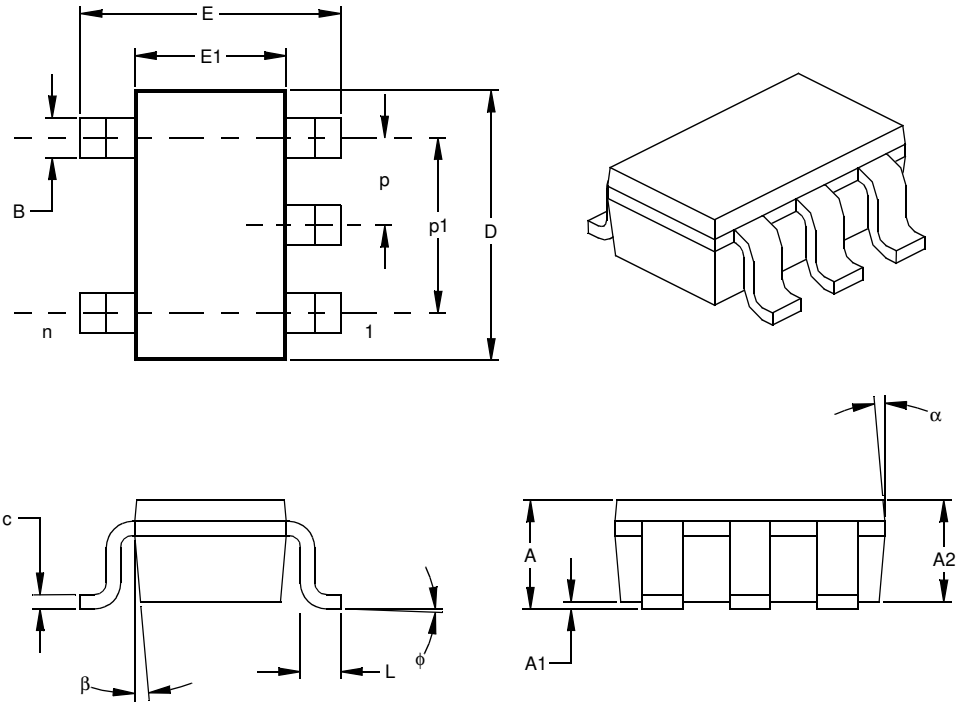
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

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5-Lead Plastic Small Outline Transistor (OT) (SOT-23)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff §	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	ϕ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-178
Drawing No. C04-091

APPENDIX A: REVISION HISTORY

Revision C

Corrections to Section 1.0, Electrical Characteristics.
Section 9.1, 24LC01B standard marking code.

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PART NO.	X	/XX	X
Device	Temperature Range	Package	Lead Finish

Device:	24AA01:	= 1.8V, 1 Kbit I^2C™ Serial EEPROM
	24AA01T:	= 1.8V, 1 Kbit I^2C Serial EEPROM (Tape and Reel)
	24LC01B:	= 2.5V, 1 Kbit I^2C Serial EEPROM
	24LC01BT:	= 2.5V, 1 Kbit I^2C Serial EEPROM (Tape and Reel)
Temperature Range:	I	= -40°C to +85°C
	E	= -40°C to +125°C
Package:	P	= Plastic DIP (300 mil body), 8-lead
	SN	= Plastic SOIC (150 mil body), 8-lead
	ST	= Plastic TSSOP (4.4 mm), 8-lead
	MS	= Plastic Micro Small Outline (MSOP), 8-lead
	OT	= SOT-23, 5-lead (Tape and Reel only)
Lead finish	Blank	= Standard 63/37 SnPb
	G	= Matte Tin (pure Sn)

Examples:

a) 24AA01-I/P: Industrial Temperature,1.8V PDIP package

b) 24AA01-I/SN: Industrial Temperature, 1.8V, SOIC package

c) 24AA01T-I/OT: Industrial Temperature, 1.8V, SOT-23 package, tape and reel

d) 24LC01B-I/P: Industrial Temperature, 2.5V, PDIP package

e) 24LC01B-E/SN: Extended Temperature, 2.5V, SOIC package

f) 24LC01BT-I/OT: Industrial Temperature, 1.8V, SOT-23 package, tape and reel

g) 24LC01B-I/PG: Industrial Temperature, 2.5V PDIP package, Pb-free

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