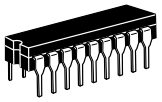
EN: This Datasheet/Document is presented by the manufacturer.

Please visit our website for pricing and availability at www.hestore.hu.

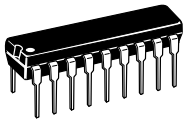
MC14513B

BCD-To-Seven Segment Latch/Decoder/Driver

CMOS MSI (Low–Power Complementary MOS)



L SUFFIX
CERAMIC
CASE 726



P SUFFIX
PLASTIC
CASE 707

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic

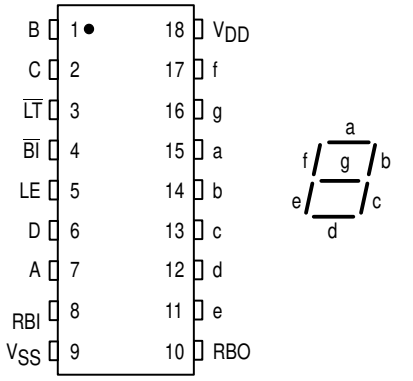
T_A = – 55° to 125°C for all packages.

The MC14513B BCD–to–seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4–bit storage latch, an 8421 BCD–to–seven segment decoder, and has output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn–off or pulse modulate the brightness of the display, and to store a BCD code, respectively. The Ripple Blanking Input (RBI) and Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes. It can be used with seven–segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

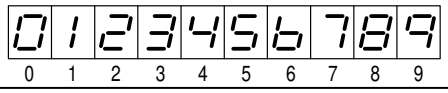
Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High–current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Binary Input
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Capability
- Adds Ripple Blanking In, Ripple Blanking Out to MC14511B
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low–Power TTL Loads, One Low–power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.

PIN ASSIGNMENT



DISPLAY



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 18	V
Input Voltage, All Inputs	V_{in}	– 0.5 to V_{DD} + 0.5	V
DC Current Drain per Input Pin	I	10	mA
Operating Temperature Range	T_A	– 55 to + 125	°C
Power Dissipation, per Package†	P_D	500	mW
Storage Temperature Range	T_{stg}	– 65 to + 150	°C
Maximum Continuous Output Drive Current (Source) per Output	I_{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output ‡	P_{OHmax}	50	mW

‡$P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$
* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

TRUTH TABLE

Inputs								Outputs							
RBI	LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	RBO	a	b	c	d	e	f	g	Display
X	X	X	0	X	X	X	X	+	1	1	1	1	1	1	1	8
X	X	0	1	X	X	X	X	+	0	0	0	0	0	0	0	Blank
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	Blank
0	0	1	1	0	0	0	0	0	1	1	1	1	1	1	0	0
X	0	1	1	0	0	0	1	0	0	1	1	0	0	0	0	1
X	0	1	1	0	0	1	0	0	1	1	0	1	1	0	1	2
X	0	1	1	0	0	1	1	0	1	1	1	1	0	0	1	3
X	0	1	1	0	1	0	0	0	0	1	1	0	0	1	1	4
X	0	1	1	0	1	0	1	0	1	0	1	1	0	1	1	5
X	0	1	1	0	1	1	0	0	0	1	0	1	1	1	1	6
X	0	1	1	0	1	1	1	0	1	1	1	0	0	0	0	7
X	0	1	1	1	0	0	0	0	1	1	1	1	1	1	1	8
X	0	1	1	1	0	0	1	0	1	1	1	1	0	1	1	9
X	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
X	1	1	1	X	X	X	X	†	*							*

X = Don't Care
†RBO = RBI ($\overline{D}\ \overline{C}\ \overline{B}\ \overline{A}$), indicated by other rows of table
*Depends upon the BCD code previously applied when LE = 0

REV 3
1/94

© Motorola, Inc. 1995

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage — Segment Outputs	V_{OL}									Vdc
"0" Level		5.0	—	0.05	—	0	0.05	—	0.05	
V_{in} = V_{DD} or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level	V_{OH}	5.0	4.1	—	4.1	5.0	—	4.1	—	Vdc
V_{in} = 0 or V_{DD}		10	9.1	—	9.1	10	—	9.1	—	
		15	14.1	—	14.1	15	—	14.1	—	
Output Voltage — RBO Output	V_{OL}									Vdc
"0" Level		5.0	—	0.05	—	0	0.05	—	0.05	
V_{in} = V_{DD} or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
V_{in} = 0 or V_{DD}		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage # "0" Level	V_{IL}									Vdc
(V_O = 3.8 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 8.8 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.8 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
(V_O = 0.5 or 3.8 Vdc) "1" Level	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 8.8 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.8 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Voltage — Segments	V_{OH}									Vdc
(I_{OH} = 0 mA) Source		5.0	4.1	—	4.1	4.57	—	4.1	—	
(I_{OH} = 5.0 mA)			—	—	—	4.24	—	—	—	
(I_{OH} = 10 mA)			3.9	—	3.9	4.12	—	3.5	—	
(I_{OH} = 15 mA)			—	—	—	3.94	—	—	—	
(I_{OH} = 20 mA)			3.4	—	3.4	3.70	—	3.0	—	
(I_{OH} = 25 mA)			—	—	—	3.54	—	—	—	
(I_{OH} = 0 mA)		10	9.1	—	9.1	9.58	—	9.1	—	Vdc
(I_{OH} = 5.0 mA)			—	—	—	9.26	—	—	—	
(I_{OH} = 10 mA)			9.0	—	9.0	9.17	—	8.6	—	
(I_{OH} = 15 mA)			—	—	—	9.04	—	—	—	
(I_{OH} = 20 mA)			8.6	—	8.6	8.90	—	8.2	—	
(I_{OH} = 25 mA)			—	—	—	8.75	—	—	—	
(I_{OH} = 0 mA)		15	14.1	—	14.1	14.59	—	14.1	—	Vdc
(I_{OH} = 5.0 mA)			—	—	—	14.27	—	—	—	
(I_{OH} = 10 mA)			14	—	14	14.18	—	13.6	—	
(I_{OH} = 15 mA)			—	—	—	14.07	—	—	—	
(I_{OH} = 20 mA)			13.6	—	13.6	13.95	—	13.2	—	
(I_{OH} = 25 mA)			—	—	—	13.80	—	—	—	

(continued)

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} is not constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS — continued (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Drive Current — RBO Output	I_{OH}									mAdc
(V_{OH} = 2.5 V) Source		5.0	– 0.40	—	– 0.32	– 0.64	—	– 0.22	—	
(V_{OH} = 9.5 V)		10	– 0.21	—	– 0.17	– 0.34	—	– 0.12	—	
(V_{OH} = 13.5 V)		15	– 0.81	—	– 0.66	– 1.30	—	– 0.46	—	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.18	—	0.15	0.29	—	0.10	—	mAdc
(V_{OL} = 0.5 V)		10	0.47	—	0.38	0.75	—	0.26	—	
(V_{OL} = 1.5 V)		15	1.80	—	1.50	2.90	—	1.0	—	
Output Drive Current — Segments	I_{OL}									mAdc
(V_{OL} = 0.4 V) Sink		5.0	0.64	—	0.51	0.88	—	0.36	—	
(V_{OL} = 0.5 V)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 V)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
(Per Package) V_{in} = 0 or V_{DD},		10	—	10	—	0.010	10	—	300	
I_{out} = 0 µA		15	—	20	—	0.015	20	—	600	
Total Supply Current**†	I_T	5.0	I_T = (1.9 µA/kHz) f + I_{DD}							µAdc
(Dynamic plus Quiescent,		10	I_T = (3.8 µA/kHz) f + I_{DD}							
Per Package)		15	I_T = (5.7 µA/kHz) f + I_{DD}							
(C_L = 50 pF on all outputs, all buffers switching)										

#Noise immunity specified for worst–case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

** The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

Input LE and RBI low, and Inputs D, $\overline{BI}$ and $\overline{LT}$ high.
f in respect to a system clock.
All outputs connected to respective C_L loads.

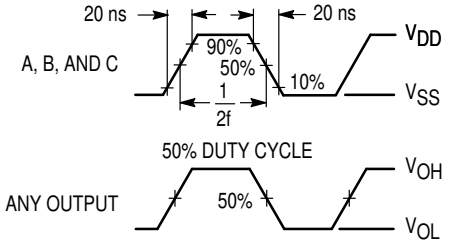
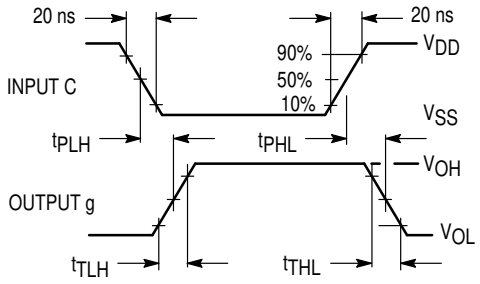


Figure 1. Dynamic Power Dissipation Signal Waveforms

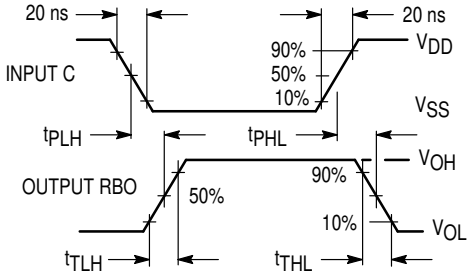
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise Time — Segment Outputs	t_{TLH}					ns
		5.0	—	40	80	
		10	—	30	60	
		15	—	25	50	
Output Rise Time — RBO Output	t_{TLH}					ns
		5.0	—	480	960	
		10	—	240	480	
		15	—	190	380	
Output Fall Time — Segment Outputs*	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 50 ns		5.0	—	125	250	
t_{THL} = (0.75 ns/pF) C_L + 37.5 ns		10	—	75	150	
t_{THL} = (0.55 ns/pF) C_L + 37.5 ns		15	—	65	130	
Output Fall Time — RBO Outputs	t_{THL}					ns
t_{THL} = (3.25 ns/pF) C_L + 107.5 ns		5.0	—	270	540	
t_{THL} = (1.35 ns/pF) C_L + 67.5 ns		10	—	135	270	
t_{THL} = (0.95 ns/pF) C_L + 62.5 ns		15	—	110	220	
Propagation Delay Time — A, B, C, D Inputs*	t_{PLH}					ns
t_{PLH} = (0.40 ns/pF) C_L + 620 ns		5.0	—	640	1280	
t_{PLH} = (0.25 ns/pF) C_L + 237.5 ns		10	—	250	500	
t_{PLH} = (0.20 ns/pF) C_L + 165 ns		15	—	175	350	
t_{PHL} = (1.3 ns/pF) C_L + 655 ns	t_{PHL}	5.0	—	720	1440	ns
t_{PHL} = (0.60 ns/pF) C_L + 260 ns		10	—	290	580	
t_{PHL} = (0.35 ns/pF) C_L + 182.5 ns		15	—	200	400	
Propagation Delay Time — RBI and $\overline{BI}$ Inputs*	t_{PLH}					ns
t_{PLH} = (1.05 ns/pF) C_L + 547.5 ns		5.0	—	600	750	
t_{PLH} = (0.45 ns/pF) C_L + 177.5 ns		10	—	200	300	
t_{PLH} = (0.30 ns/pF) C_L + 135 ns		15	—	150	220	
t_{PHL} = (0.85 ns/pF) C_L + 442.5 ns	t_{PHL}	5.0	—	485	970	ns
t_{PHL} = (0.45 ns/pF) C_L + 177.5 ns		10	—	200	400	
t_{PHL} = (0.35 ns/pF) C_L + 142.5 ns		15	—	160	320	
Propagation Delay Time — $\overline{LT}$ Input*	t_{PLH}					ns
t_{PLH} = (0.45 ns/pF) C_L + 290.5 ns		5.0	—	313	625	
t_{PLH} = (0.25 ns/pF) C_L + 112.5 ns		10	—	125	250	
t_{PLH} = (0.20 ns/pF) C_L + 80 ns		15	—	90	180	
t_{PHL} = (1.3 ns/pF) C_L + 248 ns	t_{PHL}	5.0	—	313	625	ns
t_{PHL} = (0.45 ns/pF) C_L + 102.5 ns		10	—	125	250	
t_{PHL} = (0.35 ns/pF) C_L + 72.5 ns		15	—	90	180	
Setup Time	t_{su}	5.0	100	—	—	ns
		10	40	—	—	
		15	30	—	—	
Hold Time	t_h	5.0	60	—	—	ns
		10	40	—	—	
		15	30	—	—	
Latch Enable Pulse Width	$t_{WL(LE)}$	5.0	520	260	—	ns
		10	220	110	—	
		15	130	65	—	

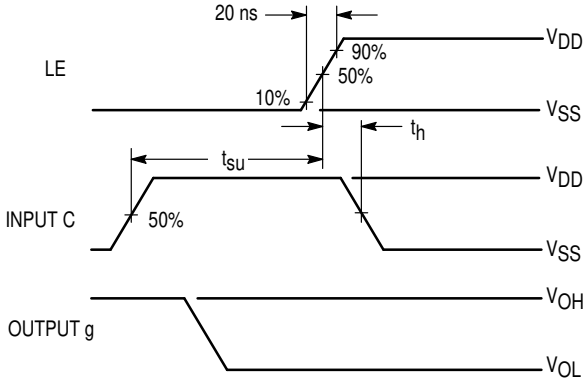
* The formulas given are for the typical characteristics only.



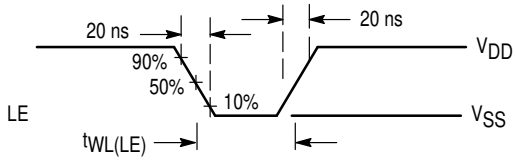
a. Data Propagation Delay: Inputs RBI, D and LE low, and Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.



b. Inputs A, B, D and LE low, and Inputs RBI, $\overline{BI}$ and $\overline{LT}$ high.



c. Setup and Hold Times: Input RBI and D low, Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.

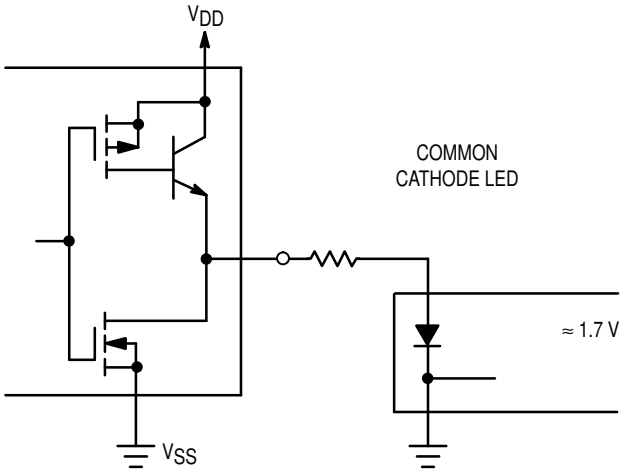


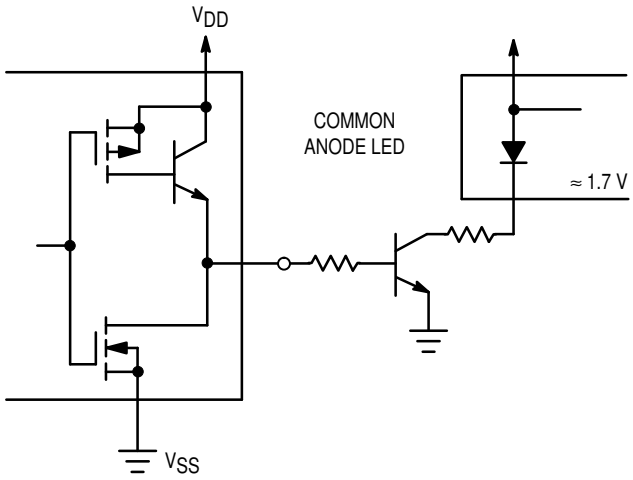
d. Pulse Width: Data DCBA strobed into latches.

Figure 2. Dynamic Signal Waveforms

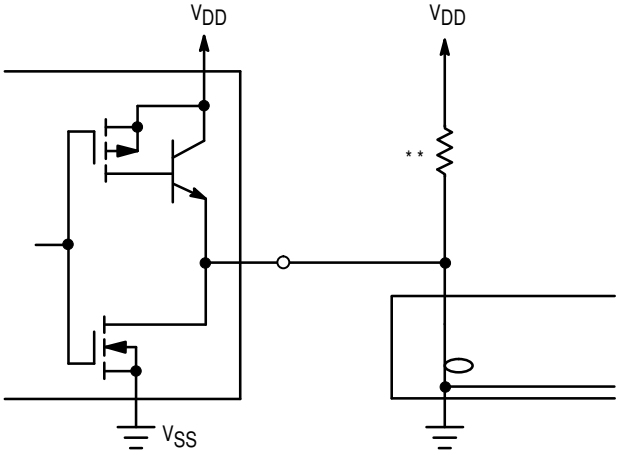
CONNECTIONS TO VARIOUS DISPLAY READOUTS

LIGHT EMITTING DIODE (LED) READOUT

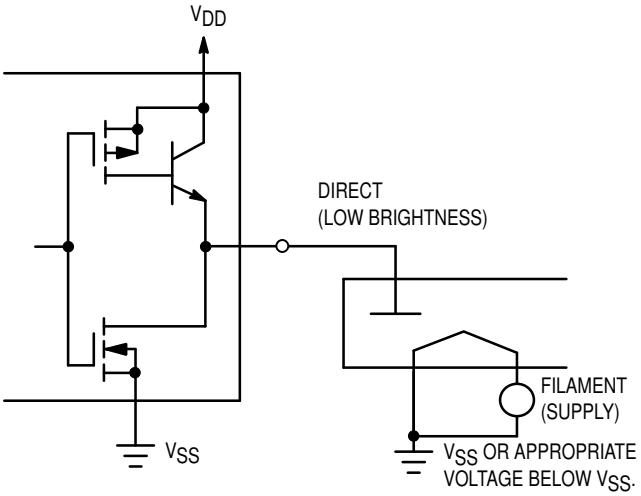




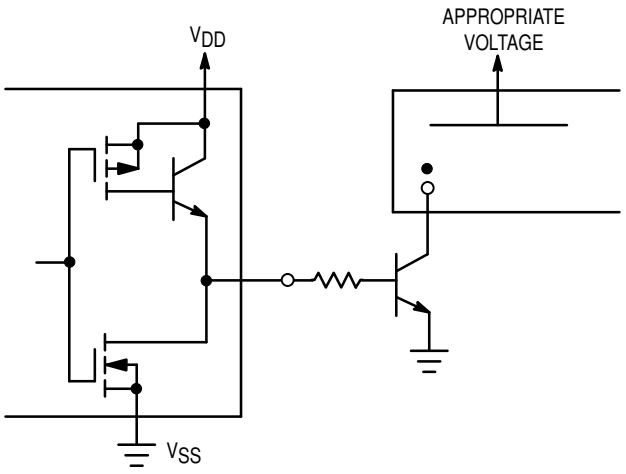
INCANDESCENT READOUT



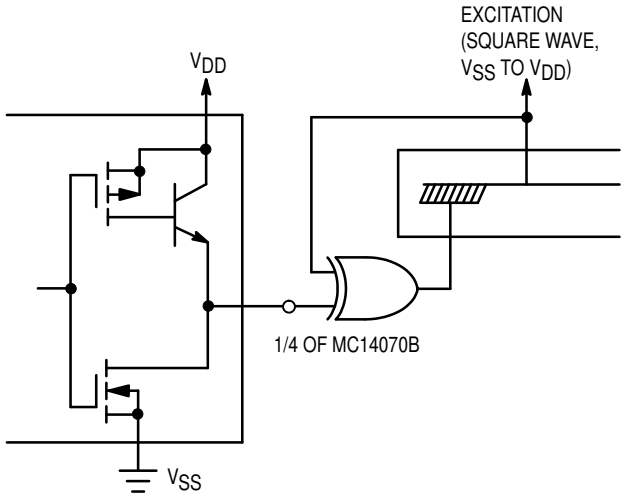
FLUORESCENT READOUT



GAS DISCHARGE READOUT



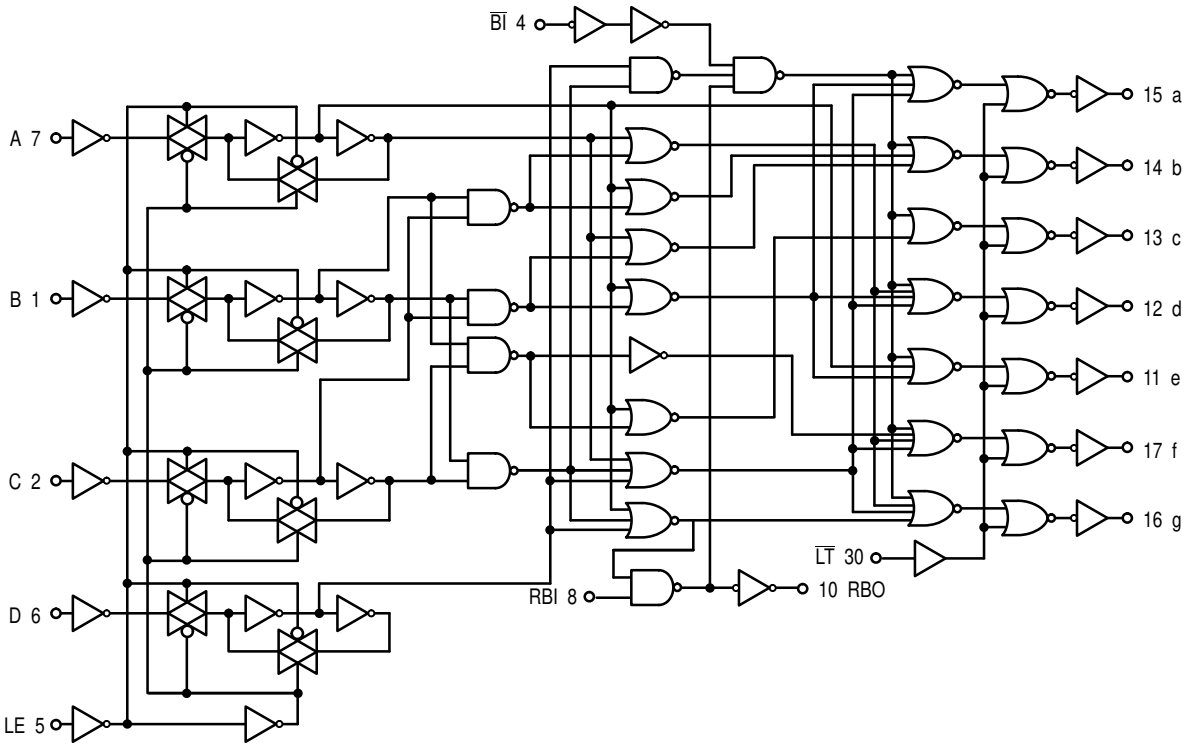
LIQUID CRYSTAL (LC) READOUT



** A filament pre–warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

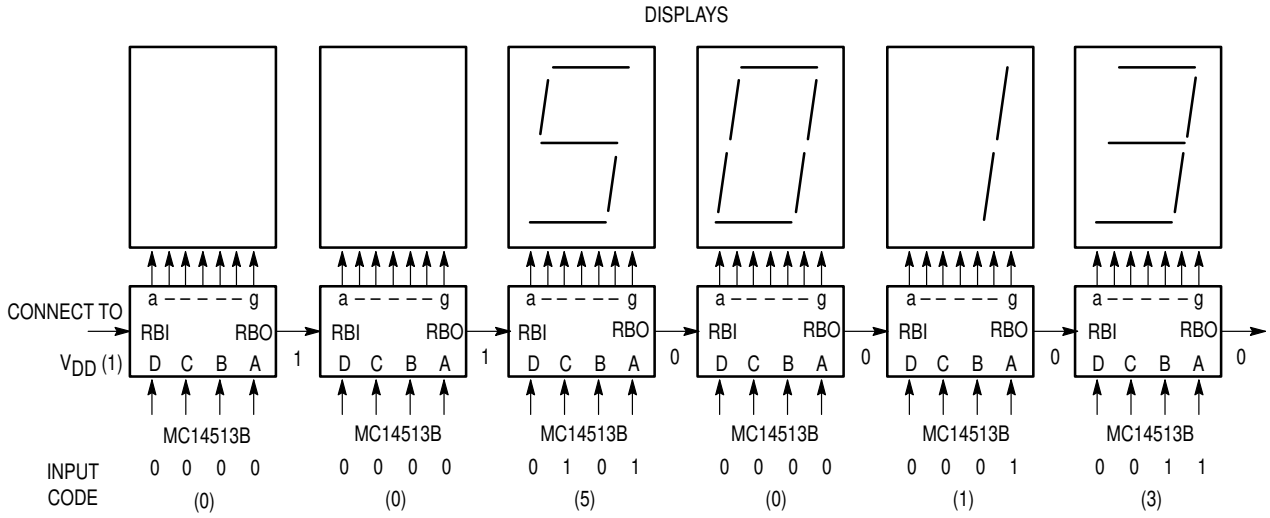
Direct dc drive of LC's not recommended for life of LC readouts.

LOGIC DIAGRAM



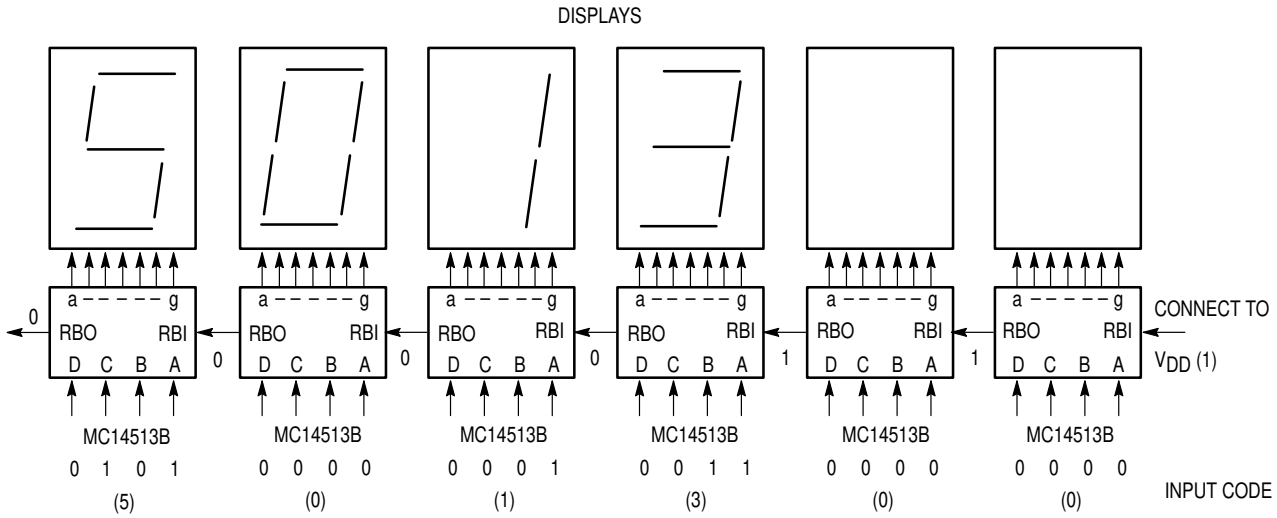
TYPICAL APPLICATIONS FOR RIPPLE BLANKING

LEADING EDGE ZERO SUPPRESSION



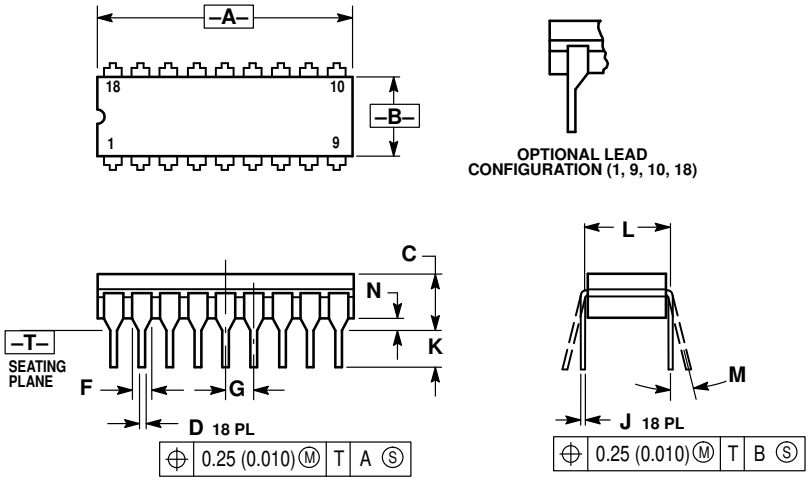
TYPICAL APPLICATIONS FOR RIPPLE BLANKING (Cont)

TRAILING EDGE ZERO SUPPRESSION



OUTLINE DIMENSIONS

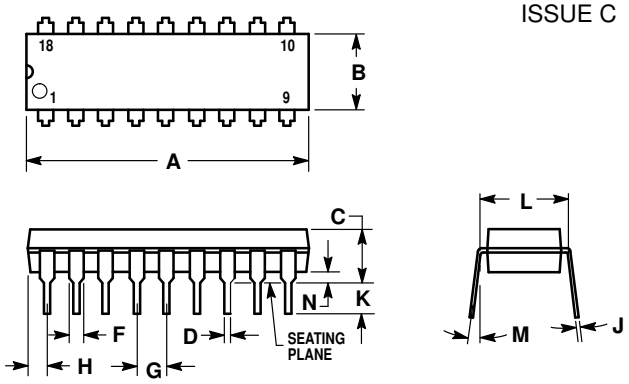
L SUFFIX
CERAMIC DIP PACKAGE
CASE 726–04
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.880	0.910	22.35	23.11
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.021	0.38	0.53
F	0.055	0.070	1.40	1.78
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.20	0.30
K	0.125	0.170	3.18	4.32
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

P SUFFIX
PLASTIC DIP PACKAGE
CASE 707–02
ISSUE C



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and M are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298