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15MHz, BiMOS Operational Amplifier with MOSFET Input/CMOS Output

CA3130A and CA3130 are op amps that combine the advantage of both CMOS and bipolar transistors.

Gate-protected P-Channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS transistors in the input stage results in common-mode input-voltage capability down to 0.5V below the negative-supply terminal, an important attribute in single-supply applications.

A CMOS transistor-pair, capable of swinging the output voltage to within 10mV of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5V to 16V, (±2.5V to ±8V). They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

- The CA3130A offers superior input characteristics over those of the CA3130.

Ordering Information

PART NO. (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. DWG. #
CA3130AE	-55 to 125	8 Ld PDIP	E8.3
CA3130AM (3130A)	-55 to 125	8 Ld SOIC	M8.15
CA3130AM96 (3130A)	-55 to 125	8 Ld SOIC Tape and Reel	M8.15
CA3130AMZ (3130AZ) (Note)	-55 to 125	8 Ld SOIC (Pb-free)	M8.15
CA3130AMZ96 (3130AZ) (Note)	-55 to 125	8 Ld SOIC Tape and Reel (Pb-free)	M8.15
CA3130E	-55 to 125	8 Ld PDIP	E8.3
CA3130EZ (Note)	-55 to 125	8 Ld PDIP* (Pb-free)	E8.3
CA3130M (3130)	-55 to 125	8 Ld SOIC	M8.15
CA3130M96 (3130)	-55 to 125	8 Ld SOIC Tape and Reel	M8.15
CA3130MZ (3130MZ) (Note)	-55 to 125	8 Ld SOIC (Pb-free)	M8.15
CA3130MZ96 (3130MZ)	-55 to 125	8 Ld SOIC Tape and Reel (Pb-free)	M8.15

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

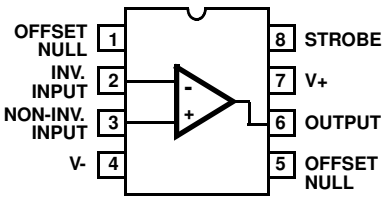
- MOSFET Input Stage Provides:
  - Very High Z_I = 1.5 TΩ (1.5 x 10^{12}Ω) (Typ)
  - Very Low I_I . . . . . 5pA (Typ) at 15V Operation
    . . . . . .= 2pA (Typ) at 5V Operation
- Ideal for Single-Supply Applications
- Common-Mode Input-Voltage Range Includes Negative Supply Rail; Input Terminals can be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or both) Supply Rails
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Ground-Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long-Duration Timers/Monostables
- High-Input-Impedance Comparators (Ideal Interface with Digital CMOS)
- High-Input-Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single-Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to 0V)
- Peak Detectors
- Single-Supply Full-Wave Precision Rectifiers
- Photo-Diode Sensor Amplifiers

Pinout

CA3130, CA3130A
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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All other trademarks mentioned are the property of their respective owners.

Absolute Maximum Ratings

DC Supply Voltage (Between V+ And V- Terminals) 16V
Differential Input Voltage 8V
DC Input Voltage . . . . . (V+ +8V) to (V- -0.5V)
Input-Terminal Current 1mA
Output Short-Circuit Duration (Note 1) . . . . . Indefinite

Operating Conditions

Temperature Range . . . . . -50°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package*	115	N/A
SOIC Package	160	N/A

Maximum Junction Temperature (Plastic Package) . . . . . .150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . .300°C
(SOIC - Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$T_A = 25°C$, V+ = 15V, V- = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA3130			CA3130A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$\|V_{IO}\|$	$V_S = \pm 7.5V$	-	8	15	-	2	5	mV
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		-	10	-	-	10	-	µV/°C
Input Offset Current	$\|I_{IO}\|$	$V_S = \pm 7.5V$	-	0.5	30	-	0.5	20	pA
Input Current	I_I	$V_S = \pm 7.5V$	-	5	50	-	5	30	pA
Large-Signal Voltage Gain	A_{OL}	$V_O = 10V_{P-P}$, $R_L = 2k\Omega$	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB
Common-Mode Rejection Ratio	CMRR		70	90	-	80	90	-	dB
Common-Mode Input Voltage Range	V_{ICR}		0	-0.5 to 12	10	0	-0.5 to 12	10	V
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V_S$	$V_S = \pm 7.5V$	-	32	320	-	32	150	µV/V
Maximum Output Voltage	$V_{OM}+$	$R_L = 2k\Omega$	12	13.3	-	12	13.3	-	V
	$V_{OM}-$	$R_L = 2k\Omega$	-	0.002	0.01	-	0.002	0.01	V
	$V_{OM}+$	$R_L = \infty$	14.99	15	-	14.99	15	-	V
	$V_{OM}-$	$R_L = \infty$	-	0	0.01	-	0	0.01	V
Maximum Output Current	$I_{OM}+$ (Source) at $V_O = 0V$		12	22	45	12	22	45	mA
	$I_{OM}-$ (Sink) at $V_O = 15V$		12	20	45	12	20	45	mA
Supply Current	I+	$V_O = 7.5V$, $R_L = \infty$	-	10	15	-	10	15	mA
	I+	$V_O = 0V$, $R_L = \infty$	-	2	3	-	2	3	mA

Electrical Specifications Typical Values Intended Only for Design Guidance, V_{SUPPLY} = ±7.5V, T_A = 25°C Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA3130, CA3130A	UNITS
Input Offset Voltage Adjustment Range		10kΩ Across Terminals 4 and 5 or 4 and 1	±22	mV
Input Resistance	R_I		1.5	TΩ
Input Capacitance	C_I	f = 1MHz	4.3	pF
Equivalent Input Noise Voltage	e_N	BW = 0.2MHz, R_S = 1MΩ (Note 3)	23	μV
Open Loop Unity Gain Crossover Frequency (For Unity Gain Stability ≥47pF Required.)	f_T	C_C = 0	15	MHz
		C_C = 47pF	4	MHz
Slew Rate:	SR			
Open Loop		C_C = 0	30	V/μs
Closed Loop		C_C = 56pF	10	V/μs
Transient Response:		C_C = 56pF, C_L = 25pF, R_L = 2kΩ (Voltage Follower)		
Rise Time	t_r		0.09	μs
Overshoot	OS		10	%
Settling Time (To <0.1%, V_{IN} = $4V_{P-P}$)	t_S		1.2	μs

NOTE:

3. Although a 1MΩ source is used for this test, the equivalent input noise remains constant for values of R_S up to 10MΩ.

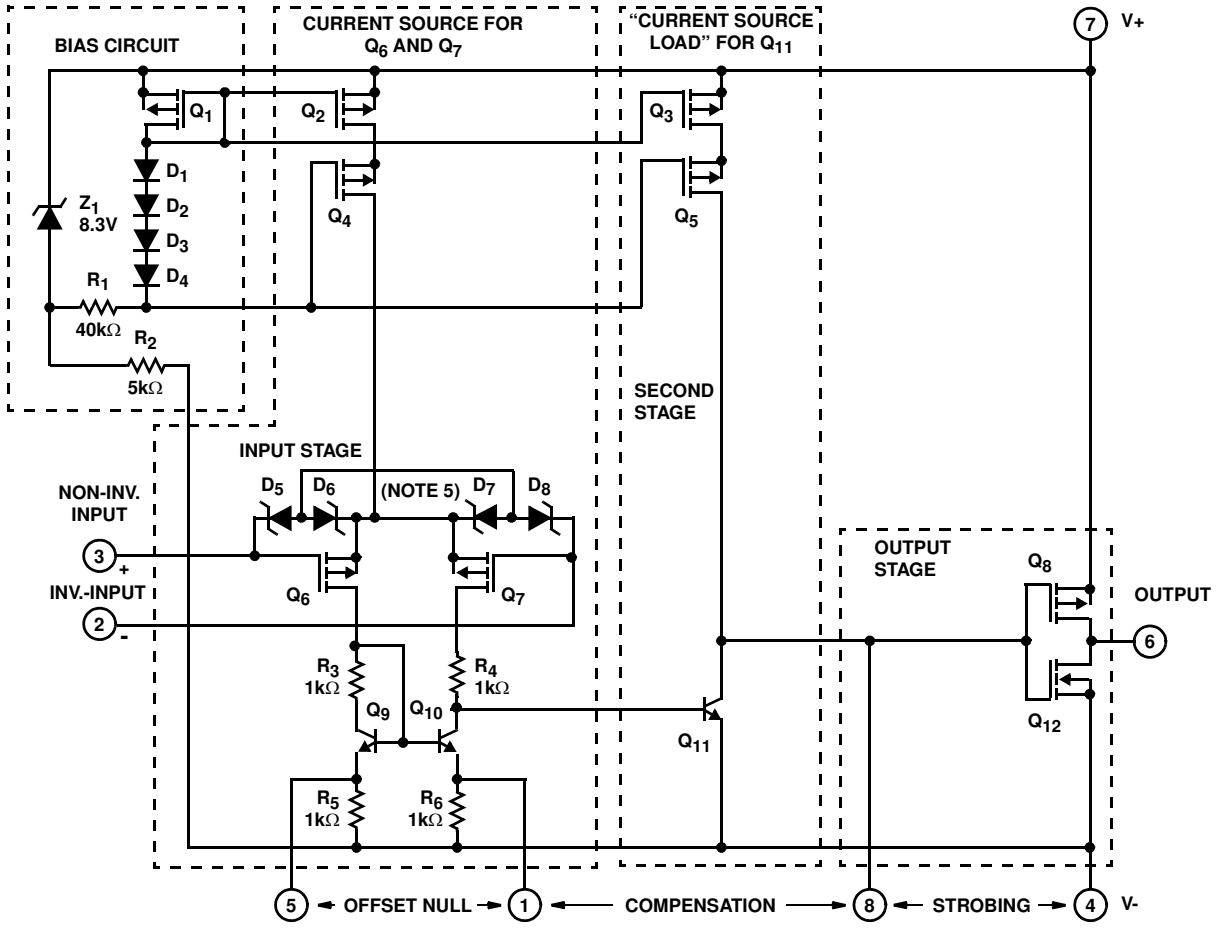
Electrical Specifications Typical Values Intended Only for Design Guidance, V+ = 5V, V- = 0V, T_A = 25°C Unless Otherwise Specified (Note 4)

PARAMETER	SYMBOL	TEST CONDITIONS	CA3130	CA3130A	UNITS
Input Offset Voltage	V_{IO}		8	2	mV
Input Offset Current	I_{IO}		0.1	0.1	pA
Input Current	I_I		2	2	pA
Common-Mode Rejection Ratio	CMRR		80	90	dB
Large-Signal Voltage Gain	A_{OL}	V_O = $4V_{P-P}$, R_L = 5kΩ	100	100	kV/V
			100	100	dB
Common-Mode Input Voltage Range	V_{ICR}		0 to 2.8	0 to 2.8	V
Supply Current	I+	V_O = 5V, R_L = ∞	300	300	μA
		V_O = 2.5V, R_L = ∞	500	500	μA
Power Supply Rejection Ratio	$\Delta V_{IO}/\Delta V+$		200	200	μV/V

NOTE:

4. Operation at 5V is not recommended for temperatures below 25°C.

Schematic Diagram



NOTE:

5. Diodes D_5 through D_8 provide gate-oxide protection for MOSFET input stage.

Application Information

Circuit Description

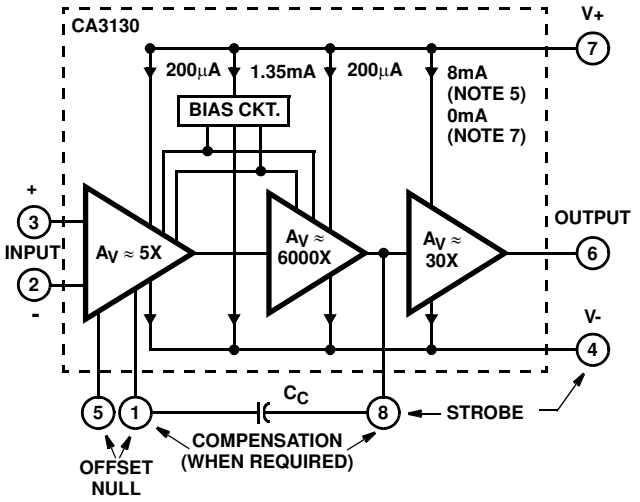
Figure 1 is a block diagram of the CA3130 Series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Figure 1, provide the total gain of the CA3130. A biasing circuit provides two potentials for common use in the first and second stages.

Terminal 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output potential at Terminal 6 essentially rises to the positive supply-rail potential at Terminal 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g.,when the amplifier output is used to drive CMOS digital circuits in Comparator applications).

Input Stage

The circuit of the CA3130 is shown in the schematic diagram. It consists of a differential-input stage using PMOS field-effect transistors (Q_6, Q_7) working into a mirror-pair of bipolar transistors (Q_9, Q_{10}) functioning as load resistors together with resistors R_3 through R_6.

The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q_{11}). Offset nulling, when desired, can be effected by connecting a 100,000Ω potentiometer across Terminals 1 and 5 and the potentiometer slider arm to Terminal 4.



NOTES:

6. Total supply voltage (for indicated voltage gains) = 15V with input terminals biased so that Terminal 6 potential is +7.5V above Terminal 4.
7. Total supply voltage (for indicated voltage gains) = 15V with output terminal driven to either supply rail.

FIGURE 1. BLOCK DIAGRAM OF THE CA3130 SERIES

Cascade-connected PMOS transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described.

The small diodes D_5 through D_8 provide gate-oxide protection against high-voltage transients, including static electricity during handling for Q_6 and Q_7.

Second-Stage

Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q_{11} and its cascade-connected load resistance provided by PMOS transistors Q_3 and Q_5. The source of bias potentials for these PMOS transistors is subsequently described. Miller Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terminals 1 and 8. A 47pF capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Bias-Source Circuit

At total supply voltages, somewhat above 8.3V, resistor R_2 and zener diode Z_1 serve to establish a voltage of 8.3V across the series-connected circuit, consisting of resistor R_1, diodes D_1 through D_4, and PMOS transistor Q_1. A tap at the junction of resistor R_1 and diode D_4 provides a gate-bias potential of about 4.5V for PMOS transistors Q_4 and Q_5 with respect to Terminal 7. A potential of about 2.2V is developed across diode-connected PMOS transistor Q_1 with respect to Terminal 7 to provide gate bias for PMOS transistors Q_2 and Q_3. It should be noted that Q_1 is "mirror-connected (see Note 8)" to both Q_2 and Q_3. Since transistors Q_1, Q_2, Q_3 are designed to be identical, the approximately 200μA current in Q_1 establishes a similar current in Q_2 and Q_3 as constant current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3V, zener diode Z_1 becomes nonconductive and the potential, developed across series-connected R_1, D_1-D_4, and Q_1, varies directly with variations in supply voltage. Consequently, the gate bias for Q_4, Q_5 and Q_2, Q_3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3V. Operation at total supply voltages below about 4.5V results in seriously degraded performance.

Output Stage

The output stage consists of a drain-loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Figure 2. Typical op amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01% accuracy levels, including the negative supply rail.

NOTE:

8. For general information on the characteristics of CMOS transistor-pairs in linear-circuit applications, see File Number 619, data sheet on CA3600E "CMOS Transistor Array".

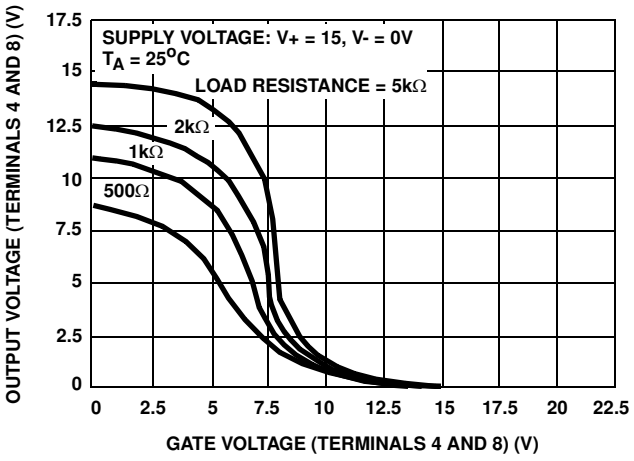


FIGURE 2. VOLTAGE TRANSFER CHARACTERISTICS OF CMOS OUTPUT STAGE

Input Current Variation with Common Mode Input Voltage

As shown in the Table of Electrical Specifications, the input current for the CA3130 Series Op Amps is typically 5pA at TA = 25oC when Terminals 2 and 3 are at a common-mode potential of +7.5V with respect to negative supply Terminal 4. Figure 3 contains data showing the variation of input current as a function of common-mode input voltage at TA = 25oC. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1pA, provided the common-mode input voltage does not exceed 2V. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the metal can package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the Metal Can case of the CA3130 is also internally tied to Terminal 4, input Terminal 3 is essentially "guarded" from spurious leakage currents.

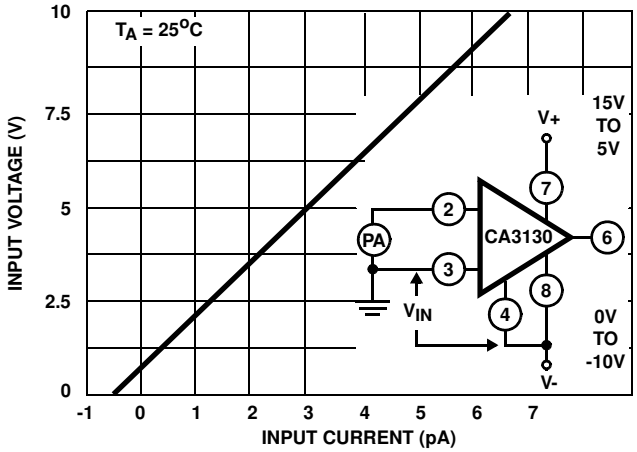


FIGURE 3. INPUT CURRENT vs COMMON-MODE VOLTAGE

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000Ω potentiometer connected across Terminals 1 and 5 and with the potentiometer slider arm connected to Terminal 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA3130 Series circuits is typically 5pA at 25oC. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10oC increase in temperature. Figure 4 provides data on the typical variation of input bias current as a function of temperature in the CA3130.

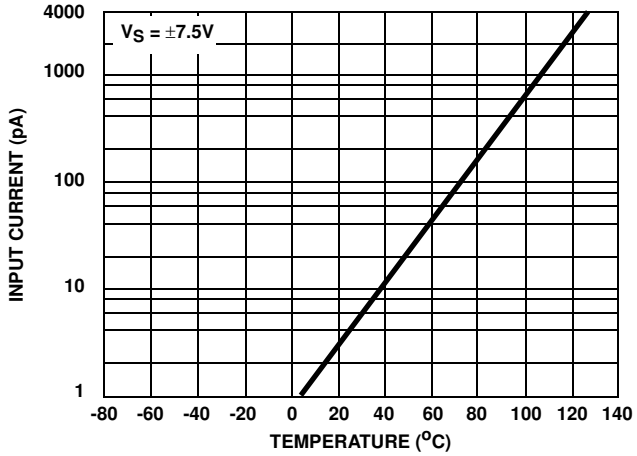


FIGURE 4. INPUT CURRENT vs TEMPERATURE

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input Offset Voltage (V_{IO}) Variation with DC Bias and Device Operating Life

It is well known that the characteristics of a MOSFET device can change slightly when a DC gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential DC bias voltage applied across Terminals 2 and 3. Figure 5 shows typical data pertinent to shifts in offset voltage encountered with CA3130 devices (metal can package) during life testing. At lower temperatures (metal can and plastic), for example at 85oC, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The 2VDC differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

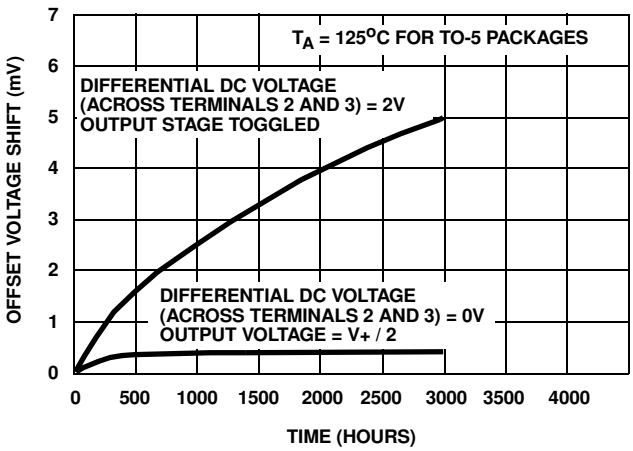


FIGURE 5. TYPICAL INCREMENTAL OFFSET-VOLTAGE SHIFT vs OPERATING LIFE

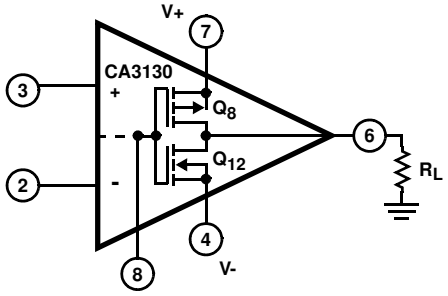


FIGURE 6A. DUAL POWER SUPPLY OPERATION

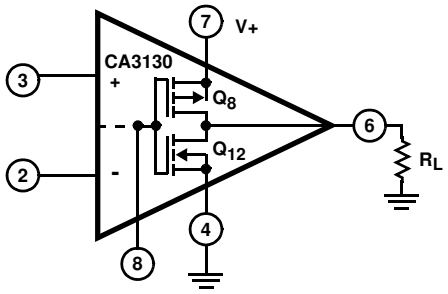


FIGURE 6B. SINGLE POWER SUPPLY OPERATION

FIGURE 6. CA3130 OUTPUT STAGE IN DUAL AND SINGLE POWER SUPPLY OPERATION

Power-Supply Considerations

Because the CA3130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single-and dual-supply service. Figures 6A and 6B show the CA3130 connected for both dual-and single-supply operation.

Dual-supply Operation: When the output voltage at Terminal 6 is 0V, the currents supplied by the two power supplies are equal. When the gate terminals of Q_8 and Q_{12} are driven increasingly positive with respect to ground, current flow through Q_{12} (from the negative supply) to the load is increased and current flow through Q_8 (from the positive supply) decreases correspondingly. When the gate terminals of Q_8 and Q_{12} are driven increasingly negative with respect to ground, current flow through Q_8 is increased and current flow through Q_{12} is decreased accordingly.

Single-supply Operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2, i.e., the voltage drops across Q_8 and Q_{12} are of equal magnitude. Figure 20 shows typical quiescent supply-current vs supply-voltage for the CA3130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Figure 2). If either Q_8 or Q_{12} are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Terminal 8 swung down to ground potential (or tied to ground), NMOS transistor Q_{12} is completely cut off and the supply-current to series-connected transistors Q_8, Q_{12} goes essentially to zero. The two preceding stages in the CA3130, however, continue to draw modest supply-current (see the lower curve in Figure 20) even though the output stage is strobed off. Figure 6A shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$ by pulling the potential of Terminal 8 down to that of Terminal 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2kΩ) is connected between Terminal 6 and ground in the circuit of Figure 6B. Let it be assumed again that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2. Since PMOS transistor Q_8 must now supply quiescent current to both R_L and transistor Q_{12}, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Figure 22 shows the voltage-drop across PMOS transistor Q_8 as a function of load current at several supply voltages. Figure 2 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3130 is most advantageous in applications where in the source resistance of the input signal is on the order of 1MΩ or more. In this case, the total input-referred noise voltage is typically only 23μV when the test-circuit amplifier of Figure 7 is operated at a total supply voltage of 15V. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for

values of source resistance very much greater than 1MΩ, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

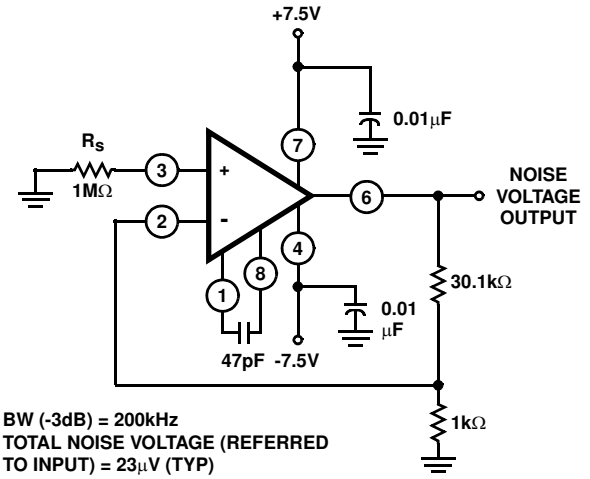


FIGURE 7. TEST-CIRCUIT AMPLIFIER (30-dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENTS

Typical Applications

Voltage Followers

Operational amplifiers with very high input resistances, like the CA3130, are particularly suited to service as voltage followers. Figure 8 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3130 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Figure 9, together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Figure 9A with input-signal ramping. The waveforms in Figure 9B show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5V below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Figure 9B also shows the manner in which the CMOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described later, illustrates the practical use of the CA3130 in a single-supply voltage-follower application.

9-Bit CMOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC) is shown in Figure 10. This system combines the concepts of multiple-switch CMOS ICs, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3130 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10V logic levels are used in the circuit of Figure 10.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three “inverters”, each “inverter” functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of 1% tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000Ω resistors from the same manufacturing lot.

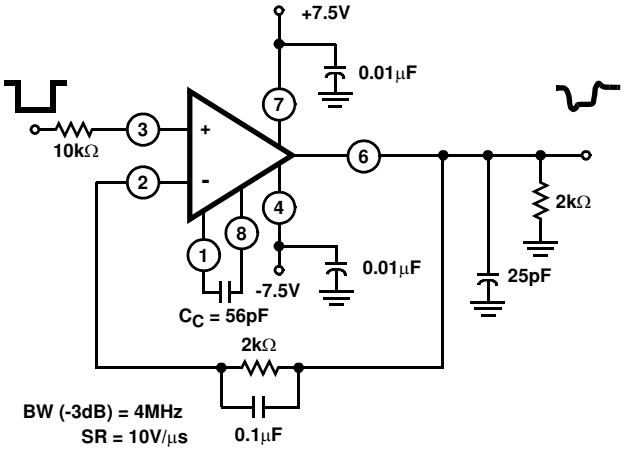
A single 15V supply provides a positive bus for the CA3130 follower amplifier and feeds the CA3085 voltage regulator. A “scale-adjust” function is provided by the regulator output control, set to a nominal 10V level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the CMOS building blocks simplifies the design of DAC systems tailored to particular needs.

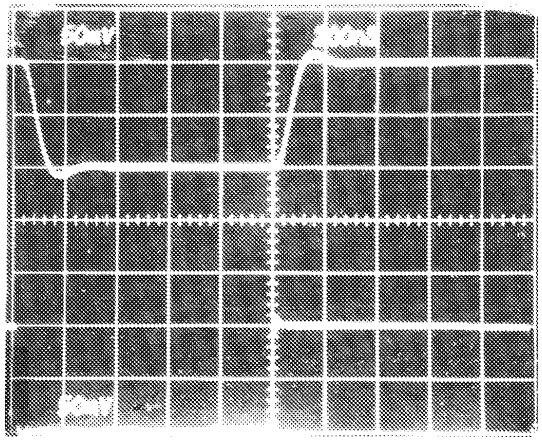
Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

The absolute-value circuit using the CA3130 is shown in Figure 11. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3130 functions as a normal inverting amplifier with a gain equal to $-R_2/R_1$. When the equality of the two equations shown in Figure 11 is satisfied, the full-wave output is symmetrical.

Peak Detectors

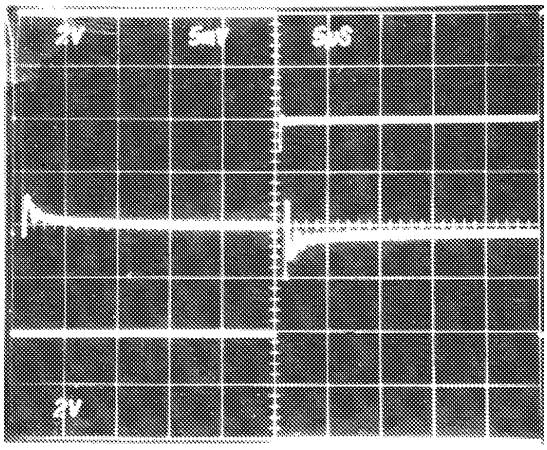
Peak-detector circuits are easily implemented with the CA3130, as illustrated in Figure 12 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA3130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q_{11}, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q_{11}, the transistor functions in an active “pull-down” mode so that the intrinsic capacitance can be discharged more expeditiously.





Top Trace: Output
Center Trace: Input

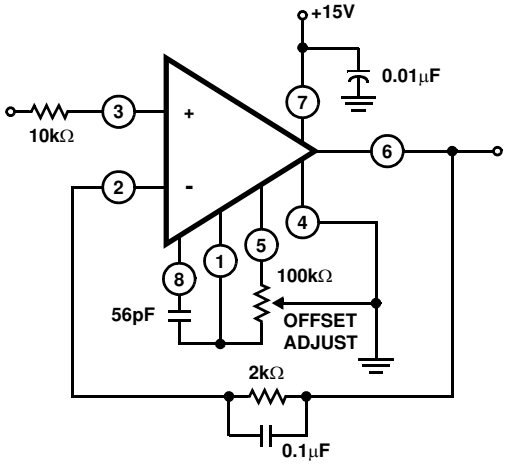
FIGURE 8A. SMALL-SIGNAL RESPONSE (50mV/DIV., 200ns/DIV.)



Top Trace: Output Signal; 2V/Div., 5μs/Div.
Center Trace: Difference Signal; 5mV/Div., 5μs/Div.
Bottom Trace: Input Signal; 2V/Div., 5μs/Div.

FIGURE 8B. INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME (MEASUREMENT MADE WITH TEKTRONIX 7A13 DIFFERENTIAL AMPLIFIER)

FIGURE 8. SPLIT SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS



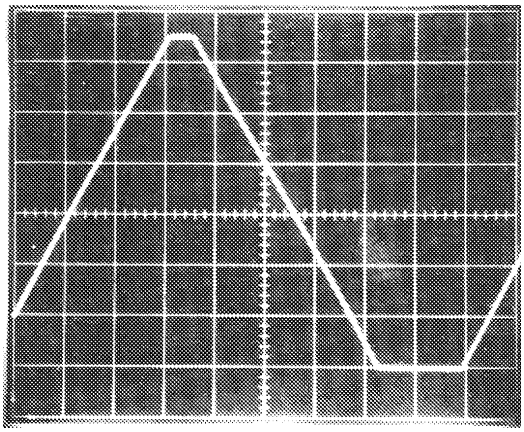
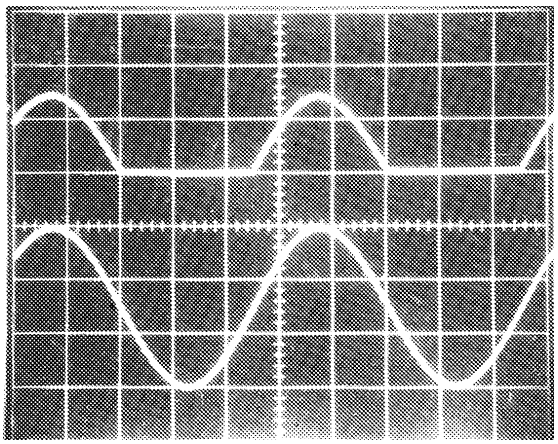


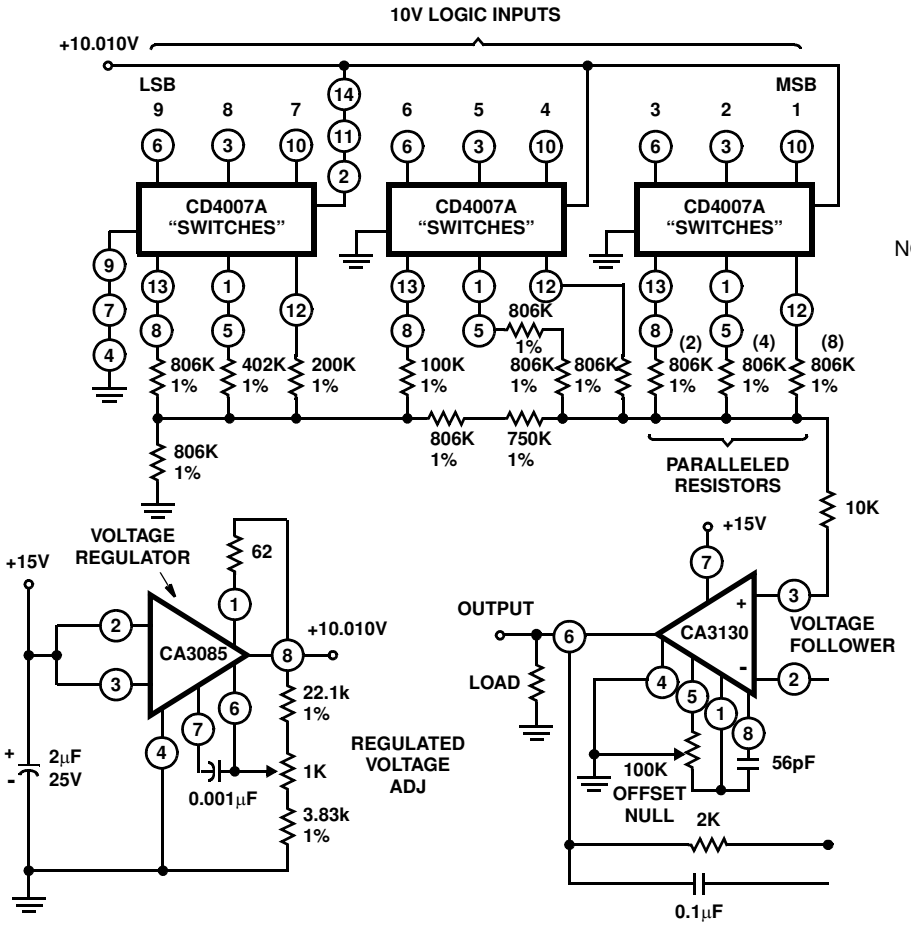
FIGURE 9A. OUTPUT WAVEFORM WITH INPUT SIGNAL RAMPING (2V/DIV., 500μs/DIV.)



Top Trace: Output; 5V/Div., 200μs/Div.
Bottom Trace: Input Signal; 5V/Div., 200μs/Div.

FIGURE 9B. OUTPUT WAVEFORM WITH GROUND REFERENCE SINE-WAVE INPUT

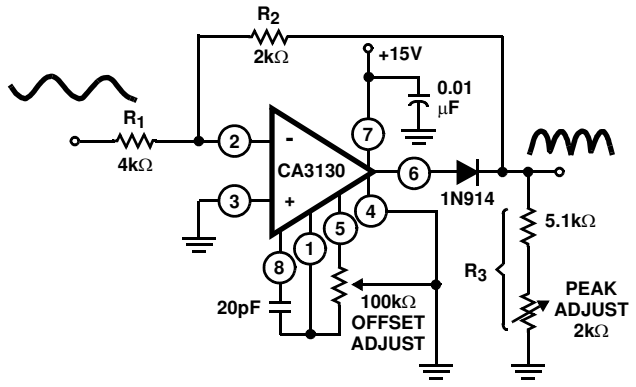
FIGURE 9. SINGLE SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS. (E.G., FOR USE IN SINGLE-SUPPLY D/A CONVERTER; SEE FIGURE 9 IN AN6080)



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6 - 9	±1% ABS

NOTE: All resistances are in ohms.

FIGURE 10. 9-BIT DAC USING CMOS DIGITAL SWITCHES AND CA3130



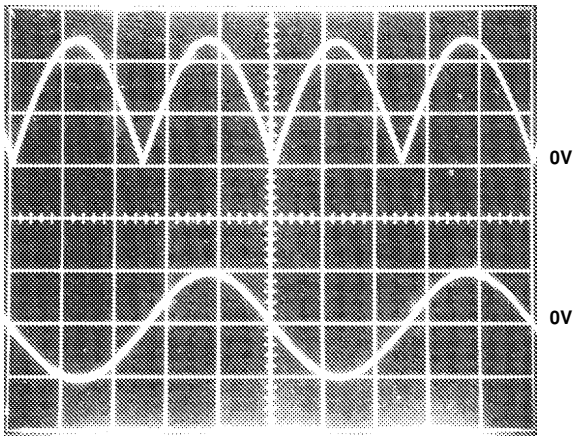
$$\text{Gain} = \frac{R_2}{R_1} = X = \frac{R_3}{R_1 + R_2 + R_3}$$

$$R_3 = R_1\left(\frac{X + X^2}{1 - X}\right) \qquad \text{For } X = 0.5: \frac{2K\Omega}{4k\Omega} = \frac{R_2}{R_1}$$

$$R_3 = 4k\Omega\left(\frac{0.75}{0.5}\right) = 6k\Omega$$

$20V_{P\text{-}P}$ Input: BW(-3dB) = 230kHz, DC Output (Avg) = 3.2V

$1V_{P\text{-}P}$ Input: BW(-3dB) = 130kHz, DC Output (Avg) = 160mV



Top Trace: Output Signal; 2V/Div.
Bottom Trace: Input Signal; 10V/Div.
Time base on both traces: 0.2ms/Div.

FIGURE 11. SINGLE SUPPLY, ABSOLUTE VALUE, IDEAL FULL-WAVE RECTIFIER WITH ASSOCIATED WAVEFORMS

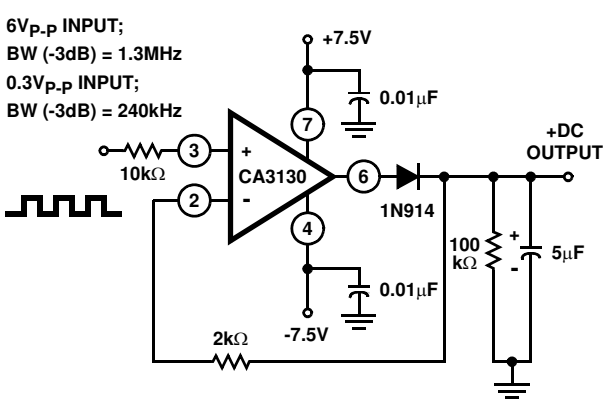


FIGURE 12A. PEAK POSITIVE DETECTOR CIRCUIT

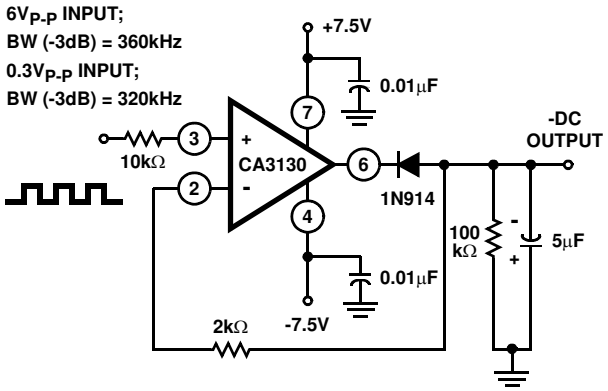
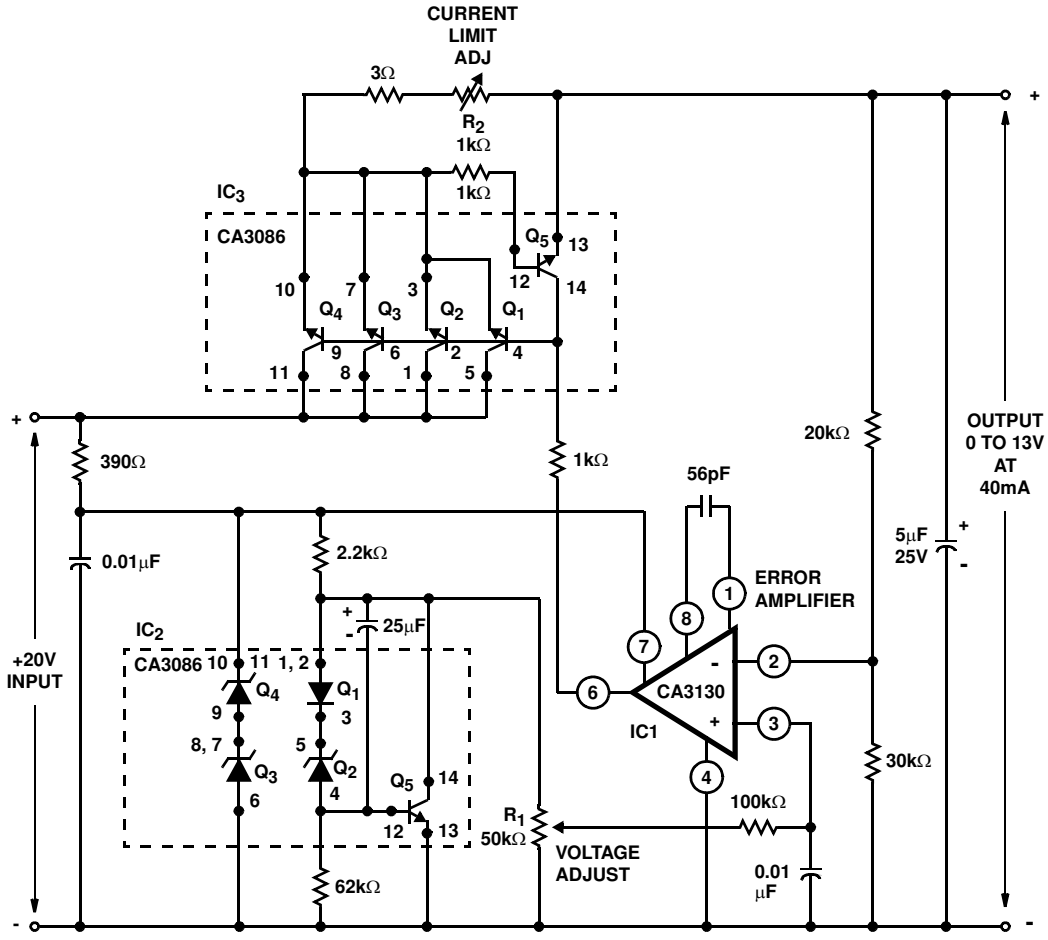


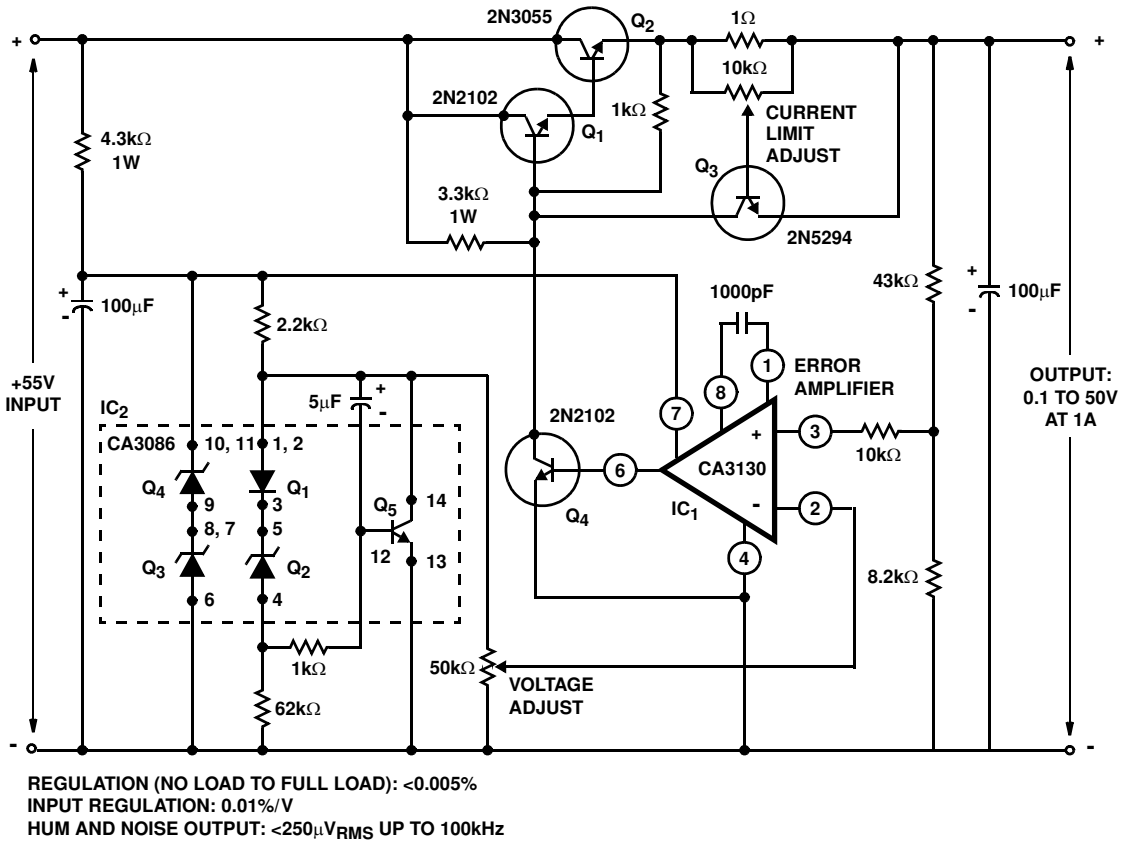
FIGURE 12B. PEAK NEGATIVE DETECTOR CIRCUIT

FIGURE 12. PEAK-DETECTOR CIRCUITS



REGULATION (NO LOAD TO FULL LOAD): <0.01%
INPUT REGULATION: 0.02%/V
HUM AND NOISE OUTPUT: <25μV UP TO 100kHz

FIGURE 13. VOLTAGE REGULATOR CIRCUIT (0V TO 13V AT 40mA)



REGULATION (NO LOAD TO FULL LOAD): <0.005%
INPUT REGULATION: 0.01%/V
HUM AND NOISE OUTPUT: <250μV_{RMS} UP TO 100kHz

FIGURE 14. VOLTAGE REGULATOR CIRCUIT (0.1V TO 50V AT 1A)

Error-Amplifier in Regulated-Power Supplies

The CA3130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero. Figure 13 shows the schematic diagram of a 40mA power supply capable of providing regulated output voltage by continuous adjustment over the range from 0V to 13V. Q_3 and Q_4 in IC_2 (a CA3086 transistor-array IC) function as zeners to provide supply-voltage for the CA3130 comparator (IC_1). Q_1, Q_2, and Q_5 in IC_2 are configured as a low impedance, temperature-compensated source of adjustable reference voltage for the error amplifier. Transistors Q_1, Q_2, Q_3, and Q_4 in IC_3 (another CA3086 transistor-array IC) are connected in parallel as the series-pass element. Transistor Q_5 in IC_3 functions as a current-limiting device by diverting base drive from the series-pass transistors, in accordance with the adjustment of resistor R_2.

Figure 14 contains the schematic diagram of a regulated power-supply capable of providing regulated output voltage by continuous adjustment over the range from 0.1V to 50V and currents up to 1A. The error amplifier (IC_1) and circuitry associated with IC_2 function as previously described, although the output of IC_1 is boosted by a discrete transistor (Q_4) to provide adequate base drive for the Darlington-connected series-pass transistors Q_1, Q_2. Transistor Q_3 functions in the previously described current-limiting circuit.

Multivibrators

The exceptionally high input resistance presented by the CA3130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Figure 15. Resistors R_1 and R_2 are used to bias the CA3130 to the mid-point of the supply-voltage and R_3 is the feedback resistor. The pulse repetition rate is selected by positioning S_1 to the desired position and the rate remains essentially constant when the resistors which determine "on-period" and "off-period" are adjusted.

Function Generator

Figure 16 contains a schematic diagram of a function generator using the CA3130 in the integrator and threshold detector functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1Hz to 100kHz) by means of a single control, R_1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA) (see Note 10), IC_1, operated as a voltage-controlled current-source. The output, I_O, is a current applied directly to the integrating capacitor, C_1, in the feedback loop of the integrator IC_2, using a CA3130, to provide the triangular-wave output. Potentiometer R_2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA3130, IC_3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C_2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

Potentiometer R_3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R_4 to the input of IC_1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

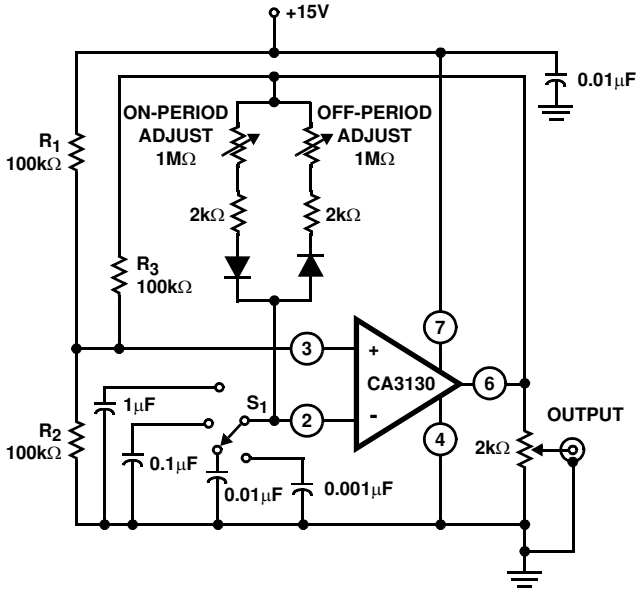
Operation with Output-Stage Power-Booster

The current-sourcing and-sinking capability of the CA3130 output stage is easily supplemented to provide power-boost capability. In the circuit of Figure 17, three CMOS transistor-pairs in a single CA3600E (see Note 12) IC array are shown parallel connected with the output stage in the CA3130. In the Class A mode of CA3600E shown, a typical device consumes 20mA of supply current at 15V operation. This arrangement boosts the current-handling capability of the CA3130 output stage by about 2.5X.

The amplifier circuit in Figure 17 employs feedback to establish a closed-loop gain of 48dB. The typical large-signal bandwidth (-3dB) is 50kHz.

NOTE:

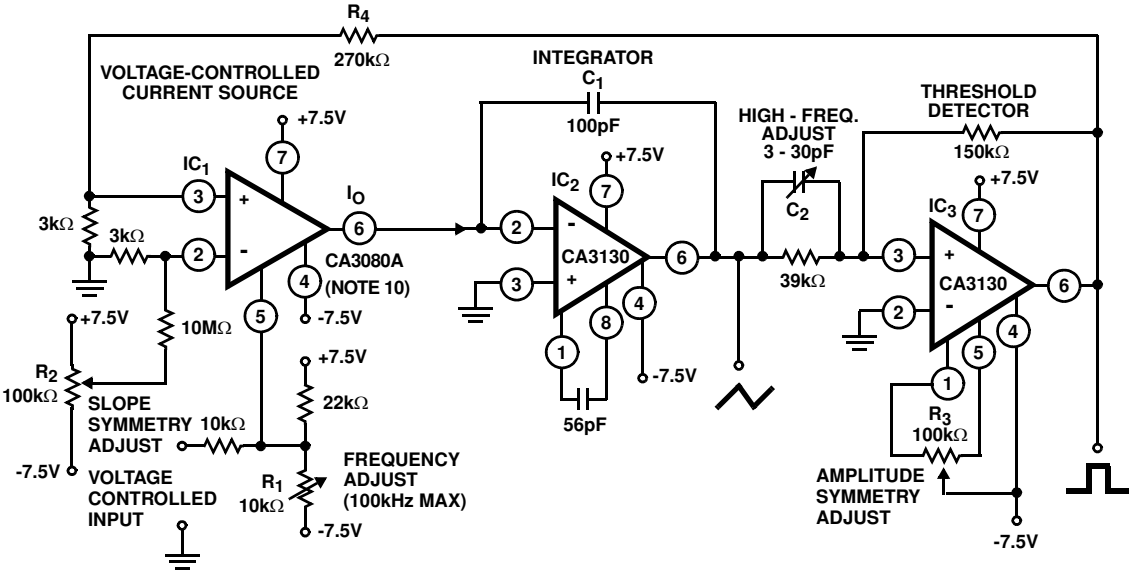
9. See file number 619 for technical information.



FREQUENCY RANGE:

POSITION OF S_1	PULSE PERIOD
0.001μF	4μs to 1ms
0.01μF	40μs to 10ms
0.1μF	0.4ms to 100ms
1μF	4ms to 1s

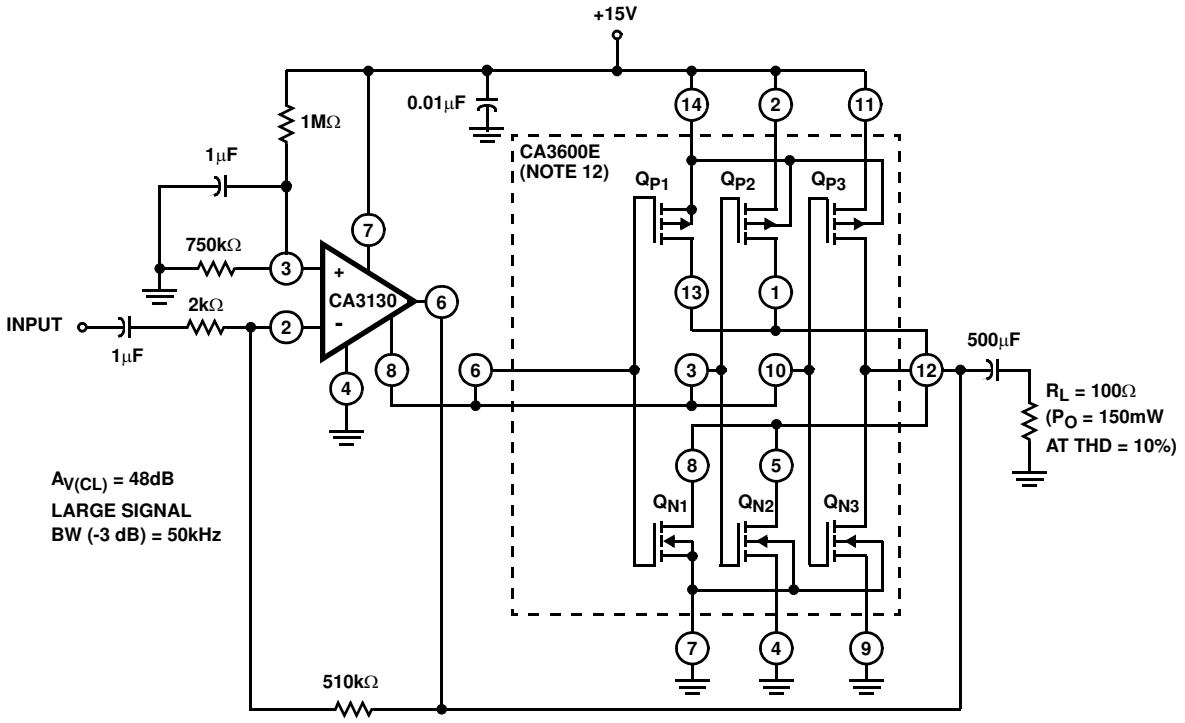
FIGURE 15. PULSE GENERATOR (ASTABLE MULTIVIBRATOR) WITH PROVISIONS FOR INDEPENDENT CONTROL OF "ON" AND "OFF" PERIODS



NOTE:

10. See file number 475 and AN6668 for technical information.

FIGURE 16. FUNCTION GENERATOR (FREQUENCY CAN BE VARIED 1,000,000/1 WITH A SINGLE CONTROL)



NOTES:

11. Transistors Q_{P1}, Q_{P2}, Q_{P3} and Q_{N1}, Q_{N2}, Q_{N3} are parallel connected with Q_8 and Q_{12}, respectively, of the CA3130.
12. See file number 619.

FIGURE 17. CMOS TRANSISTOR ARRAY (CA3600E) CONNECTED AS POWER BOOSTER IN THE OUTPUT STAGE OF THE CA3130

Typical Performance Curves

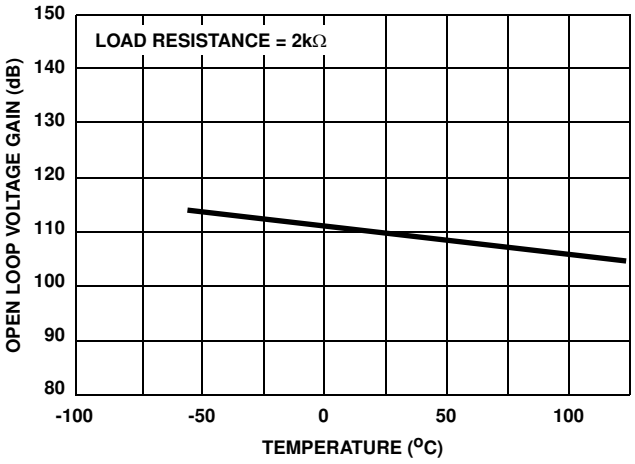
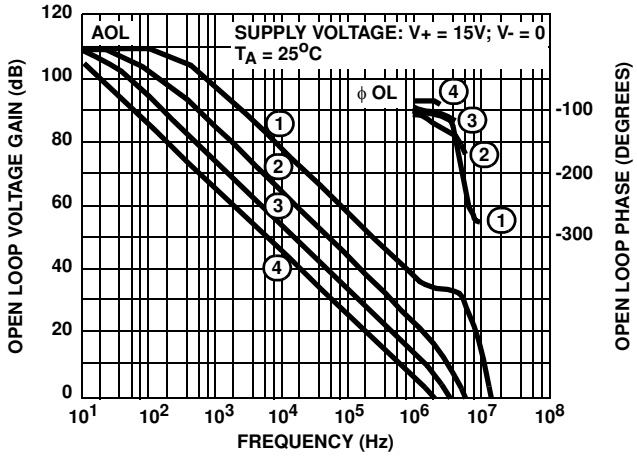


FIGURE 18. OPEN LOOP GAIN vs TEMPERATURE



1 - C_L = 9pF, C_C = 0pF, R_L = ∞
2 - C_L = 30pF, C_C = 15pF, R_L = 2kΩ
3 - C_L = 30pF, C_C = 47pF, R_L = 2kΩ
4 - C_L = 30pF, C_C = 150pF, R_L = 2kΩ

FIGURE 19. OPEN-LOOP RESPONSE

Typical Performance Curves (Continued)

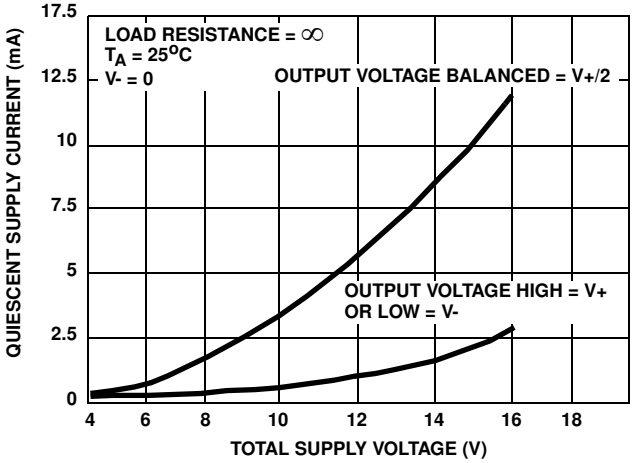


FIGURE 20. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

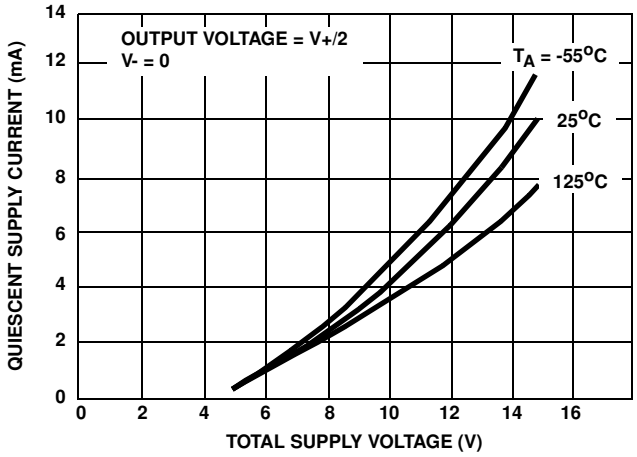


FIGURE 21. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

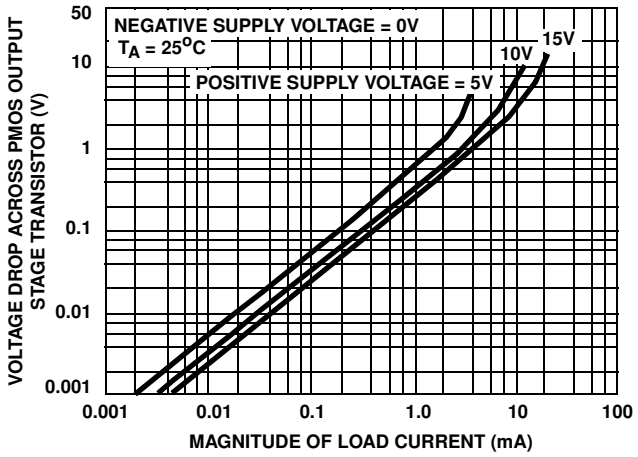


FIGURE 22. VOLTAGE ACROSS PMOS OUTPUT TRANSISTOR (Q_8) vs LOAD CURRENT

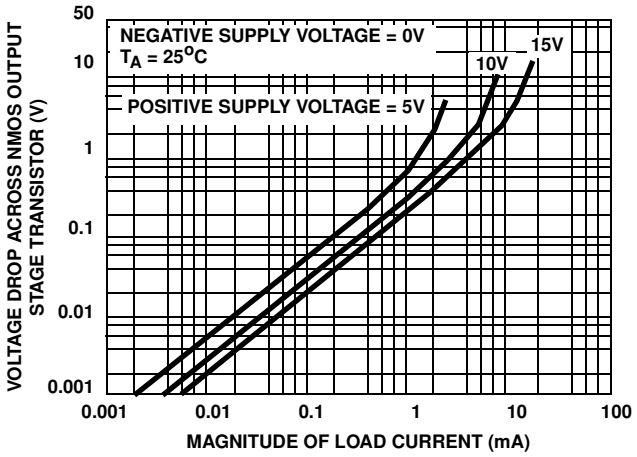
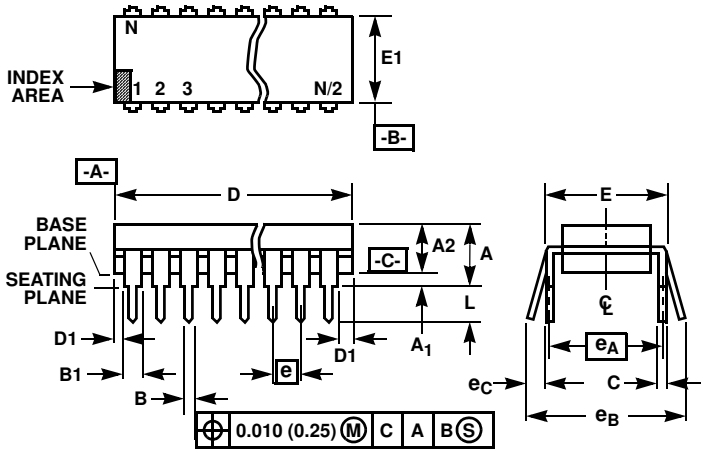


FIGURE 23. VOLTAGE ACROSS NMOS OUTPUT TRANSISTOR (Q_{12}) vs LOAD CURRENT

Dual-In-Line Plastic Packages (PDIP)



NOTES:

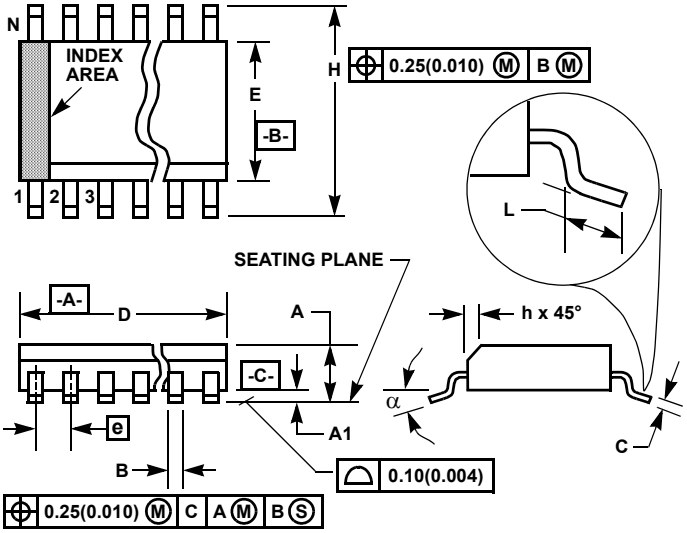
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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