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LDC1612, LDC1614 Multi-Channel 28-Bit Inductance to Digital Converter (LDC) for Inductive Sensing

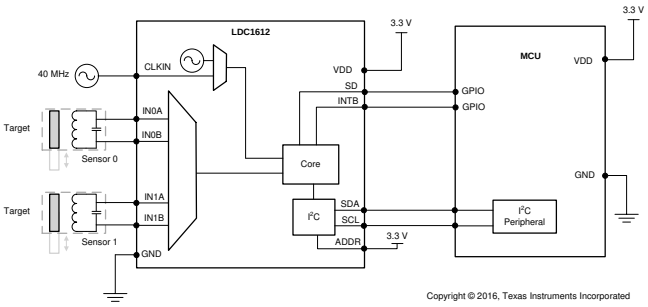
1 Features

- Easy-to-Use – Minimal Configuration Required
- Up to 4 Channels With Matched Sensor Drive
- Multiple Channels Support Environmental and Aging Compensation
- Remote Sensor Position of >20 cm Supports Operation In Harsh Environments
- Pin-Compatible Medium and High-Resolution Options:
  - LDC1312/4: 2/4-ch 12-Bit LDC
  - LDC1612/4: 2/4-ch 28-Bit LDC
- Sensing Range Beyond Two Coil Diameters
- Supports Wide Sensor Frequency Range of 1 kHz to 10 MHz
- Power Consumption:
  - 35 µA Low Power Sleep Mode
  - 200 nA Shutdown Mode
- 2.7 V to 3.6 V Operation
- Multiple Reference Clocking Options:
  - Included Internal Clock For Lower System Cost
  - Support for 40 MHz External Clock For Higher System performance
- Immunity to DC Magnetic Fields and Magnets

2 Applications

- Knobs in Consumer, Appliances, and Automotive
- Buttons in Home Electronics, Wearables, Manufacturing, and Automotive
- Keypads in Manufacturing and Appliances
- Slider Buttons in Consumer Products
- Metal Detection in Industrial and Automotive
- POS and EPOS

Simplified Schematic



3 Description

The LDC1612 and LDC1614 are 2- and 4-channel, 28-bit inductance to digital converters (LDCs) for inductive sensing solutions. With multiple channels and support for remote sensing, the LDC1612 and LDC1614 enable the performance and reliability benefits of inductive sensing to be realized at minimal cost and power. The products are easy to use, only requiring that the sensor frequency be within 1 kHz and 10 MHz to begin sensing. The wide 1 kHz to 10 MHz sensor frequency range also enables use of very small PCB coils, further reducing sensing solution cost and size.

The high resolution channels allow for a much larger sensing range, maintaining good performance beyond two coil diameters. Well-matched channels allow for differential and ratiometric measurements, which enable designers to use one channel to compensate their sensing for environmental and aging conditions such as temperature, humidity, and mechanical drift.

Given their ease of use, low power, and low system cost these products enable designers to greatly improve performance, reliability, and flexibility over existing sensing solutions and to introduce brand new sensing capabilities to products in all markets, especially consumer and industrial applications.

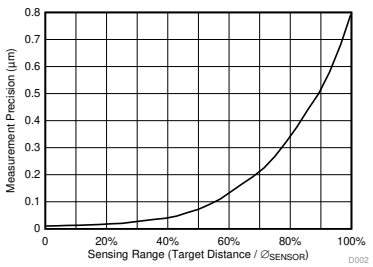
These devices are easily configured via an I2C interface. The two-channel LDC1612 is available in a WSON-12 package and the four-channel LDC1614 is available in a WQFN-16 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LDC1612	WSON-12	4 mm × 4 mm
LDC1614	WQFN-16	4 mm × 4 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Measurement Precision vs. Target Distance



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2014) to Revision A	Page
• Changed ESD values from 1000 to 2000 and from 250 to 750 on both packages.	5
• Added logic levels for ADDR, INTB, and SD pins.	6
• Changed description of clocking architecture for improved clarity.	11
• Changed register names and field names from CHx_NAME and NAME_CHx to NAMEx.	15
• Added instructions on setting registers with both R and R/W fields.	15
• Changed register names from DATA_MSB_CHx to DATAx_MSB; DATA_LSB_CHx register names to DATAx_LSB, and CHx_ERR_YY field names to ERR_YYx.	16
• Changed ERR_AE field description on DATA_MSB_CH0, DATA_MSB_CH1, DATA_MSB_CH2 and DATA_MSB_CH3 tables.	16
• Changed register names from RCOUNT_CHx to RCOUNTx; and CHx_RCOUNT field names to RCOUNTx	20
• Changed register names from OFFSET_CHx to OFFSETx; and CHx_OFFSET field names to OFFSETx	21
• Changed register names from SETTLECOUNT_CHx to SETTLECOUNTx; and CHx_SETTLECOUNT field names to SETTLECOUNTx	22
• Changed Address of SETTLECOUNT0 and SETTLECOUNT1 were not correct on table.	23
• Changed register names from CLOCK_DIVIDERS_CHx to CLOCK_DIVIDERSx; CHx_FIN_DIVIDER field names to FIN_DIVIDERx, and CHx_FREF_DIVIDER field names to FREF_DIVIDERx.	24
• Changed CHx_UNREADCONV field names to UNREADCONVx	26
• Changed register names from DRIVE_CURRENT_CHx to DRIVE_CURRENTx; CHx_IDRIVE field names to IDRIVEx, and CHx_INIT_IDRIVE to INIT_IDRIVEx	31
• Changed Application Information section for clarity, and provided additional information on device configuration and operation.	34
• Changed Equations in the *L-C Resonators* section.	35
• Changed R_P to R_S in Equation	35
• Changed IDRIVEx values	42
• Added instructions for using an oscilloscope to configure sensor drive current	44

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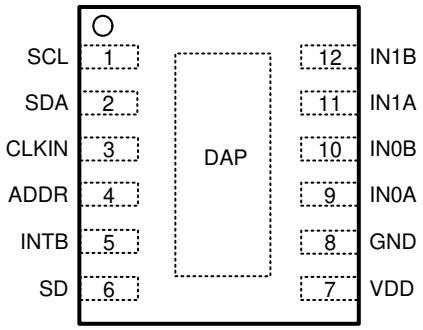
Revision History (continued)

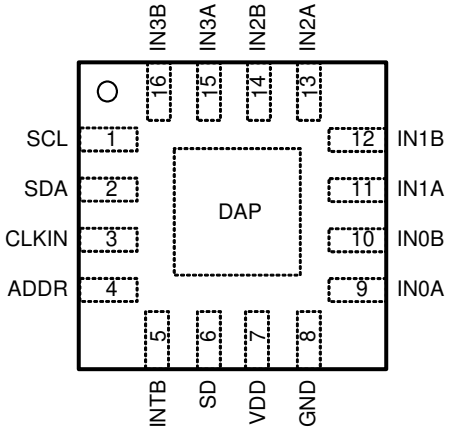
- Changed description of clocking architecture for improved clarity. 45
- Changed description of clocking usage for clarity. 45
- Changed reference frequency limits from < to ≤ 46
- Changed to a ≥ symbol in the *Clock Configuration Requirements* table. 46
- Changed last bullet in the *Design Requirements* section. 49

5 Pin Configuration and Functions

DNT and RGH Packages
Top View



LDC1612 WSON-12



LDC1614 WQFN-16

Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
SCL	1	I	I2C Clock input. Open drain output; requires resistive pullup to logic high level.
SDA	2	I/O	I2C Data input/output. Open drain output; requires resistive pullup to logic high level.
CLKIN	3	I	External Reference Clock input. Tie this pin to GND if internal oscillator is used.
ADDR	4	I	I2C Address selection pin: when ADDR=L, I2C address = 0x2A, when ADDR=H, I2C address = 0x2B. This input must not be allowed to float.
INTB	5	O	Configurable Interrupt output pin. Push-pull output; does not require pullup.
SD	6	I	Shutdown input: set SD = L for normal operation, set SD=H for inactive mode. This input must not be allowed to float.
VDD	7	P	Power Supply
GND	8	G	Ground
IN0A	9	A	External LC sensor 0 connection
IN0B	10	A	External LC sensor 0 connection
IN1A	11	A	External LC sensor 1 connection
IN1B	12	A	External LC sensor 1 connection
IN2A	13	A	External LC sensor 2 connection (LDC1614 only)
IN2B	14	A	External LC sensor 2 connection (LDC1614 only)
IN3A	15	A	External LC sensor 3 connection (LDC1614 only)
IN3B	16	A	External LC sensor 3 connection (LDC1614 only)
DAP (2)	DAP	N/A	Connect to Ground

(1) I = Input, O = Output, P=Power, G=Ground, A=Analog
(2) There is an internal electrical connection between the exposed Die Attach Pad (DAP) and the GND pin of the device. Although the DAP can be left floating, for best performance the DAP should be connected to the same potential as the device's GND pin. Do not use the DAP as the primary ground for the device. The device GND pin must always be connected to ground.

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6 Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
V_{DD}	Supply Voltage Range		5	V
V_i	Voltage on any pin	-0.3	V_{DD}+0.3	V
I_A	Input current on any INx pin	-8	8	mA
I_D	Input current on any Digital pin	-5	5	mA
T_j	Junction Temperature	-55	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
LDC1612 in WSON-12 package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (1)	±750	
LDC1614 in WQFN-16 package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (1)	±750	

(1) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Unless otherwise specified, all limits ensured for T_A = 25°C, V_{DD} = 3.3 V

		MIN	NOM	MAX	UNIT
V_{DD}	Supply Voltage	2.7		3.6	V
T_A	Operating Temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		LDC1612 WSON (DNT) 12 PINS	LDC1614 WQFN (RGH) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50	38	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise specified, all limits ensured for T_A = 25°C, V_{DD} = 3.3 V. See (1)

PARAMETER		TEST CONDITIONS(2)	MIN(3)	TYP(4)	MAX(3)	UNIT
POWER						
V_{DD}	Supply Voltage	T_A = -40°C to +125°C	2.7		3.6	V
I_{DD}	Supply Current (not including sensor current)(5)	f_{CLKIN} = 10 MHz (6)		2.1		mA
I_{DDSL}	Sleep Mode Supply Current(5)	SLEEP_MODE_EN = b1		35	60	µA
I_{SD}	Shutdown Mode Supply Current(5)	SD = V_{DD}		0.2	1	µA
SENSOR						
$I_{SENSORMAX}$	Sensor Maximum Current drive	HIGH_CURRENT_DRV = b0 DRIVE_CURRENTx = 0xF800		1.5		mA
R_P	Sensor R_P		1		100	kΩ
$IHD_{SENSORMAX}$	High current sensor drive mode: Sensor Maximum Current	HIGH_CURRENT_DRV = b1 DRIVE_CURRENT0 = 0xF800 Channel 0 only		6		mA
$R_{P_HD_MIN}$	Minimum sensor R_P			250		Ω
f_{SENSOR}	Sensor Resonance Frequency	T_A = -40°C to +125°C	0.001		10	MHz
$V_{SENSORMAX}$	Maximum oscillation amplitude (peak)			1.8		V
N_{BITS}	Number of bits				28	bits
f_{CS}	Maximum Channel Sample Rate	single active channel continuous conversion, SCL=400 kHz			4.08	kSPS
C_{IN}	Sensor Pin input capacitance			4		pF
DIGITAL PIN LEVELS						
V_{IL}	Low voltage threshold (ADDR and SD)				0.3*V_{DD}	V
V_{IH}	High voltage threshold (ADDR and SD)		0.7*V_{DD}			V
V_{OL}	INTB low voltage output level	3mA sink current			0.4	V
V_{OH}	INTB high voltage output level		2.4			V
REFERENCE CLOCK						
f_{CLKIN}	External Reference Clock Input Frequency (CLKIN)	T_A = -40°C to +125°C	2		40	MHz
$CLKIN_{DUTY_MIN}$	External Reference Clock minimum acceptable duty cycle (CLKIN)			40%		
$CLKIN_{DUTY_MAX}$	External Reference Clock maximum acceptable duty cycle (CLKIN)			60%		
V_{CLKIN_LO}	CLKIN low voltage threshold				0.3*V_{DD}	V
V_{CLKIN_HI}	CLKIN high voltage threshold		0.7*V_{DD}			V

(1) Electrical Characteristics Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Register values are represented as either binary (b is the prefix to the digits), or hexadecimal (0x is the prefix to the digits). Decimal values have no prefix.
(3) Limits are ensured by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(5) I^2C read/write communication and pull-up resistors current through SCL, SDA not included.
(6) Sensor inductor: 2 layer, 32 turns/layer, 14 mm diameter, PCB inductor with L=19.4 µH, R_P=5.7 kΩ at 2 MHz Sensor capacitor: 330 pF 1% COG/NP0 Target: Aluminum, 1.5 mm thickness Channel = Channel 0 (continuous mode) f_{CLKIN} = 40 MHz, FIN_DIVIDER0 = b0000, FREF_DIVIDER0 = 0x0001, RCOUNT0 = 0xFFFF, SETTLECOUNT0 = 0x0100, RP_OVERRIDE = b1, AUTO_AMP_DIS = b1, DRIVE_CURRENT0 = 0x9800

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Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_A = 25°C, V_{DD} = 3.3 V. See [1]

PARAMETER		TEST CONDITIONS[2]	MIN[3]	TYP[4]	MAX[3]	UNIT
f_{INTCLK}	Internal Reference Clock Frequency range		35	43.4	55	MHz
$T_{Cf_int_\mu}$	Internal Reference Clock Temperature Coefficient mean			-13		ppm/°C
TIMING CHARACTERISTICS						
t_{WAKEUP}	Wake-up Time from SD high-low transition to I2C readback				2	ms
$t_{WD\text{-}TIMEOUT}$	Sensor recovery time (after watchdog timeout)			5.2		ms

6.6 Switching Characteristics - I2C

Unless otherwise specified, all limits ensured for T_A = 25°C, VDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE LEVELS						
V_{IH}	Input High Voltage		$0.7^{x}V_{DD}$			V
V_{IL}	Input Low Voltage				$0.3^{x}V_{DD}$	V
V_{OL}	Output Low Voltage (3mA sink current)				0.4	V
HYS	Hysteresis			$0.1^{x}V_{DD}$		V
I2C TIMING CHARACTERISTICS						
f_{SCL}	Clock Frequency		10		400	kHz
t_{LOW}	Clock Low Time		1.3			µs
t_{HIGH}	Clock High Time		0.6			µs
$t_{HD;STA}$	Hold Time (repeated) START condition	After this period, the first clock pulse is generated	0.6			µs
$t_{SU;STA}$	Set-up time for a repeated START condition		0.6			µs
$t_{HD;DAT}$	Data hold time		0			µs
$t_{SU;DAT}$	Data setup time		100			ns
$t_{SU;STO}$	Set-up time for STOP condition		0.6			µs
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
$t_{VD;DAT}$	Data valid time				0.9	µs
$t_{VD;ACK}$	Data valid acknowledge time				0.9	µs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter[1]				50	ns

(1) This parameter is specified by design and/or characterization and is not tested in production.

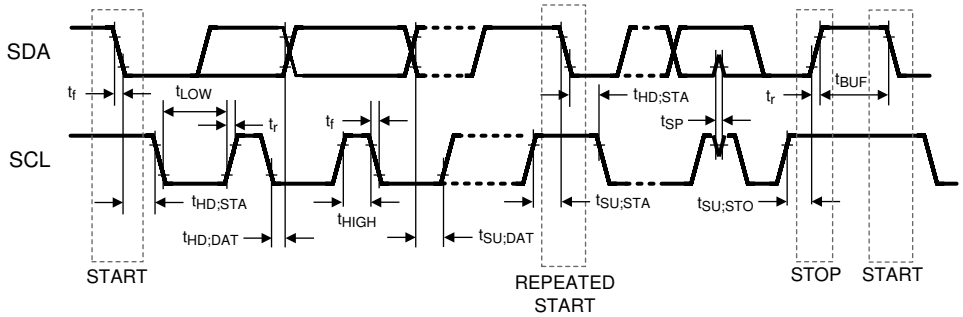
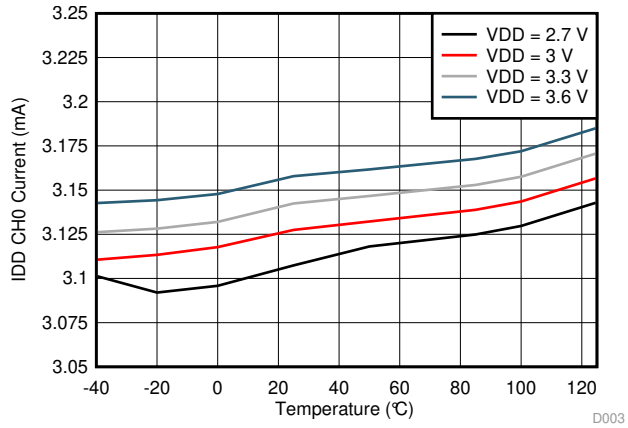


Figure 1. I2C Timing

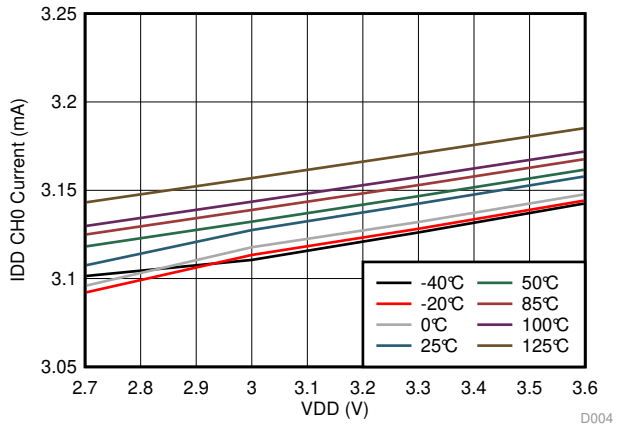
6.7 Typical Characteristics

Common test conditions (unless specified otherwise): Sensor inductor: 2 layer, 32 turns/layer, 14 mm diameter, PCB inductor with L=19.4 µH, R_P=5.7 kΩ at 2 MHz; Sensor capacitor: 330 pF 1% COG/NP0; Target: Aluminum, 1.5 mm thickness; Channel = Channel 0 (continuous mode); f_{CLKIN} = 40 MHz, FIN_DIVIDER0 = 0x1, FREF_DIVIDER0 = 0x001, RCOUNT0 = 0xFFFF, SETTLECOUNT0 = 0x0100, RP_OVERRIDE = 1, AUTO_AMP_DIS = 1, DRIVE_CURRENT0 = 0x9800



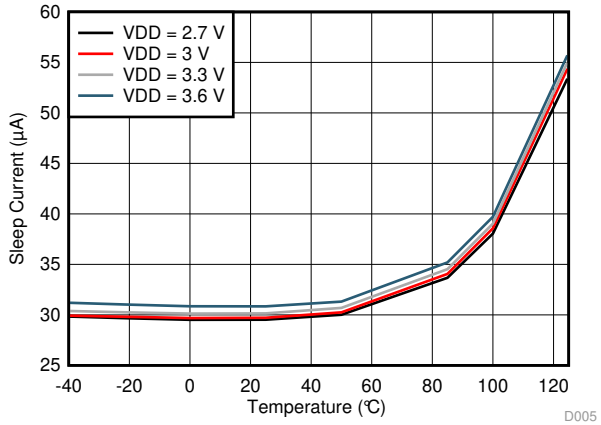
Includes 1.57 mA sensor coil current
-40°C to +125°C

Figure 2. Active Mode I_{DD} vs. Temperature



Includes 1.57 mA sensor coil current

Figure 3. Active Mode I_{DD} vs. V_{DD}



-40°C to +125°C

Figure 4. Sleep Mode I_{DD} vs. Temperature

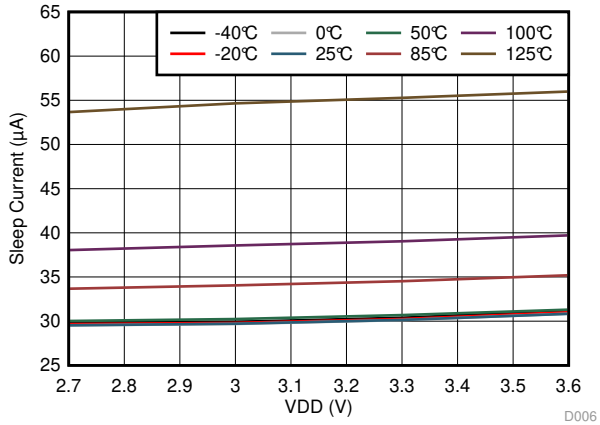
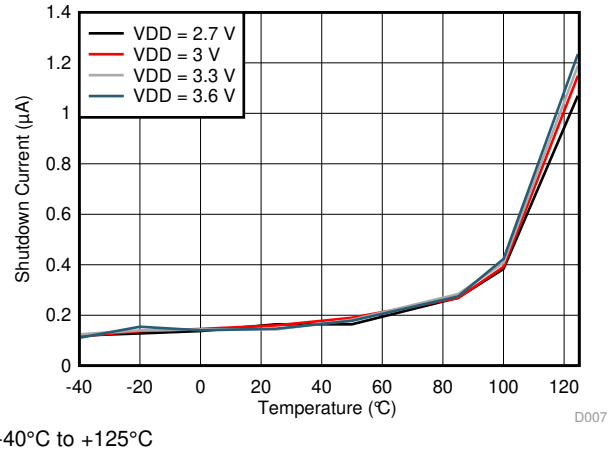


Figure 5. Sleep Mode I_{DD} vs. V_{DD}



-40°C to +125°C

Figure 6. Shutdown Mode I_{DD} vs. Temperature

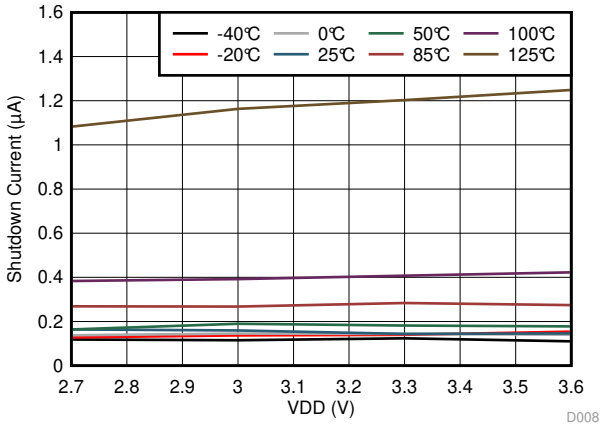


Figure 7. Shutdown Mode I_{DD} vs. V_{DD}

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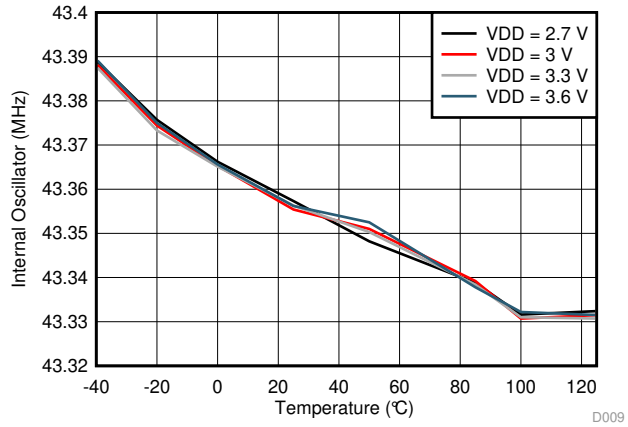
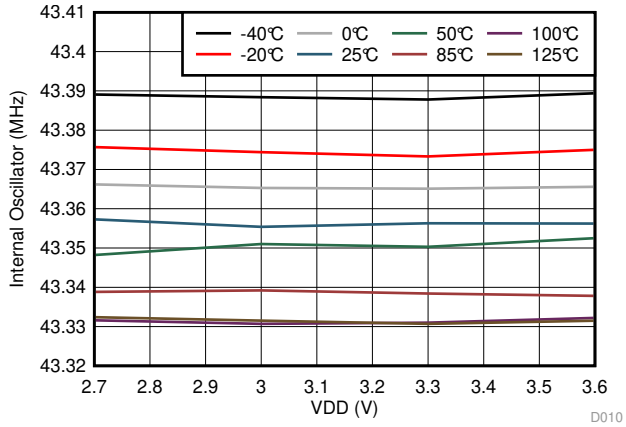
Typical Characteristics (continued)

Common test conditions (unless specified otherwise): Sensor inductor: 2 layer, 32 turns/layer, 14 mm diameter, PCB inductor with L=19.4 µH, R_P=5.7 kΩ at 2 MHz; Sensor capacitor: 330 pF 1% COG/NP0; Target: Aluminum, 1.5 mm thickness; Channel = Channel 0 (continuous mode); f_{CLKIN} = 40 MHz, FIN_DIVIDER0 = 0x1, FREF_DIVIDER0 = 0x001, RCOUNT0 = 0xFFFF, SETTLECOUNT0 = 0x0100, RP_OVERRIDE = 1, AUTO_AMP_DIS = 1, DRIVE_CURRENT0 = 0x9800



-40°C to +125°C

Figure 8. Internal Oscillator Frequency vs. Temperature



Data based on 1 unit

Figure 9. Internal Oscillator Frequency vs. V_{DD}

7 Detailed Description

7.1 Overview

The LDC1612/LDC1614 is an inductance-to-digital converter (LDC) that measures the oscillation frequency of multiple LC resonators. The device outputs a digital value that is proportional to frequency, with 28 bits of measurement resolution. This frequency measurement can be converted to an equivalent inductance, or mapped to the movement of an conductive object. The LDC1612/LDC1614 supports a wide range of inductance and capacitor combinations with oscillation frequencies varying from 1 kHz to 10 MHz with equivalent parallel resistances as low as 1.0 kΩ. The device includes a stable internal reference to reduce overall system cost, while also providing the option to drive a clean external oscillator for improved measurement noise. The conversion time of the LDC1612/LDC1614 is configurable per channel, where longer conversion times provide higher effective resolution.

The LDC1612/LDC1614 is configured through a 400-kbit/s I2C bus and includes the ADDR input pin to select an address. The power supply of the device ranges from 2.7 V to 3.6 V. The only external components necessary for operation are the supply bypassing capacitors and I2C pull-ups.

7.2 Functional Block Diagram

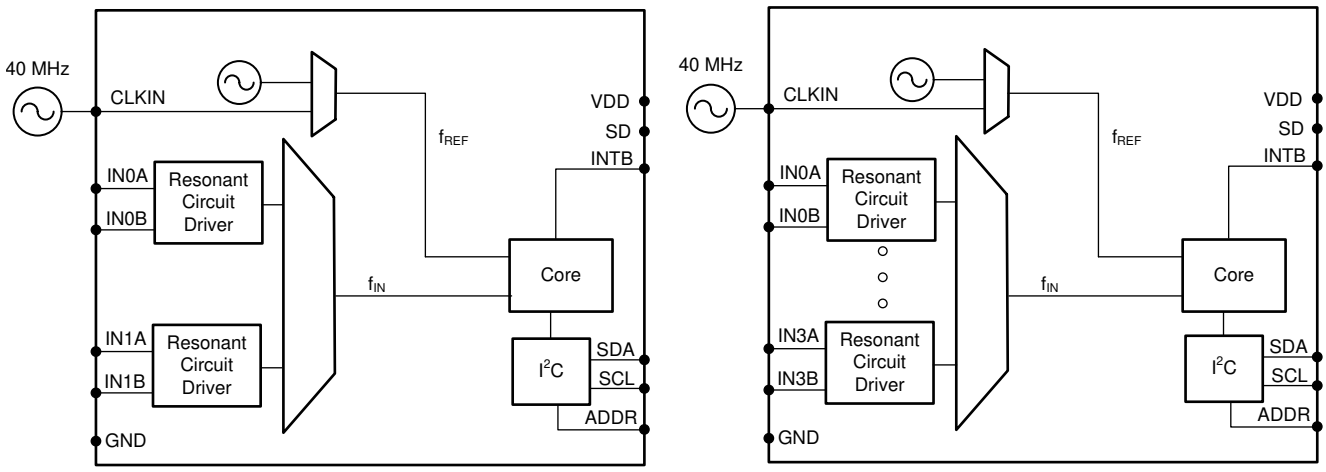


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Figure 10. Block Diagrams for the LDC1612 (Left) and LDC1614 (Right)

The LDC1612/LDC1614 is composed of front-end resonant circuit drivers, followed by a multiplexer that sequences through the active channels, connecting them to the core that measures and digitizes the sensor frequency (f_{SENSOR}). The core uses a reference frequency (f_{REF}) to measure the sensor frequency. f_{REF} is derived from either the internal reference clock (oscillator), or an externally supplied clock. The digitized output for each channel is proportional to the ratio of f_{SENSOR}/f_{REF}. The I2C interface is used to support device configuration and to transmit the digitized frequency values to a host processor. The LDC can be placed in an inactive shutdown mode to reduce current consumption by setting the SD pin to V_{DD}. The INTB pin may be configured to notify the host of changes in system status.

7.3 Feature Description

7.3.1 Multi-Channel and Single Channel Operation

The LDC1612/LDC1614 provides flexibility in channel sampling. It can continuously convert on any available single channel or automatically sequence conversions across multiple channels. When operated in multi-channel mode, the LDC sequentially samples the selected channels. In single channel mode, the LDC continuously samples only the selected channel.

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Feature Description (continued)

At the end of each conversion in single channel mode, or after converting all selected channels when in multi-channel mode, the LDC1612/LDC1614 can be configured to assert the INTB pin to indicate completion of the conversion.

Refer to *Multi-Channel and Single Channel Operation* for details on the LDC1612/LDC1614 channel functionality and configuration.

7.3.2 Adjustable Conversion Time

The LDC1612/LDC1614 conversion provides a tradeoff between measurement resolution and conversion interval. Longer conversion intervals have higher measurement resolution. The conversion interval can be configured from 3.2 µs to >26.2 ms with 16 bits of resolution. Note that it is possible to configure the conversion interval to be shorter than the time required to read back the DATAx registers. The LDC1612/LDC1614 supports per-channel adjustment of the conversion interval by setting the RCOUNTx register.

Refer to *Sensor Conversion Time* for details on the LDC1612/LDC1614 configuration and details on the setting conversion interval.

7.3.3 Sensor Startup and Glitch Configuration

For minimum noise, the sensor measurement should be performed after the sensor amplitude has stabilized. The LDC1612/LDC1614 provides an adjustable sensor startup timing per channel. The timing can be varied from 1.2 µs to >26.2 ms by setting the SETTLECOUNTx register. Sensors with lower resonant frequencies or higher Qs may require additional time to stabilize.

Refer to *Settling Time* for details on the LDC1612/LDC1614 configuration and details on the setting conversion interval.

The LDC1612/LDC1614 can be configured with a faster sensor activation, or to use a lower current sensor activation. Refer to *Sensor Activation* for details on this capability.

The LDC1612/LDC1614 provides an internal filter to attenuate interference from external noise sources. Refer to *Input Deglitch Filter* for information on configuration on the deglitch filter.

7.3.4 Reference Clock

Optimum LDC1612/LDC1614 performance requires a clean reference clock. This reference frequency is equivalent to the reference voltage of an Analog-to-Digital converter. The LDC1612/LDC1614 provide an internal reference oscillator with a typical frequency of 43 MHz. This internal oscillator has good stability, with a typical temperature coefficient of -13 ppm/°C. For applications requiring higher resolution or improved performance across temperature, an external reference frequency can be applied to the CLKIN input.

The LDC1612/LDC1614 provide digital dividers for the f_{CLK} and the sensor inputs to adjust the effective frequency measured by the LDC core. For most systems, the maximum permitted reference frequency provides the best performance. The dividers provide flexibility in system design so that the full range of sensor frequencies can be supported with a wide range of f_{CLK}. Each channel has a dedicated divider configuration.

Refer to *Reference Clock* for details on clocking requirements, configuration, and divider setup.

7.3.5 Sensor Current Drive Control

The lossy characteristic of the sensors used for inductive sensing require injection of energy to maintain a constant sensor amplitude. The LDC1612/LDC1614 provides this energy by driving an AC current matching the sensor resonant frequency across the LC sensor. To achieve optimum performance, it is necessary to set the current drive so that the sensor amplitude is within the range of 1.2 V_P to 1.8 V_P. Each channel current drive is set independently between 16 µA and 1.6 mA by setting the corresponding IDRIVEx register field. The LDC1612/LDC1614 can also automatically determine the appropriate sensor current drive, and even dynamically adjust the sensor current by use of the RP_OVERRIDE_EN function.

Refer to *Sensor Current Drive Configuration* for detailed information on configuration of the sensor drive.

Feature Description (continued)

7.3.6 Device Status Monitoring

The LDC1612/LDC1614 can monitor attached sensors and can report on device status and sensor status via the I2C interface. Reported conditions include:

- Sensor Amplitude outside of optimum range
- Sensor unable to oscillate
- New conversion data available
- Conversion errors

Use of this monitoring functionality can alert the system MCU of unexpected conditions such as sensor damage. Refer to *Device Status Registers* for more information.

7.4 Device Functional Modes

7.4.1 Startup Mode

When the LDC powers up, it enters into Sleep Mode and will wait for configuration. Once the device is configured, exit Sleep Mode and begin conversions by setting CONFIG.SLEEP_MODE_EN to b0.

It is recommended to configure the LDC while in Sleep Mode. If a setting on the LDC needs to be changed, return the device to Sleep Mode, change the appropriate register, and then exit Sleep Mode.

7.4.2 Sleep Mode (Configuration Mode)

Sleep Mode is entered by setting the CONFIG.SLEEP_MODE_EN register field to 1. While in this mode, the device configuration is retained, but the device does not perform conversions. To enter Normal mode to perform conversions, set the CONFIG.SLEEP_MODE_EN register field to 0. After setting CONFIG.SLEEP_MODE_EN to b0, sensor activation for the first conversion will begin after $16{,}384 \div f_{INT}$ elapses. Refer to *Clocking Architecture* for more information on the device timing.

While in Sleep Mode the I2C interface is functional so that register reads and writes can be performed. Entering Sleep Mode will clear all conversion results, any error conditions, and de-assert the INTB pin.

For applications which do not require continuous conversions, returning the device to Sleep mode after completion and readback of the desired number of conversions can provide power consumption savings. Refer to the TI Applications Note *Power Reduction Techniques for the LDC131x/161x for Inductive Sensing* for more information.

7.4.3 Normal (Conversion) Mode

When operating in the normal (conversion) mode, the LDC is repeatedly sampling the frequency of the sensor(s) and generating sample outputs for the active channel(s) based on the device configuration.

7.4.4 Shutdown Mode

When the SD pin is set to high, the LDC will enter Shutdown Mode. Shutdown Mode is the lowest power state. To exit Shutdown Mode and enter Sleep Mode, set the SD pin to low. Entering Shutdown Mode will return all registers to their default state.

While in Shutdown Mode, no conversions are performed. In addition, entering Shutdown Mode will clear any error condition and de-assert the INTB pin (when de-asserted, INTB will be actively driven high). While the device is in Shutdown Mode, is not possible to read to or write from the device via the I2C interface.

It is permitted to change the ADDR pin setting while in Shutdown Mode.

7.4.4.1 Reset

The device can be reset by writing to RESET_DEV.RESET_DEV. Any active conversion will stop and all registers will return to their default values. This register bit will always return 0b when read.

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7.5 Programming

The LDC1612/4 device uses an I2C interface to access control and data registers. The recommended configuration procedure is to put the device into Sleep Mode, set the appropriate registers, and then enter Normal Mode. Conversion results must be read while the device is in Normal Mode. Setting the device into Shutdown mode will reset the device configuration.

7.5.1 I2C Interface Specifications

The LDC1612/4 use I2C for register access with a maximum speed of 400 kbit/s. The device registers are 16 bits wide, and so a repeated start is used to access the 2nd byte of data. This sequence follows the standard I2C 7bit slave address followed by an 8 bit pointer register byte to set the register address. Refer to Figure 11 and Figure 12 for proper protocol diagrams. The device does not use I2C clock stretching.

When the ADDR pin is set low, the device I2C address is 0x2A; when the ADDR pin is set high, the I2C address is 0x2B. The ADDR pin setting can be changed while the device is in Shutdown Mode to select the alternate I2C address.

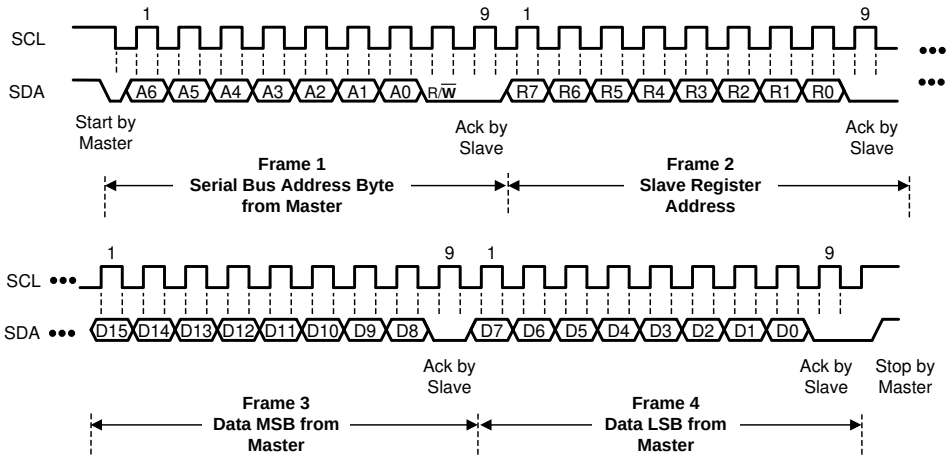

Figure 11. I2C Write Register Sequence

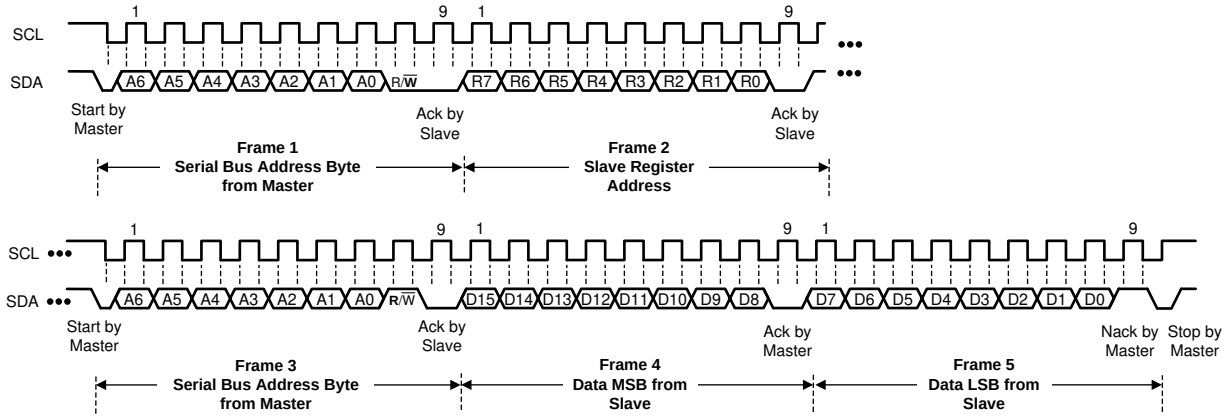

Figure 12. I2C Read Register Sequence

Programming (continued)

7.5.2 Pulses on I2C

The I2C interface of the LDC is designed to operate with the standard I2C transactions detailed in the I2C specification; however it is not suitable for use in an I2C system which supports early termination of transactions. A STOP condition or other early termination occurring before the normal end of a transaction (ACK) is not supported and may corrupt that transaction and/or the following transaction. The device is also sensitive to any (extraneous) pulse on SDA during the SCL low period of the first bit position of the i2c_address byte. To ensure proper LDC operation, the master device should not transmit this type of waveform. An example of an unsupported I2C waveform is shown in Figure 13. Any such pulses should not have a duration which exceeds the device t_{SP} specification.

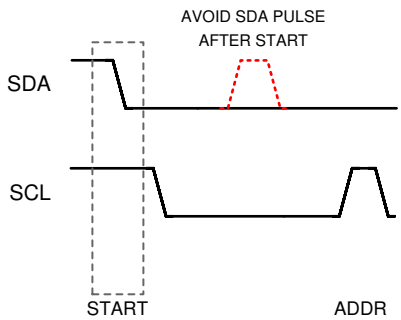

Figure 13. Example of SDA Pulse Between I2C START and ADDR Which Must be Avoided by the I2C Master

7.5.3 Multi Register Data Readback

The LDC1612/LDC1614 conversion data spans 2 registers. To avoid multi-conversion data corruption, the device uses an internal shadow register to hold conversion results for each channel. When a conversion completes, the corresponding internal shadow register is updated with the new conversion result. When the DATAx_MSB register is read, the contents of both the DATAx_MSB and DATAx_LSB registers are updated with the new conversion data.

Therefore, to correctly retrieve the conversion results for a given channel, the proper sequence is to first read the DATAx_MSB register, and then read the DATAx_LSB register.

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7.6 Register Maps

7.6.1 Register List

Fields indicated with **Reserved** must be written only with indicated value, otherwise improper device operation may occur. The R/W column indicates the Read-Write status of the corresponding field. A 'R/W' entry indicates read and write capability, a 'R' indicates read-only, and a 'W' indicates write-only.

For registers with R and R/W fields, write the reset value to the field when setting the R/W fields.

Figure 14. Register List

ADDRESS	NAME	DEFAULT VALUE	DESCRIPTION
0x00	DATA0_MSB	0x0000	Channel 0 MSB Conversion Result and Error Status
0x01	DATA0_LSB	0x0000	Channel 0 LSB Conversion Result. Must be read after Register address 0x00.
0x02	DATA1_MSB	0x0000	Channel 1 MSB Conversion Result and Error Status.
0x03	DATA1_LSB	0x0000	Channel 1 LSB Conversion Result. Must be read after Register address 0x02.
0x04	DATA2_MSB	0x0000	Channel 2 MSB Conversion Result and Error Status. **(LDC1614 only)**
0x05	DATA2_LSB	0x0000	Channel 2 LSB Conversion Result. Must be read after Register address 0x04.**(LDC1614 only)**
0x06	DATA3_MSB	0x0000	Channel 3 MSB Conversion Result and Error Status. **(LDC1614 only)**
0x07	DATA3_LSB	0x0000	Channel 3 LSB Conversion Result. Must be read after Register address 0x06. **(LDC1614 only)**
0x08	RCOUNT0	0x0080	Reference Count setting for Channel 0
0x09	RCOUNT1	0x0080	Reference Count setting for Channel 1
0x0A	RCOUNT2	0x0080	Reference Count setting for Channel 2. **(LDC1614 only)**
0x0B	RCOUNT3	0x0080	Reference Count setting for Channel 3.**(LDC1614 only)**
0x0C	OFFSET0	0x0000	Offset value for Channel 0
0x0D	OFFSET1	0x0000	Offset value for Channel 1
0x0E	OFFSET2	0x0000	Offset value for Channel 2 **(LDC1614 only)**
0x0F	OFFSET3	0x0000	Offset value for Channel 3 **(LDC1614 only)**
0x10	SETTLECOUNT0	0x0000	Channel 0 Settling Reference Count
0x11	SETTLECOUNT1	0x0000	Channel 1 Settling Reference Count
0x12	SETTLECOUNT2	0x0000	Channel 2 Settling Reference Count **(LDC1614 only)**
0x13	SETTLECOUNT3	0x0000	Channel 3 Settling Reference Count **(LDC1614 only)**
0x14	CLOCK_DIVIDERS0	0x0000	Reference and Sensor Divider settings for Channel 0
0x15	CLOCK_DIVIDERS1	0x0000	Reference and Sensor Divider settings for Channel 1
0x16	CLOCK_DIVIDERS2	0x0000	Reference and Sensor Divider settings for Channel 2 **(LDC1614 only)**
0x17	CLOCK_DIVIDERS3	0x0000	Reference and Sensor Divider settings for Channel 3 **(LDC1614 only)**
0x18	STATUS	0x0000	Device Status Report
0x19	ERROR_CONFIG	0x0000	Error Reporting Configuration
0x1A	CONFIG	0x2801	Conversion Configuration
0x1B	MUX_CONFIG	0x020F	Channel Multiplexing Configuration
0x1C	RESET_DEV	0x0000	Reset Device
0x1E	DRIVE_CURRENT0	0x0000	Channel 0 sensor current drive configuration
0x1F	DRIVE_CURRENT1	0x0000	Channel 1 sensor current drive configuration
0x20	DRIVE_CURRENT2	0x0000	Channel 2 sensor current drive configuration **(LDC1614 only)**
0x21	DRIVE_CURRENT3	0x0000	Channel 3 sensor current drive configuration **(LDC1614 only)**
0x7E	MANUFACTURER_ID	0x5449	Manufacturer ID
0x7F	DEVICE_ID	0x3055	Device ID

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7.6.2 Address 0x00, DATA0_MSB

Figure 15. Address 0x00, DATA0_MSB

15	14	13	12	11	10	9	8
ERR_UR0	ERR_OR0	ERR_WD0	ERR_AE0	DATA0 [27:16]			
7	6	5	4	3	2	1	0
DATA [27:16]							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1. Address 0x00, DATA0_MSB Field Descriptions

Bit	Field	Type	Reset	Description
15	ERR_UR0	R	0	**Channel 0 Conversion Under-range Error Flag** Cleared by reading the register
14	ERR_OR0	R	0	**Channel 0 Conversion Over-range Error Flag.** Cleared by reading the register
13	ERR_WD0	R	0	**Channel 0 Conversion Watchdog Timeout Error Flag** Cleared by reading the register
12	ERR_AE0	R	0	**Channel 0 Conversion Amplitude Error Flag** Cleared by reading the register.
11:0	DATA0[27:16]	R	0000 0000 0000	**Channel 0 MSB Conversion Result (MSB)**

7.6.3 Address 0x01, DATA0_LSB

Figure 16. Address 0x01, DATA0_LSB

15	14	13	12	11	10	9	8
DATA0 [15:0]							
7	6	5	4	3	2	1	0
DATA0 15:0]							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 2. Address 0x01 DATA0_LSB Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DATA0[15:0]	R	0x0000	**Channel 0 LSB Conversion Result (LSB)** This register must be read after DATA0_MSB to ensure data coherency.

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7.6.4 Address 0x02, DATA1_MSB

Figure 17. Address 0x02, DATA1_MSB

15	14	13	12	11	10	9	8
ERR_UR1	ERR_OR1	ERR_WD1	ERR_AE1	DATA1[27:16]			
7	6	5	4	3	2	1	0
DATA1[27:16]							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3. Address 0x02, DATA1_MSB Field Descriptions

Bit	Field	Type	Reset	Description
15	ERR_UR1	R	0	**Channel 1 Conversion Under-range Error Flag** Cleared by reading the bit.
14	ERR_OR1	R	0	**Channel 1 Conversion Over-range Error Flag** Cleared by reading the bit.
13	ERR_WD1	R	0	**Channel 1 Conversion Watchdog Timeout Error Flag** Cleared by reading the bit.
12	ERR_AE1	R	0	**Channel 1 Conversion Amplitude Error Flag** Cleared by reading the bit.
11:0	DATA1[27:16]	R	0x000	**Channel 1 MSB Conversion Result (MSB)**

7.6.5 Address 0x03, DATA1_LSB

Figure 18. Address 0x03, DATA1_LSB

15	14	13	12	11	10	9	8
DATA1 [15:0]							
7	6	5	4	3	2	1	0
DATA1 [15:0]							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. Address 0x03, DATA1_LSB Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DATA1[15:0]	R	0x0000	**Channel 1 LSB Conversion Result (LSB)** This register must be read after DATA1_MSB to ensure data coherency.

7.6.6 Address 0x04, DATA2_MSB (LDC1614 only)

Figure 19. Address 0x04, DATA2_MSB

15	14	13	12	11	10	9	8
ERR_UR2	ERR_OR2	ERR_WD2	ERR_AE2	DATA2 [27:16]			
7	6	5	4	3	2	1	0
DATA2 [27:16]							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. Address 0x04, DATA2_MSB Field Descriptions

Bit	Field	Type	Reset	Description
15	ERR_UR2	R	0	**Channel 2 Conversion Under-range Error Flag** Cleared by reading the bit.
14	ERR_OR2	R	0	**Channel 2 Conversion Over-range Error Flag** Cleared by reading the bit.
13	ERR_WD2	R	0	**Channel 2 Conversion Watchdog Timeout Error Flag** Cleared by reading the bit.
12	ERR_AE2	R	0	**Channel 2 Conversion Amplitude Error Flag** Cleared by reading the bit.
11:0	DATA2[27:16]	R	0x000	**Channel 2 MSB Conversion Result (MSB)**

7.6.7 Address 0x05, DATA2_LSB (LDC1614 only)

Figure 20. Address 0x05, DATA2_LSB

15	14	13	12	11	10	9	8
DATA2 [15:0]							
7	6	5	4	3	2	1	0
DATA2 [15:0]							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. Address 0x05 DATA2_LSB Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DATA2[15:0]	R	0x0000	**Channel 2 LSB Conversion Result (LSB)** This register must be read after DATA_MSB2 to ensure data coherency.

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7.6.8 Address 0x06, DATA3_MSB (LDC1614 only)

Figure 21. Address 0x06, DATA3_MSB

15	14	13	12	11	10	9	8
ERR_UR3	ERR_OR3	ERR_WD3	ERR_AE3	DATA3 [27:16]			
7	6	5	4	3	2	1	0
DATA3 [27:16]							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Address 0x06, DATA3_MSB Field Descriptions

Bit	Field	Type	Reset	Description
15	ERR_UR3	R	0	**Channel 3 Conversion Under-range Error Flag** Cleared by reading the bit.
14	ERR_OR3	R	0	**Channel 3 Conversion Over-range Error Flag** Cleared by reading the bit.
13	ERR_WD3	R	0	**Channel 3 Conversion Watchdog Timeout Error Flag** Cleared by reading the bit.
12	ERR_AE3	R	0	**Channel 3 Conversion Amplitude Error Flag** Cleared by reading the bit.
11:0	DATA3 [27:16]	R	0x000	**Channel 3 MSB Conversion Result (MSB)**

7.6.9 Address 0x07, DATA3_LSB (LDC1614 only)

Figure 22. Address 0x07, DATA3_LSB

15	14	13	12	11	10	9	8
DATA3[15:0]							
7	6	5	4	3	2	1	0
DATA3[15:0]							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. Address 0x07 DATA3_LSB Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DATA3[15:0]	R	0x0000	**Channel 3 LSB Conversion Result (LSB)** This register must be read after DATA_MSB3 to ensure data coherency.

7.6.10 Address 0x08, RCOUNT0

Figure 23. Address 0x08, RCOUNT0

15	14	13	12	11	10	9	8
RCOUNT0							
7	6	5	4	3	2	1	0
RCOUNT0							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. Address 0x08, RCOUNT0 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RCOUNT0	R/W	0x0080	**Channel 0 Reference Count Conversion Interval Time** 0x0000-0x0004: Reserved 0x0005-0xFFFF: Conversion Time (t_{C0}) = (RCOUNT0×16)/f_{REF0}

7.6.11 Address 0x09, RCOUNT1

Figure 24. Address 0x09, RCOUNT1

15	14	13	12	11	10	9	8
RCOUNT1							
7	6	5	4	3	2	1	0
RCOUNT1							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. Address 0x09, RCOUNT1 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RCOUNT1	R/W	0x0080	**Channel 1 Reference Count Conversion Interval Time** 0x0000-0x0004: Reserved 0x0005-0xFFFF: Conversion Time (t_{C1})= (RCOUNT1×16)/f_{REF1}

7.6.12 Address 0x0A, RCOUNT2 (LDC1614 only)

Figure 25. Address 0x0A, RCOUNT2

15	14	13	12	11	10	9	8
RCOUNT2							
7	6	5	4	3	2	1	0
RCOUNT2							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. Address 0x0A, RCOUNT2 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RCOUNT2	R/W	0x0080	**Channel 2 Reference Count Conversion Interval Time** 0x0000-0x0004: Reserved 0x0005-0xFFFF: Conversion Time (t_{C2})= (RCOUNT2×16)/f_{REF2}

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7.6.13 Address 0x0B, RCOUNT3 (LDC1614 only)

Figure 26. Address 0x0B, RCOUNT3

15	14	13	12	11	10	9	8
RCOUNT3							
7	6	5	4	3	2	1	0
RCOUNT3							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. Address 0x0B, RCOUNT3 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RCOUNT3	R/W	0x0080	**Channel 3 Reference Count Conversion Interval Time** 0x0000-0x0004: Reserved 0x0005-0xFFFF: Conversion Time (t_{C3})= (RCOUNT3×16)/f_{REF3}

7.6.14 Address 0x0C, OFFSET0

Figure 27. Address 0x0C, OFFSET0

15	14	13	12	11	10	9	8
OFFSET0							
7	6	5	4	3	2	1	0
OFFSET0							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. OFFSET0 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OFFSET0	R/W	0x0000	**Channel 0 Conversion Offset** $f_{OFFSET0}$ = (OFFSET0÷2^{16})×f_{REF0}

7.6.15 Address 0x0D, OFFSET1

Figure 28. Address 0x0D, OFFSET1

15	14	13	12	11	10	9	8
OFFSET1							
7	6	5	4	3	2	1	0
OFFSET1							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. Address 0x0D, OFFSET1 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OFFSET1	R/W	0x0000	**Channel 1 Conversion Offset** $f_{OFFSET1}$ = (OFFSET1÷2^{16})×f_{REF1}

7.6.16 Address 0x0E, OFFSET2 (LDC1614 only)

Figure 29. Address 0x0E, OFFSET2

15	14	13	12	11	10	9	8
OFFSET2							
7	6	5	4	3	2	1	0
OFFSET2							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. Address 0x0E, OFFSET2 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OFFSET2	R/W	0x0000	**Channel 2 Conversion Offset** $f_{OFFSET_2} = (OFFSET2 \div 2^{16}) \times f_{REF2}$

7.6.17 Address 0x0F, OFFSET3 (LDC1614 only)

Figure 30. Address 0x0F, OFFSET3

15	14	13	12	11	10	9	8
OFFSET3							
7	6	5	4	3	2	1	0
OFFSET3							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. Address 0x0F, OFFSET3 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OFFSET3	R/W	0x0000	**Channel 3 Conversion Offset** $f_{OFFSET3} = (OFFSET3 \div 2^{16}) \times f_{REF3}$

7.6.18 Address 0x10, SETTLECOUNT0

Figure 31. Address 0x10, SETTLECOUNT0

15	14	13	12	11	10	9	8
SETTLECOUNT0							
7	6	5	4	3	2	1	0
SETTLECOUNT0							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. Address 0x10, SETTLECOUNT0 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SETTLECOUNT0	R/W	0x0000	**Channel 0 Conversion Settling** The LDC will use this settling time to allow the LC sensor to stabilize before initiation of a conversion on Channel 0. If the amplitude has not settled prior to the conversion start, an Amplitude error will be generated if reporting of this type of error is enabled. 0x0000: Settle Time (t_{S0})= 32 ÷ f_{REF0} 0x0001: Settle Time (t_{S0})= 32 ÷ f_{REF0} 0x0002 - 0xFFFF: Settle Time (t_{S0})= (SETTLECOUNT0×16) ÷ f_{REF0}

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7.6.19 Address 0x11, SETTLECOUNT1

Figure 32. Address 0x11, SETTLECOUNT1

15	14	13	12	11	10	9	8
SETTLECOUNT1							
7	6	5	4	3	2	1	0
SETTLECOUNT1							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. Address 0x11, SETTLECOUNT1 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SETTLECOUNT1	R/W	0x0000	**Channel 1 Conversion Settling** The LDC will use this settling time to allow the LC sensor to stabilize before initiation of a conversion on a Channel 1. If the amplitude has not settled prior to the conversion start, an Amplitude error will be generated if reporting of this type of error is enabled. 0x0000: Settle Time (t_{S1})= 32 ÷ f_{REF1} 0x0001: Settle Time (t_{S1})= 32 ÷ f_{REF1} 0x0002 - 0xFFFF: Settle Time (t_{S1})= (SETTLECOUNT1×16) ÷ f_{REF1}

7.6.20 Address 0x12, SETTLECOUNT2 (LDC1614 only)

Figure 33. Address 0x12, SETTLECOUNT2

15	14	13	12	11	10	9	8
SETTLECOUNT2							
7	6	5	4	3	2	1	0
SETTLECOUNT2							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. Address 0x12, SETTLECOUNT2 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SETTLECOUNT2	R/W	0x0000	**Channel 2 Conversion Settling** The LDC will use this settling time to allow the LC sensor to stabilize before initiation of a conversion on Channel 2. If the amplitude has not settled prior to the conversion start, an Amplitude error will be generated if reporting of this type of error is enabled. 0x0000: Settle Time (t_{S2})= 32 ÷ f_{REF2} 0x0001: Settle Time (t_{S2})= 32 ÷ f_{REF2} 0x0002 - 0xFFFF: Settle Time (t_{S2})= (SETTLECOUNT2×16) ÷ f_{REF2}

7.6.21 Address 0x13, SETTLECOUNT3 (LDC1614 only)

Figure 34. Address 0x13, SETTLECOUNT3

15	14	13	12	11	10	9	8
SETTLECOUNT3							
7	6	5	4	3	2	1	0
SETTLECOUNT3							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. Address 0x13, SETTLECOUNT3 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SETTLECOUNT3	R/W	0x0000	**Channel 3 Conversion Settling** The LDC will use this settling time to allow the LC sensor to stabilize before initiation of a conversion on Channel 3. If the amplitude has not settled prior to the conversion start, an Amplitude error will be generated if reporting of this type of error is enabled 0x0000: Settle Time (t_{S3})= 32 ÷ f_{REF3} 0x0001: Settle Time (t_{S3})= 32 ÷ f_{REF3} 0x0002 - 0xFFFF: Settle Time (t_{S3})= (SETTLECOUNT3×16) ÷ f_{REF3}

7.6.22 Address 0x14, CLOCK_DIVIDERS0

Figure 35. Address 0x14, CLOCK_DIVIDERS0

15	14	13	12	11	10	9	8
FIN_DIVIDER0				RESERVED		FREF_DIVIDER0	
7	6	5	4	3	2	1	0
FREF_DIVIDER0							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. Address 0x14, CLOCK_DIVIDERS0 Field Descriptions

Bit	Field	Type	Reset	Description
15:12	FIN_DIVIDER0	R/W	0000	**Channel 0 Input Divider** Sets the divider for Channel 0 input. Must be set to ≥2 if the Sensor frequency is ≥ 8.75MHz b0000: Reserved. Do not use. FIN_DIVIDER0 ≥ b0001: f_{in0} = $f_{SENSOR0}$/FIN_DIVIDER0
11:10	RESERVED	R/W	00	Reserved. Set to b00.
9:0	FREF_DIVIDER0	R/W	0x000	**Channel 0 Reference Divider** Sets the divider for Channel 0 reference. Use this to scale the maximum conversion frequency. 0x000: Reserved. Do not use. FREF_DIVIDER0 ≥ 0x001: f_{REF0} = f_{CLK}/FREF_DIVIDER0

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7.6.23 Address 0x15, CLOCK_DIVIDERS1

Figure 36. Address 0x15, CLOCK_DIVIDERS1

15	14	13	12	11	10	9	8
FIN_DIVIDER1				RESERVED		FREF_DIVIDER1	
7	6	5	4	3	2	1	0
FREF_DIVIDER1							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. Address 0x15, CLOCK_DIVIDERS1 Field Descriptions

Bit	Field	Type	Reset	Description
15:12	FIN_DIVIDER1	R/W	0000	**Channel 1 Input Divider** Sets the divider for Channel 1 input. Used when the Sensor frequency is greater than the maximum F_{IN}. b0000: Reserved. Do not use. FIN_DIVIDER1 ≥ b0001: $f_{in1} = f_{SENSOR1} \div$FIN_DIVIDER1
11:10	RESERVED	R/W	00	Reserved. Set to b00.
9:0	FREF_DIVIDER1	R/W	0x000	**Channel 1 Reference Divider** Sets the divider for Channel 1 reference. Use this to scale the maximum conversion frequency. 0x000: Reserved. Do not use. FREF_DIVIDER1 ≥ 0x001: $f_{REF1} = f_{CLK} \div$FREF_DIVIDER1

7.6.24 Address 0x16, CLOCK_DIVIDERS2 (LDC1614 only)

Figure 37. Address 0x16, CLOCK_DIVIDERS2

15	14	13	12	11	10	9	8
FIN_DIVIDER2				RESERVED		FREF_DIVIDER2	
7	6	5	4	3	2	1	0
FREF_DIVIDER2							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. Address 0x16, CLOCK_DIVIDERS2 Field Descriptions

Bit	Field	Type	Reset	Description
15:12	FIN_DIVIDER2	R/W	0000	**Channel 2 Input Divider** Sets the divider for Channel 2 input. Must be set to ≥2 if the Sensor frequency is ≥ 8.75MHz. b0000: Reserved. Do not use. FIN_DIVIDER2 ≥ b0001: $f_{IN2} = f_{SENSOR2} \div$FIN_DIVIDER2
11:10	RESERVED	R/W	00	Reserved. Set to b00.
9:0	FREF_DIVIDER2	R/W	0x000	**Channel 2 Reference Divider** Sets the divider for Channel 2 reference. Use this to scale the maximum conversion frequency. 0x000: Reserved. Do not use. FREF_DIVIDER2 ≥ 0x001: $f_{REF2} = f_{CLK} \div$FREF_DIVIDER2

7.6.25 Address 0x17, CLOCK_DIVIDERS3 (LDC1614 only)

Figure 38. Address 0x17, CLOCK_DIVIDERS3

15	14	13	12	11	10	9	8
FIN_DIVIDER3				RESERVED		FREF_DIVIDER3	
7	6	5	4	3	2	1	0
FREF_DIVIDER3							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. Address 0x17, CLOCK_DIVIDERS3

Bit	Field	Type	Reset	Description
15:12	FIN_DIVIDER3	R/W	0000	**Channel 3 Input Divider** Sets the divider for Channel 3 input. Must be set to ≥2 if the Sensor frequency is ≥ 8.75MHz. b0000: Reserved. Do not use. FIN_DIVIDER3 ≥ b0001: $f_{IN3} = f_{SENSOR3} \div$FIN_DIVIDER3
11:10	RESERVED	R/W	00	Reserved. Set to b00.
9:0	FREF_DIVIDER3	R/W	0x000	**Channel 3 Reference Divider** Sets the divider for Channel 3 reference. Use this to scale the maximum conversion frequency. 0x000: reserved FREF_DIVIDER3 ≥ 0x001: $f_{REF3} = f_{CLK} \div$FREF_DIVIDER3

7.6.26 Address 0x18, STATUS

Figure 39. Address 0x18, STATUS

15	14	13	12	11	10	9	8
ERR_CHAN		ERR_UR	ERR_OR	ERR_WD	ERR_AHE	ERR_ALE	ERR_ZC
7	6	5	4	3	2	1	0
RESERVED	DRDY	RESERVED		UNREADCONV0	UNREADCONV1	UNREADCONV2	UNREADCONV3

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. Address 0x18, STATUS Field Descriptions

Bit	Field	Type	Reset	Description
15:14	ERR_CHAN	R	00	**Error Channel** Indicates which channel has generated a Flag or Error. Once flagged, any reported error is latched and maintained until either the STATUS register or the DATAx_MSB register corresponding to the Error Channel is read. b00: Channel 0 is source of flag or error. b01: Channel 1 is source of flag or error. b10: Channel 2 is source of flag or error (LDC1614 only). b11: Channel 3 is source of flag or error (LDC1614 only).
13	ERR_UR	R	0	**Conversion Under-range Error** b0: No Conversion Under-range error was recorded since the last read of the STATUS register. b1: An active channel has generated a Conversion Under-range error. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this error.
12	ERR_OR	R	0	**Conversion Over-range Error** b0: No Conversion Over-range error was recorded since the last read of the STATUS register. b1: An active channel has generated a Conversion Over-range error. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this error.

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Table 25. Address 0x18, STATUS Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ERR_WD	R	0	**Watchdog Timeout Error** b0: No Watchdog Timeout error was recorded since the last read of the STATUS register. b1: An active channel has generated a Watchdog Timeout error. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this error.
10	ERR_AHE	R	0	**Sensor Amplitude High Error** b0: No Amplitude High error was recorded since the last read of the STATUS register. b1: An active channel has generated an Amplitude High error - this occurs when the sensor amplitude is above a nominal 1.8 V. It is recommended to reduce the corresponding sensor IDRIVEx setting. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this error.
9	ERR_ALE	R	0	**Sensor Amplitude Low Error** b0: No Amplitude Low error was recorded since the last read of the STATUS register. b1: An active channel has generated an Amplitude Low error - this occurs when the sensor amplitude is below a nominal 1.2 V. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this error.
8	ERR_ZC	R	0	**Zero Count Error** b0: No Zero Count error was recorded since the last read of the STATUS register. b1: An active channel has generated a Zero Count error. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this error.
7	Reserved	R	0	Reserved. Reads 0.
6	DRDY	R	0	**Data Ready Flag** b0: No new conversion result was recorded in the STATUS register. b1: A new conversion result is ready. When in Single Channel Conversion, this indicates a single conversion is available. When in sequential mode, this indicates that a new conversion result for all active channels is now available.
5:4	Reserved	R	00	Reserved. Reads 00b.
3	UNREADCONV0	R	0	**Channel 0 Unread Conversion** b0: No unread conversion is present for Channel 0. b1: An unread conversion is present for Channel 0. Read Registers DATA0_MSB and DATA0_LSB to retrieve conversion results.
2	UNREADCONV1	R	0	**Channel 1 Unread Conversion** b0: No unread conversion is present for Channel 1. b1: An unread conversion is present for Channel 1. Read Registers DATA1_MSB and DATA1_LSB to retrieve conversion results.
1	UNREADCONV2	R	0	**Channel 2 Unread Conversion** b0: No unread conversion is present for Channel 2. b1: An unread conversion is present for Channel 2. Read Registers DATA2_MSB and DATA2_LSB to retrieve conversion results (LDC1614 only)
0	UNREADCONV3	R	0	**Channel 3 Unread Conversion** b0: No unread conversion is present for Channel 3. b1: An unread conversion is present for Channel 3. Read Registers DATA3_MSB and DATA3_LSB to retrieve conversion results (LDC1614 only)

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7.6.27 Address 0x19, ERROR_CONFIG

Figure 40. Address 0x19, ERROR_CONFIG

15	14	13	12	11	10	9	8
UR_ERR2OUT	OR_ERR2OUT	WD_ ERR2OUT	AH_ERR2OUT	AL_ERR2OUT	RESERVED		
7	6	5	4	3	2	1	0
UR_ERR2INT	OR_ERR2INT	WD_ERR2INT	AH_ERR2INT	AL_ERR2INT	ZC_ERR2INT	Reserved	DRDY_2INT

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. Address 0x19, ERROR_CONFIG

Bit	Field	Type	Reset	Description
15	UR_ERR2OUT	R/W	0	**Under-range Error to Output Register** b0: Do not report Under-range errors in the DATAx_MSB registers. b1: Report Under-range errors in the DATAx_MSB.ERR_URx register field corresponding to the channel that generated the error.
14	OR_ERR2OUT	R/W	0	**Over-range Error to Output Register** b0: Do not report Over-range errors in the DATAx_MSB registers. b1: Report Over-range errors in the DATAx_MSB.ERR_ORx register field corresponding to the channel that generated the error.
13	WD_ ERR2OUT	R/W	0	**Watchdog Timeout Error to Output Register** b0: Do not report Watchdog Timeout errors in the DATAx_MSB registers. b1: Report Watchdog Timeout errors in the DATAx_MSB.ERR_WDx register field corresponding to the channel that generated the error.
12	AH_ERR2OUT	R/W	0	**Amplitude High Error to Output Register** b0:Do not report Amplitude High errors in the DATAx_MSB registers. b1: Report Amplitude High errors in the DATAx_MSB.ERR_AEx register field corresponding to the channel that generated the error.
11	AL_ERR2OUT	R/W	0	**Amplitude Low Error to Output Register** b0: Do not report Amplitude High errors in the DATAx_MSB registers. b1: Report Amplitude High errors in the DATAx_MSB.ERR_AEx register field corresponding to the channel that generated the error.
10:8	Reserved	R/W	00	Reserved. Set to b00.
7	UR_ERR2INT	R/W	0	**Under-range Error to INTB** b0: Do not report Under-range errors by asserting INTB pin and STATUS register. b1: Report Under-range errors by asserting INTB pin and updating STATUS.ERR_UR register field.
6	OR_ERR2INT	R/W	0	**Over-range Error to INTB** b0: Do not report Over-range errors by asserting INTB pin and STATUS register. b1: Report Over-range errors by asserting INTB pin and updating STATUS.ERR_OR register field.
5	WD_ERR2INT	R/W	0	**Watchdog Timeout Error to INTB** b0: Do not report Watchdog errors by asserting INTB pin and STATUS register. b1: Report Watchdog Timeout errors by asserting INTB pin and updating STATUS.ERR_WD register field.
4	AH_ERR2INT	R/W	0	**Amplitude High Error to INTB** b0: Do not report Amplitude High errors by asserting INTB pin and STATUS register. b1: Report Amplitude High errors by asserting INTB pin and updating STATUS.ERR_AHE register field.

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Table 26. Address 0x19, ERROR_CONFIG (continued)

Bit	Field	Type	Reset	Description
3	AL_ERR2INT	R/W	0	**Amplitude Low Error to INTB** b0: Do not report Amplitude Low errors by asserting INTB pin and STATUS register. b1: Report Amplitude Low errors by asserting INTB pin and updating STATUS.ERR_ALE register field.
2	ZC_ERR2INT	R/W	0	**Zero Count Error to INTB** b0: Do not report Zero Count errors by asserting INTB pin and STATUS register. b1: Report Zero Count errors by asserting INTB pin and updating STATUS. ERR_ZC register field.
1	Reserved	R/W	0	Reserved. Set to b0.
0	DRDY_2INT	R/W	0	**Data Ready Flag to INTB** b0: Do not report Data Ready Flag by asserting INTB pin and STATUS register. b1: Report Data Ready Flag by asserting INTB pin and updating STATUS. DRDY register field.

7.6.28 Address 0x1A, CONFIG

Figure 41. Address 0x1A, CONFIG

15	14	13	12	11	10	9	8
ACTIVE_CHAN		SLEEP_MODE_EN	RP_OVERRIDE_EN	SENSOR_ACTIVATE_SEL	AUTO_AMP_DIS	REF_CLK_SRC	RESERVED
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTB_DIS	HIGH_CURRENT_DRV	RESERVED					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. Address 0x1A, CONFIG Field Descriptions

Bit	Field	Type	Reset	Description
15:14	ACTIVE_CHAN	R/W	00	**Active Channel Selection** Selects channel for continuous conversions when MUX_CONFIG.AUTOSCAN_EN is 0. b00: Perform continuous conversions on Channel 0 b01: Perform continuous conversions on Channel 1 b10: Perform continuous conversions on Channel 2 (LDC1614 only) b11: Perform continuous conversions on Channel 3 (LDC1614 only)
13	SLEEP_MODE_EN	R/W	1	**Sleep Mode Enable** Enter or exit low power Sleep Mode. b0: Device is active. b1: Device is in Sleep Mode.
12	RP_OVERRIDE_EN	R/W	0	**Sensor R_P Override Enable** Provides control over Sensor current drive used during the conversion time for Ch. x, based on the programmed value in the IDRIVEx field. Refer to Automatic IDRIVE Setting with RP_OVERRIDE_EN for details. b0: Override off b1: R_P Override on
11	SENSOR_ACTIVATE_SEL	R/W	1	**Sensor Activation Mode Selection** Set the mode for sensor initialization. Refer to Sensor Activation for details. b0: Full Current Activation Mode – the LDC will drive maximum sensor current for a shorter sensor activation time. b1: Low Power Activation Mode – the LDC uses the value programmed in DRIVE_CURRENTx during sensor activation to minimize power consumption.

Table 27. Address 0x1A, CONFIG Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	AUTO_AMP_DIS	R/W	0	**Automatic Sensor Amplitude Correction Disable** Setting this bit will disable the automatic Amplitude correction algorithm and stop the updating of the INIT_IDRIVEx field. b0: Automatic Amplitude correction enabled. b1: Automatic Amplitude correction is disabled. Recommended for precision applications.
9	REF_CLK_SRC	R/W	0	**Select Reference Frequency Source** b0: Use Internal oscillator as reference frequency. b1: Reference frequency is provided from CLKIN pin.
8	RESERVED	R/W	0	Reserved. Set to b0.
7	INTB_DIS	R/W	0	**INTB Disable** b0: INTB pin will be asserted when status register updates. b1: INTB pin will not be asserted when status register updates. If this mode is selected, the INTB pin level will be high.
6	HIGH_CURRENT_DRV	R/W	0	**High Current Sensor Drive** b0: The LDC will drive all channels with normal sensor current (1.5mA max). b1: The LDC will drive channel 0 with current >1.5mA. This mode is not supported if AUTOSCAN_EN = b1 (multi-channel mode).
5:0	RESERVED	R/W	00 0001	Reserved. Set to b00'0001.

7.6.29 Address 0x1B, MUX_CONFIG

Figure 42. Address 0x1B, MUX_CONFIG

15	14	13	12	11	10	9	8
AUTOSCAN_EN	RR_SEQUENCE		RESERVED				
7	6	5	4	3	2	1	0
RESERVED					DEGLITCH		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. Address 0x1B, MUX_CONFIG Field Descriptions

Bit	Field	Type	Reset	Description
15	AUTOSCAN_EN	R/W	0	**Auto-Scan Mode Enable** b0: Continuous conversion on the single channel selected by CONFIG.ACTIVE_CHAN register field. b1: Auto-Scan conversions as selected by MUX_CONFIG.RR_SEQUENCE register field.
14:13	RR_SEQUENCE	R/W	00	**Auto-Scan Sequence Configuration** Configure multiplexing channel sequence. The LDC will perform a single conversion on each channel in the sequence selected, and then restart the sequence continuously. b00: Ch0, Ch1 b01: Ch0, Ch1, Ch2 (LDC1614 only) b10: Ch0, Ch1, Ch2, Ch3 (LDC1614 only) b11: Ch0, Ch1
12:3	RESERVED	R/W	00 0100 0001	Reserved. Set to 00 0100 0001.
2:0	DEGLITCH	R/W	111	**Input Deglitch Filter Bandwidth** Select the lowest setting that exceeds the maximum sensor oscillation frequency. b001: 1.0 MHz b100: 3.3 MHz b101: 10 MHz b111: 33 MHz

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7.6.30 Address 0x1C, RESET_DEV

Figure 43. Address 0x1C, RESET_DEV

15	14	13	12	11	10	9	8
RESET_DEV	RESERVED						
7	6	5	4	3	2	1	0
RESERVED							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. Address 0x1C, RESET_DEV Field Descriptions

Bit	Field	Type	Reset	Description
15	RESET_DEV	R/W	0	**Device Reset** Write b1 to reset the device. Will always readback 0.
14:0	RESERVED	R/W	0x0000	Reserved. Set to b000 0000 0000 0000.

7.6.31 Address 0x1E, DRIVE_CURRENT0

Figure 44. Address 0x1E, DRIVE_CURRENT0

15	14	13	12	11	10	9	8
IDRIVE0					INIT_IDRIVE0		
7	6	5	4	3	2	1	0
INIT_IDRIVE0		RESERVED					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. Address 0x1E, DRIVE_CURRENT0 Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IDRIVE0	R/W	0 0000	**Channel 0 L-C Sensor Drive Current** This field sets the Sensor Drive Current used during the settling + conversion time of Channel 0 sensor. RP_OVERRIDE_EN bit must be set to 1.
10:6	INIT_IDRIVE0	R	0 0000	**Channel 0 Sensor Current Drive** This field stores the Initial Drive Current measured during the initial Amplitude Calibration phase. It is updated after each Amplitude Correction phase of the sensor conversion if AUTO_AMP_DIS=0. When writing to DRIVE_CURRENT0, set this field to b0 0000.
5:0	RESERVED	R/W	00 0000	Reserved. Set to b00 0000

7.6.32 Address 0x1F, DRIVE_CURRENT1

Figure 45. Address 0x1F, DRIVE_CURRENT1

15	14	13	12	11	10	9	8
IDRIVE1					INIT_IDRIVE1		
7	6	5	4	3	2	1	0
INIT_IDRIVE1		RESERVED					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. Address 0x1F, DRIVE_CURRENT1 Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IDRIVE1	R/W	0 0000	**Channel 1 L-C Sensor Drive Current** This field sets the Sensor Drive Current used during the settling + conversion time of Channel 0 sensor. RP_OVERRIDE_EN bit must be set to 1.
10:6	INIT_IDRIVE1	R	0 0000	**Channel 1 Sensor Current Drive** This field stores the Initial Drive Current calculated during the initial Amplitude Calibration phase. It is updated after each Amplitude Correction phase of the sensor conversion if AUTO_AMP_DIS=0. When writing to DRIVE_CURRENT1, set this field to b0 0000.
5:0	RESERVED	-	00 0000	Reserved

7.6.33 Address 0x20, DRIVE_CURRENT2 (LDC1614 only)

Figure 46. Address 0x20, DRIVE_CURRENT2

15	14	13	12	11	10	9	8
IDRIVE2					INIT_IDRIVE2		
7	6	5	4	3	2	1	0
INIT_IDRIVE2		RESERVED					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. Address 0x20, DRIVE_CURRENT2 Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IDRIVE2	R/W	0 0000	**Channel 2 L-C Sensor Drive Current** This field sets the Sensor Drive Current used during the settling + conversion time of Channel 0 sensor. RP_OVERRIDE_EN bit must be set to 1.
10:6	INIT_IDRIVE2	R	0 0000	**Channel 2 Sensor Current Drive** This field stores the Initial Drive Current calculated during the initial Amplitude Calibration phase. It is updated after each Amplitude Correction phase of the sensor conversion if AUTO_AMP_DIS=0. When writing to DRIVE_CURRENT2, set this field to b0 0000.
5:0	RESERVED	–	00 0000	Reserved

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7.6.34 Address 0x21, DRIVE_CURRENT3 (LDC1614 only)

Figure 47. Address 0x21, DRIVE_CURRENT3

15	14	13	12	11	10	9	8
IDRIVE3					INIT_IDRIVE3		
7	6	5	4	3	2	1	0
INIT_IDRIVE3		RESERVED					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. DRIVE_CURRENT3 Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IDRIVE3	R/W	0 0000	**Channel 3 L-C Sensor Drive Current** This field sets the Sensor Drive Current used during the settling + conversion time of Channel 0 sensor. RP_OVERRIDE_EN bit must be set to 1.
10:6	INIT_IDRIVE3	R	0 0000	**Channel 3 Sensor Current Drive** This field stores the Initial Drive Current calculated during the initial Amplitude Calibration phase.It is updated after each Amplitude Correction phase of the sensor conversion if AUTO_AMP_DIS =0. When writing to DRIVE_CURRENT3, set this field to b0 0000.
5:0	RESERVED	–	00 0000	Reserved

7.6.35 Address 0x7E, MANUFACTURER_ID

Table 34. Address 0x7E, MANUFACTURER_ID Field Descriptions

Bit	Field	Type	Reset	Description
15:0	MANUFACTURER_ID	R	0101 0100 0100 1001	Manufacturer ID = 0x5449

7.6.36 Address 0x7F, DEVICE_ID

Figure 48. Address 0x7F, DEVICE_ID

15	14	13	12	11	10	9	8
DEVICE_ID							
7	6	5	4	3	2	1	0
DEVICE_ID							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. Address 0x7F, DEVICE_ID Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID	R	0011 0000 0101 0101	Device ID = 0x3055

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Conductive Objects in a Time-Varying EM Field

An AC current flowing through an inductor will generate an AC magnetic field. If a conductive material, such as a metal object, is brought into the vicinity of the inductor, the magnetic field will induce a circulating current (eddy current) on the surface of the conductor.

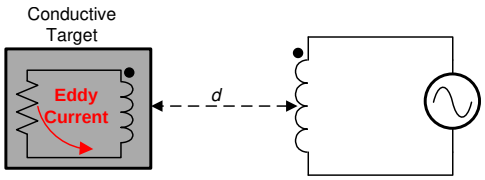

Figure 49. Conductor in AC Magnetic Field

The eddy current is a function of the distance, size, and composition of the conductor. The eddy current generates its own magnetic field, which opposes the original field generated by the sensor inductor. This effect is equivalent to a set of coupled inductors, where the sensor inductor is the primary winding and the eddy current in the target object represents the secondary inductor. The coupling between the inductors is a function of the sensor inductor, and the resistivity, distance, size, and shape of the conductive target. The resistance and inductance of the secondary winding caused by the eddy current can be modeled as a distance dependent resistive and inductive component on the primary side (coil). Figure 49 shows a simplified circuit model of the sensor and the target as coupled coils.

8.1.2 L-C Resonators

An EM field can be generated using an L-C resonator, or L-C tank. One topology for an L-C tank is a parallel R-L-C construction, as shown in Figure 50.

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Application Information (continued)

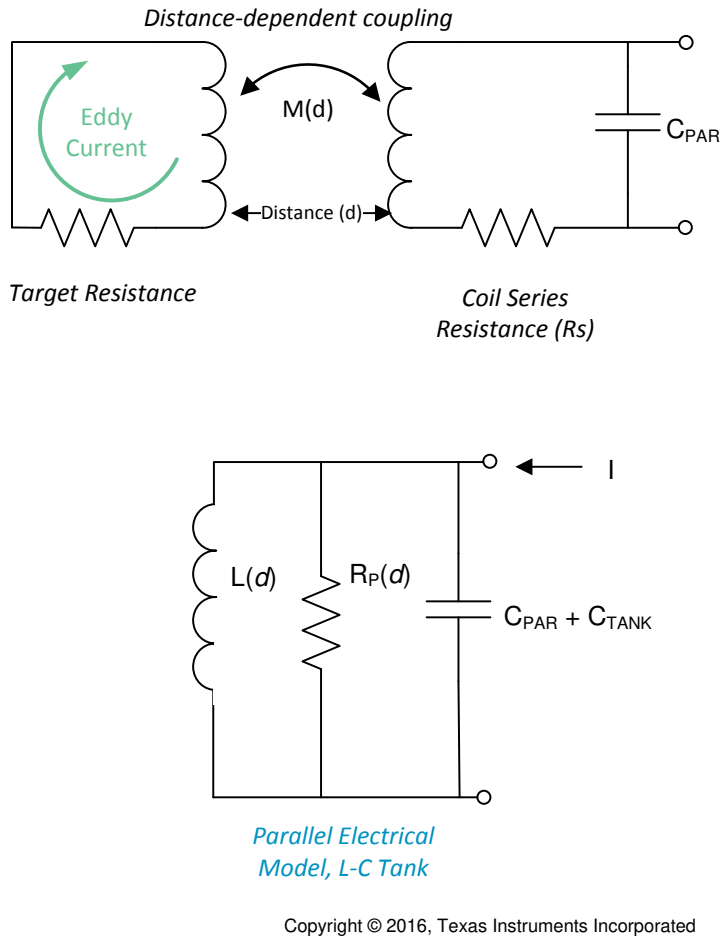

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Figure 50. Electrical Model of the L-C Tank Sensor

A resonant oscillator can be constructed by combining a frequency selective circuit (resonator) with a gain block in a closed loop. The criteria for oscillation are: (1) loop gain > 1, and (2) closed loop phase shift of 2π radians. The R-L-C resonator provides the frequency selectivity and contributes to the phase shift. At the resonance frequency, the impedance of the reactive components (L and C) cancels, leaving only R_P, the lossy (resistive) element in the circuit. The voltage amplitude is maximized at this frequency. The R_P can be used to determine the sensor drive current for a given oscillation amplitude. A lower R_P requires a larger sensor current to maintain a constant oscillation amplitude. The sensor oscillation frequency is given by:

$$f_{SENSOR} = \frac{1}{2\pi\sqrt{LC}} * \sqrt{1 - \frac{1}{Q^2} - \frac{5*10^{-9}}{Q\sqrt{LC}}} \approx \frac{1}{2\pi\sqrt{LC}}$$

where:

- C is the sensor capacitance (C_{SENSOR} + $C_{PARASITIC}$)
- L is the sensor inductance
- Q is the quality factor of the resonator. Q can be calculated by: (1)

$$Q = R_P\sqrt{\frac{C}{L}}$$

where:

- R_P is the AC parallel resistance of the LC resonator at the operating frequency. (2)

Application Information (continued)

Texas Instruments' WEBENCH design tool can be used for coil design, in which the parameter values for R_P, L and C are calculated. See http://www.ti.com/webench.

R_P is a function of target distance, target material, and sensor characteristics. Figure 51 shows an example of R_P variation based on the distance between the sensor and the target. The graph represents a 14 mm diameter PCB coil (23 turns, 4 mil trace width, 4 mil spacing between traces, 1 oz. copper thickness, on FR4 material). This curve is a typical response where the target distance scales based on the sensor size and the sensor R_P scales based on the free-space of the inductor.

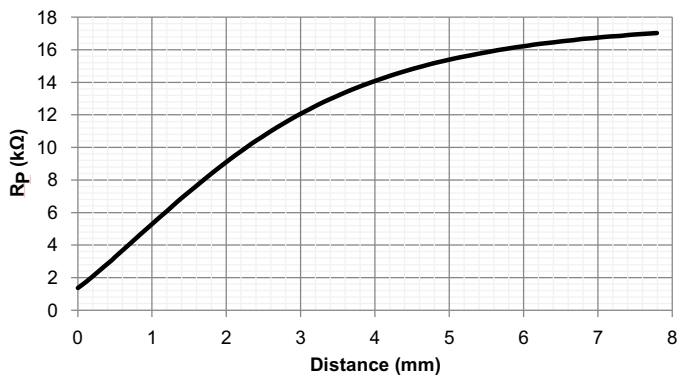

Figure 51. Example R_P vs. Distance with a 14 mm PCB Coil and 2 mm Thick Stainless Steel Target

It is important to configure the sensor current drive so that the sensor will still oscillate at the minimum R_P value (which typically occurs with maximum target interaction). As an example, if the closest target distance in a system with the response shown in Figure 51 is 1mm, then the sensor current drive needs to support a R_P value is 5 kΩ. Both the minimum and maximum R_P conditions should have oscillation amplitudes that are within the device operating range. See section *Sensor Current Drive Control* for details on setting the current drive.

The inductance that is measured by the LDC is:

$$L(d) = L_{inf} - M(d) = \frac{1}{(2\pi * f_{SENSOR})^2 * C}$$

where:

- L(d) is the measured sensor inductance, for a distance *d* between the sensor coil and target
- L_{inf} is the inductance of the sensing coil without a conductive target (target at infinite distance)
- M(d) is the mutual inductance
- f_{SENSOR} = sensor oscillation frequency for a distance *d* between the sensor coil and target
- $C = C_{SENSOR} + C_{PARASITIC}$ (3)

Figure 52 shows an example of variation in sensor frequency and inductance as a function of distance for a 14 mm diameter PCB coil (23 turns, 4 mil trace width, 4 mil spacing between traces, 1 oz copper thickness, FR4 material). The frequency and inductance graphs will scale based on the sensor free-space characteristics, and the target distance scales based on the sensor diameter.

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Application Information (continued)

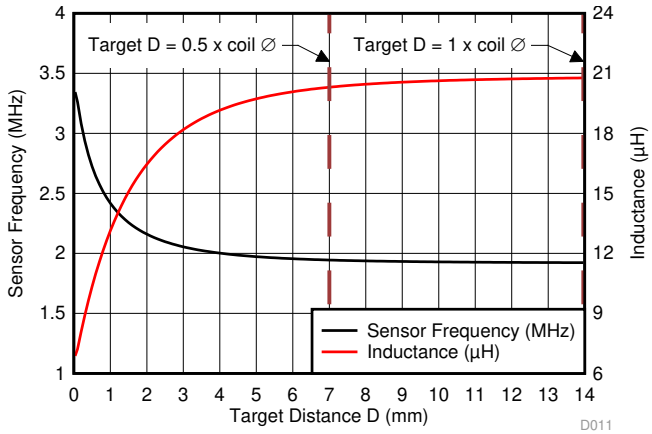

Figure 52. Example Sensor Frequency, Inductance vs. Target Distance with 14 mm PCB Coil and 1.5 mm Thick Aluminum Target

The Texas Instruments Application Notes *LDC Sensor Design* and *LDC Target Design* provide more information on construction of sensors and targets charactersitics to consider based on system requirements.

8.1.3 Multi-Channel and Single Channel Operation

The multi-channel package of the LDC enables the user to save board space and support flexible system design. For example, temperature drift can often cause a shift in component values, resulting in a shift in resonant frequency of the sensor. Using a second sensor as a reference or in a differential configuration provides the capability to cancel out temperature shifts and other environmental variations. When operated in multi-channel mode, the LDC sequentially samples the selected channels - only one channel is active at any time while the other selected channels are held in an inactive state. In single channel mode, the LDC samples a single channel, which is selectable. Refer to *Inactive Channel Sensor Connections* for more details on inactive channels.

Inactive channels have the corresponding INAx and INBx pins tied to ground. The following table shows the registers and values that are used to configure either multi-channel or single channel modes.

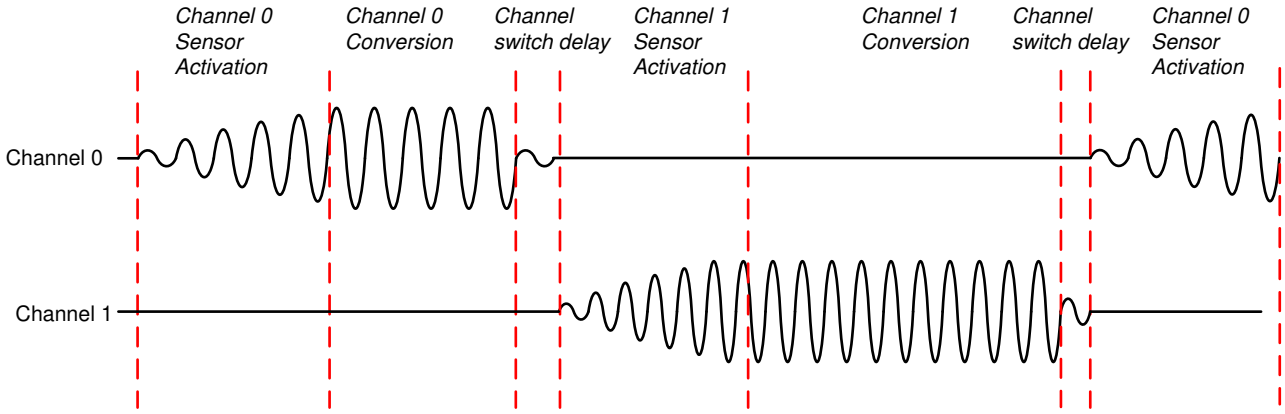

Figure 53. Multi-Channel Mode Sequencing

Application Information (continued)

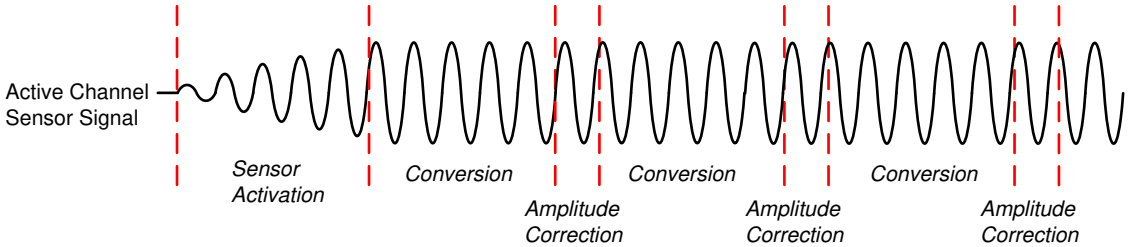

Figure 54. Single-Channel Mode Sequencing

Table 36. Single and Multi-Channel Configuration Registers

MODE	REGISTER	FIELD	VALUE (1)
Single channel	CONFIG, addr 0x1A	ACTIVE_CHAN [15:14]	00 = chan 0 01 = chan 1 10 = chan 2 11 = chan 3
	MUX_CONFIG addr 0x1B	AUTOSCAN_EN [15]	0 = continuous conversion on a single channel (default)
Multi-channel	MUX_CONFIG addr 0x1B	AUTOSCAN_EN [15]	1 = continuous conversion on multiple channels
	MUX_CONFIG addr 0x1B	RR_SEQUENCE [14:13]	00 = Ch0, Ch 1 01 = Ch0, Ch 1, Ch 2 10 = Ch0, CH1, Ch2, Ch3

(1) Channels 2 and 3 are only available for LDC1614

The digitized sensor measurement for each channel (DATAx) represents the ratio of the sensor frequency to the reference frequency.

With FREF_DIVIDERx and FIN_DIVIDERx set to 1, the sensor frequency can be calculated from:

$$f_{sensor} = \frac{DATAx * f_{REFx}}{2^{28}} \tag{4}$$

The following table illustrates the registers that contain the fixed point sample values for each channel. The conversion result for each channel, DATAx, can be calculated with:

$$DATAx = DATAx_MSB \times 65536 + DATAx_LSB \tag{5}$$

Table 37. LDC1612/1614 Sample Data Registers

CHANNEL (1)	REGISTER (2)	FIELD NAME [BITS(S)]	VALUE (3) (4)
0	DATA0_MSB, addr 0x00	DATA0 [27:16]	12 MSBs of the 28 bit conversion for Channel 0
	DATA0_LSB addr 0x01	DATA0 [15:0]	16 LSBs of the 28 bit conversion for Channel 0
1	DATA1_MSB, addr 0x02	DATA1 [27:16]	12 MSBs of the 28 bit conversion for Channel 1
	DATA1_LSB, addr 0x03	DATA1 [15:0]	16 LSBs of the 28 bit conversion for Channel 1
2	DATA1_MSB, addr 0x04	DATA2 [27:16]	12 MSBs of the 28 bit conversion for Channel 2
	DATA1_LSB, addr 0x05	DATA2 [15:0]	16 LSBs of the 28 bit conversion for Channel 2
3	DATA1_MSB, addr 0x06	DATA3 [27:16]	12 MSBs of the 28 bit conversion for Channel 3
	DATA1_LSB, addr 0x07	DATA3 [15:0]	16 LSBs of the 28 bit conversion for Channel 0

(1) Channels 2 and 3 available only in LDC1614.
(2) The DATAx_MSB register must always be read prior to the DATAx_LSB register of the same channel to ensure data coherency.
(3) A DATAx value of 0x000'0000 indicates an under-range condition for LDC1612/LDC1614 corresponding channel
(4) A DATAx value of 0xFFF'FFFF indicates an over-range condition for LDC1612/LDC1614 corresponding channel

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8.1.3.1 Data Offset

An offset value may be subtracted from each DATA value to compensate for a frequency offset or maximize the dynamic range of the sample data. The offset values should be < $f_{SENSORx_MIN}$ / f_{REFx}. Otherwise, the offset might be so large that it masks the LSBs which are changing.

Table 38. Frequency Offset Registers

CHANNEL	REGISTER	FIELD	VALUE
0	OFFSET0, addr 0x0C	OFFSET0 [15:0]	$f_{OFFSET0}$ = OFFSET0 × (f_{REF0}÷2^{16})
1	OFFSET1, addr 0x0D	OFFSET1 [15:0]	$f_{OFFSET1}$ = OFFSET1 × (f_{REF1}÷2^{16})
2	OFFSET2, addr 0x0E	OFFSET2 [15:0]	$f_{OFFSET2}$ = OFFSET2 × (f_{REF2}÷2^{16})
3	OFFSET3, addr 0x0F	OFFSET3 [15:0]	$f_{OFFSET3}$ = OFFSET3 × (f_{REF3}÷2^{16})

The sensor frequency can be determined by:

$$f_{SENSORx} = CHx_FIN_DIVIDER * f_{REFx}\left(\frac{DATAx}{2^{28}} + \frac{CHx_OFFSET}{2^{16}}\right)$$

where:

- DATAx = Channel x Conversion results from the DATAx_MSB and DATAx_LSB registers
- OFFSETx = Offset value set in the OFFSETx register (6)

8.1.4 Sensor Conversion Time

The LDC1612/LDC1614 provides a configurable conversion time by setting an internal register. The conversion interval can be configured across a range of 1.2 µs to >26.2 ms with 16 bits of resolution. Note that it is possible to configure the conversion interval to be significantly shorter than the time required to readback the DATAx registers; when configured in this manner, older conversions for a channel are overwritten when new conversion data is completed for each channel. The conversion interval is set in multiples of the reference clock period by setting the RCOUNTx register value. The conversion time for any channel x is:

$$t_{Cx} = (RCOUNTx \times 16 + 4) / f_{REFx} \quad (7)$$

In general, a longer conversion time will provide a higher resolution inductance measurement. The maximum setting, 0xFFFF, is required for full resolution. The reference count value should be chosen to support both the required sample rate and the necessary resolution. Refer to the TI Application Note *Optimizing L Measurement Resolution for the LDC161x and LDC1101* for more information.

Table 39. Conversion Time Configuration Registers, Channels 0 - 3(1)

CHANNEL	REGISTER	FIELD	CONVERSION TIME
0	RCOUNT0, addr 0x08	RCOUNT0 [15:0]	(RCOUNT0×16)/f_{REF0}
1	RCOUNT1, addr 0x09	RCOUNT1 [15:0]	(RCOUNT1×16)/f_{REF1}
2	RCOUNT2, addr 0x0A	RCOUNT2 [15:0]	(RCOUNT2×16)/f_{REF2}
3	RCOUNT3, addr 0x0B	RCOUNT3 [15:0]	(RCOUNT3×16)/f_{REF3}

(1) Channels 2 and 3 are available only for LDC1614.

The typical channel switch delay time between the end of conversion and the beginning of sensor activation of the subsequent channel is:

$$\text{Channel Switch Delay} = 692\ \text{ns} + 5 / f_{ref} \quad (8)$$

The deterministic conversion time of the LDC allows data polling at a fixed interval. A data ready flag (DRDY) can assert the INTB pin for use in interrupt driven system designs (see the STATUS register description in *Register Maps*).

8.1.4.1 Settling Time

When the LDC sequences through the channels in multi-channel mode, the dwell time interval for each channel is the sum of 3 parts: sensor activation time + conversion time + channel switch delay.

The sensor activation time is the amount of settling time required for the sensor oscillation amplitude to stabilize, as shown in Figure 53. The settling wait time is programmable and should be set to a value that is long enough to allow stable oscillation. The settling wait time for channel x is given by:

$$t_{Sx} = (\text{SETTLECOUNTx} \times 16)/f_{REFx} \tag{9}$$

Table 40 illustrates the registers and values for configuring the settling time for each channel.

Table 40. Settling Time Register Configuration

CHANNEL (1)	REGISTER	FIELD	CONVERSION TIME (2)
0	SETTLECOUNT0, addr 0x10	SETTLECOUNT0 ['15:0]	$(\text{SETTLECOUNT0} \times 16)/f_{REF0}$
1	SETTLECOUNT1, addr 0x11	SETTLECOUNT1 [15:0]	$(\text{SETTLECOUNT1} \times 16)/f_{REF1}$
2	SETTLECOUNT2, addr 0x12	SETTLECOUNT2 [15:0]	$(\text{SETTLECOUNT2} \times 16)/f_{REF2}$
3	SETTLECOUNT3, addr 0x13	SETTLECOUNT3 [15:0]	$(\text{SETTLECOUNT3} \times 16)/f_{REF3}$

(1) Channels 2 and 3 are available only in the LDC1614.
(2) f_{REFx} is the reference frequency configured for the channel.

The SETTLECOUNTx for any channel x must satisfy:

$$\text{SETTLECOUNTx} \geq Q_{SENSORx} \times f_{REFx} / (16 \times f_{SENSORx})$$

where:

- $f_{SENSORx}$ = Sensor Frequency of Channel x
- f_{REFx} = Reference frequency for Channel x
- $Q_{SENSORx}$ = Quality factor of the sensor on Channel x. The sensor Q can be calculated with: (10)

$$Q = R_P \sqrt{\frac{C}{L}} \tag{11}$$

Round the result to the next highest integer (for example, if Equation 10 recommends a minimum value of 6.08, program the register to 7 or higher).

L, R_P and C values can be obtained by using Texas Instrument's WEBENCH® for the coil design.

8.1.4.2 Sensor Activation

The LDC1612/LDC1614 provides option to either reduce the sensor activation time or to reduce the device current consumption during the sensor activation time.

This can reduce the sensor activation time for higher-Q sensors by driving the maximum sensor drive current during the sensor settling time. The maximum sensor drive current is nominally 1.56 mA. Sensors already configured to use the maximum drive current setting (IDRIVEx = b11111) will see no change in operation based on this setting.

This mode is selected by setting SENSOR_ACTIVATE_SEL to 0.

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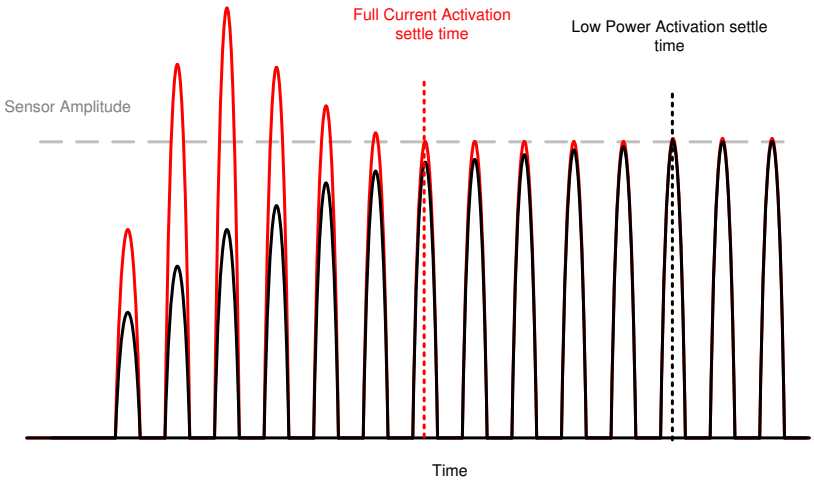

Figure 55. Sensor Full Current Activation vs. Low Power Activation

8.1.5 Sensor Current Drive Configuration

The registers listed in *Table 41* are used to control the sensor drive current so that the sensor signal amplitude is within the optimum range of 1.2 V_P to 1.8 V_P (sensor amplitudes outside this optimum range can be reported in the status register - refer to *Device Status Registers*). The device can still convert with sensor amplitudes lower than 0.6 V_P, however the conversion noise will increase with lower sensor amplitudes. Below 0.6 V_P the sensor oscillations may not be stable or may completely stop and the LDC will stop converting. If the current drive results in the oscillation amplitude greater than 1.8 V, the internal ESD clamping circuit will become active. This may cause the sensor frequency to shift so that the output values no longer represent a valid system state. Figure 56 shows the block diagram of the sensor driver. Each channel has an independent setting for the IDRIVE current used to set the sensor oscillation amplitude.

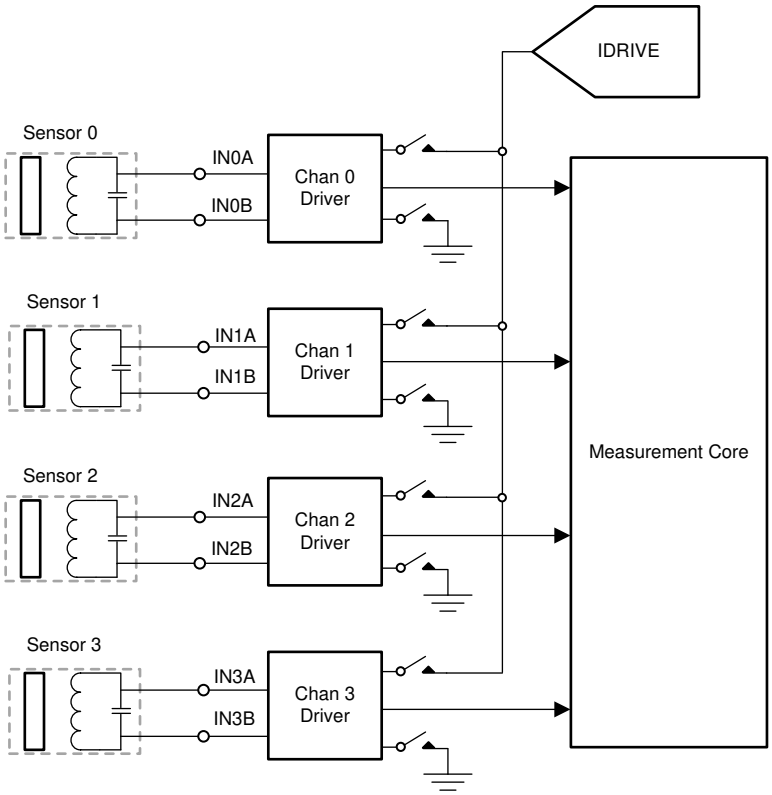

Figure 56. LDC1614 Sensor Driver Block Diagram

Table 41. Current Drive Control Registers

CHANNEL (1)	REGISTER	FIELD [BIT(S)]	VALUE
All	CONFIG, addr 0x1A	SENSOR_ACTIVATE_SEL [11]	Sets current drive for sensor activation. Recommended value is b0 (Full Current mode).
		RP_OVERRIDE_EN [12]	Set to b1 for normal operation (RP Override enabled)
		AUTO_AMP_DIS [10]	Disables Automatic amplitude correction. Set to b1 for normal operation (disabled)
0	CONFIG, addr 0x1A	HIGH_CURRENT_DRV [6]	b0 = normal current drive (1.5 mA) b1 = Increased current drive (> 1.5 mA) for Ch 0 in single channel mode only. Cannot be used in multi-channel mode.
0	DRIVE_CURRENT0, addr 0x1E	IDRIVE0 [15:11]	Drive current used during the settling and conversion time for Ch. 0 (auto-amplitude correction must be disabled and RP over ride=1)
		INIT_IDRIVE0 [10:6]	Initial drive current stored during auto-calibration. Not used for normal operation.
1	DRIVE_CURRENT1, addr 0x1F	IDRIVE1 [15:11]	Drive current used during the settling and conversion time for Ch. 1 (auto-amplitude correction must be disabled and RP over ride=1)
		INIT_IDRIVE1 [10:6]	Initial drive current stored during auto-calibration. Not used for normal operation.
2	DRIVE_CURRENT2, addr 0x20	IDRIVE2 [15:11]	Drive current used during the settling and conversion time for Ch. 2 (auto-amplitude correction must be disabled and RP over ride=1)
		INIT_IDRIVE2 [10:6]	Initial drive current stored during auto-calibration. Not used for normal operation.
3	DRIVE_CURRENT3, addr 0x21	IDRIVE3 [15:11]	Drive current used during the settling and conversion time for Ch. 3 (auto-amplitude correction must be disabled and RP over ride=1)
		INIT_IDRIVE3 [10:6]	Initial drive current stored during auto-calibration. Not used for normal operation.

(1) Channels 2 and 3 are available for LDC1614 only.

If the R_P value of the sensor attached to Channel x is known, Table 42 can be used to select the 5-bit value to be programmed into the IDRIVEx field for the channel. If the measured R_P (at maximum spacing between the sensor and the target) falls between two of the table values, use the current drive value associated with the lower R_P from the table. All channels that use an identical sensor/target configuration can use the same IDRIVEx value. The appropriate sensor drive current can be calculated with:

$$I_{DRIVE} = \pi V_P \div 4R_P \tag{12}$$

Table 42. Optimum Sensor R_P Ranges for Sensor IDRIVEx Setting.

IDRIVEx Register Field Value		Nominal Sensor Current (µA)	Minimum Sensor R_P (kΩ)	Maximum Sensor R_P (kΩ)
0	b00000	16	60.0	90.0
1	b00001	18	51.8	77.6
2	b00010	20	44.6	66.9
3	b00011	23	38.4	57.6
4	b00100	28	33.7	49.7
5	b00101	32	29.5	42.8
6	b00110	40	23.6	36.9
7	b00111	46	20.5	31.8
8	b01000	52	18.1	27.4

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Table 42. Optimum Sensor R_P Ranges for Sensor IDRIVEx Setting. (continued)

IDRIVEx Register Field Value		Nominal Sensor Current (µA)	Minimum Sensor R_P (kΩ)	Maximum Sensor R_P (kΩ)
9	b01001	59	16.1	23.6
10	b01010	72	13.1	20.4
11	b01011	82	11.5	17.6
12	b01100	95	9.92	15.1
13	b01101	110	8.57	13.0
14	b01110	127	7.42	11.2
15	b01111	146	6.46	9.69
16	b10000	169	5.58	8.35
17	b10001	195	4.83	7.20
18	b10010	212	4.45	6.21
19	b10011	244	3.86	5.35
20	b10100	297	3.17	4.61
21	b10101	342	2.76	3.97
22	b10110	424	2.22	3.42
23	b10111	489	1.93	2.95
24	b11000	551	1.71	2.54
25	b11001	635	1.48	2.19
26	b11010	763	1.24	1.89
27	b11011	880	1.07	1.63
28	b11100	1017	0.93	1.40
29	b11101	1173	0.80	1.21
30	b11110	1355	0.70	1.05
31	b11111	1563	0.60	0.90

Sensors with R_P greater than 90 kΩ can be driven by placing a 100 kΩ resistor in parallel with the sensor inductor to reduce the effective R_P.

Sensors which have a wide range of R_P may require more than one current drive setting across the range of operation - the current would need to be dynamically set based on the target position. Note that some high-resolution applications will experience an output code offset when the current drive is changed. Another approach for systems which have a wide range of R_P is to place a discrete resistor in parallel with the inductor to limit the range of R_P variation in the system. This will also reduce the sensor Q, and so may not be feasible for some implementations.

8.1.5.1 Inactive Channel Sensor Connections

The LDC1612/LDC1614 ties the INAx and INBx pins for all channels to ground by ~10 Ω except for the active channel; in Sleep and Shutdown modes there are no active channels and so all channels are tied to ground. By grounding the channels, potential interactions between sensors are minimized. For multi-channel sequencing, only the active channel is driven with the IDRIVE current during the conversion time; once the conversion for the specific channel completes, the sensor is tied to ground to shut off the sensor, and the next sensor is activated.

For systems which do not use all sensor channels, it is acceptable to leave the unused INAx and INBx pins No-Connect.

8.1.5.2 Automatic IDRIVE Setting with RP_OVERRIDE_EN

The LDC1612/LDC1614 can automatically determine the appropriate sensor current drive when entering Active Mode. For the majority of applications, it is recommended to program a fixed current drive for consistent measurement performance. The automatic sensor amplitude setting is useful for initial system prototyping if the sensor amplitude is unknown. When this function is enabled, the LDC attempts to find the IDRIVEx setting which results in a sensor amplitude between 1.2 V_P and 1.8V_P. For systems which have a large variation in target interaction, the LDC1612/LDC1614 may select a current drive setting which has poorer repeatability over the range of target interactions. In addition, measurement repeatability will be poorer with different sensor current drives. To enable the automatic sensor amplitude, set RP_OVERRIDE to b0.

The following sequence uses auto-calibration to configure sensor drive current for a sensor with an unknown R_P:

1. Set target at the maximum planned operating distance from the sensor.
2. Place the device into SLEEP mode by setting CONFIG.SLEEP_MODE_EN to b0.
3. Program the desired values of SETTLECOUNT and RCOUNT values for the channel.
4. Enable auto-calibration by setting RP_OVERRIDE_EN to b0.
5. Take the device out of SLEEP mode by setting CONFIG.SLEEP_MODE_EN to b1.
6. Allow the device to perform at least one measurement, with the target stable (fixed) at the maximum operating range.
7. Read the channel current drive value from the appropriate DRIVE_CURRENTx register (addresses 0x1e, 0x1f, 0x20, or 0x21), in the INIT_DRIVEx field (bits 10:6). Save this value.
8. During startup for normal operating mode, write the value saved from the INIT_DRIVEx bit field into the IDRIVEx bit field (bits 15:11).
9. During normal operating mode, the RP_OVERRIDE_EN should be set to b1 for a fixed current drive.

If the current drive results in the oscillation amplitude greater than 1.8 V, the internal ESD clamping circuit will become active. This may cause the sensor frequency to shift so that the output values no longer represent a valid system state. If the current drive is set at a lower value, the SNR performance of the system will decrease, and at near zero target range, oscillations may completely stop, and the output sample values will be all zeroes.

If there are significant differences in the sensor construction for different channels, then this process should be repeated for each channel.

8.1.5.3 Determining Sensor IDRIVE for an Unknown Sensor R_P Using an Oscilloscope

If the sensor R_P is not known, probing the sensor amplitude with an oscilloscope can be used set IDRIVEx.

An iterative process of adjusting the drive current setting while monitoring the signal amplitude on INAx or INBx to ground is sufficient. Simply move the sensor target to the farthest planned operating distance from the sensor, and measure the channel amplitude after the amplitude has stabilized. If the sensor amplitude is less than 1.5 V_P, increase the channel IDRIVE setting. If the sensor amplitude settles to greater than 1.75 V_P, decrease the channel IDRIVE setting. If there are significant differences in the sensor construction for different channels, then this process should be repeated for each channel.

8.1.5.4 Sensor Auto-Calibration Mode

The LDC includes a sensor current Auto-calibration mode which can be dynamically set the sensor drive current. The auto-amplitude correction attempts to maintain the sensor oscillation amplitude between 1.2V and 1.8V by adjusting the sensor drive current between conversions.

This functionality is enabled by setting AUTO_AMP_DIS to b0, and applies to all active channels. The INIT_IDRIVEx register field will be updated with the current drive value as the sensor current drive setting changes. The value of the INIT_IDRIVEx register field matches the setting of the IDRIVEx register field. For example, an INIT_IDRIVEx field with b10001 corresponds to a current drive of 195 µA.

When auto-amplitude correction is active, the output data may experience offsets in the channel output code due to adjustments in drive current. Due to these offsets, Auto-amplitude correction is generally not recommended for use in high precision applications.

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8.1.5.5 Channel 0 High Current Drive

Channel 0 provides a high sensor current drive mode to drive sensor coils with a typical drive current >3.5 mA. This feature can be used to drive sensors with an R_P lower than 350 Ω. Set the HIGH_CURRENT_DRV field to b1 to enable this mode. This drive mode is only available on Channel 0, and can only be enabled in single channel mode (AUTOSCAN_EN = 0).

8.1.6 Clocking Architecture

Optimum LDC1612/LDC1614 performance requires a clean reference clock with a limited frequency range. The device provides digital dividers for the f_{CLK} and the sensor inputs to adjust the effective frequency. For most systems, the maximum permitted reference frequency provides the best performance. The dividers provide flexibility in system design so that the full range of sensor frequencies can be supported with available f_{CLK}. Each channel has a dedicated divider configuration.

Figure 57 shows the clock dividers and multiplexers of the LDC.

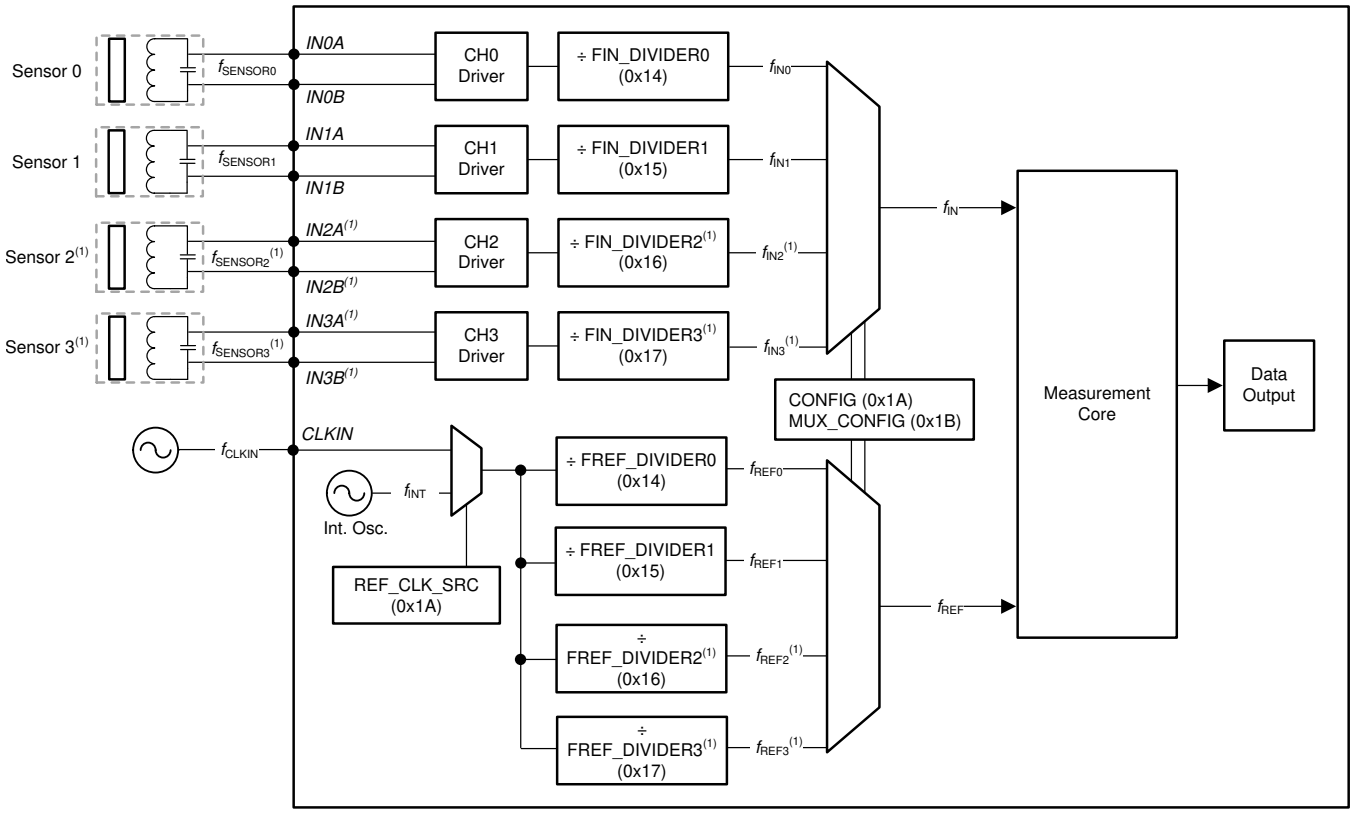

Figure 57. Clocking Diagram

(1) LDC1614 only

In Figure 57, the key clocks are f_{INx}, f_{REFx}, and f_{CLK}. f_{CLK} is selected from either the internal clock source or external clock source (CLKIN). The frequency measurement reference clock, f_{REF}, is derived from the f_{CLK} source.

The internal oscillator (f_{INT}) is highly stable across temperature and is suitable for applications when the maximum performance of the LDC1612/4 is not needed or when an external oscillator is not available. For precision applications, it is recommended to use an external oscillator for the reference clock; the external oscillator should offer the stability and accuracy requirements suitable for the application. Note that some internal functions, such as watchdog timers, always use f_{INT} for timing.

The f_{INx} clock is derived from sensor frequency for channel x, $f_{SENSORx}$. f_{REFx} and f_{INx} must meet the requirements listed in Table 43, depending on whether f_{CLK} (reference clock) is the internal or external clock.

Table 43. Clock Frequency Requirements

MODE (1)	REFERENCE SOURCE	VALID f_{REFx} RANGE	VALID f_{INx} RANGE	SET FIN_DIVIDERx to	VALID SETTLECOUNTx SETTINGS	VALID RCOUNTx SETTINGS
Multi-Channel	Internal	f_{REFx} ≤ 55 MHz	< f_{REFx} /4	≥ b0001 (2)	> 3	> 8
	External	f_{REFx} ≤ 40 MHz				
Single-Channel	Either external or internal	f_{REFx} ≤ 35 MHz				

(1) Channels 2 and 3 are only available for LDC1614
(2) If f_{SENSOR} ≥ 8.75 MHz, then FIN_DIVIDERx must be ≥ 2

Table 44 shows the clock configuration registers. Each input channel has a dedicated configuration which can be set independently.

Table 44. Clock Configuration Registers

CHANNEL (1)	CLOCK	REGISTER	FIELD	VALUE
All	f_{CLK} = Reference Clock Source	CONFIG, addr 0x1A	REF_CLK_SRC [9]	b0 = internal oscillator is used as the reference clock b1 = external clock source is used as the reference clock
0	f_{REF0}	CLOCK_DIVIDERS0, addr 0x14	FREF_DIVIDER0 [9:0]	f_{REF0} = f_{CLK} / FREF_DIVIDER0
1	f_{REF1}	CLOCK_DIVIDERS1, addr 0x15	FREF_DIVIDER1 [9:0]	f_{REF1} = f_{CLK} / FREF_DIVIDER1
2	f_{REF2}	CLOCK_DIVIDERS2, addr 0x16	FREF_DIVIDER2 [9:0]	f_{REF2} = f_{CLK} / FREF_DIVIDER2
3	f_{REF3}	CLOCK_DIVIDERS3, addr 0x17	FREF_DIVIDER3 [9:0]	f_{REF3} = f_{CLK} / FREF_DIVIDER3
0	f_{IN0}	CLOCK_DIVIDERS0, addr 0x14	FIN_DIVIDER0 [15:12]	f_{IN0} = $f_{SENSOR0}$ / FIN_DIVIDER0
1	f_{IN1}	CLOCK_DIVIDERS1, addr 0x15	FIN_DIVIDER1 [15:12]	f_{IN1} = $f_{SENSOR1}$ / FIN_DIVIDER1
2	f_{IN2}	CLOCK_DIVIDERS2, addr 0x16	FIN_DIVIDER2 [15:12]	f_{IN2} = $f_{SENSOR2}$ / FIN_DIVIDER2
3	f_{IN3}	CLOCK_DIVIDERS3, addr 0x17	FIN_DIVIDER3 [15:12]	f_{IN3} = $f_{SENSOR3}$ / FIN_DIVIDER3

(1) Channels 2 and 3 are only available for LDC1614

8.1.7 Input Deglitch Filter

The input deglitch filter suppresses EMI and ringing above the sensor frequency. It does not impact the conversion result as long as its bandwidth is configured to be above the maximum sensor frequency. The input deglitch filter can be configured in MUX_CONFIG.DEGLITCH register field as shown in Table 45. This setting applies to all channels. For optimal performance, it is recommended to select the lowest setting that exceeds the highest sensor oscillation frequency for all selected channels. For example, if the maximum sensor frequency is 2.8 MHz, choose MUX_CONFIG.DEGLITCH = b100 (3.3 MHz).

Table 45. Input Deglitch Filter Register

CHANNEL (1)	MUX_CONFIG.DEGLITCH REGISTER VALUE	DEGLITCH FREQUENCY
ALL	b001	1.0 MHz
ALL	b100	3.3 MHz
ALL	b101	10 MHz
ALL	b011	33 MHz

(1) Channels 2 and 3 are available for LDC1614 only.

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8.1.8 Device Status Registers

The LDC1612/LDC1614 can monitor and report on conversion results and the status of attached sensors using the registers listed in Table 46.

Table 46. Status Registers

CHANNEL (1)	REGISTER	FIELDS [BIT(S)]	VALUES
All	STATUS, addr 0x18	12 fields are available that contain various status bits [15:0]	Refer to Register Maps section for a description of the individual status bits.
All	ERROR_CONFIG, addr 0x19	12 fields are available that are used to configure error reporting [15:0]	Refer to Register Maps section for a description of the individual error configuration bits.

(1) Channels 2 and 3 are available for LDC1614 only.

See the STATUS (Table 25) and ERROR_CONFIG (Table 26) register descriptions in the Register Map section. These registers can be configured to trigger an interrupt on the INTB pin for certain events. The following conditions must be met:

1. The error or status register must be unmasked by enabling the appropriate register bit in the ERROR_CONFIG register.
2. The INTB function must be enabled by setting CONFIG.INTB_DIS to 0.

When a bit field in the STATUS register is set, the entire STATUS register content is held until read or until the DATAx_MSB register is read. Reading also de-asserts INTB. After first starting conversions in active mode, the first read of STATUS should performed be after assertion of INTB.

Interrupts are cleared by one of the following events:

1. Entering Sleep Mode
2. Power-on reset (POR)
3. Device enters Shutdown Mode (SD is asserted)
4. S/W reset
5. I2C read of the STATUS register: Reading the STATUS register will clear any error status bit set in STATUS along with the ERR_CHAN field and de-assert INTB

Setting register CONFIG.INTB_DIS to b1 disables the INTB function and holds the INTB pin high.

The TI Application Note *LDC1312, LDC1314, LDC1612, LDC1614 Sensor Status Monitoring* provides detailed information on sensor status reporting.

8.1.9 Multi-Channel Data Readback

When in multi-channel mode, the LDC1612/LDC1614 alternates conversions on all selected channels. After each channel conversion completes, the conversion results for that channel overwrites the previous conversion results with the new data. Note that the LDC1612/LDC1614 conversion data spans 2 registers. To avoid multi-conversion data corruption, the conversion results are stored in an internal buffer after every conversion, but the I2C DATAx field is only updated to reflect new data when the DATAx_MSB register is read.

When the device completes a conversion on the last channel in the selected group, the device will pull INTB low if DRDY2INT is set to 1. At this time, the conversion results should be retrieved via the I2C bus.

If the device is put into Sleep mode or Shutdown mode, all DATAx_MSB and DATAx_LSB registers are cleared of conversion data.

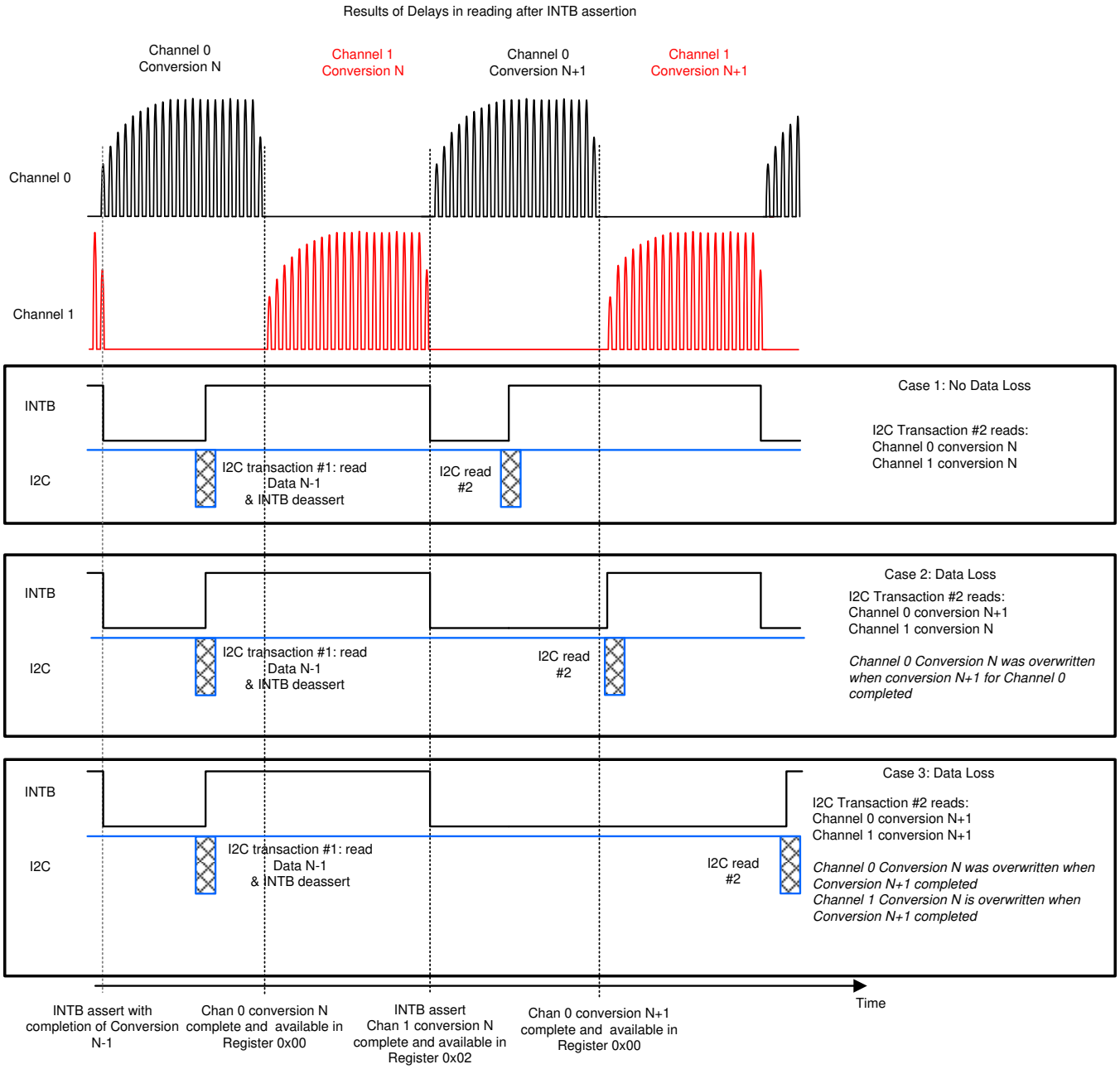

Figure 58. Data Readback Timing

The STATUS register (Address 0x18) flags UNREADCONVx monitor the accesses to the DATAx registers.

When the DATAx_MSB register is read, the DATAx_LSB register is updated with the corresponding LSB conversion data, and the UNREADCONVx flag is cleared. If the DATAx_LSB register alone is read, it will not update and will continuously return data corresponding to the last DATAx_MSB register read.

As shown in Figure 58 , if the I2C data readback is delayed, then it is possible to lose older, unread conversion results. Monitoring the UNREADCONVx flags are useful to assess whether data loss is occurring.

A delayed read of previous conversion results can produce the condition in which reading the STATUS register immediately after INTB asserts shows that Channel 0 has no unread data (where the UNREADCONV0 flag is 0), but other channels do have unread data indicated by the corresponding UNREADCONVx flags.

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8.2 Typical Application

8.2.1 System Sensing Functionality

Inductive sensing provides a wide range of system advantages that no other technology can provide - contact-less measurement, resistance to dirt/dust/water, immunity to external magnets, remote sensor positioning, inexpensive and robust sensors, and extremely high resolution measurement of relative movement.

The LDC1612/LDC1614 can be used to sense a wide range of applications for measuring a variety of target movement:

- Angular Measurement: refer to *1-Degree Dial Reference Design* for an example implementation.
- Linear Position Sensing: details on sensor and target construction are available in *LDC1612/LDC1614 Linear Position Sensing Application Note*. For absolute positioning needs, it is recommended to use a differential 2 channel construction.
- Inductive Touch-on-Metal buttons: refer to TI Applications Note *Inductive Sensing Touch-On-Metal Buttons Design Guide* for system design information and *16 Button Inductive Touch Stainless Steel Keypad Reference Design* for an example system implementation.
-

8.2.2 Example Application

Example of a multi-channel implementation using the LDC1612. This example is representative of an axial displacement application, in which the target movement is perpendicular to the plane of the coil. The second channel can be used to sense proximity of a second target, or it can be used for environmental compensation by connecting a reference coil.

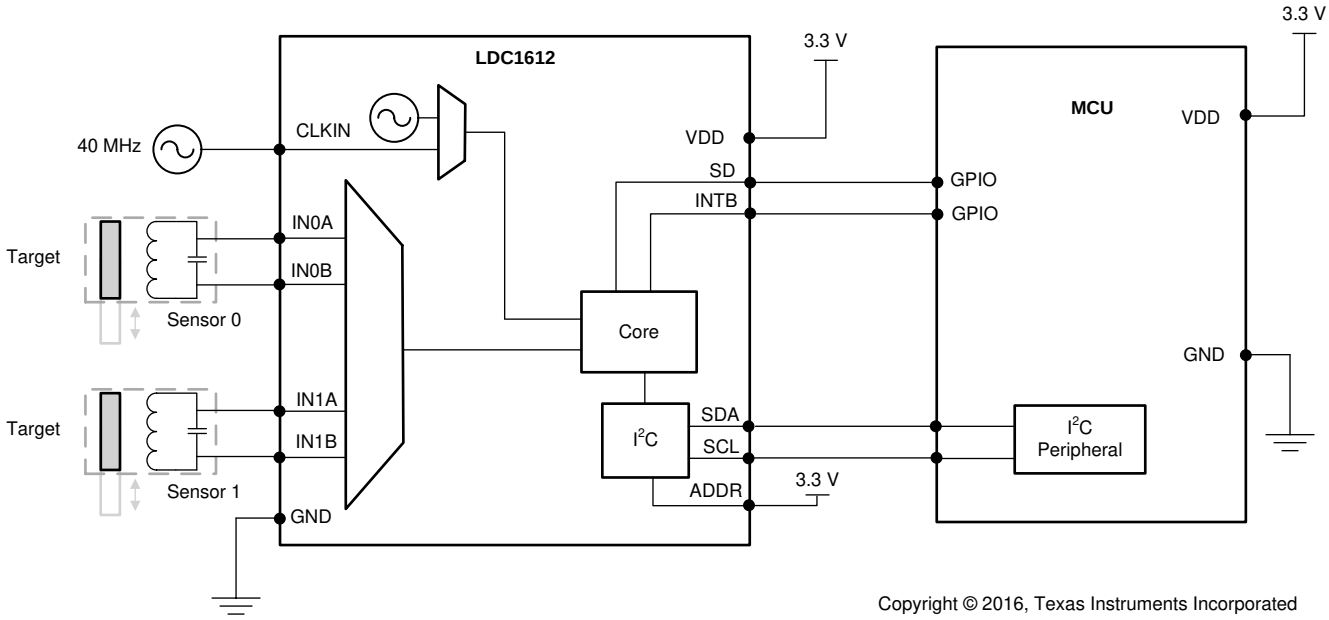

Figure 59. Example Multi-Channel Application - LDC1612

8.2.3 Design Requirements

Design example in which Sensor 0 is used for proximity measurement and Sensor 1 is used for temperature compensation. WEBENCH coil designer tool used to create sensor. System measurement requirements:

- Target distance = 1.0 mm
- Distance resolution = 0.2 µm
- Target diameter = 10 mm
- Target material = stainless steel (SS416)
- Number of PCB layers for the coil = 2
- The application requires 500 SPS (T_{SAMPLE} = 2.00 ms)

Typical Application (continued)

8.2.4 Detailed Design Procedure

The target distance, resolution and diameter are used as inputs to WEBENCH to design the sensor coil, The resulting coil design is a 2 layer coil, with an area of 2.5 cm^2, diameter of 17.7 mm, and 39 turns. The values for R_P, L and C are: R_P = 6.6 kΩ, L = 43.9 µH, C = 100 pF.

Using the L and C to determine $f_{SENSOR} = 1/2\pi\sqrt{(LC)} = 1/2\pi\sqrt{(43.9*10^{-6} * 100*10^{-12})} = 2.4$ MHz

With a system reference clock of 40 MHz applied to the CLKIN pin allows flexibility for setting the internal clock frequencies. The sensor coil is connected to channel 0 (IN0A and IN0B pins).

After powering on the LDC, it will be in Sleep Mode. Program the registers as follows (this example sets registers for channel 0 only; channel 1 registers can use equivalent configuration):

1. Set the dividers for Channel 0.
   a. Because the sensor frequency is less than 8.75 MHz, the sensor divider can be set to 1, which means setting field FIN_DIVIDER0 to 0x1. By default, $f_{IN0} = f_{SENSOR}$ = 2.4 MHz.
   b. The design constraint for f_{REF0} is > 4 × f_{SENSOR}. The 40 MHz reference frequency satisfies this constraint, so the reference divider can be set to 1. This is done by setting the FREF_DIVIDER0 field to 0x01.
   c. The combined value for Chan. 0 divider register (0x14) is 0x1002.
2. Program the settling time for Channel 0. The calculated Q of the coil is 10 (see *Multi-Channel and Single Channel Operation*).
   a. SETTLECOUNT0 ≥ Q × f_{REF0} / (16 × $f_{SENSOR0}$) → 5.2, rounded up to 6. To provide margin to account for system tolerances, a higher value of 10 is chosen.
   b. Register 0x10 should be programmed to a minimum of 10.
   c. The settle time is: (10 x 16)/20,000,000 = 8 µs
   d. The value for SETTLECOUNT0 register (0x10) is 0x000A.
3. The channel switching delay is ~1 µs for f_{REF} = 20 MHz (see *Multi-Channel and Single Channel Operation*)
4. Set the conversion time by the programming the reference count for Channel 0. The budget for the conversion time is : T_{SAMPLE} – settling time – channel switching delay = 1000 – 8 – 1 = 991 µs
   a. To determine the conversion time register value, use the following equation and solve for RCOUNT0: Conversion Time (t_{C0})= (RCOUNT0×16)/f_{REF0}.
   b. This results in RCOUNT0 having a value of 1238 decimal (rounded down)
   c. Set the RCOUNT0 register (0x08) to 0x04D6.
5. Use the default values for the ERROR_CONFIG register (address 0x19). By default, no interrupts are enabled
6. Sensor drive current: to set the IDRIVE0 field value, read the value from Figure 55 using R_P = 6.6 kΩ. In this case IDRIVE0 value should be set to 18 (decimal). The INIT_DRIVE0 current field should be set to 0x00. The combined value for the DRIVE_CURRENT0 register (addr 0x1E) is 0x9000.
7. Program the MUX_CONFIG register
   a. Set the AUTOSCAN_EN to b1 bit to enable sequential mode
   b. Set RR_SEQUENCE to b00 to enable data conversion on two channels (channel 0, channel 1)
   c. Set DEGLITCH to b100 to set the input deglitch filter bandwidth to 3.3MHz, the lowest setting that exceeds the oscillation tank frequency.
   d. The combined value for the MUX_CONFIG register (address 0x1B) is 0x820C
8. Finally, program the CONFIG register as follows:
   a. Set the ACTIVE_CHAN field to b00 to select channel 0.
   b. Set SLEEP_MODE_EN field to b0 to enable conversion.
   c. Set RP_OVERRIDE_EN to b1 to disable auto-calibration.
   d. Set SENSOR_ACTIVATE_SEL = b0, for full current drive during sensor activation
   e. Set the AUTO_AMP_DIS field to b1 to disable auto-amplitude correction
   f. Set the REF_CLK_SRC field to b1 to use the external clock source.
   g. Set the other fields to their default values.

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Typical Application (continued)

h. The combined value for the CONFIG register (address 0x1A) is 0x1601.

We then read the conversion results for channel 0 and channel 1 every 1.00 ms from register addresses 0x00 to 0x03.

8.2.5 Recommended Initial Register Configuration Values

Based on the example configuration in section *Detailed Design Procedure*, the following register write sequence is recommended:

Table 47. Recommended Initial Register Configuration Values (Single-Channel Operation)

ADDRESS	VALUE	REGISTER NAME	COMMENTS
0x08	0x04D6	RCOUNT0	Reference count calculated from timing requirements (1 kSPS) and resolution requirements
0x10	0x000A	SETTLECOUNT0	Minimum settling time for chosen sensor
0x14	0x1002	CLOCK_DIVIDERS0	FIN_DIVIDER0 = 1, FREF_DIVIDER0 = 2
0x19	0x0000	ERROR_CONFIG	Can be changed from default to report status and error conditions
0x1B	0x020C	MUX_CONFIG	Enable Channel 0 in continuous mode, set Input deglitch bandwidth to 3.3MHz
0x1E	0x9000	DRIVE_CURRENT0	Sets sensor drive current on channel 0
0x1A	0x1601	CONFIG	Select active channel = ch 0, disable auto-amplitude correction and auto-calibration, enable full current drive during sensor activation, select external clock source, wake up device to start conversion. This register write must occur last because device configuration is not permitted while the LDC is in active mode.

Table 48. Recommended Initial Register Configuration Values (Multi-Channel Operation)

ADDRESS	VALUE	REGISTER NAME	COMMENTS
0x08	0x04D6	RCOUNT0	Reference count calculated from timing requirements (1 kSPS) and resolution requirements
0x09	0x04D6	RCOUNT1	Reference count calculated from timing requirements (1 kSPS) and resolution requirements
0x10	0x000A	SETTLECOUNT0	Minimum settling time for chosen sensor
0x11	0x000A	SETTLECOUNT1	Minimum settling time for chosen sensor
0x14	0x1002	CLOCK_DIVIDERS0	FIN_DIVIDER0 = 1, FREF_DIVIDER0 = 2
0x15	0x1002	CLOCK_DIVIDERS_1	FIN_DIVIDER1 = 1, FREF_DIVIDER1 = 2
0x19	0x0000	ERROR_CONFIG	Can be changed from default to report status and error conditions
0x1B	0x820C	MUX_CONFIG	Enable Ch 0 and Ch 1 (sequential mode), set Input deglitch bandwidth to 3.3MHz
0x1E	0x9000	DRIVE_CURRENT0	Sets sensor drive current on ch 0
0x1F	0x9000	DRIVE_CURRENT1	Sets sensor drive current on ch 1
0x1A	0x1601	CONFIG	Disable auto-amplitude correction and auto-calibration, enable full current drive during sensor activation, select external clock source, wake up device to start conversion. This register write must occur last because device configuration is not permitted while the LDC is in active mode.

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8.2.6 Application Curves

Common Test Conditions (unless specified otherwise):

- Sensor inductor: 2 layer, 32 turns/layer, 14mm diameter, PCB inductor with L=19.4 µH, R_P=5.7 kΩ at 2 MHz
- Sensor capacitor: 330 pF 1% COG/NP0
- Target: Aluminum, 1.5 mm thickness
- Channel = Channel 0 (continuous mode)
- f_{CLKIN} = 40 MHz, FIN_DIVIDERx = 0x01, FREF_DIVIDERx = 0x001
- RCOUNT0 = 0xFFFF, SETTLECOUNT0 = 0x0100
- RP_OVERRIDE = 1, AUTO_AMP_DIS = 1, DRIVE_CURRENT0 = 0x9800

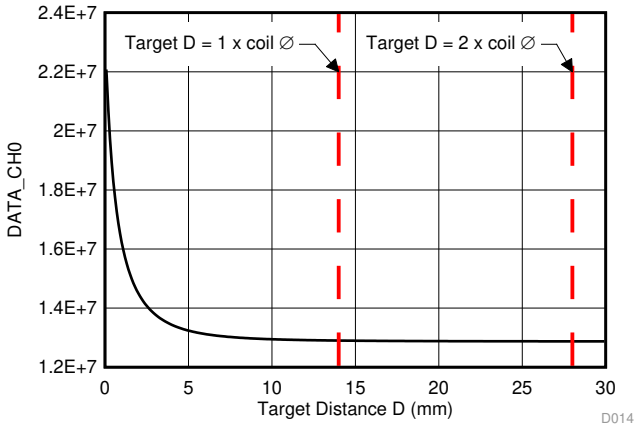

Figure 60. Output Code vs. Target Distance (0 to 30mm)

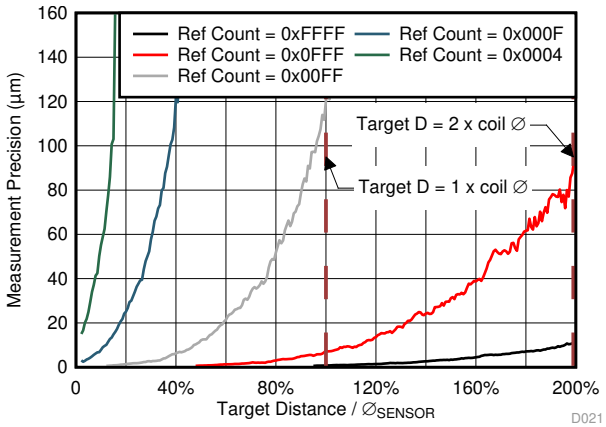

Figure 61. Measurement Precision in Distance vs. Target Distance (0 to 30mm)

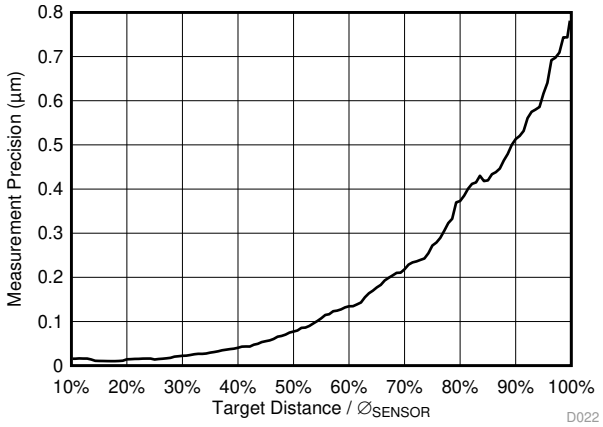

Figure 62. Measurement Precision in Distance vs. Target Distance (0 to 10mm)

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8.2.7 Inductor Self-Resonant Frequency

Every inductor has a distributed parasitic capacitance, which is dependent on construction and geometry. At the Self-Resonant Frequency (SRF), the reactance of the inductor cancels the reactance of the parasitic capacitance. Above the SRF, the inductor will electrically appear to be a capacitor. Because the parasitic capacitance is not well-controlled or stable, it is recommended that: $f_{SENSOR} < 0.8 \times f_{SR}$.

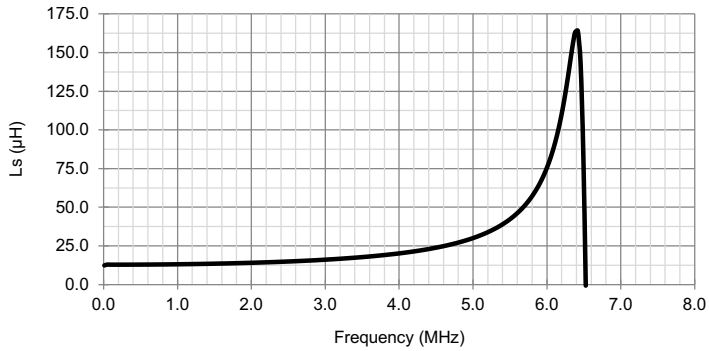

Figure 63. Example Coil Inductance vs. Frequency

In Figure 63, the inductor has a SRF at 6.38 MHz; therefore the inductor should not be operated above 0.8×6.38 MHz, or 5.1 MHz.

9 Power Supply Recommendations

- The LDC requires a voltage supply within 2.7 V and 3.6 V. A multilayer ceramic X7R bypass capacitor of 1 µF between the VDD and GND pins is recommended. If the supply is located more than a few inches from the LDC, additional capacitance may be required in addition to the ceramic bypass capacitor. A ceramic capacitor with a value of 10 µF is a typical choice.
- The optimum placement of bypass capacitors is closest to the VDD and GND terminals of the device. Care should be taken to minimize the loop area formed by the bypass capacitor connection, the VDD pin, and the GND pin of the IC. See Figure 64 for a layout example.

10 Layout

10.1 Layout Guidelines

Avoid long traces between the sensor and the LDC - higher frequency sensors may need to be placed closer to the device to minimize noise. The INAx and INBx traces should be routed as differential pairs - run the traces in parallel and close together. Lower trace impedances (even well below 100 Ω) are acceptable, as they reduce any parasitic inductance.

The sensor capacitor should be placed close to the inductor to minimize the sensor R_P.

Do not place filled planes underneath or between the sensor layers. If the sensor is placed in a plane, there should be a gap of at least 20% of a sensor diameter between the plane and the outermost coil of the sensor. There should not be any continuous ring of conductors encircling the sensor. This can be managed with a small cut in the conductor.

Refer to the TI Application Note *LDC Sensor Design* for more information on sensor design and optimization.

10.2 Layout Example

Figure 64 shows an example layout for the LDC1612, including a pair of sensors.

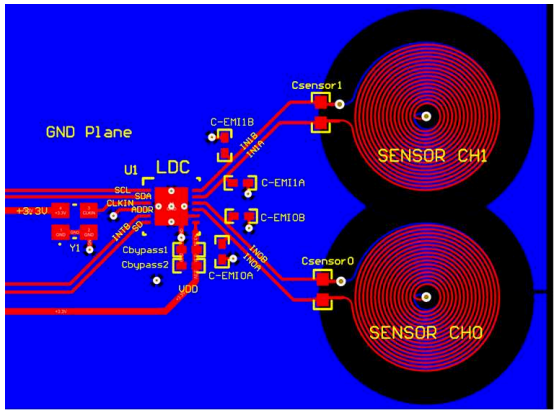

Figure 64. Example PCB Layout

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For related links, see the following:

- Texas Instruments' WEBENCH tool: http://www.ti.com/webench

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, refer to the following:

- *LDC1000 Temperature Compensation* SNAA212
- *LDC Sensor Design* SNOA930
- *LDC1612/LDC1614 Linear Position Sensing Application Note* SNOA931
- *Optimizing L Measurement Resolution for the LDC1312 and LDC1314* SNOA945
- *Power Reduction Techniques for the LDC131x/161x for Inductive Sensing* SNOA949
- *Optimizing L Measurement Resolution for the LDC161x and LDC1101* SNOA950
- *Inductive Sensing Touch-On-Metal Buttons Design Guide* SNOA951
- *LDC Target Design* SNOA957
- *LDC1312, LDC1314, LDC1612, LDC1614 Sensor Status Monitoring* SNOA959
- *16 Button Inductive Touch Stainless Steel Keypad Reference Design*
- *Inductive Sensing 32-Position Encoder Knob Reference Design*
- *16-Button Inductive Keypad Reference Design*
- *1-Degree Dial Reference Design*

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 49. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LDC1612	Click here	Click here	Click here	Click here	Click here
LDC1614	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

11.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LDC1612DNTR	Active	Production	WSON (DNT) | 12	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LDC1612
LDC1612DNTR.A	Active	Production	WSON (DNT) | 12	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LDC1612
LDC1612DNTR.B	Active	Production	WSON (DNT) | 12	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LDC1612
LDC1612DNTT	Obsolete	Production	WSON (DNT) | 12	-	-	Call TI	Call TI	-40 to 125	LDC1612
LDC1614RGHR	Active	Production	WQFN (RGH) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LDC1614
LDC1614RGHR.A	Active	Production	WQFN (RGH) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LDC1614
LDC1614RGHR.B	Active	Production	WQFN (RGH) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LDC1614
LDC1614RGHT	Obsolete	Production	WQFN (RGH) | 16	-	-	Call TI	Call TI	-40 to 125	LDC1614

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LDC1612, LDC1614 :

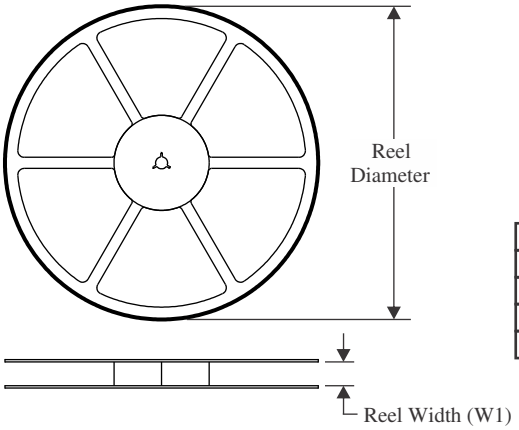
- Automotive : LDC1612-Q1, LDC1614-Q1

NOTE: Qualified Version Definitions:

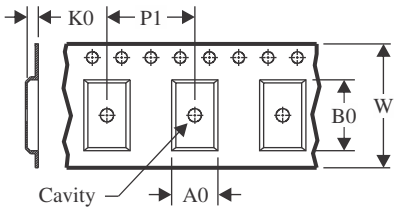
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

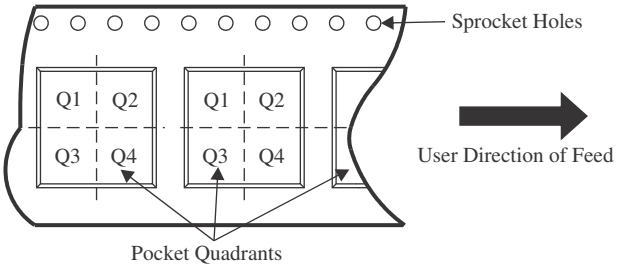


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

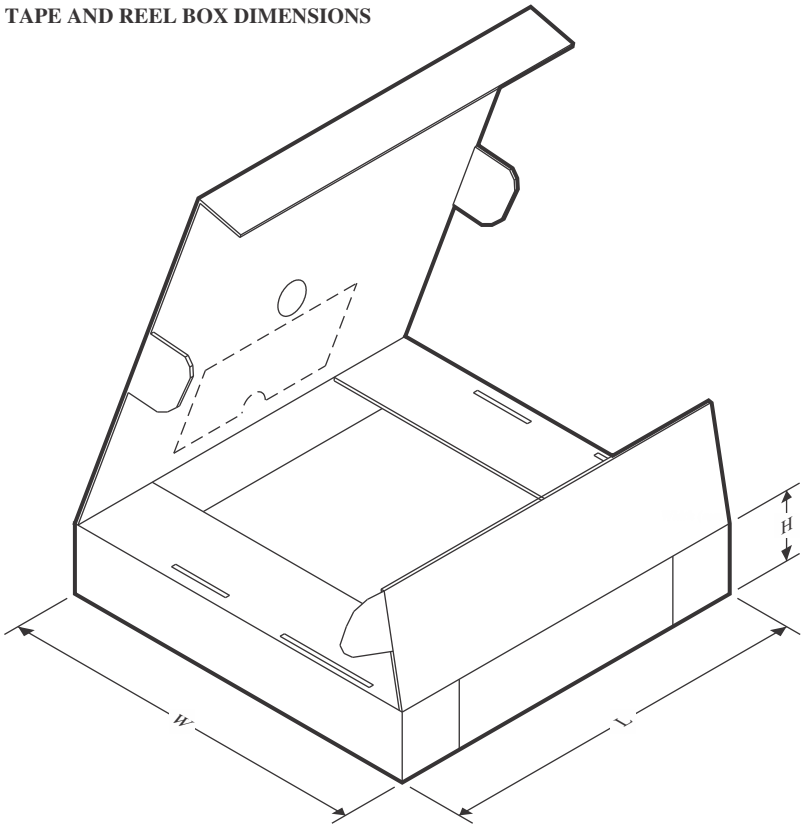
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

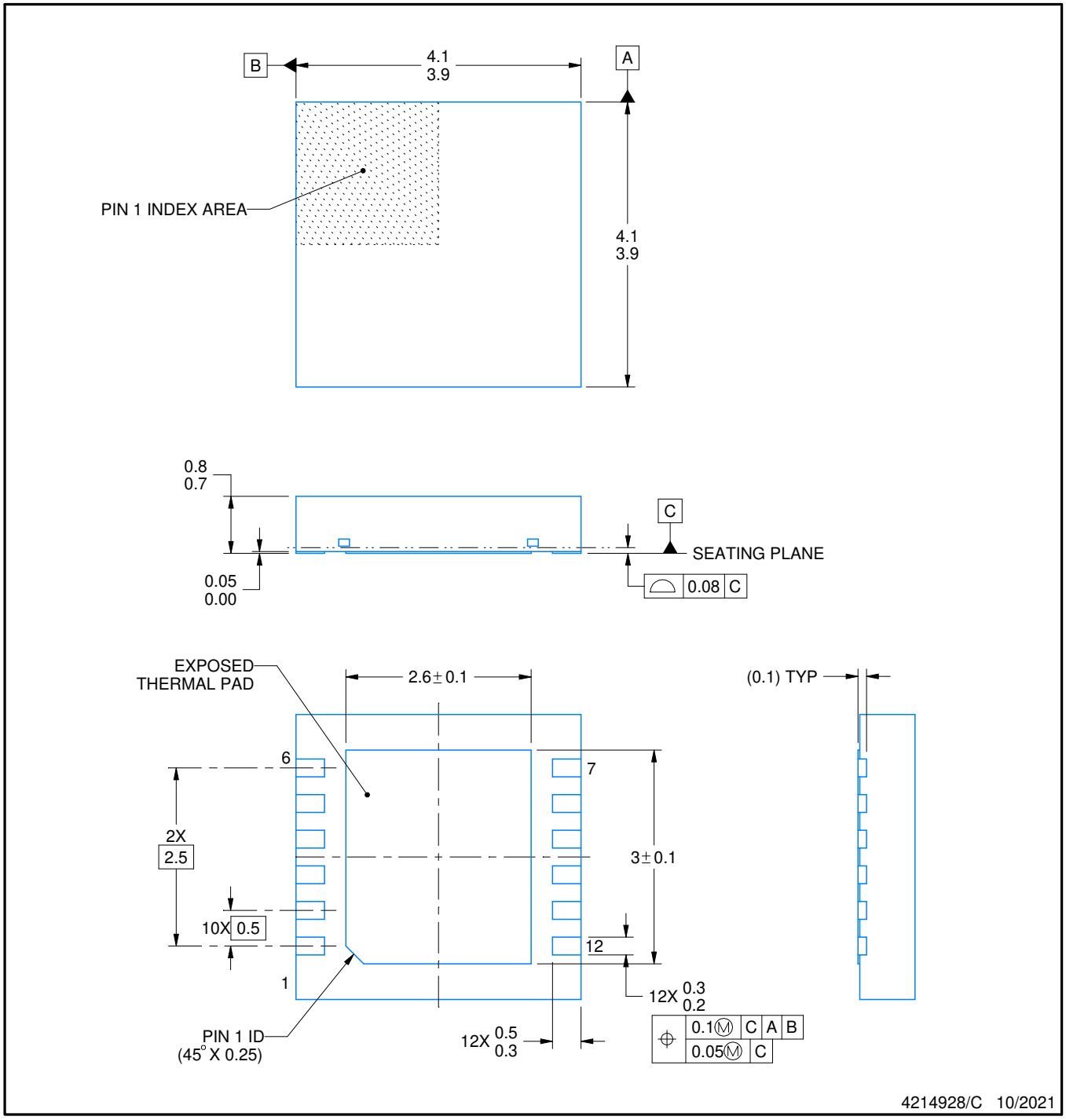
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LDC1612DNTR	WSON	DNT	12	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LDC1614RGHR	WQFN	RGH	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



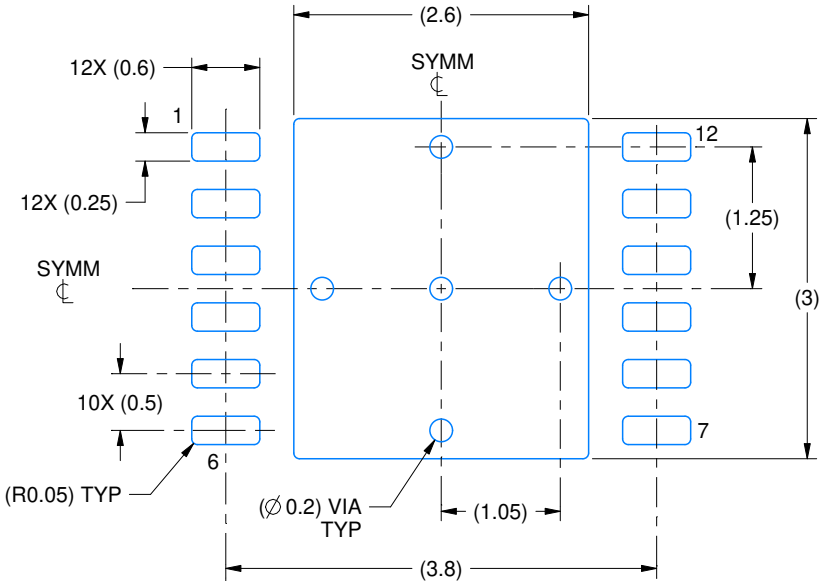
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LDC1612DNTR	WSON	DNT	12	4500	367.0	367.0	35.0
LDC1614RGHR	WQFN	RGH	16	4500	367.0	367.0	35.0

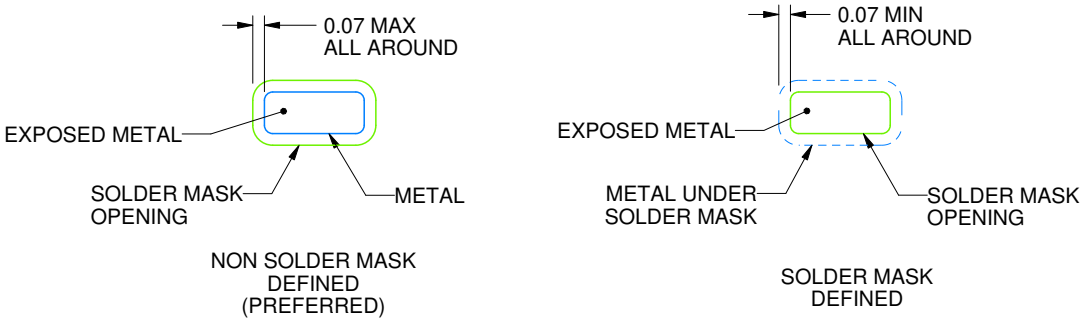


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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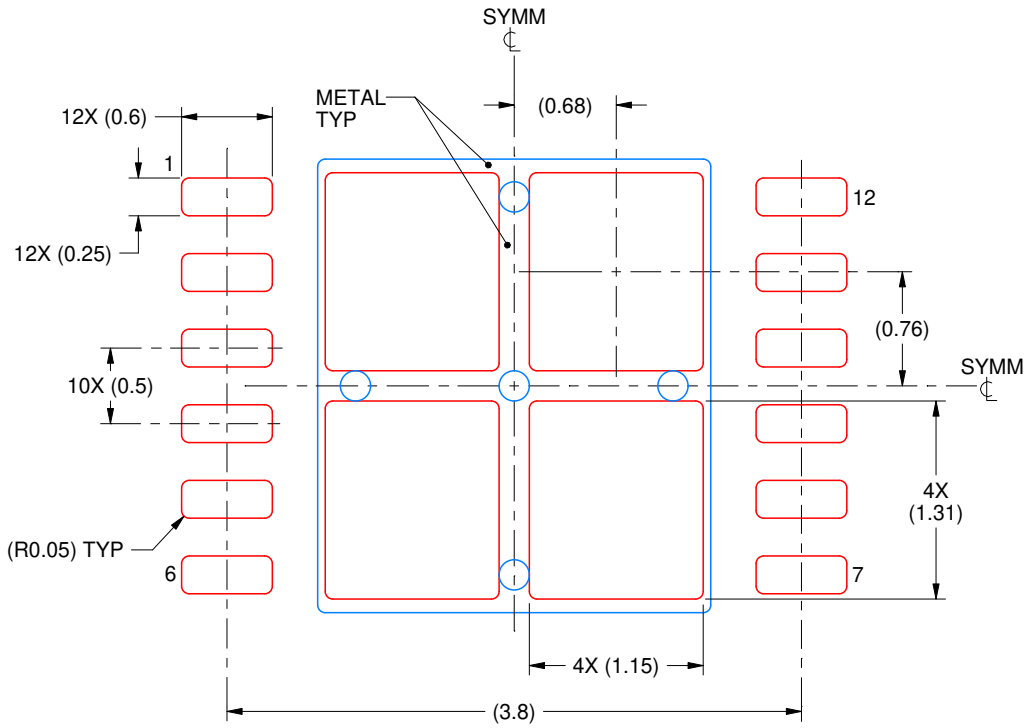
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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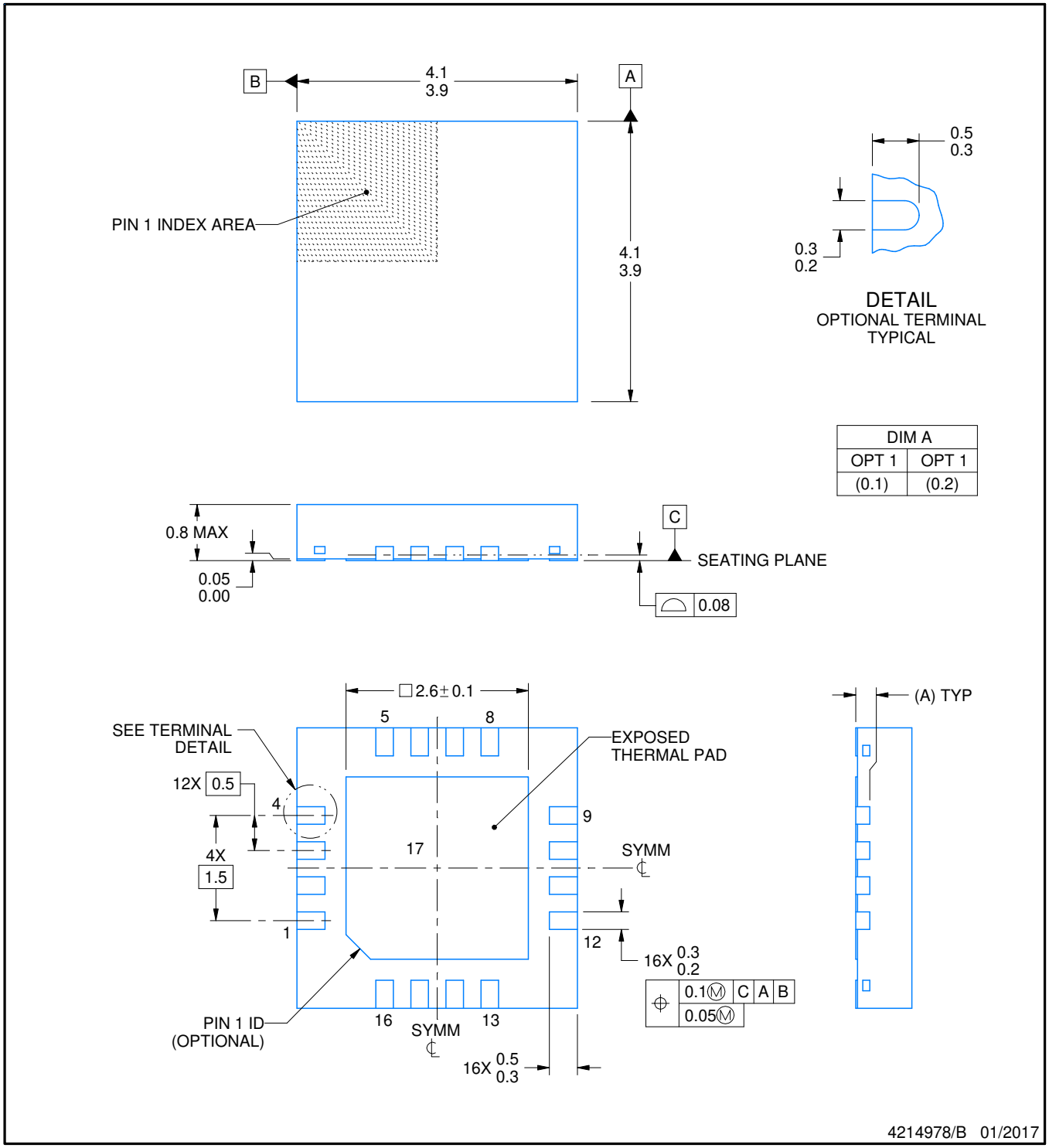
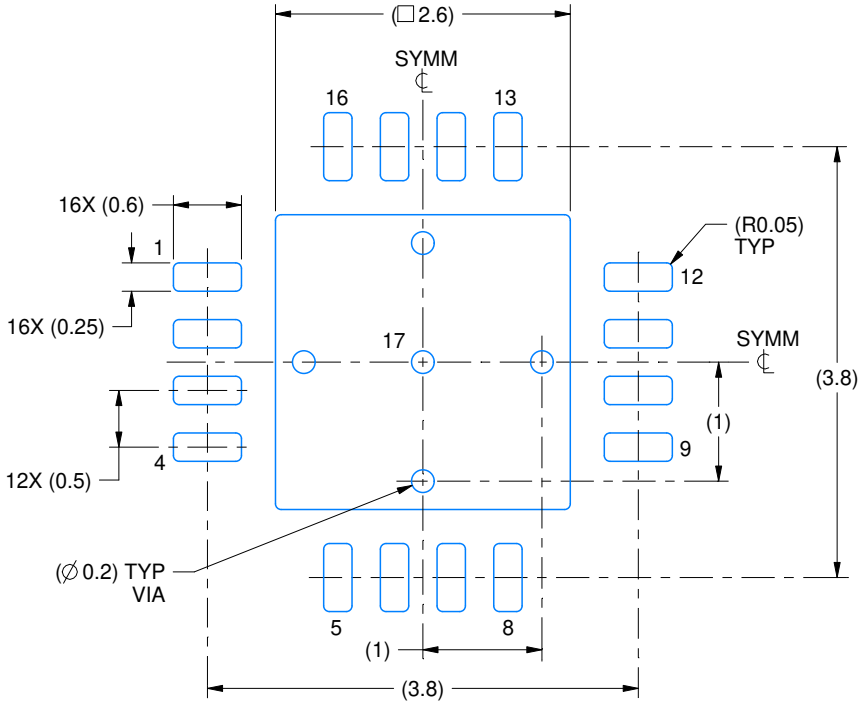
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

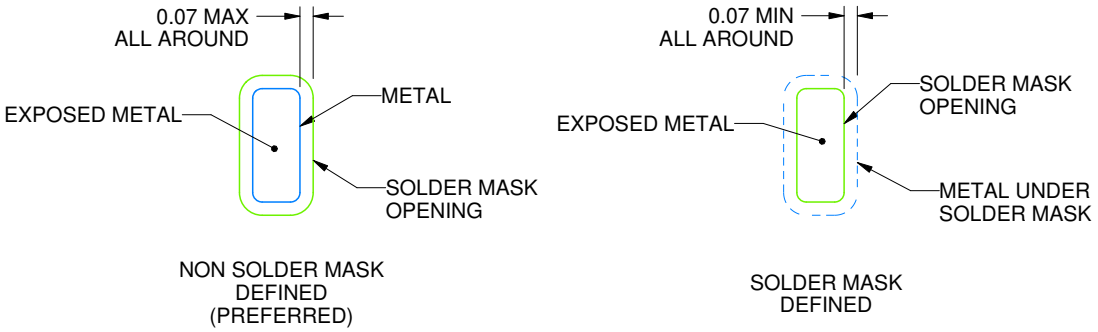


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

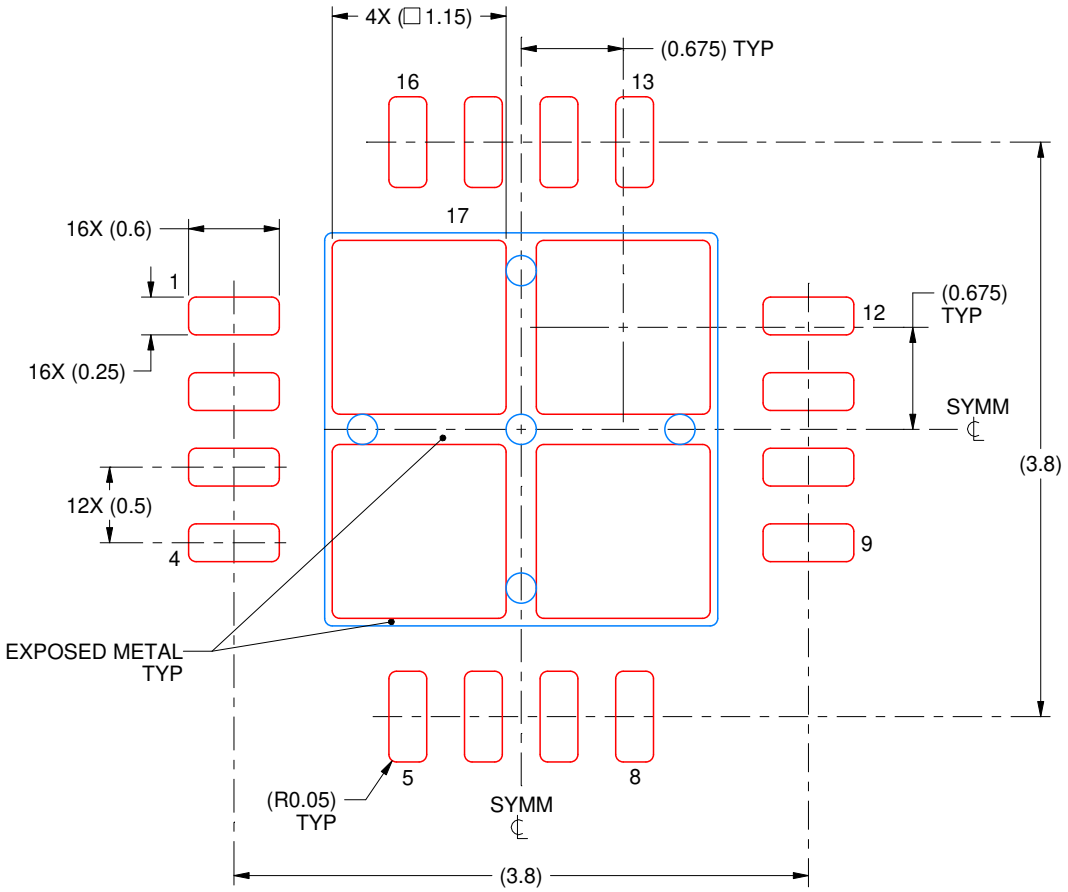


SOLDER MASK DETAILS

4214978/B 01/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214978/B 01/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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