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RA4M1 Group

Datasheet

R01DS0355EJ0110
Rev.1.10
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High efficiency 48-MHz Arm® Cortex®-M4 core, 256-KB code flash memory, 32-KB SRAM, Segment LCD Controller, Capacitive Touch Sensing Unit, USB 2.0 Full-Speed Module, 14-bit A/D Converter, 12-bit D/A Converter, security and safety features

# Features

### ■ Arm Cortex-M4 Core with Floating Point Unit (FPU)
- Armv7E-M architecture with DSP instruction set
- Maximum operating frequency: 48 MHz
- Support for 4-GB address space
- Arm Memory Protection Unit (Arm MPU) with 8 regions
- Debug and Trace: ITM, DWT, FPB, TPIU, ETB
- CoreSight™ Debug Port: JTAG-DP and SW-DP

### ■ Memory
- 256-KB code flash memory
- 8-KB data flash memory (100,000 program/erase (P/E) cycles)
- 32-KB SRAM
- Flash Cache (FCACHE)
- Memory Protection Unit (MPU)
- 128-bit unique ID

### ■ Connectivity
- USB 2.0 Full-Speed Module (USBFS)
  - On-chip transceiver with voltage regulator
  - Compliant with USB Battery Charging Specification 1.2
- Serial Communications Interface (SCI) × 4
  - UART
  - Simple IIC
  - Simple SPI
- Serial Peripheral Interface (SPI) × 2
- $I^2C$ bus interface (IIC) × 2
- Controller Area Network (CAN) module
- Serial Sound Interface Enhanced (SSIE)

### ■ Analog
- 14-bit A/D Converter (ADC14)
- 12-bit D/A Converter (DAC12)
- 8-bit D/A Converter (DAC8) ×2 (for ACMPLP)
- Low-Power Analog Comparator (ACMPLP) × 2
- Operational Amplifier (OPAMP) × 4
- Temperature Sensor (TSN)

### ■ Timers
- General PWM Timer 32-Bit (GPT32) × 2
- General PWM Timer 16-Bit (GPT16) × 6
- Low Power Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

### ■ Safety
- Error Correction Code (ECC) in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

### ■ System and Power Management
- Low power modes
- Realtime Clock (RTC) with calendar and Battery Backup support
- Event Link Controller (ELC)
- DMA Controller (DMAC) × 4
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

### ■ Security and Encryption
- AES128/256
- GHASH
- True Random Number Generator (TRNG)

### ■ Human Machine Interface (HMI)
- Segment LCD Controller (SLCDC)
  - Up to 38 segments × 4 commons
  - Up to 34 segments × 8 commons
- Capacitive Touch Sensing Unit (CTSU)

### ■ Multiple Clock Sources
- Main clock oscillator (MOSC)
  (1 to 20 MHz when VCC = 2.4 to 5.5 V)
  (1 to 8 MHz when VCC = 1.8 to 2.4 V)
  (1 to 4 MHz when VCC = 1.6 to 1.8 V)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO)
  (24, 32, 48, 64 MHz when VCC = 2.4 to 5.5 V)
  (24, 32, 48 MHz when VCC = 1.8 to 5.5 V)
  (24, 32 MHz when VCC = 1.6 to 5.5 V)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

### ■ General Purpose I/O Ports
- Up to 84 input/output pins
  - Up to 3 CMOS input
  - Up to 81 CMOS input/output
    - Up to 9 input/output 5-V tolerant
    - Up to 2 high current (20 mA)

### ■ Operating Voltage
- VCC: 1.6 to 5.5 V

### ■ Operating Temperature and Packages
- Ta = -40°C to +85°C
  - 100-pin LGA (7 mm × 7 mm, 0.65 mm pitch)
- Ta = -40°C to +105°C
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 64-pin QFN (8 mm × 8 mm, 0.4 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)
  - 40-pin QFN (6 mm × 6 mm, 0.5 mm pitch)

# 1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU provides an optimal combination of low-power, high-performance Arm Cortex®-M4 core running up to 48 MHz with the following features:

- 256-KB code flash memory
- 32-KB SRAM
- Segment LCD Controller (SLCDC)
- Capacitive Touch Sensing Unit (CTSU)
- USB 2.0 Full-Speed Module (USBFS)
- 14-bit A/D Converter (ADC14)
- 12-bit D/A Converter (DAC12)
- Security features.

## 1.1 Function Outline

**Table 1.1 Arm core**

| Feature | Functional description |
|---|---|
| Arm Cortex-M4 core | • Maximum operating frequency: up to 48 MHz<br>• Arm Cortex-M4 core<br>- Revision: r0p1-01rel0<br>- Armv7E-M architecture profile<br>- Single precision floating-point unit compliant with the ANSI/IEEE Std 754-2008.<br>• Arm Memory Protection Unit (Arm MPU)<br>- Armv7 Protected Memory System Architecture<br>- 8 protected regions.<br>• SysTick timer<br>- Driven by SYSTICCLK (LOCO) or ICLK. |

**Table 1.2 Memory**

| Feature | Functional description |
|---|---|
| Code flash memory | Maximum 256-KB code flash memory. See section 44, Flash Memory in User's Manual. |
| Data flash memory | 8-KB data flash memory. See section 44, Flash Memory in User's Manual. |
| Option-setting memory | The option-setting memory determines the state of the MCU after a reset. See section 6, Option-Setting Memory in User's Manual. |
| SRAM | On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC). An area in SRAM0 provides error correction capability using ECC. See section 43, SRAM in User's Manual. |

**Table 1.3 System (1 of 2)**

| Feature | Functional description |
|---|---|
| Operating modes | Two operating modes:<br>• Single-chip mode<br>• SCI/USB boot mode.<br>See section 3, Operating Modes in User's Manual. |
| Resets | 14 resets:<br>• RES pin reset<br>• Power-on reset<br>• VBATT-selected voltage power-on reset<br>• Independent watchdog timer reset<br>• Watchdog timer reset<br>• Voltage monitor 0 reset<br>• Voltage monitor 1 reset<br>• Voltage monitor 2 reset<br>• SRAM parity error reset<br>• SRAM ECC error reset<br>• Bus master MPU error reset<br>• Bus slave MPU error reset<br>• CPU stack pointer error reset<br>• Software reset.<br>See section 5, Resets in User's Manual. |
| Low Voltage Detection (LVD) | Low Voltage Detection (LVD) function monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 7, Low Voltage Detection (LVD) in User's Manual. |
| Clocks | • Main clock oscillator (MOSC)<br>• Sub-clock oscillator (SOSC)<br>• High-speed on-chip oscillator (HOCO)<br>• Middle-speed on-chip oscillator (MOCO)<br>• Low-speed on-chip oscillator (LOCO)<br>• PLL frequency synthesizer<br>• IWDT-dedicated on-chip oscillator<br>• Clock out support.<br>See section 8, Clock Generation Circuit in User's Manual. |
| Clock Frequency Accuracy Measurement Circuit (CAC) | The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.<br>When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.<br>See section 9, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual. |
| Interrupt Controller Unit (ICU) | The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 13, Interrupt Controller Unit (ICU) in User's Manual. |
| Key Interrupt Function (KINT) | A key interrupt can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 20, Key Interrupt Function (KINT) in User's Manual. |
| Low power modes | Power consumption can be reduced in multiple ways, such as by setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 10, Low Power Modes in User's Manual. |
| Battery backup function | A battery backup function is provided for partial powering by a battery. The battery powered area includes RTC, SOSC, LOCO, wakeup control, backup memory, VBATT_R low voltage detection, and switches between VCC and VBATT.<br>During normal operation, the battery powered area is powered by the main power supply, which is the VCC pin. When a VCC voltage drop is detected, the power source is switched to the dedicated battery backup power pin, the VBATT pin.<br>When the voltage rises again, the power source is switched from the VBATT pin to the VCC pin. See section 11, Battery Backup Function in User's Manual. |
| Register write protection | The register write protection function protects important registers from being overwritten because of software errors. See section 12, Register Write Protection in User's Manual. |

**Table 1.3 System (2 of 2)**

| Feature | Functional description |
|---|---|
| Memory Protection Unit (MPU) | Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 15, Memory Protection Unit (MPU) in User's Manual. |
| Watchdog Timer (WDT) | The Watchdog Timer (WDT) is a 14-bit down-counter. It can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and used as the condition to detect when the system runs out of control. See section 25, Watchdog Timer (WDT) in User's Manual. |
| Independent Watchdog Timer (IWDT) | The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. It can be used to reset the MCU or to generate a non-maskable interrupt/interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, refresh error, or by a refresh of the count value in the registers. See section 26, Independent Watchdog Timer (IWDT) in User's Manual. |

**Table 1.4 Event link**

| Feature | Functional description |
|---|---|
| Event Link Controller (ELC) | The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 18, Event Link Controller (ELC) in User's Manual. |

**Table 1.5 Direct memory access**

| Feature | Functional description |
|---|---|
| Data Transfer Controller (DTC) | A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 17, Data Transfer Controller (DTC) in User's Manual. |
| DMA Controller (DMAC) | A 4-channel DMA Controller (DMAC) module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 16, DMA Controller (DMAC) in User's Manual. |

**Table 1.6 Timers**

| Feature | Functional description |
|---|---|
| General PWM Timer (GPT) | The General PWM Timer (GPT) is a 32-bit timer with 2 channels and a 16-bit timer with 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 22, General PWM Timer (GPT) in User's Manual. |
| Port Output Enable for GPT (POEG) | Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 21, Port Output Enable for GPT (POEG) in User's Manual. |
| Low Power Asynchronous General Purpose Timer (AGT) | The Low Power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting of external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and they can be accessed with the AGT register. See section 23, Low Power Asynchronous General Purpose Timer (AGT) in User's Manual. |
| Realtime Clock (RTC) | The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings.<br>For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years.<br>For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar.<br>See section 24, Realtime Clock (RTC) in User's Manual. |

**Table 1.7 Communication interfaces (1 of 2)**

| Feature | Functional description |
|---|---|
| Serial Communications Interface (SCI) | The Serial Communications Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces:<br>• Asynchronous interfaces (UART and asynchronous communications interface adapter (ACIA))<br>• 8-bit clock synchronous interface<br>• Simple IIC (master-only)<br>• Simple SPI<br>• Smart card interface.<br>The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol.<br>SCI0 and SCI1 have FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.<br>See section 28, Serial Communications Interface (SCI) in User's Manual. |
| $I^2C$ Bus Interface (IIC) | The 3-channel $I^2C$ Bus Interface (IIC) module conforms with and provides a subset of the NXP $I^2C$ bus (Inter-Integrated Circuit bus) interface functions. See section 29, $I^2C$ Bus Interface (IIC) in User's Manual. |
| Serial Peripheral Interface (SPI) | Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 31, Serial Peripheral Interface (SPI) in User's Manual. |
| Serial Sound Interface Enhanced (SSIE) | The Serial Sound Interface Enhanced (SSIE) peripheral provides functionality to interface with digital audio devices for transmitting PCM audio data over a serial bus with the MCU. The SSIE supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSIE includes 8-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission. See section 33, Serial Sound Interface Enhanced (SSIE) in User's Manual. |
| Controller Area Network (CAN) module | The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically noisy applications.<br>The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 30, Controller Area Network (CAN) Module in User's Manual. |

**Table 1.7 Communication interfaces (2 of 2)**

| Feature | Functional description |
|---|---|
| USB 2.0 Full-Speed Module (USBFS) | The USB 2.0 Full-Speed Module (USBFS) can operate as a host controller or device controller. The module supports full-speed and low-speed (only for the host controller) transfer as defined in the Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on the user system. The MCU supports revision 1.2 of the Battery Charging specification. Because the MCU can be powered at 5 V, the USB LDO regulator provides the internal USB transceiver power supply at 3.3 V. See section 27, USB 2.0 Full-Speed Module (USBFS) in User's Manual. |

**Table 1.8 Analog**

| Feature | Functional description |
|---|---|
| 14-bit A/D Converter (ADC14) | A 14-bit successive approximation A/D converter is provided. Up to 25 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-bit and 14-bit conversion making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 35, 14-Bit A/D Converter (ADC14) in User's Manual. |
| 12-Bit D/A Converter (DAC12) | The 12-Bit D/A Converter (DAC12) converts data and includes an output amplifier. See section 36, 12-Bit D/A Converter (DAC12) in User's Manual. |
| 8-Bit D/A Converter (DAC8) for ACMPLP | The 8-Bit D/A Converter (DAC8) converts data and does not include an output amplifier (DAC8). The DAC8 is used only as the reference voltage for ACMPLP. See section 40, 8-Bit D/A Converter (DAC8) in User's Manual. |
| Temperature Sensor (TSN) | The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC14 for conversion and can be further used by the end application. See section 37, Temperature Sensor (TSN) in User's Manual. |
| Low-Power Analog Comparator (ACMPLP) | The Low-Power Analog Comparator (ACMPLP) compares the reference input voltage and analog input voltage. The comparison result can be read through software and also be output externally. The reference voltage can be selected from an input to the CMPREFi(i = 0,1) pin, an internal 8-bit D/A converter output, or the internal reference voltage (Vref) generated internally in the MCU.<br>The ACMPLP response speed can be set before starting an operation. Setting the high-speed mode decreases the response delay time, but increases current consumption. Setting the low-speed mode increases the response delay time, but decreases current consumption. See section 39, Low-Power Analog Comparator (ACMPLP) in User's Manual. |
| Operational Amplifier (OPAMP) | The Operational Amplifier (OPAMP) amplifies small analog input voltages and outputs the amplified voltages. A total of four differential operational amplifier units with two input pins and one output pin are provided. See section 38, Operational Amplifier (OPAMP) in User's Manual. |

**Table 1.9 Human machine interfaces**

| Feature | Functional description |
|---|---|
| Segment LCD Controller (SLCDC) | The Segment LCD Controller (SLCDC) provides the following functions:<br>• Waveform A or B selectable<br>• The LCD driver voltage generator can switch between an internal voltage boosting method, a capacitor split method, and an external resistance division method<br>• Automatic output of segment and common signals based on automatic display data register read<br>• The reference voltage generated when operating the voltage boost circuit can be selected in 16 steps (contrast adjustment)<br>• The LCD can be made to blink.<br>See section 45, Segment LCD Controller (SLCDC) in User's Manual. |
| Capacitive Touch Sensing Unit (CTSU) | The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed within an electrical insulator so that fingers do not come into direct contact with the electrode. See section 41, Capacitive Touch Sensing Unit (CTSU) in User's Manual. |

**Table 1.10 Data processing**

| Feature | Functional description |
|---|---|
| Cyclic Redundancy Check (CRC) calculator | The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC generation polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 32, Cyclic Redundancy Check (CRC) Calculator in User's Manual. |
| Data Operation Circuit (DOC) | The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 42, Data Operation Circuit (DOC) in User's Manual. |

**Table 1.11 Security**

| Feature | Functional description |
|---|---|
| Secure Crypto Engine 5 (SCE5) | • Security algorithm<br>- Symmetric algorithm: AES.<br>• Other support features<br>- TRNG (True Random Number Generator)<br>- Hash-value generation: GHASH. |

**Table 1.12 I/O ports**

| Feature | Functional description |
|---|---|
| I/O ports | • I/O ports for the 100-pin LQFP, 100-pin LGA<br>- I/O pins: 81<br>- Input pins: 3<br>- Pull-up resistors: 79<br>- N-ch open-drain outputs: 64<br>- 5-V tolerance: 9<br>• I/O ports for the 64-pin LQFP, 64-pin QFN<br>- I/O pins: 49<br>- Input pins: 3<br>- Pull-up resistors: 47<br>- N-ch open-drain outputs: 36<br>- 5-V tolerance: 7<br>• I/O ports for the 48-pin LQFP, 48-pin QFN<br>- I/O pins: 33<br>- Input pins: 3<br>- Pull-up resistors: 31<br>- N-ch open-drain outputs: 22<br>- 5-V tolerance: 4<br>• I/O ports for the 40-pin QFN<br>- I/O pins: 25<br>- Input pins: 3<br>- Pull-up resistors: 23<br>- N-ch open-drain outputs: 15<br>- 5-V tolerance: 2 |

## 1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

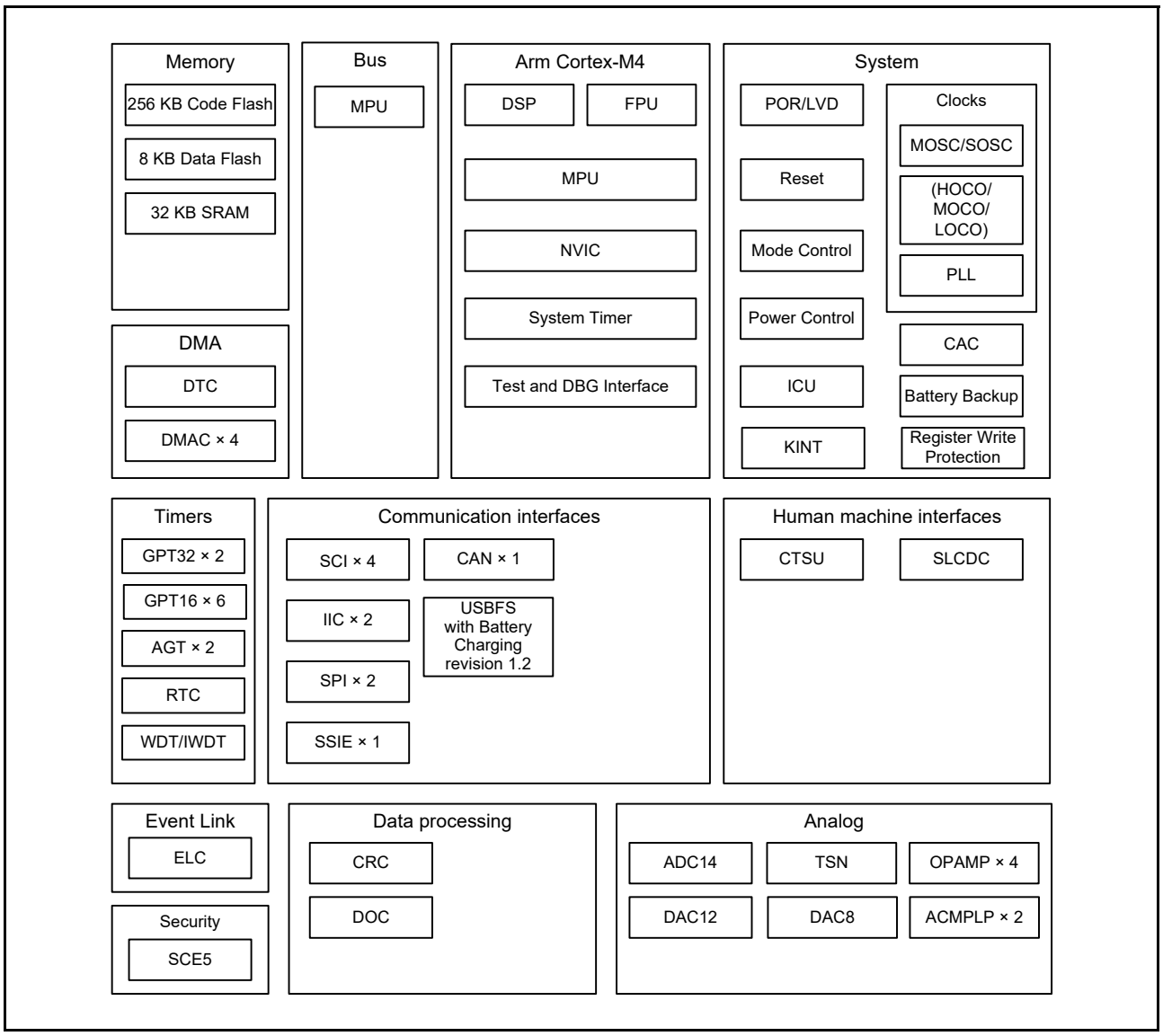



**Figure 1.1 Block diagram**

## 1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity, and package type. Table 1.13 shows a product list.

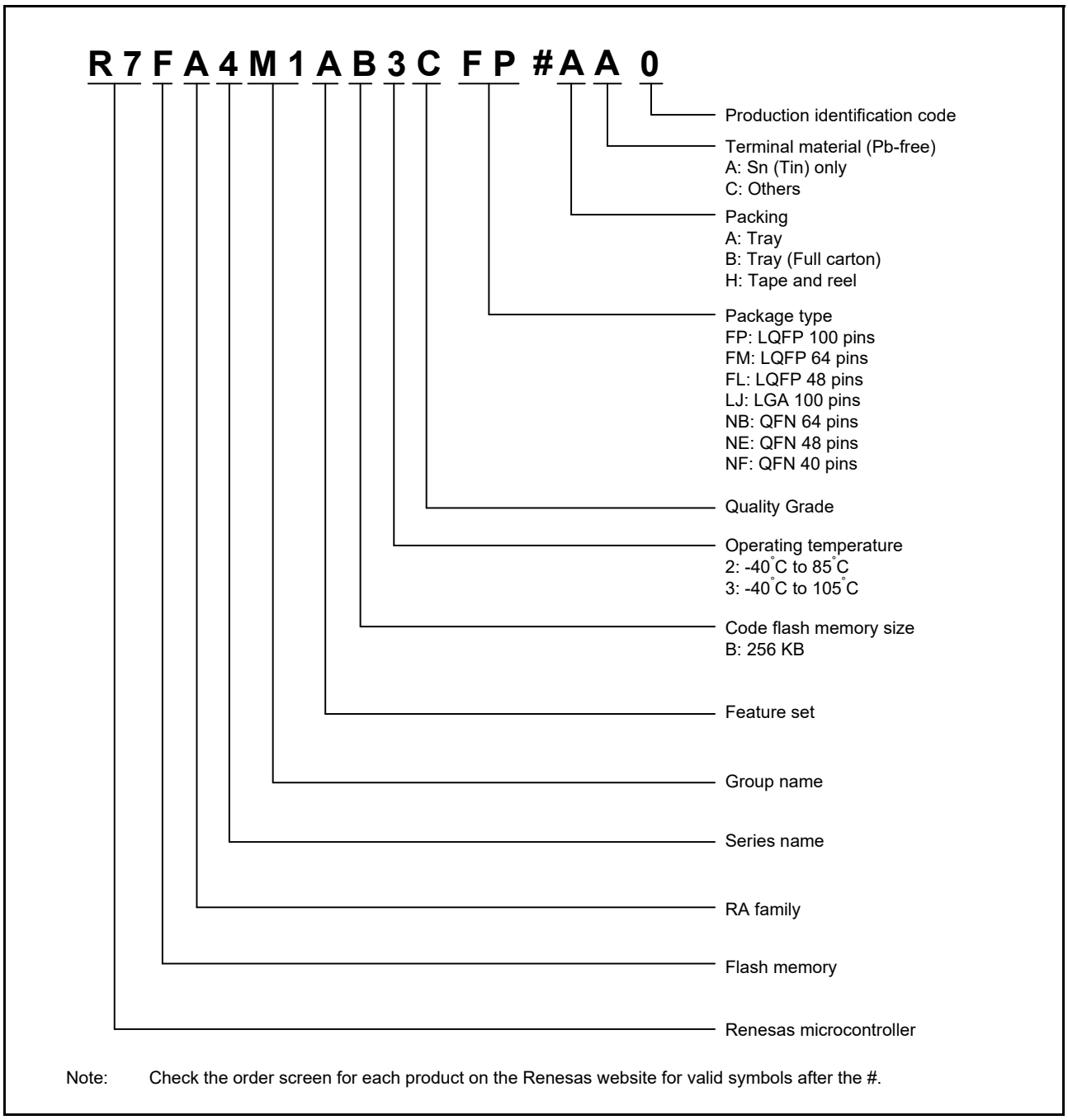



**Figure 1.2 Part numbering scheme**

**Table 1.13 Product list**

| Product part number | Package code | Code flash | Data flash | SRAM | Operating temperature |
|---|---|---|---|---|---|
| R7FA4M1AB3CFP | PLQP0100KB-B | 256 KB | 8 KB | 32 KB | -40 to +105°C |
| R7FA4M1AB2CLJ | PTLG0100JA-A | | | | -40 to +85°C |
| R7FA4M1AB3CFM | PLQP0064KB-C | | | | -40 to +105°C |
| R7FA4M1AB3CNB | PWQN0064LA-A | | | | -40 to +105°C |
| | PWQN0064LB-B | | | | |
| R7FA4M1AB3CFL | PLQP0048KB-B | | | | -40 to +105°C |
| R7FA4M1AB3CNE | PWQN0048KB-A | | | | -40 to +105°C |
| | PWQN0048KC-A | | | | |
| R7FA4M1AB3CNF | PWQN0040KC-A | | | | -40 to +105°C |
| | PWQN0040KD-A | | | | |

## 1.4 Function Comparison

**Table 1.14 Function comparison**

| Part numbers | | R7FA4M1AB3CFP | R7FA4M1AB2CLJ | R7FA4M1AB3CFM/ R7FA4M1AB3CNB | R7FA4M1AB3CFL/ R7FA4M1AB3CNE | R7FA4M1AB3CNF |
|---|---|---|---|---|---|---|
| Pin count | | 100 | 100 | 64 | 48 | 40 |
| Package | | LQFP | LGA | LQFP/QFN | LQFP/QFN | QFN |
| Code flash memory | | 256 KB | | | | |
| Data flash memory | | 8 KB | | | | |
| SRAM | | 32 KB | | | | |
| | Parity | 16 KB | | | | |
| | ECC | 16 KB | | | | |
| System | CPU clock | 48 MHz | | | | |
| | Backup registers | 512 bytes | | | | |
| | ICU | Yes | | | | |
| | KINT | 8 | | | 5 | 3 |
| Event control | ELC | Yes | | | | |
| DMA | DTC | Yes | | | | |
| | DMAC | 4 | | | | |
| Bus | External bus | No | | | | |
| Timers | GPT32 | 2 | | | | |
| | GPT16 | 6 | | | 4 | 2 |
| | AGT | 2 | | | No | |
| | RTC | Yes | | | | |
| | WDT/IWDT | Yes | | | | |
| Communication | SCI | 4 | | | | |
| | IIC | 2 | | | | |
| | SPI | 2 | | | | 1 |
| | SSIE | 1 | | No | | |
| | QSPI | No | | | | |
| | SDHI | No | | | | |
| | CAN | 1 | | | | |
| | USBFS | Yes | | | | |
| Analog | ADC14 | 25 | | 18 | 14 | 11 |
| | DAC12 | 1 | | | | |
| | DAC8 | 2 | | | | |
| | ACMPLP | 2 | | | | 1 |
| | OPAMP | 4 | 4 | 3 | 1 | No |
| | TSN | Yes | | | | |
| HMI | SLCDC | 4 com × 38 seg or 8 com × 34 seg | | 4 com × 21 seg or 8 com × 17 seg | No | |
| | CTSU | 27 | | 24 | 15 | 10 |
| Data processing | CRC | Yes | | | | |
| | DOC | Yes | | | | |
| Security | | SCE5 | | | | |
| I/O ports | I/O pins | 81 | | 49 | 33 | 25 |
| | Input pins | 3 | | 3 | 3 | 3 |
| | Pull-up resistors | 79 | | 47 | 31 | 23 |
| | N-ch open-drain outputs | 64 | | 36 | 22 | 15 |
| | 5-V tolerance | 9 | | 7 | 4 | 2 |

## 1.5 Pin Functions

**Table 1.15 Pin functions (1 of 4)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| Power supply | VCC | Input | Power supply pin. Connect this pin to the system power supply. Connect it to VSS through a 0.1-μF capacitor. The capacitor should be placed close to the pin. |
| | VCL | I/O | Connect this pin to the VSS pin through the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin. |
| | VSS | Input | Ground pin. Connect to the system power supply (0 V). |
| | VBATT | Input | Backup power supply pin |
| Clock | XTAL | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| | XCIN | Input | Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN. |
| | XCOUT | Output | |
| | CLKOUT | Output | Clock output pin |
| Operating mode control | MD | Input | Pins for setting the operating mode. The signal levels on these pins must not be changed during operation mode transition on release from the reset state. |
| System control | RES | Input | Reset signal input pin. The MCU enters the reset state when this signal goes low. |
| CAC | CACREF | Input | Measurement reference clock input pin |
| Interrupt | NMI | Input | Non-maskable interrupt request pin |
| | IRQ0 to IRQ12, IRQ14, IRQ15 | Input | Maskable interrupt request pins |
| KINT | KR00 to KR07 | Input | Key interrupt input pins.<br>A key interrupt (KINT) can be generated by inputting a falling edge to the key interrupt input pins. |
| On-chip debug | TMS | I/O | On-chip emulator or boundary scan pins |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | SWDIO | I/O | Serial wire debug data input/output pin |
| | SWCLK | Input | Serial wire clock pin |
| | SWO | Output | Serial wire trace output pin |
| Battery Backup | VBATWIO0 to VBATWIO2 | I/O | Output wakeup signal for the VBATT wakeup control function.<br>External event input for the VBATT wakeup control function. |
| GPT | GTETRGA, GTETRGB | Input | External trigger input pin |
| | GTIOC0A to GTIOC7A, GTIOC0B to GTIOC7B | I/O | Input capture, output capture, or PWM output pin |
| | GTIU | Input | Hall sensor input pin U |
| | GTIV | Input | Hall sensor input pin V |
| | GTIW | Input | Hall sensor input pin W |
| | GTOUUP | Output | 3-phase PWM output for BLDC motor control (positive U phase) |
| | GTOULO | Output | 3-phase PWM output for BLDC motor control (negative U phase) |
| | GTOVUP | Output | 3-phase PWM output for BLDC motor control (positive V phase) |
| | GTOVLO | Output | 3-phase PWM output for BLDC motor control (negative V phase) |
| | GTOWUP | Output | 3-phase PWM output for BLDC motor control (positive W phase) |
| | GTOWLO | Output | 3-phase PWM output for BLDC motor control (negative W phase) |

**Table 1.15 Pin functions (2 of 4)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| AGT | AGTEE0, AGTEE1 | Input | External event input enable signals |
| | AGTIO0, AGTIO1 | I/O | External event input and pulse output pins |
| | AGTO0, AGTO1 | Output | Pulse output pins |
| | AGTOA0, AGTOA1 | Output | Output compare match A output pins |
| | AGTOB0, AGTOB1 | Output | Output compare match B output pins |
| RTC | RTCOUT | Output | Output pin for 1-Hz/64-Hz clock |
| | RTCIC0 to RTCIC2 | Input | Time capture event input pins |
| SCI | SCK0 to SCK2, SCK9 | I/O | Clock (clock synchronous mode) input/output pins |
| | RXD0 to RXD2, RXD9 | Input | Received data (asynchronous mode/clock synchronous mode) input pins |
| | TXD0 to TXD2, TXD9 | Output | Transmitted data (asynchronous mode/clock synchronous mode) output pins |
| | CTS0_RTS0 to CTS2_RTS2, CTS9_RTS9 | I/O | Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low |
| | SCL0 to SCL2, SCL9 | I/O | $I^2C$ clock (simple IIC) input/output pins |
| | SDA0 to SDA2, SDA9 | I/O | $I^2C$ data (simple IIC) input/output pins |
| | SCK0 to SCK2, SCK9 | I/O | Clock (simple SPI) input/output pins |
| | MISO0 to MISO2, MISO9 | I/O | Slave transmission of data (simple SPI) input/output pins |
| | MOSI0 to MOSI2, MOSI9 | I/O | Master transmission of data (simple SPI) input/output pins |
| | SS0 to SS2, SS9 | Input | Slave-select input pins (simple SPI), active-low |
| IIC | SCL0, SCL1 | I/O | Clock input/output pins |
| | SDA0, SDA1 | I/O | Data input/output pins |
| SSIE | SSIBCK0 | I/O | SSIE serial bit clock pin |
| | SSILRCK0/SSIFS0 | I/O | Word select pins |
| | SSITXD0 | Output | Serial data output pin |
| | SSIRXD0 | Input | Serial data input pin |
| | AUDIO_CLK | Input | External clock pin for audio (input oversampling clock) |
| SPI | RSPCKA, RSPCKB | I/O | Clock input/output pin |
| | MOSIA, MOSIB | I/O | Input/output pins for data output from the master |
| | MISOA, MISOB | I/O | Input/output pins for data output from the slave |
| | SSLA0, SSLB0 | I/O | Input/output pins for slave selection |
| | SSLA1, SSLA2, SSLA3, SSLB1, SSLB2, SSLB3 | Output | Output pins for slave selection |
| CAN | CRX0 | Input | Receive data |
| | CTX0 | Output | Transmit data |

**Table 1.15 Pin functions (3 of 4)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| USBFS | VSS_USB | Input | Ground pin |
| | VCC_USB_LDO | Input | Power supply pin for USB LDO regulator |
| | VCC_USB | I/O | Input: USB transceiver power supply pin.<br>Output: USB LDO regulator output pin. This pin should be connected to an external capacitor. |
| | USB_DP | I/O | D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus. |
| | USB_DM | I/O | D- I/O pin of the USB on-chip transceiver. This pin should be connected to the D- pin of the USB bus. |
| | USB_VBUS | Input | USB cable connection monitor pin. This pin should be connected to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a device controller. |
| | USB_EXICEN | Output | Low power control signal for external power supply (OTG) chip |
| | USB_VBUSEN | Output | VBUS (5 V) supply enable signal for external power supply chip |
| | USB_OVRCURA, USB_OVRCURB | Input | Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected. |
| | USB_ID | Input | Connect the MicroAB connector ID input signal to this pin during operation in OTG mode |
| Analog power supply | AVCC0 | Input | Analog voltage supply pin |
| | AVSS0 | Input | Analog voltage supply ground pin |
| | VREFH0 | Input | Analog reference voltage supply pin |
| | VREFL0 | Input | Reference power supply ground pin |
| | VREFH | Input | Analog reference voltage supply pin for D/A converter |
| | VREFL | Input | Analog reference ground pin for D/A converter |
| ADC14 | AN000 to AN014, AN016 to AN025 | Input | Input pins for the analog signals to be processed by the A/D converter |
| | ADTRG0 | Input | Input pins for the external trigger signals that start the A/D conversion, active-low |
| DAC12 | DA0 | Output | Output pins for the analog signals to be processed by the D/A converter |
| Comparator output | VCOUT | Output | Comparator output pin |
| ACMPLP | CMPREF0, CMPREF1 | Input | Reference voltage input pin |
| | CMPIN0, CMPIN1 | Input | Analog voltage input pins |
| OPAMP | AMP0+ to AMP3+ | Input | Analog voltage input pins |
| | AMP0- to AMP3- | Input | Analog voltage input pins |
| | AMP0O to AMP3O | Output | Analog voltage output pins |
| CTSU | TS00 to TS13, TS17 to TS22, TS27 to TS31, TS34, TS35 | Input | Capacitive touch detection pins (touch pins) |
| | TSCAP | - | Secondary power supply pin for the touch driver |

**Table 1.15 Pin functions (4 of 4)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| I/O ports | P000 to P008, P010 to P015 | I/O | General-purpose input/output pins |
| | P100 to P115 | I/O | General-purpose input/output pins |
| | P200 | Input | General-purpose input pin |
| | P201 to P206, P212, P213 | I/O | General-purpose input/output pins |
| | P214, P215 | Input | General-purpose input pins |
| | P300 to P307 | I/O | General-purpose input/output pins |
| | P400 to P415 | I/O | General-purpose input/output pins |
| | P500 to P505 | I/O | General-purpose input/output pins |
| | P600 to P603, P608 to P610 | I/O | General-purpose input/output pins |
| | P708 | I/O | General-purpose input/output pins |
| | P808, P809 | I/O | General-purpose input/output pins |
| | P914, P915 | I/O | General-purpose input/output pins |
| SLCDC | VL1, VL2, VL3, VL4 | I/O | Voltage pin for driving the LCD |
| | CAPH, CAPL | I/O | Capacitor connection pin for the LCD controller/driver |
| | COM0 to COM7 | Output | Common signal output pins for the LCD controller/driver |
| | SEG00 to SEG37 | Output | Segment signal output pins for the LCD controller/driver |

## 1.6 Pin Assignments

Figure 1.3 to Figure 1.6 show the pin assignments.

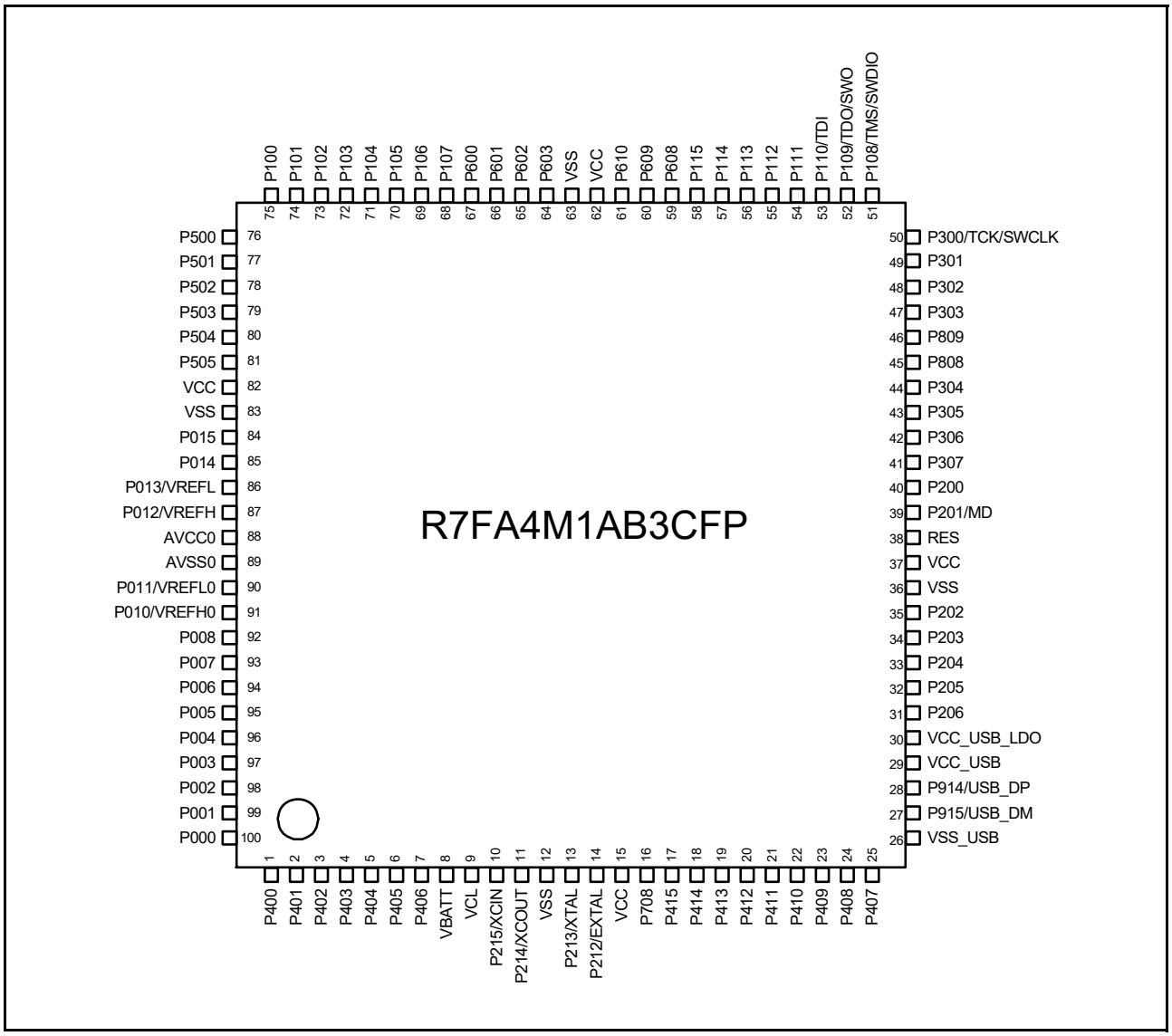



**Figure 1.3 Pin assignment for 100-pin LQFP (top view)**

# R7FA4M1AB2CLJ

| | A | B | C | D | E | F | G | H | J | K | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | P407 | P409 | P412 | VCC | P212/ EXTAL | P215/ XCIN | VCL | P403 | P400 | P000 | 10 |
| 9 | P915/ USB_DM | P914/ USB_DP | P413 | VSS | P213/ XTAL | P214/ XCOUT | VBATT | P405 | P401 | P001 | 9 |
| 8 | VCC_ USB | VSS_ USB | VCC_US B_LDO | P411 | P415 | P708 | P404 | P003 | P004 | P002 | 8 |
| 7 | P205 | P204 | P206 | P408 | P414 | P406 | P006 | P007 | P008 | P005 | 7 |
| 6 | VSS | VCC | P202 | P203 | P410 | P402 | P505 | AVSS0 | P011/ VREFL0 | P010/ VREFH0 | 6 |
| 5 | P200 | P201/MD | P307 | RES | P113 | P600 | P504 | AVCC0 | P013/ VREFL | P012/ VREFH | 5 |
| 4 | P305 | P304 | P808 | P306 | P115 | P601 | P503 | P100 | P015 | P014 | 4 |
| 3 | P809 | P303 | P110/TDI | P111 | P609 | P602 | P107 | P103 | VSS | VCC | 3 |
| 2 | P300/ TCK/ SWCLK | P302 | P301 | P114 | P610 | P603 | P106 | P101 | P501 | P502 | 2 |
| 1 | P108/ TMS/ SWDIO | P109/ TDO/ SWO | P112 | P608 | VCC | VSS | P105 | P104 | P102 | P500 | 1 |
| | A | B | C | D | E | F | G | H | J | K | |

**Figure 1.4 Pin assignment for 100-pin LGA (top view)**

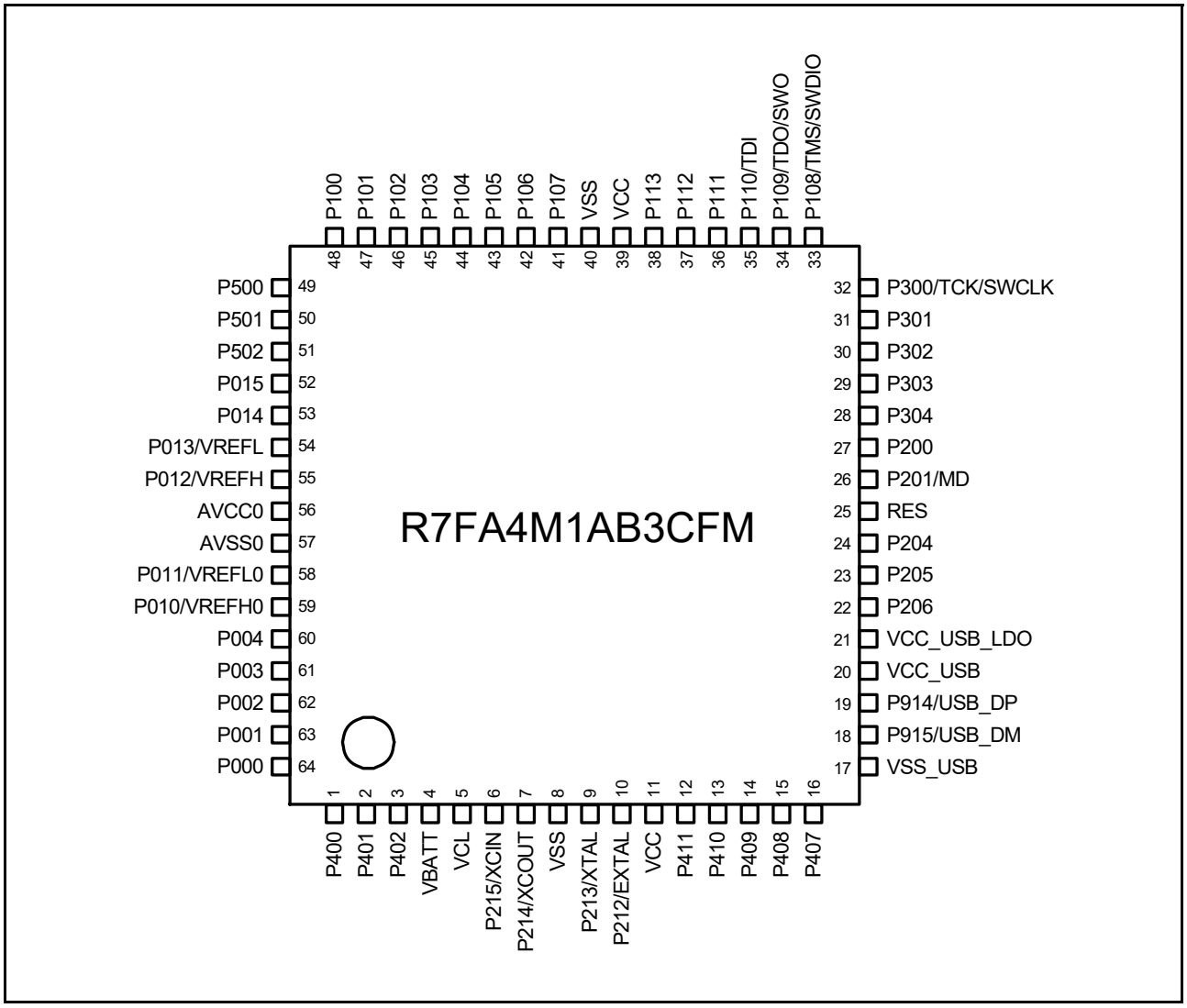
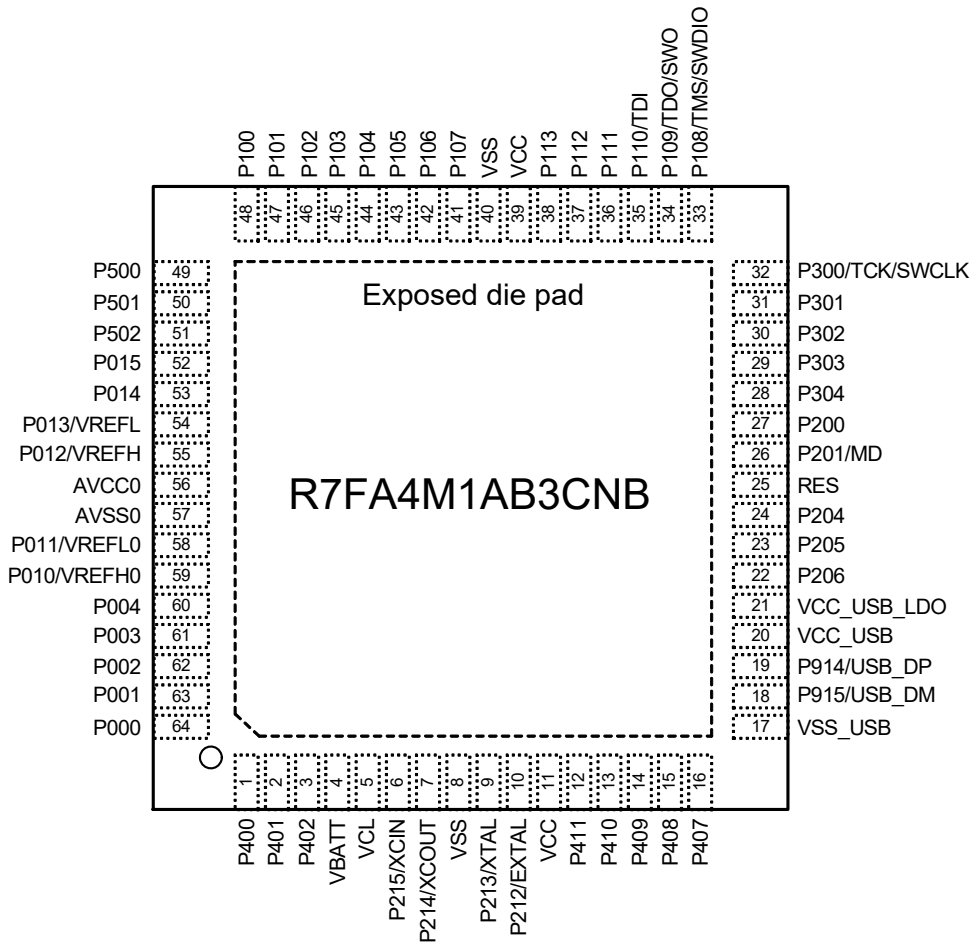



**Figure 1.5 Pin assignment for 64-pin LQFP (top view)**




Note: Exposed die pad is recommended to connect to VSS.

**Figure 1.6 Pin assignment for 64-pin QFN (top view)**

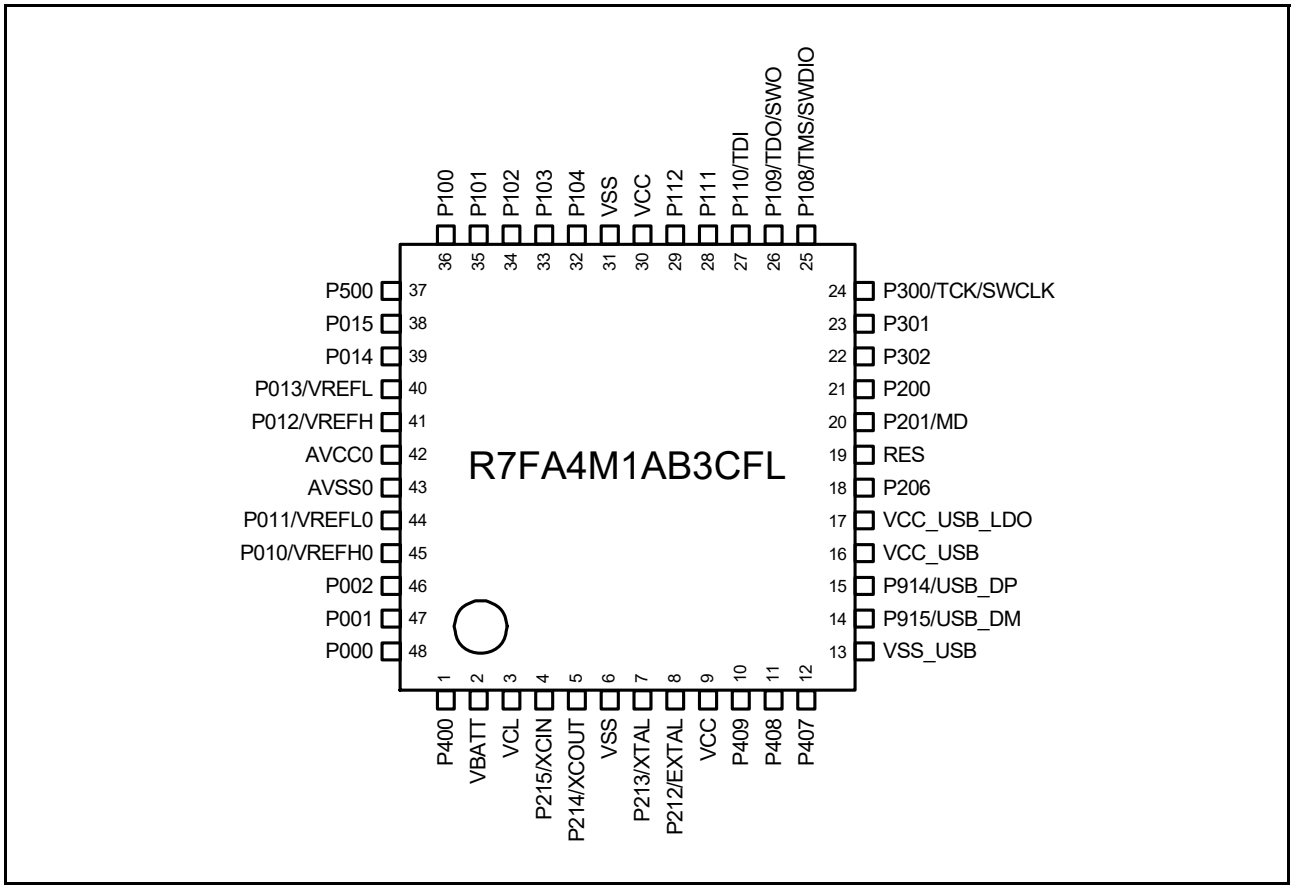
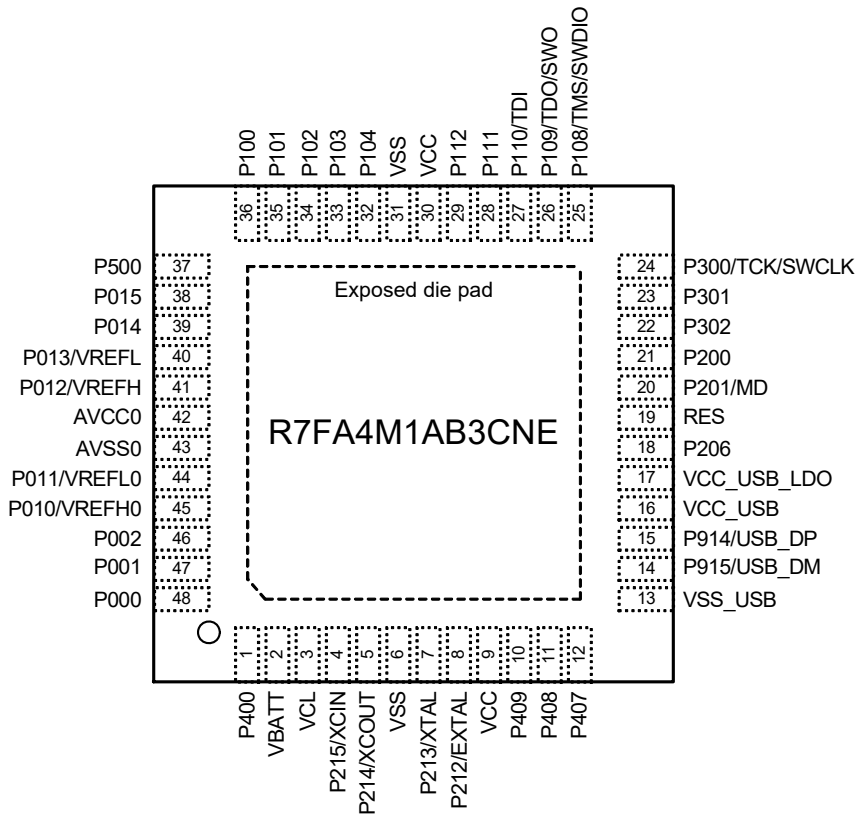
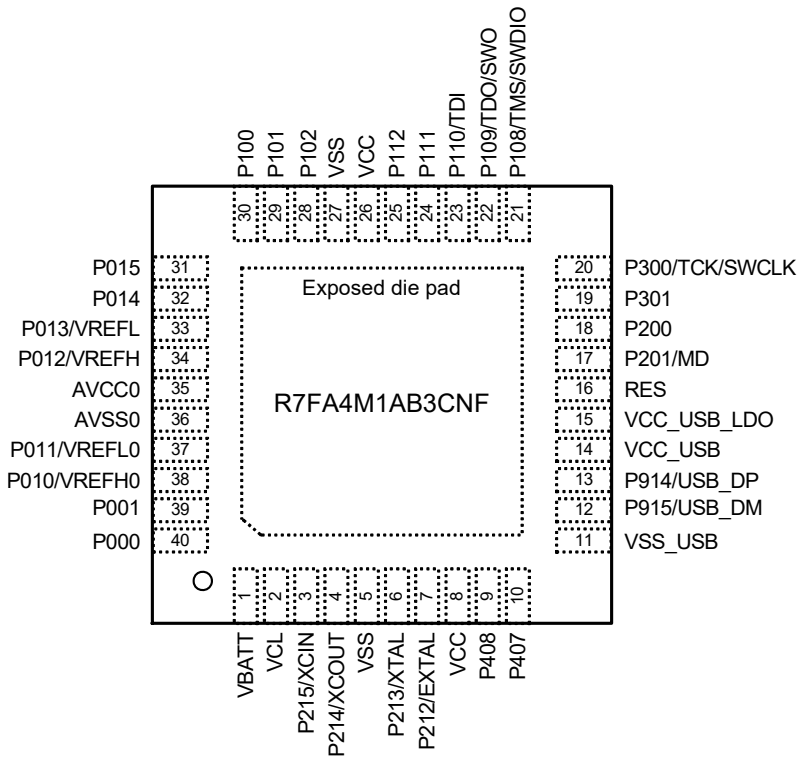



**Figure 1.7 Pin assignment for 48-pin LQFP (top view)**




Note: Exposed die pad is recommended to connect to VSS.

**Figure 1.8 Pin assignment for 48-pin QFN (top view)**




Note: Exposed die pad is recommended to connect to VSS.

**Figure 1.9 Pin assignment for 40-pin QFN (top view)**

## 1.7 Pin Lists

| Pin number | | | | | | | | | | Timers | | | | Communication interfaces | | | | | Analogs | | | HMI | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LGA100 | LQFP64 | QFN64 | LQFP48 | QFN48 | QFN40 | Power, System, Clock, Debug, CAC, VBATT | Interrupt | I/O ports | AGT | GPT_OPS, POEG | GPT | RTC | USBFS,CAN | SCI | IIC | SPI | SSIE | ADC14 | DAC12, OPAMP | ACMPLP | SLCDC | CTSU |
| 1 | J10 | 1 | 1 | 1 | 1 | | CACREF | IRQ0 | P400 | AGTIO1 | | GTIOC6A | | | SCK0<br>SCK1 | SCL0 | | AUDIO_CLK | | | | SEG04 | TS20 |
| 2 | J9 | 2 | 2 | | | | | IRQ5 | P401 | | GTETRGA | GTIOC6B | | CTX0 | CTS0_<br>RTS0/<br>SS0<br>TXD1/<br>MOSI1/<br>SDA1 | SDA0 | | | | | | SEG05 | TS19 |
| 3 | F6 | 3 | 3 | | | | VBATWIO0 | IRQ4 | P402 | AGTIO0/<br>AGTIO1 | | | RTCIC0 | CRX0 | RXD1/<br>MISO1/<br>SCL1 | | | | | | | SEG06 | TS18 |
| 4 | H10 | | | | | | VBATWIO1 | | P403 | AGTIO0/<br>AGTIO1 | | GTIOC3A | RTCIC1 | | CTS1_<br>RTS1/<br>SS1 | | | SSIBCK0 | | | | | TS17 |
| 5 | G8 | | | | | | VBATWIO2 | | P404 | | | GTIOC3B | RTCIC2 | | | | | SSILRCK0/<br>SSIFS0 | | | | | |
| 6 | H9 | | | | | | | | P405 | | | GTIOC1A | | | | | | SSITXD0 | | | | | |
| 7 | F7 | | | | | | | | P406 | | | GTIOC1B | | | | | | SSIRXD0 | | | | | |
| 8 | G9 | 4 | 4 | 2 | 2 | 1 | VBATT | | | | | | | | | | | | | | | | |
| 9 | G10 | 5 | 5 | 3 | 3 | 2 | VCL | | | | | | | | | | | | | | | | |
| 10 | F10 | 6 | 6 | 4 | 4 | 3 | XCIN | | P215 | | | | | | | | | | | | | | |
| 11 | F9 | 7 | 7 | 5 | 5 | 4 | XCOUT | | P214 | | | | | | | | | | | | | | |
| 12 | D9 | 8 | 8 | 6 | 6 | 5 | VSS | | | | | | | | | | | | | | | | |
| 13 | E9 | 9 | 9 | 7 | 7 | 6 | XTAL | IRQ2 | P213 | | GTETRGA | GTIOC0A | | | TXD1/<br>MOSI1/<br>SDA1 | | | | | | | | |
| 14 | E10 | 10 | 10 | 8 | 8 | 7 | EXTAL | IRQ3 | P212 | AGTEE1 | GTETRGB | GTIOC0B | | | RXD1/<br>MISO1/<br>SCL1 | | | | | | | | |
| 15 | D10 | 11 | 11 | 9 | 9 | 8 | VCC | | | | | | | | | | | | | | | | |
| 16 | F8 | | | | | | | | P708 | | | | | | RXD1/<br>MISO1/<br>SCL1 | | SSLA3 | | | | | | |
| 17 | E8 | | | | | | | IRQ8 | P415 | | | GTIOC0A | | | | | SSLA2 | | | | | | |
| 18 | E7 | | | | | | | IRQ9 | P414 | | | GTIOC0B | | | | | SSLA1 | | | | | | |
| 19 | C9 | | | | | | | | P413 | | | | | | CTS0_<br>RTS0/<br>SS0 | | SSLA0 | | | | | | |
| 20 | C10 | | | | | | | | P412 | | | | | | SCK0 | | RSPCKA | | | | | | |
| 21 | D8 | 12 | 12 | | | | | IRQ4 | P411 | AGTOA1 | GTOVUP | GTIOC6A | | | TXD0/<br>MOSI0/<br>SDA0 | | MOSIA | | | | | SEG07 | TS07 |
| 22 | E6 | 13 | 13 | | | | | IRQ5 | P410 | AGTOB1 | GTOVLO | GTIOC6B | | | RXD0/<br>MISO0/<br>SCL0 | | MISOA | | | | | SEG08 | TS06 |
| 23 | B10 | 14 | 14 | 10 | 10 | | | IRQ6 | P409 | | GTOWUP | GTIOC5A | | USB_EXICEN | TXD9/<br>MOSI9/<br>SDA9 | | | | | | | SEG09 | TS05 |
| 24 | D7 | 15 | 15 | 11 | 11 | 9 | | IRQ7 | P408 | | GTOWLO | GTIOC5B | | USB_ID | CTS1_<br>RTS1/<br>SS1<br>RXD9/<br>MISO9/<br>SCL9 | SCL0 | | | | | | SEG10 | TS04 |
| 25 | A10 | 16 | 16 | 12 | 12 | 10 | | | P407 | AGTIO0 | | | RTCOUT | USB_VBUS | CTS0_<br>RTS0/<br>SS0 | SDA0 | SSLB3 | | ADTRG0 | | | SEG11 | TS03 |
| 26 | B8 | 17 | 17 | 13 | 13 | 11 | VSS_USB | | | | | | | | | | | | | | | | |
| 27 | A9 | 18 | 18 | 14 | 14 | 12 | | | P915 | | | | | USB_DM | | | | | | | | | |
| 28 | B9 | 19 | 19 | 15 | 15 | 13 | | | P914 | | | | | USB_DP | | | | | | | | | |

| Pin number | | | | | | | | | | Timers | | | | Communication interfaces | | | | | Analogs | | | HMI | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LGA100 | LQFP64 | QFN64 | LQFP48 | QFN48 | QFN40 | Power, System, Clock, Debug, CAC, VBATT | Interrupt | I/O ports | AGT | GPT_OPS, POEG | GPT | RTC | USBFS,CAN | SCI | IIC | SPI | SSIE | ADC14 | DAC12, OPAMP | ACMPLP | SLCDC | CTSU |
| 29 | A8 | 20 | 20 | 16 | 16 | 14 | VCC_USB | | | | | | | | | | | | | | | | |
| 30 | C8 | 21 | 21 | 17 | 17 | 15 | VCC_USB_LDO | | | | | | | | | | | | | | | | |
| 31 | C7 | 22 | 22 | 18 | 18 | | | IRQ0 | P206 | | GTIU | | | USB_VBUSEN | RXD0/MISO0/SCL0 | SDA1 | SSLB1 | | | | | SEG12 | TS01 |
| 32 | A7 | 23 | 23 | | | | CLKOUT | IRQ1 | P205 | AGTO1 | GTIV | GTIOC4A | | USB_OVRCURA | TXD0/MOSI0/SDA0 CTS9_RTS9/SS9 | SCL1 | SSLB0 | | | | | SEG13 | TSCAP |
| 33 | B7 | 24 | 24 | | | | CACREF | | P204 | AGTIO1 | GTIW | GTIOC4B | | USB_OVRCURB | SCK0 SCK9 | SCL0 | RSPCKB | | | | | SEG14 | TS00 |
| 34 | D6 | | | | | | | | P203 | | | GTIOC5A | | | CTS2_RTS2/SS2 TXD9/MOSI9/SDA9 | | MOSIB | | | | | SEG15 | TSCAP |
| 35 | C6 | | | | | | | | P202 | | | GTIOC5B | | | SCK2 RXD9/MISO9/SCL9 | | MISOB | | | | | SEG16 | |
| 36 | A6 | | | | | | VSS | | | | | | | | | | | | | | | | |
| 37 | B6 | | | | | | VCC | | | | | | | | | | | | | | | | |
| 38 | D5 | 25 | 25 | 19 | 19 | 16 | RES | | | | | | | | | | | | | | | | |
| 39 | B5 | 26 | 26 | 20 | 20 | 17 | MD | | P201 | | | | | | | | | | | | | | |
| 40 | A5 | 27 | 27 | 21 | 21 | 18 | | NMI | P200 | | | | | | | | | | | | | | |
| 41 | C5 | | | | | | | | P307 | | | | | | | | | | | | | SEG17 | |
| 42 | D4 | | | | | | | | P306 | | | | | | | | | | | | | SEG18 | |
| 43 | A4 | | | | | | | IRQ8 | P305 | | | | | | | | | | | | | SEG19 | |
| 44 | B4 | 28 | 28 | | | | | IRQ9 | P304 | | | GTIOC7A | | | | | | | | | | SEG20 | TS11 |
| 45 | C4 | | | | | | | | P808 | | | | | | | | | | | | | SEG21 | |
| 46 | A3 | | | | | | | | P809 | | | | | | | | | | | | | SEG22 | |
| 47 | B3 | 29 | 29 | | | | | | P303 | | | GTIOC7B | | | | | | | | | | SEG03/COM7 | TS02 |
| 48 | B2 | 30 | 30 | 22 | 22 | | | IRQ5 | P302 | | GTOUUP | GTIOC4A | | | TXD2/MOSI2/SDA2 | | SSLB3 | | | | | SEG02/COM6 | TS08 |
| 49 | C2 | 31 | 31 | 23 | 23 | 19 | | IRQ6 | P301 | AGTIO0 | GTOULO | GTIOC4B | | | RXD2/MISO2/SCL2 CTS9_RTS9/SS9 | | SSLB2 | | | | | SEG01/COM5 | TS09 |
| 50 | A2 | 32 | 32 | 24 | 24 | 20 | TCK/SWCLK | | P300 | | GTOUUP | GTIOC0A | | | | | SSLB1 | | | | | | |
| 51 | A1 | 33 | 33 | 25 | 25 | 21 | TMS/SWDIO | | P108 | | GTOULO | GTIOC0B | | | CTS9_RTS9/SS9 | | SSLB0 | | | | | | |
| 52 | B1 | 34 | 34 | 26 | 26 | 22 | TDO/SWO/CLKOUT | | P109 | | GTOVUP | GTIOC1A | | CTX0 | SCK1 TXD9/MOSI9/SDA9 | | MOSIB | | | | | SEG23 | TS10 |
| 53 | C3 | 35 | 35 | 27 | 27 | 23 | TDI | IRQ3 | P110 | | GTOVLO | GTIOC1B | | CRX0 | CTS2_RTS2/SS2 RXD9/MISO9/SCL9 | | MISOB | | | | VCOUT | SEG24 | |

| Pin number | | | | | | | | | | Timers | | | | Communication interfaces | | | | | Analogs | | | HMI | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LGA100 | LQFP64 | QFN64 | LQFP48 | QFN48 | QFN40 | Power, System, Clock, Debug, CAC, VBATT | Interrupt | I/O ports | AGT | GPT_OPS, POEG | GPT | RTC | USBFS,CAN | SCI | IIC | SPI | SSIE | ADC14 | DAC12, OPAMP | ACMPLP | SLCDC | CTSU |
| 54 | D3 | 36 | 36 | 28 | 28 | 24 | | IRQ4 | P111 | | | GTIOC3A | | | SCK2<br>SCK9 | | RSPCKB | | | | | CAPH | TS12 |
| 55 | C1 | 37 | 37 | 29 | 29 | 25 | | | P112 | | | GTIOC3B | | | TXD2/<br>MOSI2/<br>SDA2<br>SCK1 | | SSLB0 | SSIBCK0 | | | | CAPL | TSCAP |
| 56 | E5 | 38 | 38 | | | | | | P113 | | | GTIOC2A | | | | | | SSILRCK0/<br>SSIFS0 | | | | SEG00/<br>COM4 | TS27 |
| 57 | D2 | | | | | | | | P114 | | | GTIOC2B | | | | | | SSIRXD0 | | | | SEG25 | TS29 |
| 58 | E4 | | | | | | | | P115 | | | GTIOC4A | | | | | | SSITXD0 | | | | SEG26 | TS35 |
| 59 | D1 | | | | | | | | P608 | | | GTIOC4B | | | | | | | | | | SEG27 | |
| 60 | E3 | | | | | | | | P609 | | | GTIOC5A | | | | | | | | | | SEG28 | |
| 61 | E2 | | | | | | | | P610 | | | GTIOC5B | | | | | | | | | | SEG29 | |
| 62 | E1 | 39 | 39 | 30 | 30 | 26 | VCC | | | | | | | | | | | | | | | | |
| 63 | F1 | 40 | 40 | 31 | 31 | 27 | VSS | | | | | | | | | | | | | | | | |
| 64 | F2 | | | | | | | | P603 | | | GTIOC7A | | | CTS9_<br>RTS9/<br>SS9 | | | | | | | SEG30 | |
| 65 | F3 | | | | | | | | P602 | | | GTIOC7B | | | TXD9/<br>MOSI9/<br>SDA9 | | | | | | | SEG31 | |
| 66 | F4 | | | | | | | | P601 | | | GTIOC6A | | | RXD9/<br>MISO9/<br>SCL9 | | | | | | | SEG32 | |
| 67 | F5 | | | | | | | | P600 | | | GTIOC6B | | | SCK9 | | | | | | | SEG33 | |
| 68 | G3 | 41 | 41 | | | | | KR07 | P107 | | | GTIOC0A | | | | | | | | | | COM3 | |
| 69 | G2 | 42 | 42 | | | | | KR06 | P106 | | | GTIOC0B | | | | | SSLA3 | | | | | COM2 | |
| 70 | G1 | 43 | 43 | | | | | KR05/<br>IRQ0 | P105 | | GTETRGA | GTIOC1A | | | | | SSLA2 | | | | | COM1 | TS34 |
| 71 | H1 | 44 | 44 | 32 | 32 | | | KR04/<br>IRQ1 | P104 | | GTETRGB | GTIOC1B | | | RXD0/<br>MISO0/<br>SCL0 | | SSLA1 | | | | | COM0 | TS13 |
| 72 | H3 | 45 | 45 | 33 | 33 | | | KR03 | P103 | | GTOWUP | GTIOC2A | | CTX0 | CTS0_<br>RTS0/<br>SS0 | | SSLA0 | | AN019 | | CMPREF1 | VL4 | |
| 73 | J1 | 46 | 46 | 34 | 34 | 28 | | KR02 | P102 | AGTO0 | GTOWLO | GTIOC2B | | CRX0 | SCK0<br>TXD2/<br>MOSI2/<br>SDA2 | | RSPCKA | | AN020/<br>ADTRG0 | | CMPIN1 | VL3 | |
| 74 | H2 | 47 | 47 | 35 | 35 | 29 | | KR01/<br>IRQ1 | P101 | AGTEE0 | GTETRGB | GTIOC5A | | | TXD0/<br>MOSI0/<br>SDA0<br>CTS1_<br>RTS1/<br>SS1 | SDA1 | MOSIA | | AN021 | | CMPREF0 | VL2 | |
| 75 | H4 | 48 | 48 | 36 | 36 | 30 | | KR00/<br>IRQ2 | P100 | AGTIO0 | GTETRGA | GTIOC5B | | | RXD0/<br>MISO0/<br>SCL0<br>SCK1 | SCL1 | MISOA | | AN022 | | CMPIN0 | VL1 | |
| 76 | K1 | 49 | 49 | 37 | 37 | | | | P500 | AGTOA0 | GTIU | GTIOC2A | | USB_VB<br>USEN | | | | | AN016 | | CMPREF1 | SEG34 | |
| 77 | J2 | 50 | 50 | | | | | IRQ11 | P501 | AGTOB0 | GTIV | GTIOC2B | | USB_OV<br>RCURA | TXD1/<br>MOSI1/<br>SDA1 | | | | AN017 | | CMPIN1 | SEG35 | |
| 78 | K2 | 51 | 51 | | | | | IRQ12 | P502 | | GTIW | GTIOC3B | | USB_OV<br>RCURB | RXD1/<br>MISO1/<br>SCL1 | | | | AN018 | | CMPREF0 | SEG36 | |
| 79 | G4 | | | | | | | | P503 | | | | | USB_EXI<br>CEN | SCK1 | | | | AN023 | | CMPIN0 | SEG37 | |
| 80 | G5 | | | | | | | | P504 | | | | | USB_ID | CTS1_<br>RTS1/<br>SS1 | | | | AN024 | | | | |
| 81 | G6 | | | | | | | IRQ14 | P505 | | | | | | | | | | AN025 | | | | |
| 82 | K3 | | | | | | VCC | | | | | | | | | | | | | | | | |

| Pin number | | | | | | | | | | Timers | | | | Communication interfaces | | | | | Analogs | | | HMI | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LGA100 | LQFP64 | QFN64 | LQFP48 | QFN48 | QFN40 | Power, System, Clock, Debug, CAC, VBATT | Interrupt | I/O ports | AGT | GPT_OPS, POEG | GPT | RTC | USBFS,CAN | SCI | IIC | SPI | SSIE | ADC14 | DAC12, OPAMP | ACMPLP | SLCDC | CTSU |
| 83 | J3 | | | | | | VSS | | | | | | | | | | | | | | | | |
| 84 | J4 | 52 | 52 | 38 | 38 | 31 | | IRQ7 | P015 | | | | | | | | | | AN010 | | | | TS28 |
| 85 | K4 | 53 | 53 | 39 | 39 | 32 | | | P014 | | | | | | | | | | AN009 | DA0 | | | |
| 86 | J5 | 54 | 54 | 40 | 40 | 33 | VREFL | | P013 | | | | | | | | | | AN008 | AMP1+ | | | |
| 87 | K5 | 55 | 55 | 41 | 41 | 34 | VREFH | | P012 | | | | | | | | | | AN007 | AMP1- | | | |
| 88 | H5 | 56 | 56 | 42 | 42 | 35 | AVCC0 | | | | | | | | | | | | | | | | |
| 89 | H6 | 57 | 57 | 43 | 43 | 36 | AVSS0 | | | | | | | | | | | | | | | | |
| 90 | J6 | 58 | 58 | 44 | 44 | 37 | VREFL0 | IRQ15 | P011 | | | | | | | | | | AN006 | AMP2+ | | | TS31 |
| 91 | K6 | 59 | 59 | 45 | 45 | 38 | VREFH0 | | P010 | | | | | | | | | | AN005 | AMP2- | | | TS30 |
| 92 | J7 | | | | | | | | P008 | | | | | | | | | | AN014 | | | | |
| 93 | H7 | | | | | | | | P007 | | | | | | | | | | AN013 | AMP3O | | | |
| 94 | G7 | | | | | | | | P006 | | | | | | | | | | AN012 | AMP3- | | | |
| 95 | K7 | | | | | | | IRQ10 | P005 | | | | | | | | | | AN011 | AMP3+ | | | |
| 96 | J8 | 60 | 60 | | | | | IRQ3 | P004 | | | | | | | | | | AN004 | AMP2O | | | |
| 97 | H8 | 61 | 61 | | | | | | P003 | | | | | | | | | | AN003 | AMP1O | | | |
| 98 | K8 | 62 | 62 | 46 | 46 | | | IRQ2 | P002 | | | | | | | | | | AN002 | AMP0O | | | |
| 99 | K9 | 63 | 63 | 47 | 47 | 39 | | IRQ7 | P001 | | | | | | | | | | AN001 | AMP0- | | | TS22 |
| 100 | K10 | 64 | 64 | 48 | 48 | 40 | | IRQ6 | P000 | | | | | | | | | | AN000 | AMP0+ | | | TS21 |

# 2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC*1 = AVCC0 = VCC_USB*2 = VCC_USB_LDO*2 = 1.6 to 5.5V, VREFH = VREFH0 = 1.6 to AVCC0, VBATT = 1.6 to 3.6V, VSS = AVSS0 = VREFL = VREFL0 = VSS_USB = 0V, $T_a = T_{opr}$

Note 1. The typical condition is set to VCC = 3.3V.
Note 2. When USBFS is not used.

Figure 2.1 shows the timing conditions.

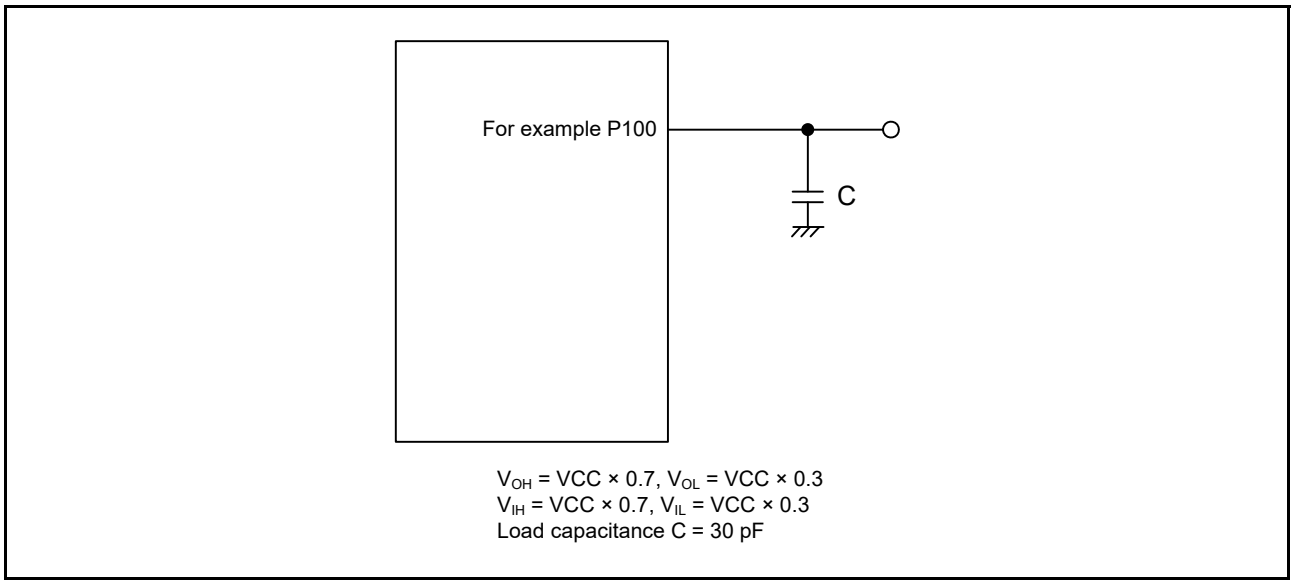



**Figure 2.1 Input or output timing measurement conditions**

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the AC specification of each function is not guaranteed.

## 2.1 Absolute Maximum Ratings

**Table 2.1 Absolute maximum ratings**

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power supply voltage | | VCC | -0.5 to +6.5 | V |
| Input voltage | 5 V-tolerant ports*1 | $V_{in}$ | -0.3 to +6.5 | V |
| | P000 to P008, P010 to P015 | $V_{in}$ | -0.3 to AVCC0 + 0.3 | V |
| | Others | $V_{in}$ | -0.3 to VCC + 0.3 | V |
| Reference power supply voltage | | VREFH0 | -0.3 to +6.5 | V |
| | | VREFH | | V |
| VBATT power supply voltage | | VBATT | -0.5 to +6.5 | V |
| Analog power supply voltage | | AVCC0 | -0.5 to +6.5 | V |
| USB power supply voltage | | VCC_USB | -0.5 to +6.5 | V |
| | | VCC_USB_LDO | -0.5 to +6.5 | V |
| Analog input voltage | When AN000 to AN014 are used | $V_{AN}$ | -0.3 to AVCC0 + 0.3 | V |
| | When AN016 to AN025 are used | | -0.3 to VCC + 0.3 | V |
| LCD voltage | VL1 voltage | $V_{L1}$ | -0.3 to +2.8 | V |
| | VL2 voltage | $V_{L2}$ | -0.3 to +6.5 | V |
| | VL3 voltage | $V_{L3}$ | -0.3 to +6.5 | V |
| | VL4 voltage | $V_{L4}$ | -0.3 to +6.5 | V |
| Operating temperature*2,*3,*4 | | $T_{opr}$ | -40 to +105 | °C |
| | | | -40 to +85 | |
| Storage temperature | | $T_{stg}$ | -55 to +125 | °C |

**Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.**
**To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, between the VREFH0 and VREFL0 pins, and between the VREFH and VREFL pins. Place capacitors of about 0.1 μF as close as possible to every power supply pin and use the shortest and heaviest possible traces. Also, connect capacitors as stabilization capacitance.**
**Connect the VCL pin to a VSS pin by a 4.7 μF capacitor. The capacitor must be placed close to the pin.**
**Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.**

Note 1. Ports P205, P206, P400 to P404, P407, P408 are 5 V tolerant.
Note 2. See section 2.2.1, Tj/Ta Definition.
Note 3. Contact a Renesas Electronics sales office for information on derating operation under $T_a$ = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.
Note 4. The upper limit of operating temperature is +85°C or +105°C, depending on the product. For details, see section 1.3, Part Numbering.

**Table 2.2 Recommended operating conditions**

| Parameter | Symbol | Value | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power supply voltages | VCC*1, *2 | When USBFS is not used | 1.6 | - | 5.5 | V |
| | | When USBFS is used USB Regulator Disable | VCC_USB | - | 3.6 | V |
| | | When USBFS is used USB Regulator Enable | VCC_USB _LDO | - | 5.5 | V |
| | VSS | | - | 0 | - | V |
| USB power supply voltages | VCC_USB | When USBFS is not used | - | VCC | - | V |
| | | When USBFS is used USB Regulator Disable (Input) | 3.0 | 3.3 | 3.6 | V |
| | VCC_USB_LDO | When USBFS is not used | - | VCC | - | V |
| | | When USBFS is used USB Regulator Disable | - | VCC | - | V |
| | | When USBFS is used USB Regulator Enable | 3.8 | - | 5.5 | V |
| | VSS_USB | | - | 0 | - | V |
| VBATT power supply voltage | VBATT | When the battery backup function is not used | - | VCC | - | V |
| | | When the battery backup function is used | 1.6 | - | 3.6 | V |
| Analog power supply voltages | AVCC0*1, *2 | | 1.6 | - | 5.5 | V |
| | AVSS0 | | - | 0 | - | V |
| | VREFH0 | When used as ADC14 Reference | 1.6 | - | AVCC0 | V |
| | VREFL0 | | - | 0 | - | V |
| | VREFH | When used as DAC12 Reference | 1.6 | - | AVCC0 | V |
| | VREFL | | - | 0 | - | V |

Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.2 V and AVCC0 ≥ 2.2 V.
AVCC0 = VCC when VCC < 2.2 V or AVCC0 < 2.2 V.

Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time, or power the VCC pin first and then the AVCC0 pin.

## 2.2 DC Characteristics

### 2.2.1 Tj/$T_a$ Definition

**Table 2.3 DC Characteristics**

Conditions: Products with operating temperature ($T_a$) -40 to +105°C

| Parameter | Symbol | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Permissible junction temperature | Tj | - | 125 | °C | High-speed mode<br>Middle-speed mode<br>Low-voltage mode<br>Low-speed mode<br>Subosc-speed mode |
| | | | 105*1 | | |

Note: Make sure that Tj = $T_a$ + θja × total power consumption (W),
where total power consumption = (VCC - $V_{OH}$) × $\Sigma I_{OH}$ + $V_{OL}$ × $\Sigma I_{OL}$ + $I_{CC}$max × VCC.

Note 1. The upper limit of operating temperature is +85°C or +105°C, depending on the product. For details, see section 1.3, Part Numbering. If the part number shows the operation temperature at 85°C, then the maximum value of $T_j$ is +105°C, otherwise, it is +125°C.

### 2.2.2 I/O $V_{IH}$, $V_{IL}$

**Table 2.4 I/O $V_{IH}$, $V_{IL}$ (1)**

Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 2.7 to 5.5V, VBATT = 1.6 to 3.6 V, VSS = AVSS0 = 0 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | IIC*1 (except for SMBus) | $V_{IH}$ | VCC × 0.7 | - | 5.8 | V | - |
| | | $V_{IL}$ | - | - | VCC × 0.3 | | |
| | | $\Delta V_T$ | VCC × 0.05 | - | - | | |
| | RES, NMI<br>Other peripheral input pins excluding IIC | $V_{IH}$ | VCC × 0.8 | - | - | | |
| | | $V_{IL}$ | - | - | VCC × 0.2 | | |
| | | $\Delta V_T$ | VCC × 0.1 | - | - | | |
| Input voltage (except for Schmitt trigger input pin) | IIC (SMBus)*2 | $V_{IH}$ | 2.2 | - | - | | VCC = 3.6 to 5.5 V |
| | | $V_{IH}$ | 2.0 | - | - | | VCC = 2.7 to 3.6 V |
| | | $V_{IL}$ | - | - | 0.8 | | - |
| | 5 V-tolerant ports*3 | $V_{IH}$ | VCC × 0.8 | - | 5.8 | | |
| | | $V_{IL}$ | - | - | VCC × 0.2 | | |
| | P914, P915 | $V_{IH}$ | VCC_USB × 0.8 | - | VCC_USB + 0.3 | | |
| | | $V_{IL}$ | - | - | VCC_USB × 0.2 | | |
| | P000 to P008, P010 to P015 | $V_{IH}$ | AVCC0 × 0.8 | - | - | | |
| | | $V_{IL}$ | - | - | AVCC0 × 0.2 | | |
| | EXTAL<br>Input ports pins except for P000 to P008, P010 to P015, P914, P915 | $V_{IH}$ | VCC × 0.8 | - | - | | |
| | | $V_{IL}$ | - | - | VCC × 0.2 | | |
| When $V_{BATT}$ power supply is selected | P402, P403, P404 | $V_{IH}$ | $V_{BATT}$ × 0.8 | - | $V_{BATT}$ + 0.3 | | |
| | | $V_{IL}$ | - | - | $V_{BATT}$ × 0.2 | | |
| | | $\Delta V_T$ | $V_{BATT}$ × 0.05 | - | - | | |

Note 1. P205, P206, P400, P401, P407, P408 (total 6 pins).
Note 2. P100, P101, P204, P205, P206, P400, P401, P407, P408 (total 9 pins).
Note 3. P205, P206, P400 to P404, P407, P408 (total 9 pins).

**Table 2.5 I/O $V_{IH}$, $V_{IL}$ (2)**

Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.6 to 2.7 V, VBATT = 1.6 to 3.6 V, VSS = AVSS0 = 0 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | RES, NMI Peripheral input pins | $V_{IH}$ | VCC × 0.8 | - | - | V | - |
| | | $V_{IL}$ | - | - | VCC × 0.2 | | |
| | | $\Delta V_T$ | VCC × 0.01 | - | - | | |
| Input voltage (except for Schmitt trigger input pin) | 5 V-tolerant ports*1 | $V_{IH}$ | VCC × 0.8 | - | 5.8 | | |
| | | $V_{IL}$ | - | - | VCC × 0.2 | | |
| | P914, P915 | $V_{IH}$ | VCC_USB × 0.8 | - | VCC_USB + 0.3 | | |
| | | $V_{IL}$ | - | - | VCC_USB × 0.2 | | |
| | P000 to P008, P010 to P015 | $V_{IH}$ | AVCC0 × 0.8 | - | - | | |
| | | $V_{IL}$ | - | - | AVCC0 × 0.2 | | |
| | EXTAL Input ports pins except for P000 to P008, P010 to P015, P914, P915 | $V_{IH}$ | VCC × 0.8 | - | - | | |
| | | $V_{IL}$ | - | - | VCC × 0.2 | | |
| When $V_{BATT}$ power supply is selected | P402, P403, P404 | $V_{IH}$ | $V_{BATT}$ × 0.8 | - | $V_{BATT}$ + 0.3 | | |
| | | $V_{IL}$ | - | - | $V_{BATT}$ × 0.2 | | |
| | | $\Delta V_T$ | $V_{BATT}$ × 0.01 | - | - | | |

Note 1. P205, P206, P400 to P404, P407, P408 (total 9 pins)

### 2.2.3 I/O $I_{OH}$, $I_{OL}$

**Table 2.6 I/O $I_{OH}$, $I_{OL}$ (1 of 2)**
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.6 to 5.5 V

| Parameter | | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Permissible output current (average value per pin) | Ports P212, P213 | - | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | Port P408 | Low drive*1 | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | | Middle drive for IIC Fast-mode*4 VCC = 2.7 to 5.5 V | $I_{OH}$ | - | - | -8.0 | mA |
| | | | $I_{OL}$ | - | - | 8.0 | mA |
| | | Middle drive*2 VCC = 3.0 to 5.5 V | $I_{OH}$ | - | - | -20.0 | mA |
| | | | $I_{OL}$ | - | - | 20.0 | mA |
| | Port P409 | Low drive*1 | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | | Middle drive*2 VCC = 2.7 to 3.0 V | $I_{OH}$ | - | - | -8.0 | mA |
| | | | $I_{OL}$ | - | - | 8.0 | mA |
| | | Middle drive*2 VCC = 3.0 to 5.5 V | $I_{OH}$ | - | - | -20.0 | mA |
| | | | $I_{OL}$ | - | - | 20.0 | mA |
| | Ports P100 to P115, P201 to P204, P300 to P307, P500 to P503, P600 to P603, P608 to P610, P808, P809 (total 41 pins) | Low drive*1 | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | | Middle drive*2 | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 8.0 | mA |
| | Ports P914, P915 | - | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | Other output pin*3 | Low drive*1 | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | | Middle drive*2 | $I_{OH}$ | - | - | -8.0 | mA |
| | | | $I_{OL}$ | - | - | 8.0 | mA |

**Table 2.6 I/O $I_{OH}$, $I_{OL}$ (2 of 2)**

Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.6 to 5.5 V

| Parameter | | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Permissible output current (Max value per pin) | Ports P212, P213 | - | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | Port P408 | Low drive*1 | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | | Middle drive for IIC Fast-mode*4 VCC = 2.7 to 5.5 V | $I_{OH}$ | - | - | -8.0 | mA |
| | | | $I_{OL}$ | - | - | 8.0 | mA |
| | | Middle drive*2 VCC = 3.0 to 5.5 V | $I_{OH}$ | - | - | -20.0 | mA |
| | | | $I_{OL}$ | - | - | 20.0 | mA |
| | Port P409 | Low drive*1 | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | | Middle drive*2 VCC = 2.7 to 3.0 V | $I_{OH}$ | - | - | -8.0 | mA |
| | | | $I_{OL}$ | - | - | 8.0 | mA |
| | | Middle drive*2 VCC = 3.0 to 5.5 V | $I_{OH}$ | - | - | -20.0 | mA |
| | | | $I_{OL}$ | - | - | 20.0 | mA |
| | Ports P100 to P115, P201 to P204, P300 to P307, P500 to P503, P600 to P603, P608 to P610, P808, P809 (total 41 pins) | Low drive*1 | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | | Middle drive*2 | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 8.0 | mA |
| | Ports P914, P915 | - | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | Other output pin*3 | Low drive*1 | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | | Middle drive*2 | $I_{OH}$ | - | - | -8.0 | mA |
| | | | $I_{OL}$ | - | - | 8.0 | mA |
| Permissible output current (max value total pins) | Total of ports P000 to P008, P010 to P015 | | $\Sigma I_{OH\ (max)}$ | - | - | -30 | mA |
| | | | $\Sigma I_{OL\ (max)}$ | - | - | 30 | mA |
| | Ports P914, P915 | | $\Sigma I_{OH\ (max)}$ | - | - | -2.0 | mA |
| | | | $\Sigma I_{OL\ (min)}$ | - | - | 2.0 | mA |
| | Total of all output pin*5 | | $\Sigma I_{OH\ (max)}$ | - | - | -60 | mA |
| | | | $\Sigma I_{OL\ (max)}$ | - | - | 60 | mA |

**Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 μs.**

Note 1. This is the value when low driving ability is selected with the Port Drive Capability bit in PmnPFS register.
Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in PmnPFS register.
Note 3. Except for ports P200, P214, P215, which are input ports.
Note 4. This is the value when middle driving ability for IIC Fast-mode is selected with the Port Drive Capability bit in PmnPFS register.
Note 5. For details on the permissible output current used with CTSU, see section 2.11, CTSU Characteristics.

### 2.2.4 I/O $V_{OH}$, $V_{OL}$, and Other Characteristics

**Table 2.7 I/O $V_{OH}$, $V_{OL}$ (1)**
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 4.0 to 5.5 V

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| Output voltage | IIC*1 | | $V_{OL}$ | - | - | 0.4 | V | $I_{OL}$ = 3.0 mA |
| | | | $V_{OL}$*2,*5 | - | - | 0.6 | | $I_{OL}$ = 6.0 mA |
| | Ports P408, P409*2, *3 | | $V_{OH}$ | VCC - 1.0 | - | - | | $I_{OH}$ = -20 mA |
| | | | $V_{OL}$ | - | - | 1.0 | | $I_{OL}$ = 20 mA |
| | Ports P000 to P008, P010 to P015 | Low drive | $V_{OH}$ | AVCC0 - 0.8 | - | - | | $I_{OH}$ = -2.0 mA |
| | | | $V_{OL}$ | - | - | 0.8 | | $I_{OL}$ = 2.0 mA |
| | | Middle drive | $V_{OH}$ | AVCC0 - 0.8 | - | - | | $I_{OH}$ = -4.0 mA |
| | | | $V_{OL}$ | - | - | 0.8 | | $I_{OL}$ = 4.0 mA |
| | Ports P914, P915 | | $V_{OH}$ | VCC_USB - 0.8 | - | - | | $I_{OH}$ = -2.0 mA |
| | | | $V_{OL}$ | - | - | 0.8 | | $I_{OL}$ = 2.0 mA |
| | Other output pins*4 | Low drive | $V_{OH}$ | VCC - 0.8 | - | - | | $I_{OH}$ = -2.0 mA |
| | | | $V_{OL}$ | - | - | 0.8 | | $I_{OL}$ = 2.0 mA |
| | | Middle drive*6 | $V_{OH}$ | VCC - 0.8 | - | - | | $I_{OH}$ = -4.0 mA |
| | | | $V_{OL}$ | - | - | 0.8 | | $I_{OL}$ = 4.0 mA |

Note 1. P100, P101, P204, P205, P206, P400, P401, P407, P408 (total 9 pins).
Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in PmnPFS register.
Note 3. Based on characterization data, not tested in production.
Note 4. Except for ports P200, P214, P215, which are input ports.
Note 5. This is the value when middle driving ability for IIC is selected in the Port Drive Capability bit in PmnPFS register for P408.
Note 6. Except for P212, P213.

**Table 2.8 I/O $V_{OH}$, $V_{OL}$ (2)**
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 2.7 to 4.0 V

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| Output voltage | IIC*1 | | $V_{OL}$ | - | - | 0.4 | V | $I_{OL}$ = 3.0 mA |
| | | | $V_{OL}$*2,*5 | - | - | 0.6 | | $I_{OL}$ = 6.0 mA |
| | Ports P408, P409*2, *3 | | $V_{OH}$ | VCC - 1.0 | - | - | | $I_{OH}$ = -20 mA<br>VCC = 3.3 V |
| | | | $V_{OL}$ | - | - | 1.0 | | $I_{OL}$ = 20 mA<br>VCC = 3.3 V |
| | Ports P000 to P008, P010 to P015 | Low drive | $V_{OH}$ | AVCC0 - 0.5 | - | - | | $I_{OH}$ = -1.0 mA |
| | | | $V_{OL}$ | - | - | 0.5 | | $I_{OL}$ = 1.0 mA |
| | | Middle drive | $V_{OH}$ | AVCC0 - 0.5 | - | - | | $I_{OH}$ = -2.0 mA |
| | | | $V_{OL}$ | - | - | 0.5 | | $I_{OL}$ = 2.0 mA |
| | Ports P914, P915 | | $V_{OH}$ | VCC_USB - 0.5 | - | - | | $I_{OH}$ = -1.0 mA |
| | | | $V_{OL}$ | - | - | 0.5 | | $I_{OL}$ = 1.0 mA |
| | Other output pins*4 | Low drive | $V_{OH}$ | VCC - 0.5 | - | - | | $I_{OH}$ = -1.0 mA |
| | | | $V_{OL}$ | - | - | 0.5 | | $I_{OL}$ = 1.0 mA |
| | | Middle drive*6 | $V_{OH}$ | VCC - 0.5 | - | - | | $I_{OH}$ = -2.0 mA |
| | | | $V_{OL}$ | - | - | 0.5 | | $I_{OL}$ = 2.0 mA |

Note 1. P100, P101, P204, P205, P206, P400, P401, P407, P408 (total 9 pins).
Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in PmnPFS register.
Note 3. Based on characterization data, not tested in production.
Note 4. Except for ports P200, P214, P215, which are input ports.
Note 5. This is the value when middle driving ability for IIC is selected in the Port Drive Capability bit in PmnPFS register for P408.
Note 6. Except for P212, P213.

**Table 2.9 I/O $V_{OH}$, $V_{OL}$ (3)**

Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.6 to 2.7 V

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| Output voltage | Ports P000 to P015 | Low drive | $V_{OH}$ | AVCC0 - 0.3 | - | - | V | $I_{OH}$ = -0.5 mA |
| | | | $V_{OL}$ | - | - | 0.3 | | $I_{OL}$ = 0.5 mA |
| | | Middle drive | $V_{OH}$ | AVCC0 - 0.3 | - | - | | $I_{OH}$ = -1.0 mA |
| | | | $V_{OL}$ | - | - | 0.3 | | $I_{OL}$ = 1.0 mA |
| | Ports P914, P915 | | $V_{OH}$ | VCC_USB - 0.3 | - | - | | $I_{OH}$ = -0.5 mA |
| | | | $V_{OL}$ | - | - | 0.3 | | $I_{OL}$ = 0.5 mA |
| | Other output pins*1 | Low drive | $V_{OH}$ | VCC - 0.3 | - | - | | $I_{OH}$ = -0.5 mA |
| | | | $V_{OL}$ | - | - | 0.3 | | $I_{OL}$ = 0.5 mA |
| | | Middle drive*2 | $V_{OH}$ | VCC - 0.3 | - | - | | $I_{OH}$ = -1.0 mA |
| | | | $V_{OL}$ | - | - | 0.3 | | $I_{OL}$ = 1.0 mA |

Note 1. Except for ports P200, P214, P215, which are input ports.
Note 2. Except for P212, P213.

**Table 2.10 I/O other characteristics**

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Input leakage current | RES, P200, P214, P215 | $\lvert I_{in} \rvert$ | - | - | 1.0 | μA | $V_{in}$ = 0 V<br>$V_{in}$ = VCC |
| Three-state leakage current (off state) | 5 V-tolerant ports | $\lvert I_{TSI} \rvert$ | - | - | 1.0 | μA | $V_{in}$ = 0 V<br>$V_{in}$ = 5.8 V |
| | Other ports (except for ports P200, P214, P215 and 5 V tolerant) | | - | - | 1.0 | | $V_{in}$ = 0 V<br>$V_{in}$ = VCC |
| Input pull-up resistor | All ports (except for ports P200, P214, P215, P914, P915) | $R_U$ | 10 | 20 | 50 | kΩ | $V_{in}$ = 0 V |
| Input capacitance | P914, P915, P100 to P103, P111, P112, P200 | $C_{in}$ | - | - | 30 | pF | $V_{in}$ = 0 V<br>f = 1 MHz<br>$T_a$ = 25°C |
| | Other input pins | | - | - | 15 | | |

### 2.2.5 I/O Pin Output Characteristics of Low Drive Capacity

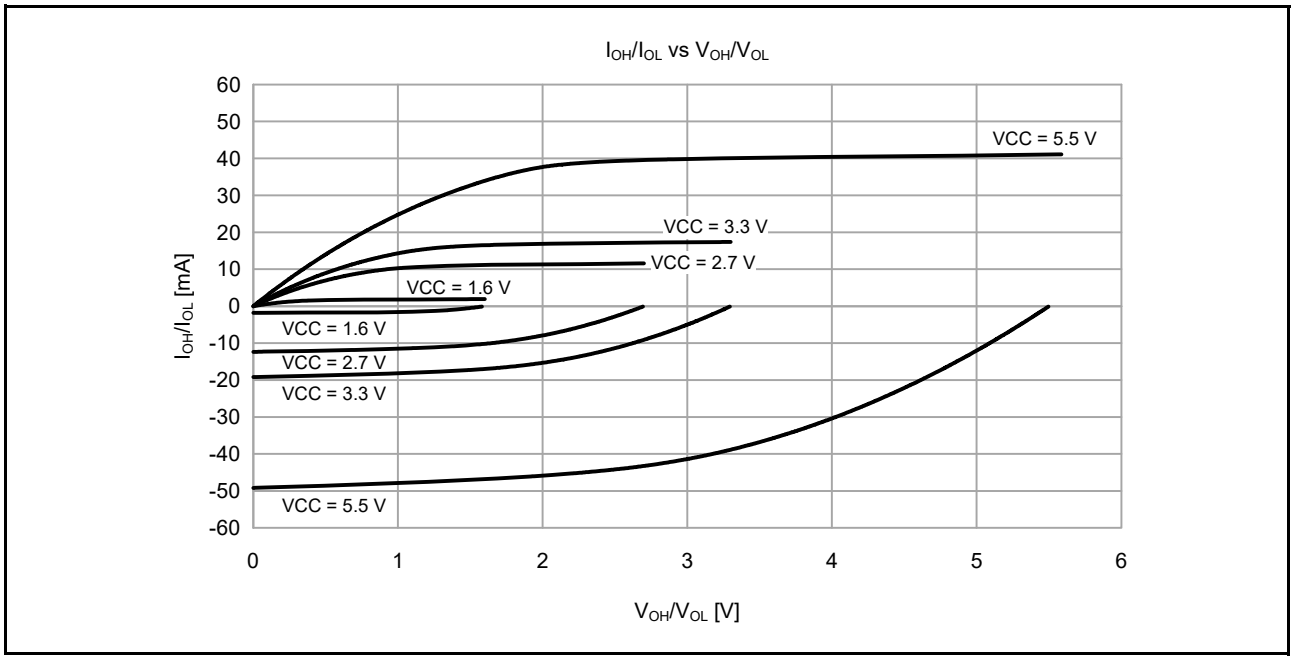



**Figure 2.2** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ Voltage Characteristics at $T_a$ = 25°C when low drive output is selected (reference data)**

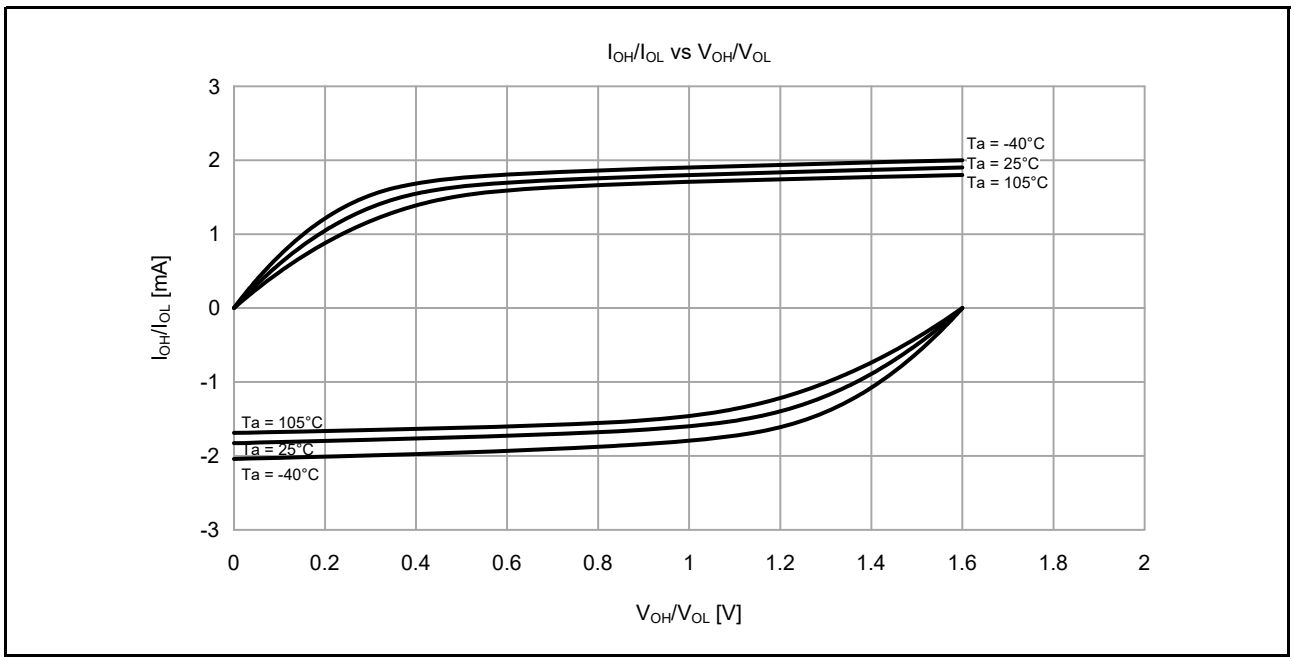



**Figure 2.3** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ temperature characteristics at VCC = 1.6 V when low drive output is selected (reference data)**

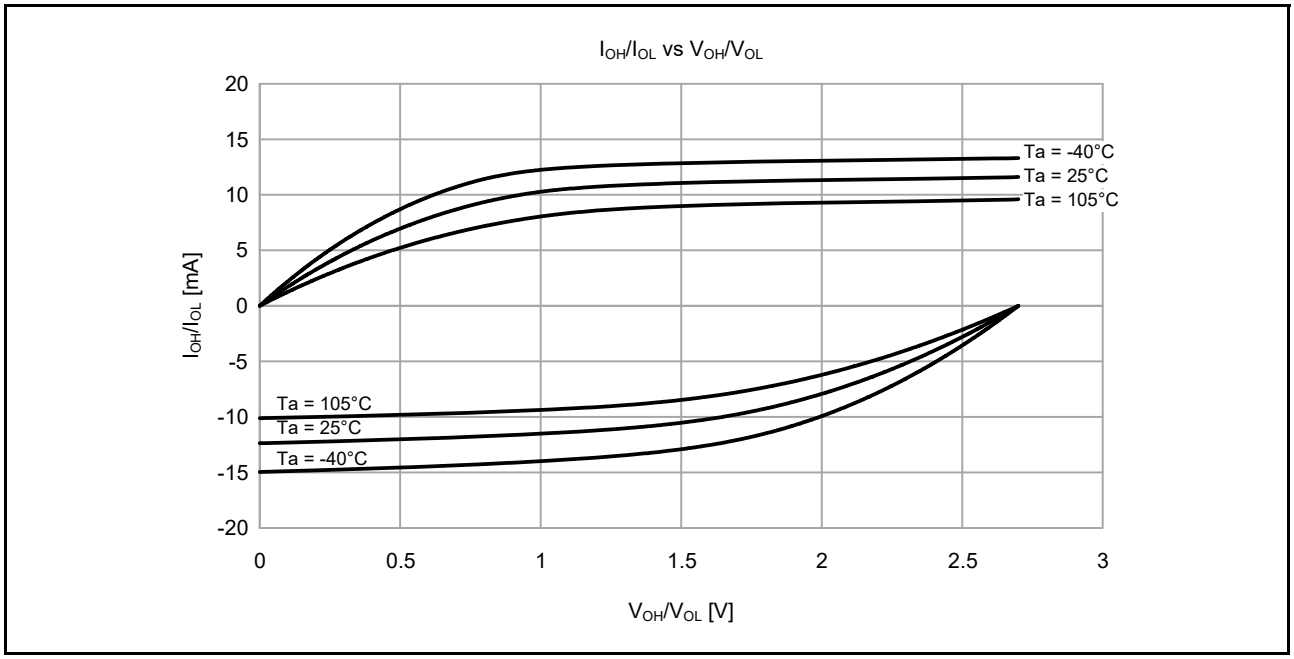



**Figure 2.4** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ temperature characteristics at VCC = 2.7 V when low drive output is selected (reference data)**

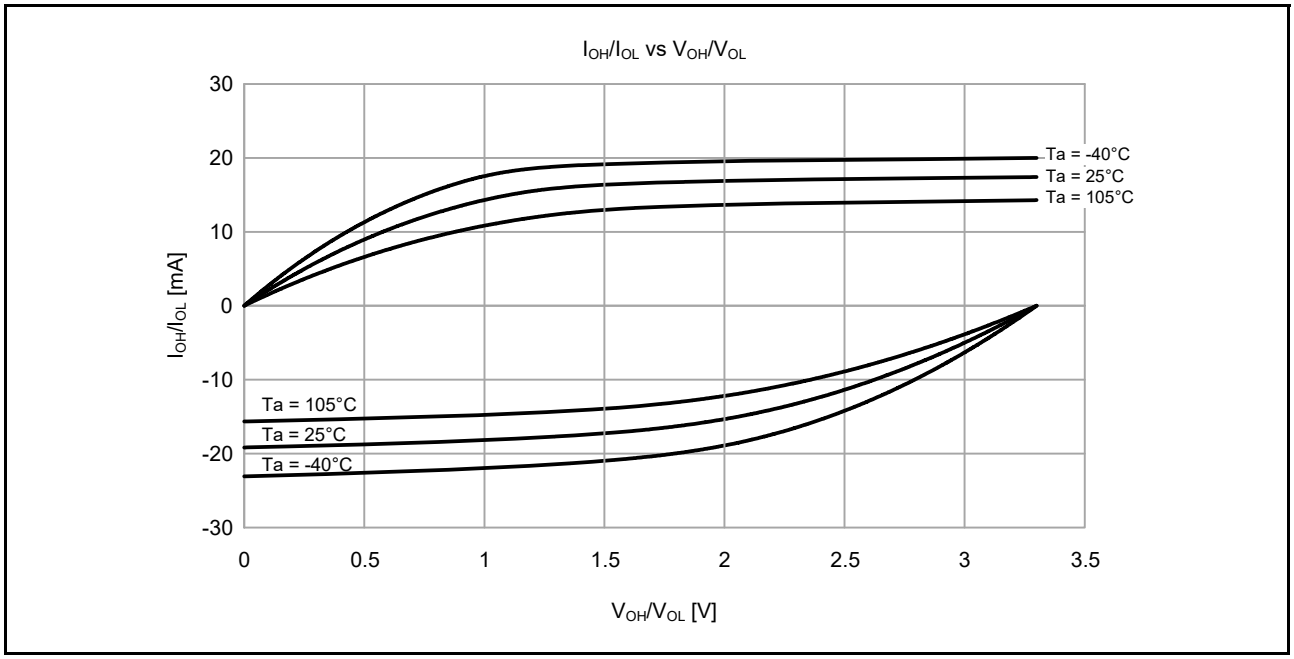



**Figure 2.5** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ temperature characteristics at VCC = 3.3 V when low drive output is selected (reference data)**

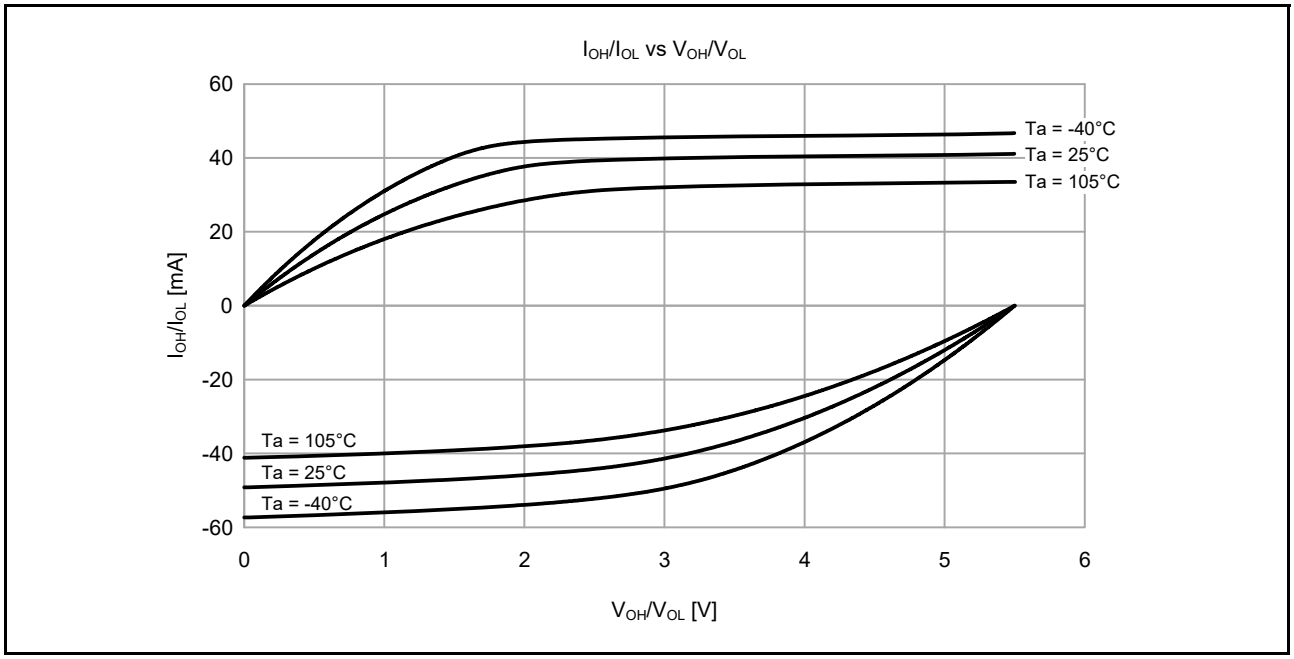



**Figure 2.6** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ temperature characteristics at VCC = 5.5 V when low drive output is selected (reference data)**

### 2.2.6 I/O Pin Output Characteristics of Middle Drive Capacity

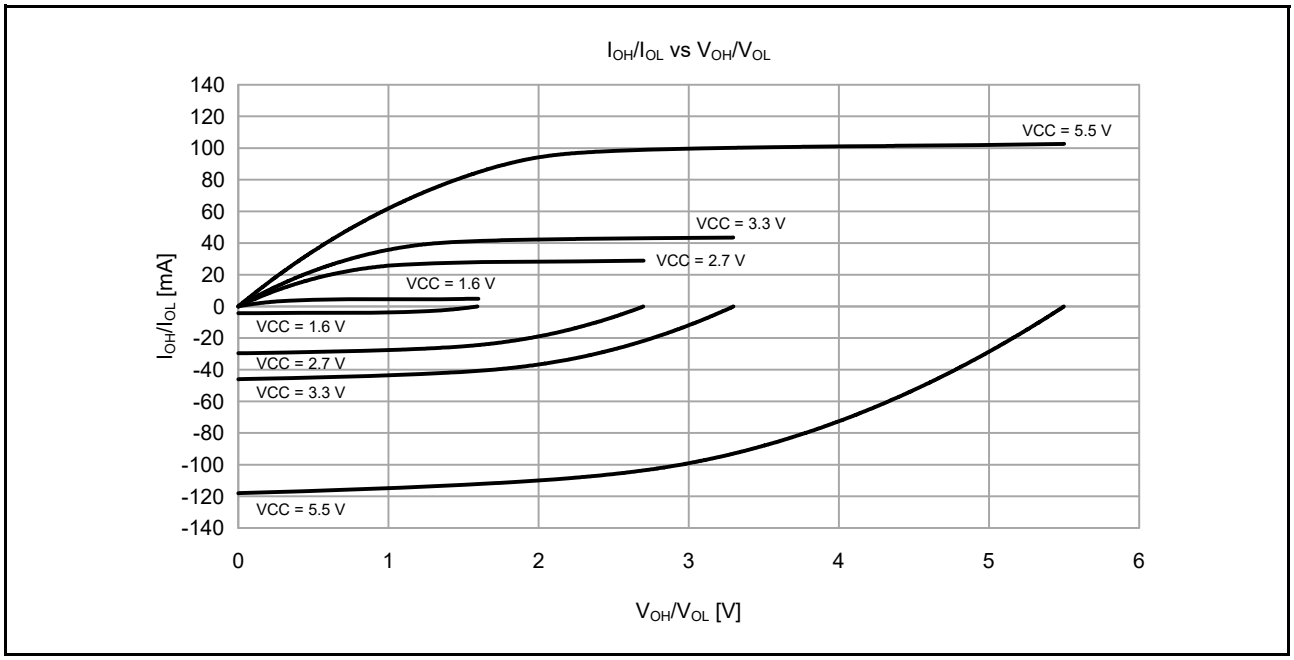



**Figure 2.7** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ voltage characteristics at $T_a$ = 25°C when middle drive output is selected (reference data)**

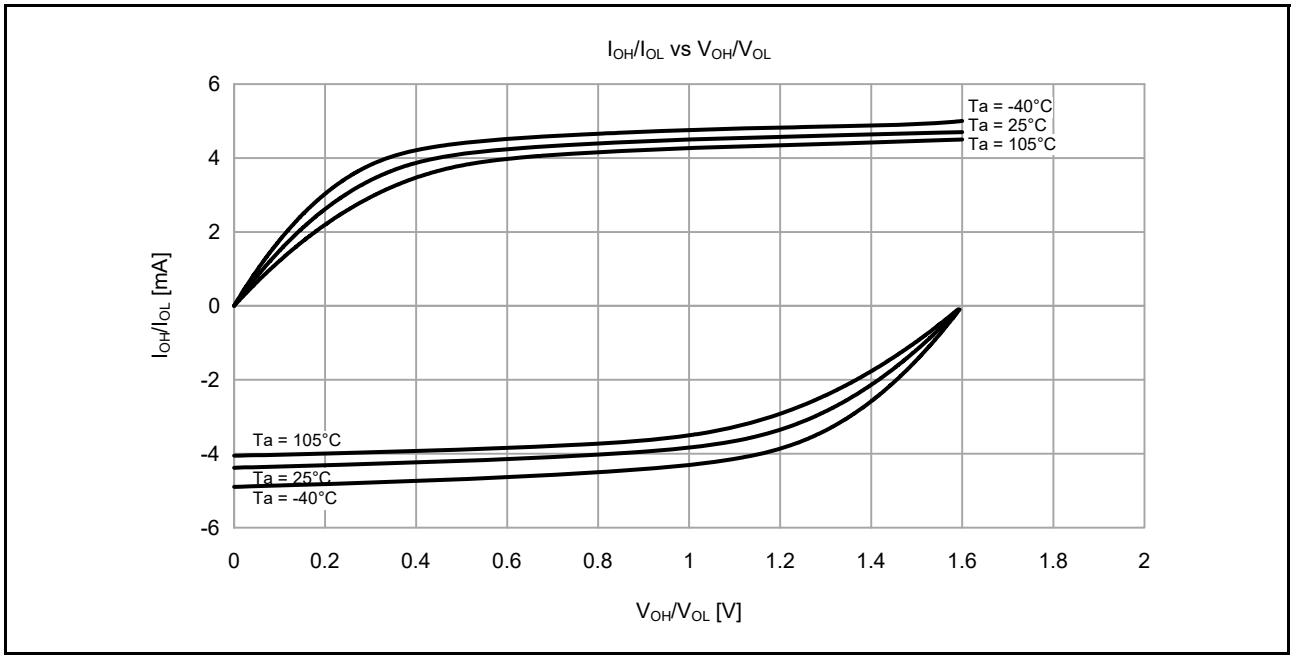



**Figure 2.8** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ temperature characteristics at VCC = 1.6 V when middle drive output is selected (reference data)**

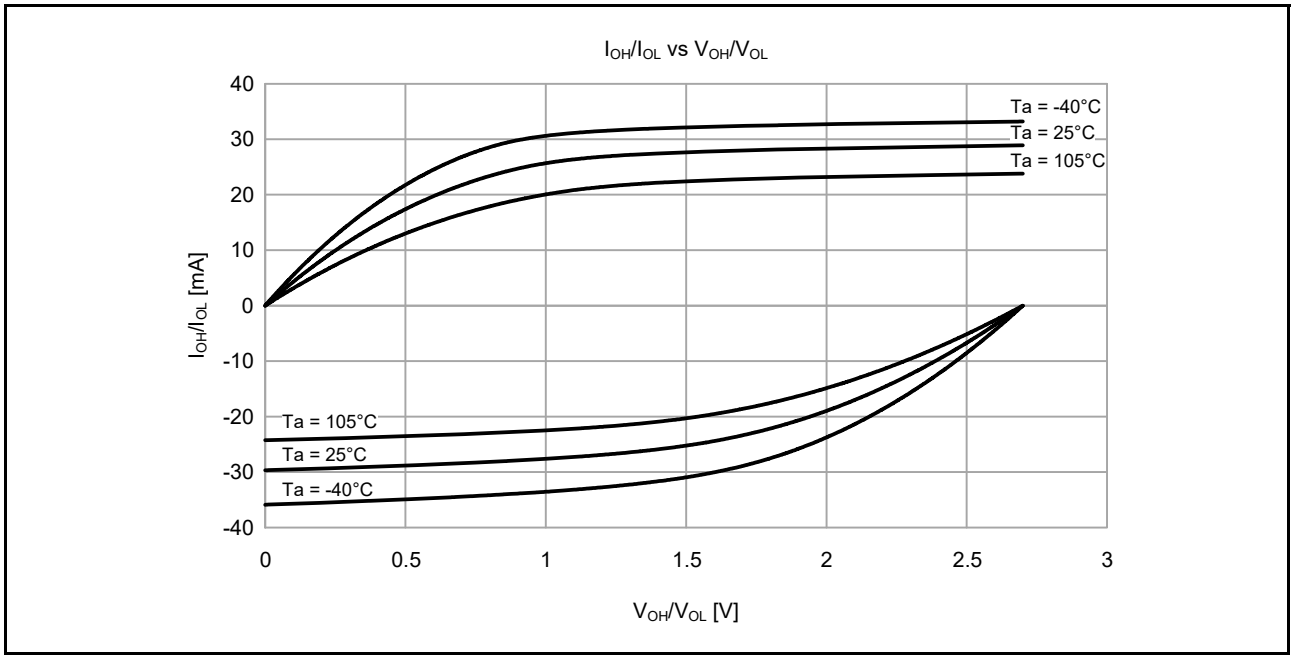



**Figure 2.9** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ temperature characteristics at VCC = 2.7 V when middle drive output is selected (reference data)**

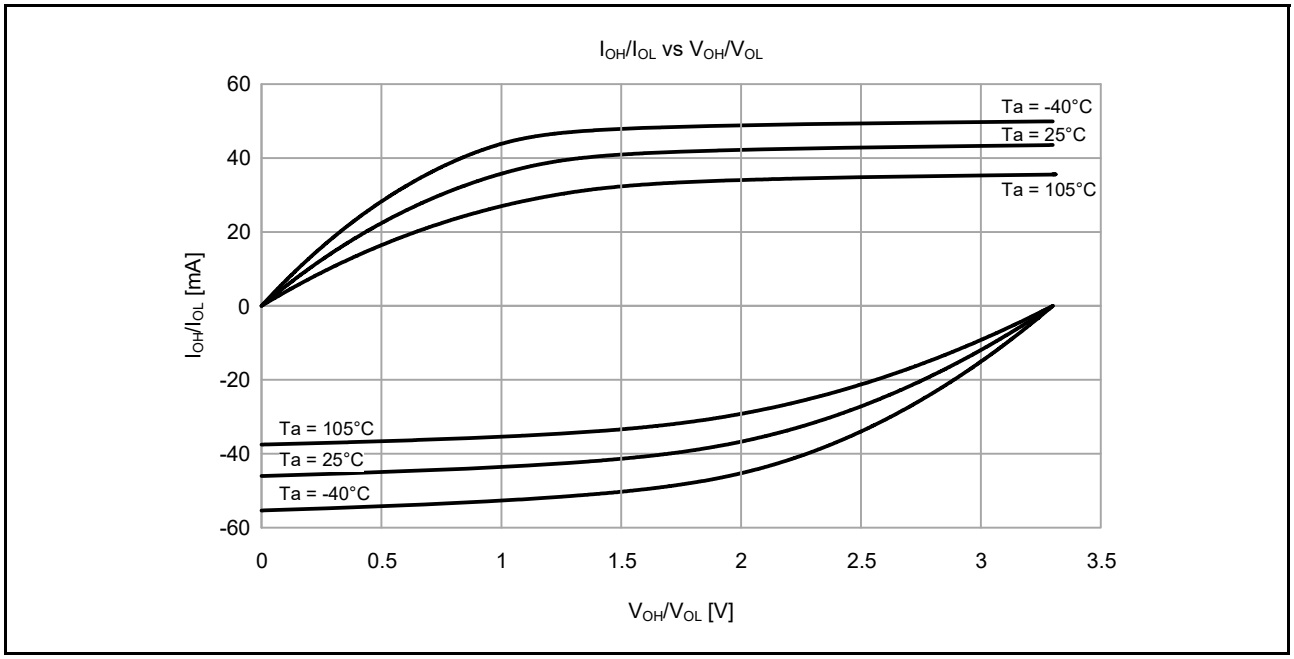



**Figure 2.10** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ temperature characteristics at VCC = 3.3 V when middle drive output is selected (reference data)**

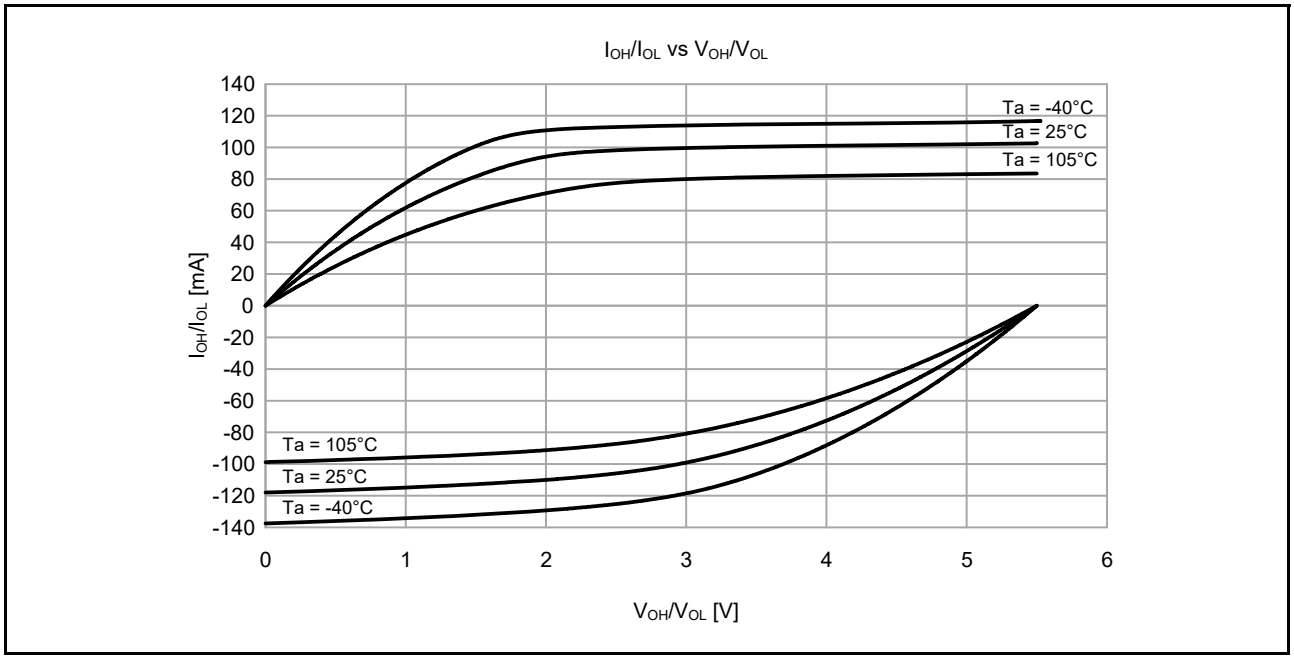



**Figure 2.11** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ temperature characteristics at VCC = 5.5 V when middle drive output is selected (reference data)**

### 2.2.7 P408, P409 I/O Pin Output Characteristics of Middle Drive Capacity

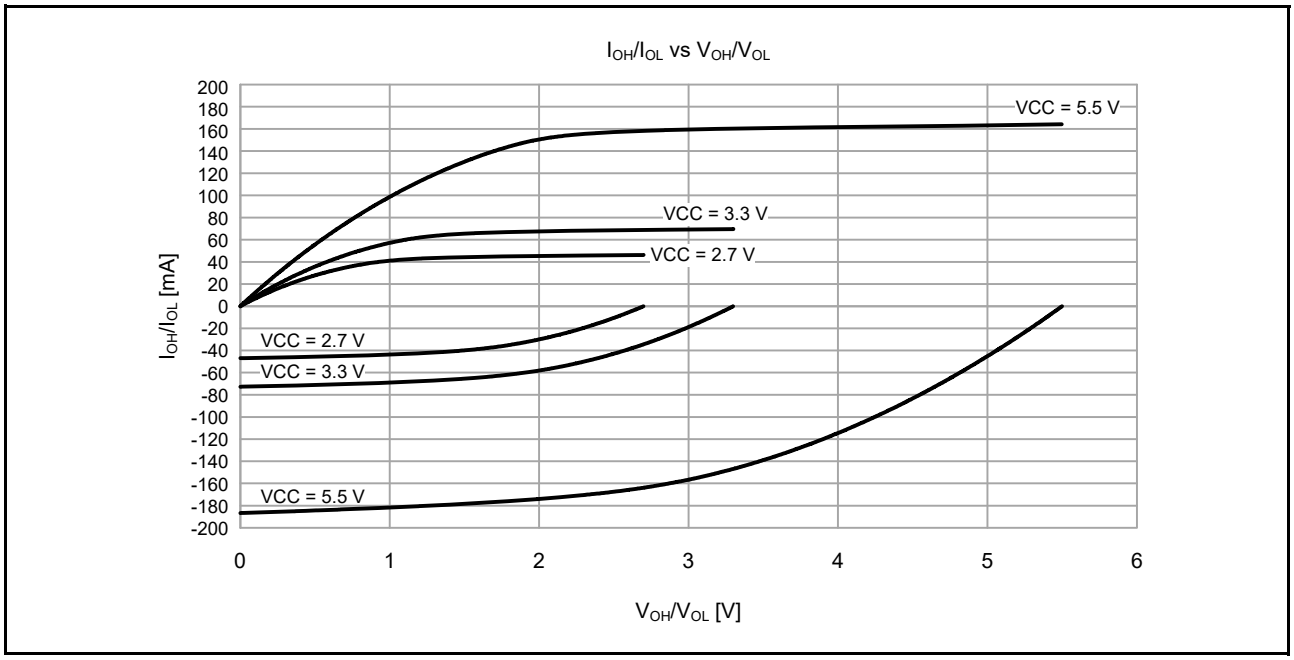



**Figure 2.12** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ voltage characteristics at Ta = 25°C when middle drive output is selected (reference data)**

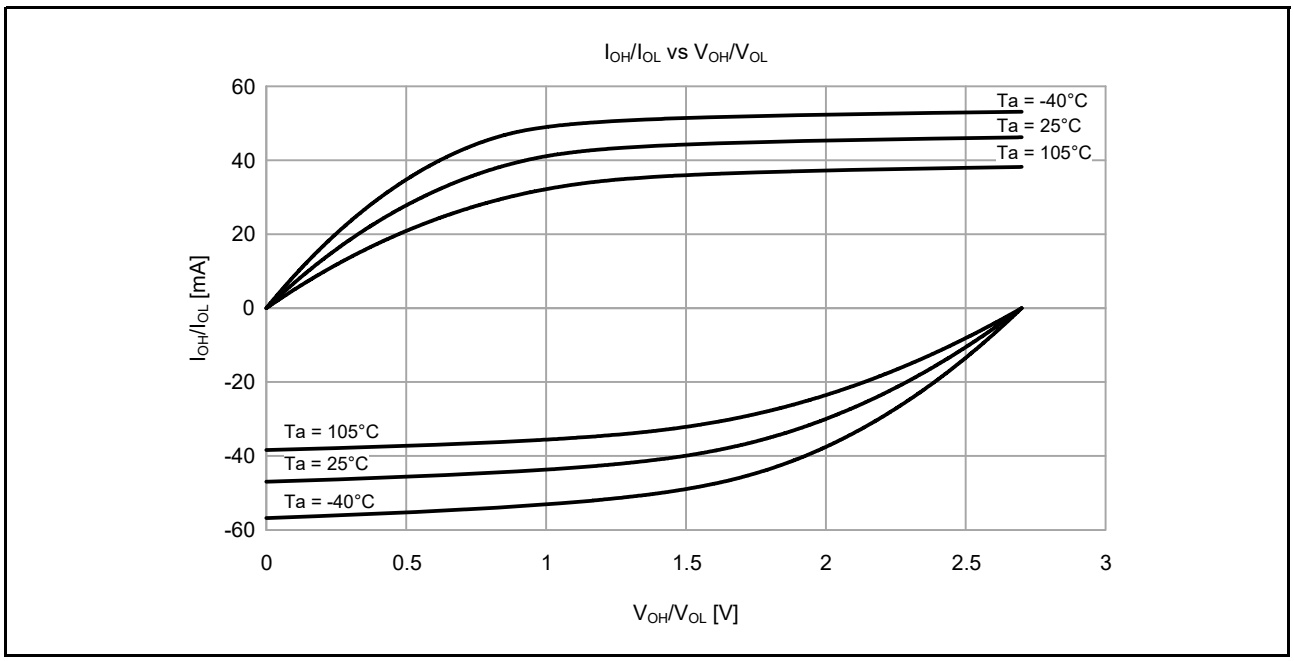



**Figure 2.13** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ temperature characteristics at VCC = 2.7 V when middle drive output is selected (reference data)**

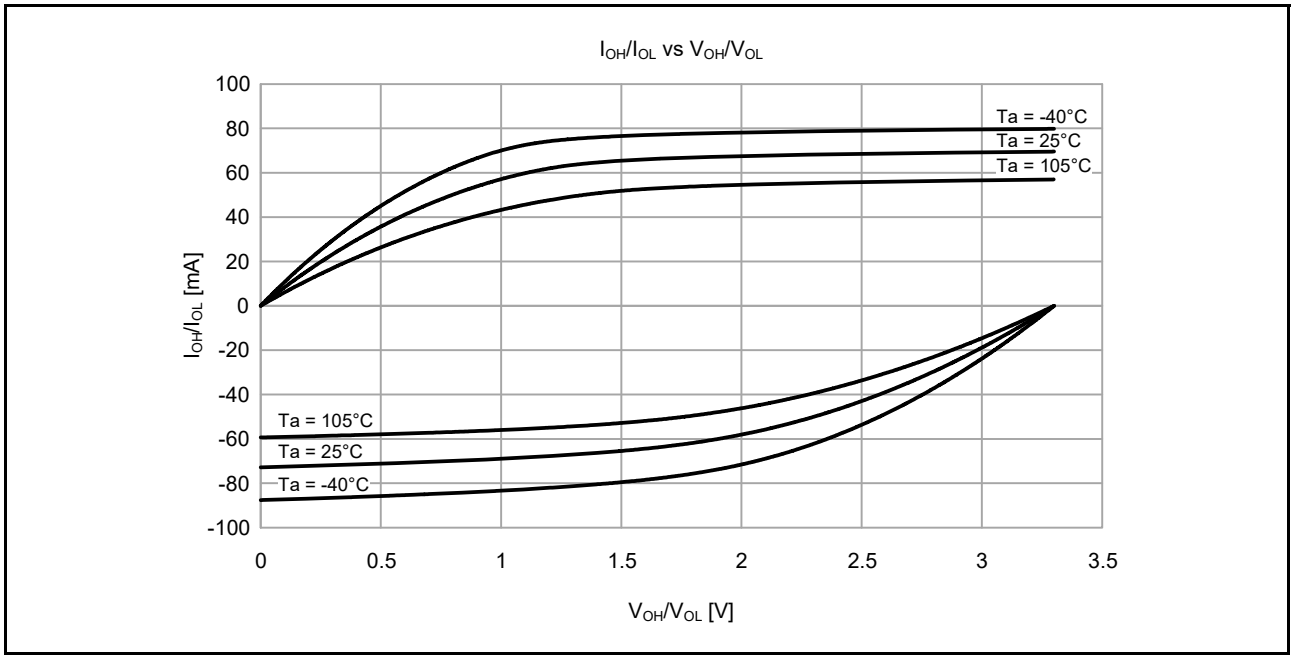



**Figure 2.14** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ temperature characteristics at VCC = 3.3 V when middle drive output is selected (reference data)**

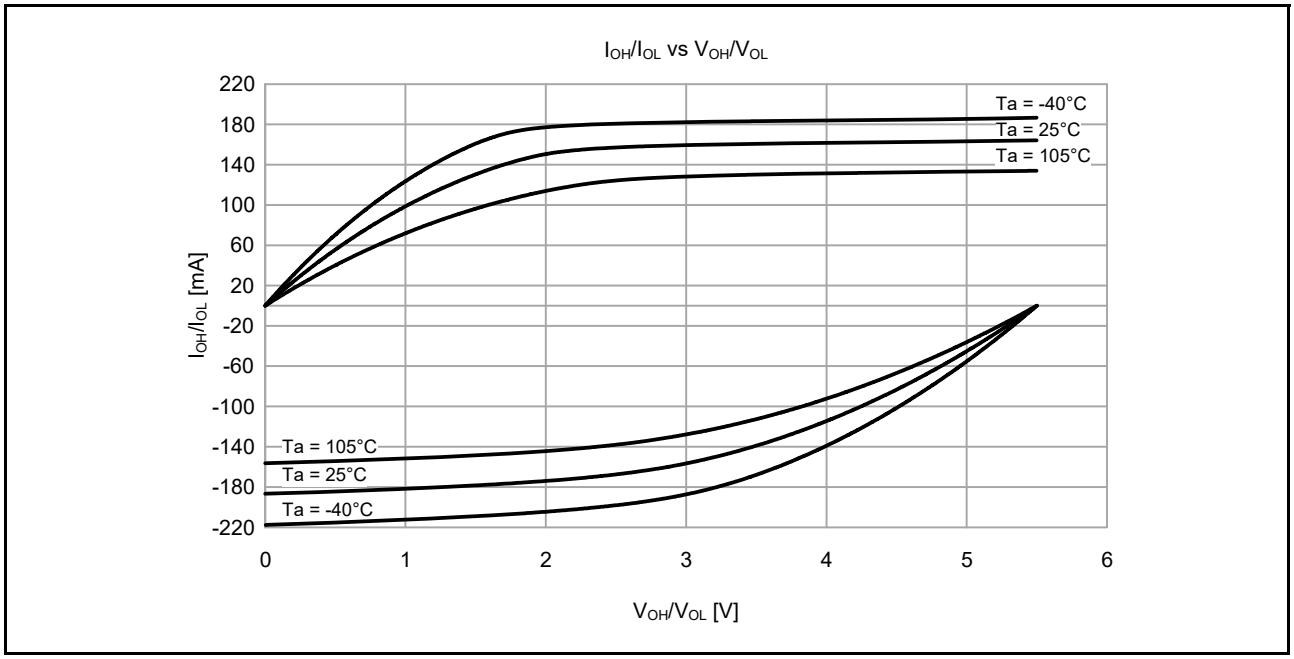



**Figure 2.15** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ temperature characteristics at VCC = 5.5 V when middle drive output is selected (reference data)**

### 2.2.8 IIC I/O Pin Output Characteristics

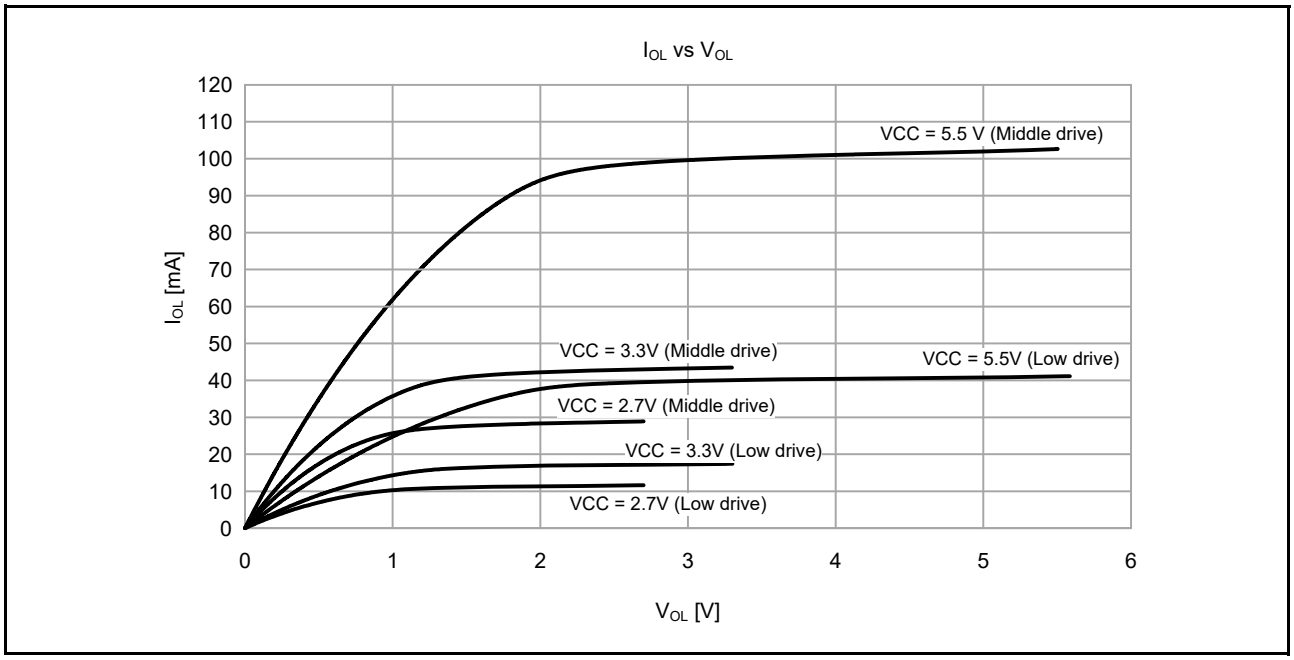



**Figure 2.16** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ voltage characteristics at Ta = 25°C**

## 2.2.9 Operating and Standby Current

**Table 2.11 Operating and standby current (1) (1 of 2)**

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

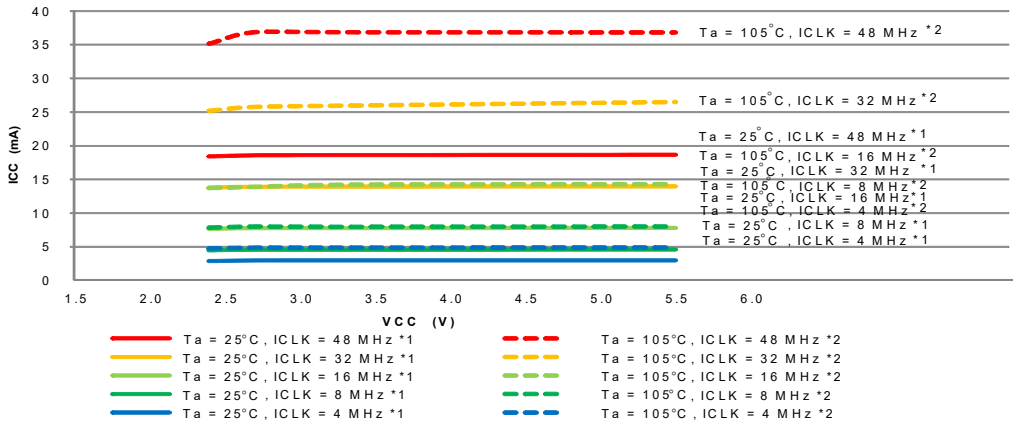
| Parameter | | | | | Symbol | Typ*10 | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|
| Supply current*1 | High-speed mode*2 | Normal mode | All peripheral clock disabled, while (1) code executing from flash*5 | ICLK = 48 MHz | $I_{CC}$ | 8.3 | - | mA | *7 |
| | | | | ICLK = 32 MHz | | 5.8 | - | | |
| | | | | ICLK = 16 MHz | | 3.5 | - | | |
| | | | | ICLK = 8 MHz | | 2.2 | - | | |
| | | | All peripheral clock disabled, CoreMark code executing from flash*5 | ICLK = 48 MHz | | 16.4 | - | | |
| | | | | ICLK = 32 MHz | | 11.3 | - | | |
| | | | | ICLK = 16 MHz | | 6.4 | - | | |
| | | | | ICLK = 8 MHz | | 4.0 | - | | |
| | | | All peripheral clock enabled, while (1) code executing from flash*5 | ICLK = 48 MHz | | 18.5 | - | | *9 |
| | | | | ICLK = 32 MHz | | 13.8 | - | | *8 |
| | | | | ICLK = 16 MHz | | 7.7 | - | | |
| | | | | ICLK = 8 MHz | | 4.5 | - | | |
| | | | All peripheral clock enabled, code executing from SRAM*5 | ICLK = 48 MHz | | - | 50.0 | | *9 |
| | | Sleep mode | All peripheral clock disabled*5 | ICLK = 48 MHz | | 3.3 | - | | *7 |
| | | | | ICLK = 32 MHz | | 2.4 | - | | |
| | | | | ICLK = 16 MHz | | 1.8 | - | | |
| | | | | ICLK = 8 MHz | | 1.4 | - | | |
| | | | All peripheral clock enabled*5 | ICLK = 48 MHz | | 13.4 | - | | *9 |
| | | | | ICLK = 32 MHz | | 10.4 | - | | *8 |
| | | | | ICLK = 16 MHz | | 6.0 | - | | |
| | | | | ICLK = 8 MHz | | 3.6 | - | | |
| | | Increase during BGO operation*6 | | | | 2.5 | - | | - |
| | Middle-speed mode*2 | Normal mode | All peripheral clock disabled, while (1) code executing from flash*5 | ICLK = 12 MHz | $I_{CC}$ | 2.5 | - | mA | *7 |
| | | | | ICLK = 8 MHz | | 2.0 | - | | |
| | | | | ICLK = 1 MHz | | 0.9 | - | | |
| | | | All peripheral clock disabled, CoreMark code executing from flash*5 | ICLK = 12 MHz | | 4.7 | - | | |
| | | | | ICLK = 8 MHz | | 3.7 | - | | |
| | | | | ICLK = 1 MHz | | 1.2 | - | | |
| | | | All peripheral clock enabled, while (1) code executing from flash*5 | ICLK = 12 MHz | | 5.7 | - | | *8 |
| | | | | ICLK = 8 MHz | | 4.3 | - | | |
| | | | | ICLK = 1 MHz | | 1.5 | - | | |
| | | | All peripheral clock enabled, code executing from SRAM*5 | ICLK = 12 MHz | | - | 20.0 | | |
| | | Sleep mode | All peripheral clock disabled*5 | ICLK = 12 MHz | | 1.2 | - | | *7 |
| | | | | ICLK = 8 MHz | | 1.2 | - | | |
| | | | | ICLK = 1 MHz | | 0.8 | - | | |
| | | | All peripheral clock enabled*5 | ICLK = 12 MHz | | 4.4 | - | | *8 |
| | | | | ICLK = 8 MHz | | 3.4 | - | | |
| | | | | ICLK = 1 MHz | | 1.4 | - | | |
| | | Increase during BGO operation*6 | | | | 2.5 | - | | - |

**Table 2.11 Operating and standby current (1) (2 of 2)**

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

| Parameter | | | | | Symbol | Typ*10 | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|
| Supply current*1 | Low-speed mode*3 | Normal mode | All peripheral clock disabled, while (1) code executing from flash*5 | ICLK = 1 MHz | $I_{CC}$ | 0.4 | - | mA | *7 |
| | | | All peripheral clock disabled, CoreMark code executing from flash*5 | ICLK = 1 MHz | | 0.6 | - | | |
| | | | All peripheral clock enabled, while (1) code executing from flash*5 | ICLK = 1 MHz | | 1.0 | - | | *8 |
| | | | All peripheral clock enabled, code executing from SRAM*5 | ICLK = 1 MHz | | - | 2.2 | | |
| | | Sleep mode | All peripheral clock disabled*5 | ICLK = 1 MHz | | 0.3 | - | | *7 |
| | | | All peripheral clock enabled*5 | ICLK = 1 MHz | | 0.9 | - | | *8 |
| | Low-voltage mode*3 | Normal mode | All peripheral clock disabled, while (1) code executing from flash*5 | ICLK = 4 MHz | $I_{CC}$ | 1.7 | - | mA | *7 |
| | | | All peripheral clock disabled, CoreMark code executing from flash*5 | ICLK = 4 MHz | | 2.8 | - | | |
| | | | All peripheral clock enabled, while (1) code executing from flash*5 | ICLK = 4 MHz | | 3.0 | - | | *8 |
| | | | All peripheral clock enabled, code executing from SRAM*5 | ICLK = 4 MHz | | - | 8.0 | | |
| | | Sleep mode | All peripheral clock disabled*5 | ICLK = 4 MHz | | 1.3 | - | | *7 |
| | | | All peripheral clock enabled*5 | ICLK = 4 MHz | | 2.5 | - | | *8 |
| | Subosc-speed mode*4 | Normal mode | All peripheral clock disabled, while (1) code executing from flash*5 | ICLK = 32.768 kHz | $I_{CC}$ | 8.5 | - | μA | *8 |
| | | | All peripheral clock enabled, while (1) code executing from flash*5 | ICLK = 32.768 kHz | | 14.9 | - | | |
| | | | All peripheral clock enabled, code executing from SRAM*5 | ICLK = 32.768 kHz | | - | 83.0 | | |
| | | Sleep mode | All peripheral clock disabled*5 | ICLK = 32.768 kHz | | 5.0 | - | | |
| | | | All peripheral clock enabled*5 | ICLK = 32.768 kHz | | 11.4 | - | | |

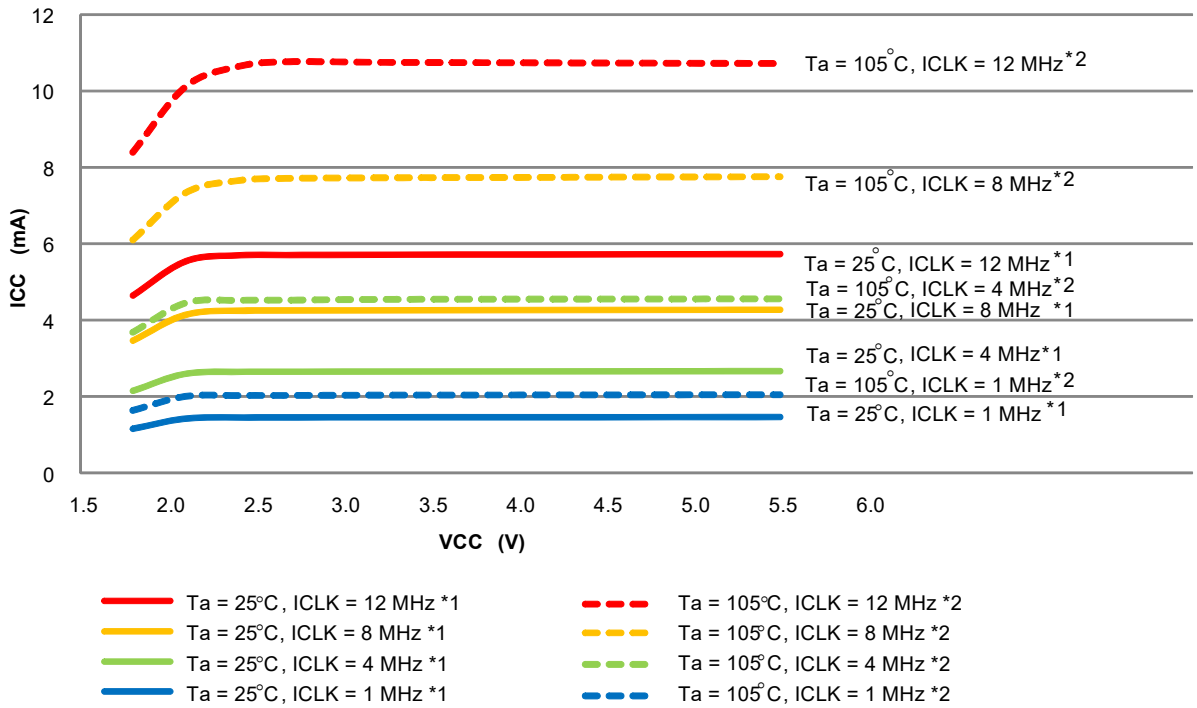
Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The clock source is HOCO.
Note 3. The clock source is MOCO.
Note 4. The clock source is the sub-clock oscillator.
Note 5. This does not include BGO operation.
Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.
Note 7. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64.
Note 8. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are the same frequency as that of ICLK.
Note 9. FCLK and PCLKB are set to divided by 2 and PCLKA, PCLKC, and PCLKD are the same frequency as that of ICLK.
Note 10. VCC = 3.3 V.




Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.

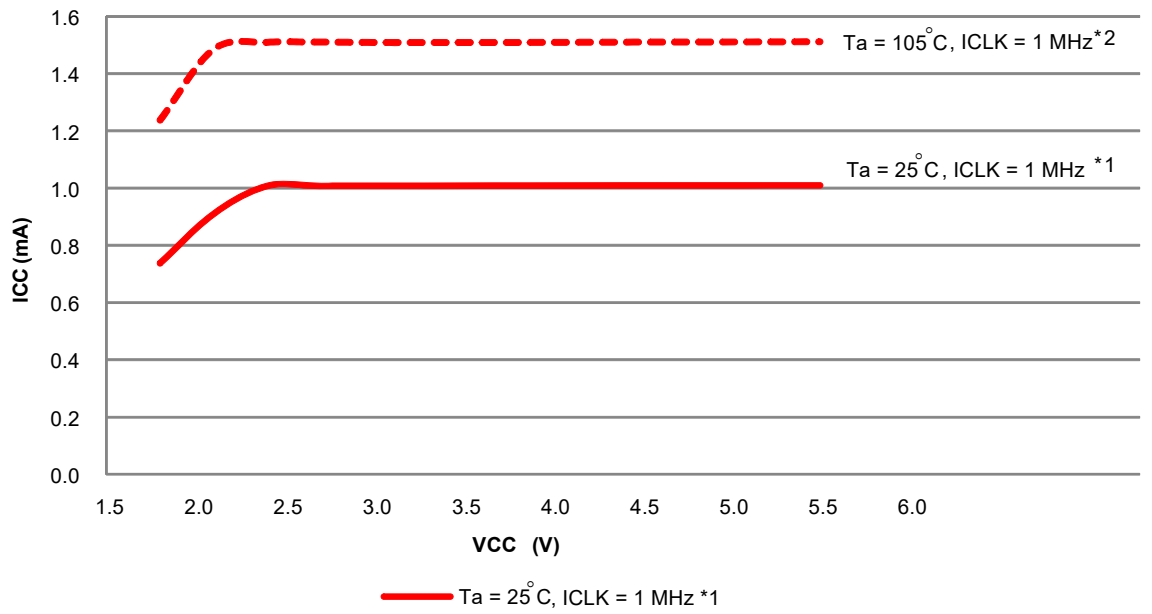
**Figure 2.17 Voltage dependency in high-speed operating mode (reference data)**




Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.

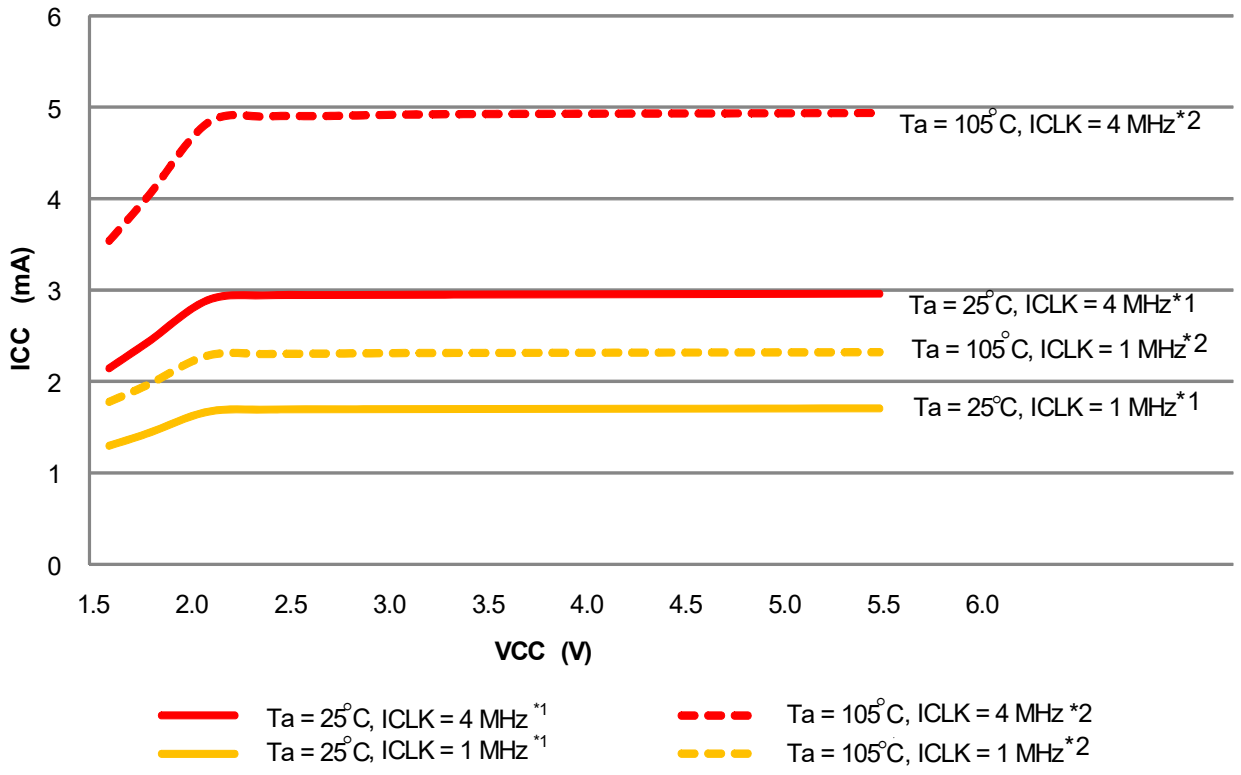
**Figure 2.18 Voltage dependency in middle-speed operating mode (reference data)**




Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.

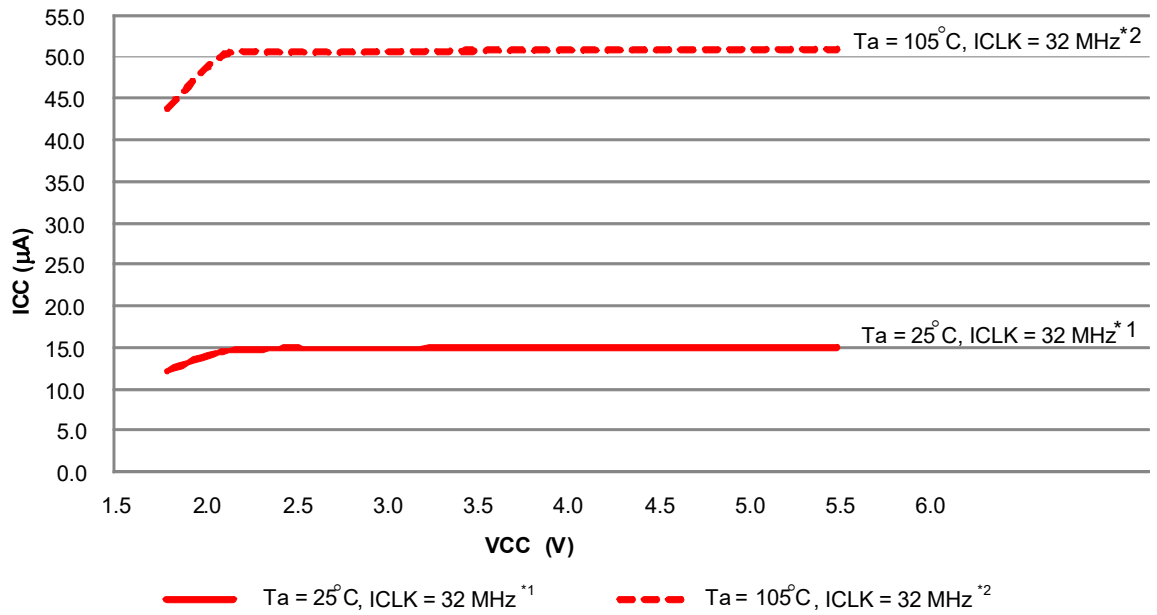
**Figure 2.19 Voltage dependency in Low-speed mode (reference data)**




Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.

**Figure 2.20 Voltage dependency in low-voltage mode (reference data)**




Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.

**Figure 2.21 Voltage dependency in Subosc-speed mode (reference data)**

**Table 2.12 Operating and standby current (2)**

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

| Parameter | | | Symbol | Typ*4 | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Supply current*1 | Software Standby mode*2 | $T_a$ = 25°C | $I_{CC}$ | 0.8 | 4.5 | μA | - |
| | | $T_a$ = 55°C | | 1.3 | 7.1 | | |
| | | $T_a$ = 85°C | | 3.5 | 20.2 | | |
| | | $T_a$ = 105°C | | 8.7 | 53.7 | | |
| | Increment for RTC operation with low-speed on-chip oscillator*3 | | | 0.5 | - | | - |
| | Increment for RTC operation with sub-clock oscillator*3 | | | 0.4 | - | | SOMCR.SODRV[1:0] are 11b (Low power mode 3) |
| | | | | 1.2 | - | | SOMCR.SODRV[1:0] are 00b (Normal mode) |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. The IWDT and LVD are not operating.

Note 3. Includes the current of sub-oscillation circuit or low-speed on-chip oscillator.

Note 4. VCC = 3.3 V.

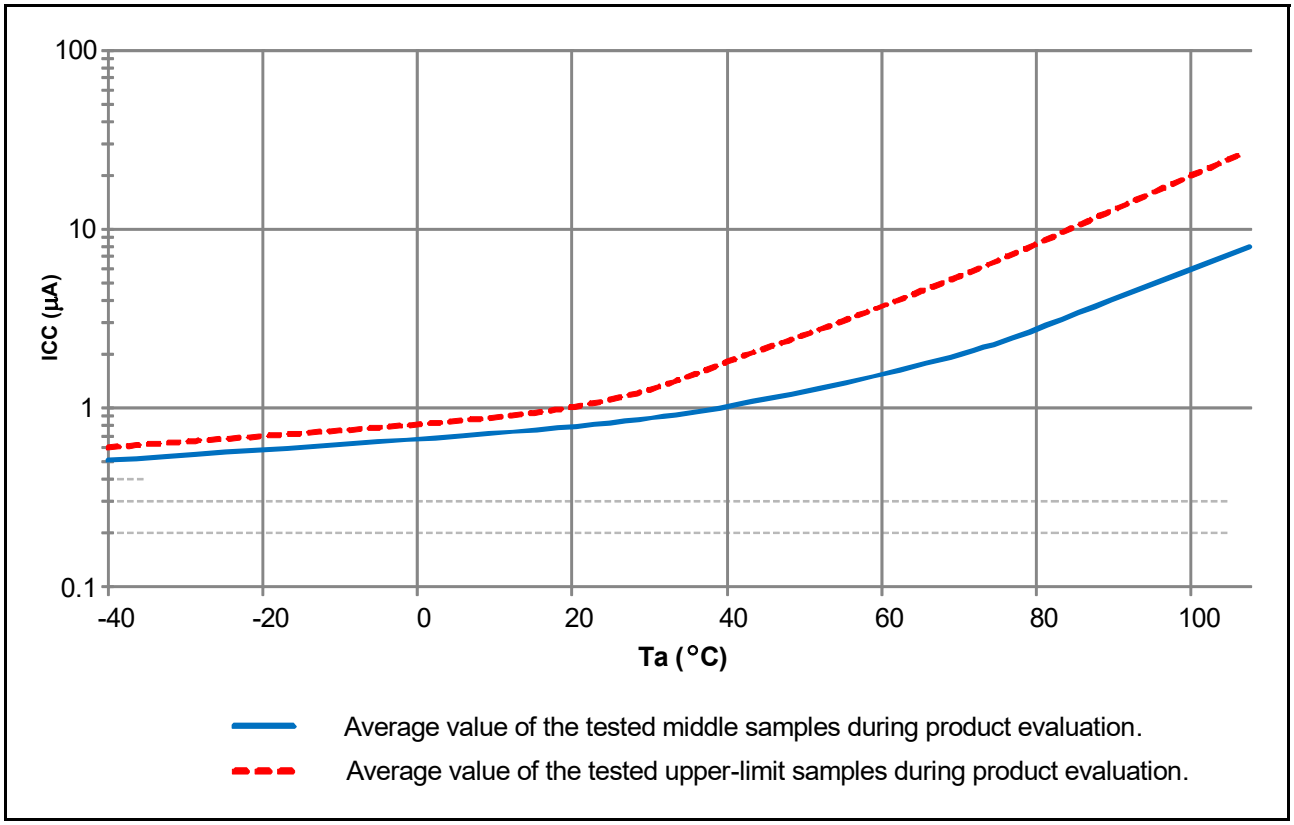



**Figure 2.22 Temperature dependency in Software Standby mode all SRAM (reference data)**

**Table 2.13 Operating and standby current (3)**

Conditions: VCC = AVCC0 = 0V, VBATT = 1.6 to 3.6 V, VSS = AVSS0 = 0V

| Parameter | | | Symbol | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Supply current*1 | RTC operation when VCC is off | $T_a$ = 25°C | $I_{CC}$ | 0.8 | - | µA | VBATT = 2.0 V<br>SOMCR.SORDRV[1:0] = 11b<br>(Low power mode 3) |
| | | $T_a$ = 55°C | | 0.9 | - | | |
| | | $T_a$ = 85°C | | 1.0 | - | | |
| | | $T_a$ = 105°C | | 1.1 | - | | |
| | | $T_a$ = 25°C | | 0.9 | - | | VBATT = 3.3 V<br>SOMCR.SORDRV[1:0] = 11b<br>(Low power mode 3) |
| | | $T_a$ = 55°C | | 1.0 | - | | |
| | | $T_a$ = 85°C | | 1.1 | - | | |
| | | $T_a$ = 105°C | | 1.2 | - | | |
| | | $T_a$ = 25°C | | 1.5 | - | | VBATT = 2.0 V<br>SOMCR.SORDRV[1:0] = 00b<br>(Normal mode) |
| | | $T_a$ = 55°C | | 1.7 | - | | |
| | | $T_a$ = 85°C | | 2.0 | - | | |
| | | $T_a$ = 105°C | | 2.2 | - | | |
| | | $T_a$ = 25°C | | 1.6 | - | | VBATT = 3.3 V<br>SOMCR.SORDRV[1:0] = 00b<br>(Normal mode) |
| | | $T_a$ = 55°C | | 1.8 | - | | |
| | | $T_a$ = 85°C | | 2.1 | - | | |
| | | $T_a$ = 105°C | | 2.3 | - | | |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

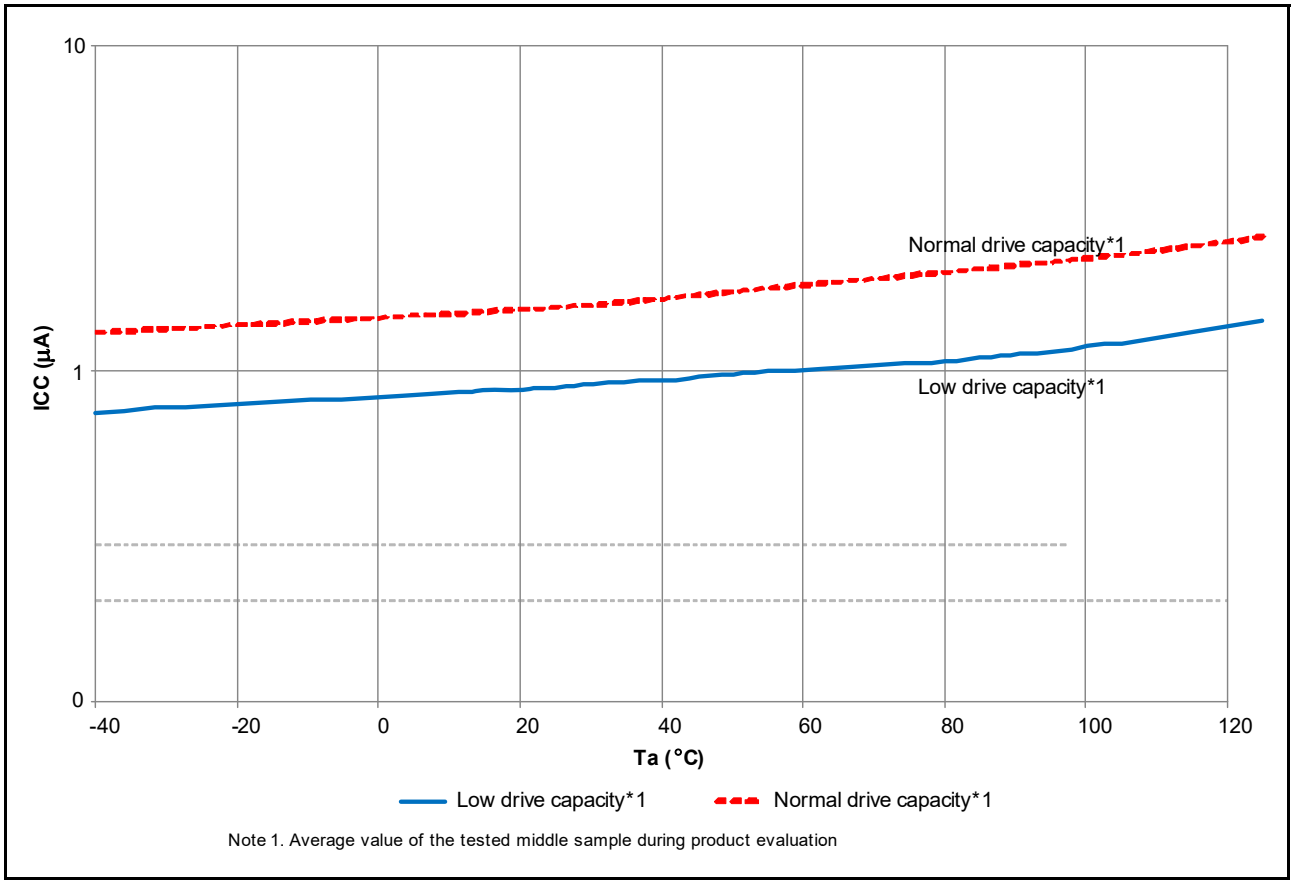



**Figure 2.23 Temperature dependency of RTC operation with VCC off (reference data)**

**Table 2.14 Operating and standby current (4)**

Conditions: VCC = AVCC0 = 1.6 to 5.5 V, VREFH0 = 2.7 V to AVCC0

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| Analog power supply current | During A/D conversion (at high-speed conversion) | | $I_{AVCC}$ | - | - | 3.0 | mA | - |
| | During A/D conversion (at low-power conversion) | | | - | - | 1.0 | mA | - |
| | During D/A conversion (per channel)*1 | | | - | 0.4 | 0.8 | mA | - |
| | Waiting for A/D and D/A conversion (all units)*6 | | | - | - | 1.0 | μA | - |
| Reference power supply current | During A/D conversion | | $I_{REFH0}$ | - | - | 150 | μA | - |
| | Waiting for A/D conversion (all units) | | | - | - | 60 | nA | - |
| | During D/A conversion | | $I_{REFH}$ | - | 50 | 100 | μA | - |
| | Waiting for D/A conversion (all units) | | | - | - | 100 | μA | - |
| Temperature sensor | | | $I_{TNS}$ | - | 75 | - | μA | - |
| Low-Power Analog Comparator operating current | Window mode | | $I_{CMPLP}$ | - | 15 | - | μA | - |
| | Comparator High-speed mode | | | - | 10 | - | μA | - |
| | Comparator Low-speed mode | | | - | 2 | - | μA | - |
| | Comparator Low-speed mode using DAC8 | | | - | 820 | - | μA | - |
| Operational Amplifier operating current | Low power mode | 1 unit operating | $I_{AMP}$ | - | 2.5 | 4.0 | μA | - |
| | | 2 units operating | | - | 4.5 | 8.0 | μA | - |
| | | 3 units operating | | - | 6.5 | 11.0 | μA | - |
| | | 4 units operating | | - | 8.5 | 14.0 | μA | - |
| | High-speed mode | 1 unit operating | | - | 140 | 220 | μA | - |
| | | 2 units operating | | - | 280 | 410 | μA | - |
| | | 3 units operating | | - | 420 | 600 | μA | - |
| | | 4 units operating | | - | 560 | 780 | μA | - |
| LCD operating current | External resistance division method<br>$f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 4-time slice | | $I_{LCD1}$*5 | - | 0.34 | - | μA | - |
| | Internal voltage boosting method (VLCD.VLCD = 04)<br>$f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 4-time slice | | $I_{LCD2}$*5 | - | 0.92 | - | μA | - |
| | Capacitor split method<br>$f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 4-time slice | | $I_{LCD3}$*5 | - | 0.19 | - | μA | - |
| USB operating current | During USB communication operation under the following settings and conditions:<br>• Host controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1<br>• Connect peripheral devices via a 1-meter USB cable from the USB port. | | $I_{USBH}$*2 | - | 4.3 (VCC)<br>0.9 (VCC_USB)*4 | - | mA | - |
| | During USB communication operation under the following settings and conditions:<br>• Device controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1<br>• Connect the host device via a 1-meter USB cable from the USB port. | | $I_{USBF}$*2 | - | 3.6 (VCC)<br>1.1 (VCC_USB)*4 | - | mA | - |
| | During suspended state under the following setting and conditions:<br>• Device controller operation is set to full-speed mode (pull up the USB_DP pin)<br>• Software standby mode<br>• Connect the host device via a 1-meter USB cable from the USB port. | | $I_{SUSP}$*3 | - | 0.35 (VCC)<br>170 (VCC_USB)*4 | - | μA | - |

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.
Note 2. Current consumed only by the USBFS.
Note 3. Includes the current supplied from the pull-up resistor of the USB_DP pin to the pull-down resistor of the host device, in addition to the current consumed by the MCU during the suspended state.
Note 4. When VCC = VCC_USB = 3.3 V.
Note 5. Current flowing only to the LCD controller. Not including the current that flows through the LCD panel.
Note 6. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC140 module stop bit) is in the module-stop state.

### 2.2.10 VCC Rise and Fall Gradient and Ripple Frequency

**Table 2.15 Rise and fall gradient characteristics**

Conditions: VCC = AVCC0 = 0 to 5.5 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Power-on VCC rising gradient | Voltage monitor 0 reset disabled at startup (normal startup) | SrVCC | 0.02 | - | 2 | ms/V | - |
| | Voltage monitor 0 reset enabled at startup*1 | | 0.02 | - | - | | |
| | SCI/USB boot mode*2 | | 0.02 | - | 2 | | |

Note 1. When OFS1.LVDAS = 0.

Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

**Table 2.16 Rising and falling gradient and ripple frequency characteristics**

Conditions: VCC = AVCC0 = VCC_USB = 1.6 to 5.5 V

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (1.6 V).

When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Allowable ripple frequency | $f_{r\ (VCC)}$ | - | - | 10 | kHz | Figure 2.24<br>$V_{r\ (VCC)} \leq VCC \times 0.2$ |
| | | - | - | 1 | MHz | Figure 2.24<br>$V_{r\ (VCC)} \leq VCC \times 0.08$ |
| | | - | - | 10 | MHz | Figure 2.24<br>$V_{r\ (VCC)} \leq VCC \times 0.06$ |
| Allowable voltage change rising and falling gradient | dt/dVCC | 1.0 | - | - | ms/V | When VCC change exceeds VCC ±10% |

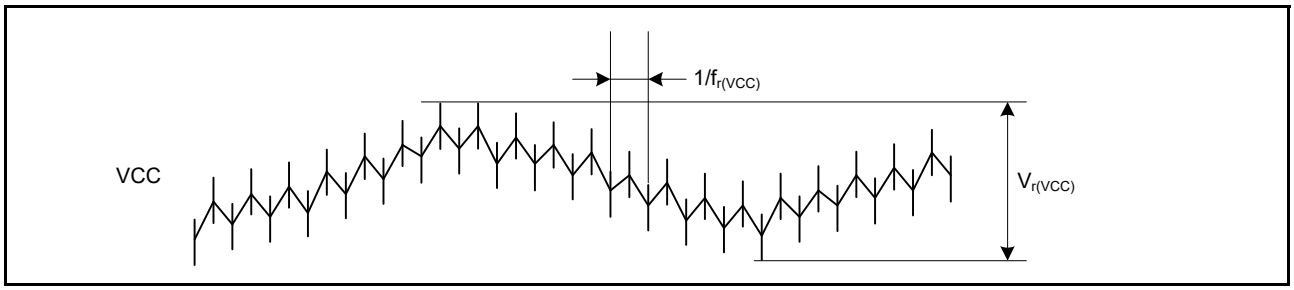



**Figure 2.24 Ripple waveform**

## 2.3 AC Characteristics

### 2.3.1 Frequency

**Table 2.17 Operation frequency value in high-speed operating mode**

Conditions: VCC = AVCC0 = 2.4 to 5.5 V

| Parameter | | | Symbol | Min | Typ | Max*5 | Unit |
|---|---|---|---|---|---|---|---|
| Operation frequency | System clock (ICLK)*4 | 2.7 to 5.5 V | f | 0.032768 | - | 48 | MHz |
| | | 2.4 to 2.7 V | | 0.032768 | - | 16 | |
| | Flash interface clock (FCLK)*1, *2, *4 | 2.7 to 5.5 V | | 0.032768 | - | 32 | |
| | | 2.4 to 2.7 V | | 0.032768 | - | 16 | |
| | Peripheral module clock (PCLKA)*4 | 2.7 to 5.5 V | | - | - | 48 | |
| | | 2.4 to 2.7 V | | - | - | 16 | |
| | Peripheral module clock (PCLKB)*4 | 2.7 to 5.5 V | | - | - | 32 | |
| | | 2.4 to 2.7 V | | - | - | 16 | |
| | Peripheral module clock (PCLKC)*3, *4 | 2.7 to 5.5 V | | - | - | 64 | |
| | | 2.4 to 2.7 V | | - | - | 16 | |
| | Peripheral module clock (PCLKD)*4 | 2.7 to 5.5 V | | - | - | 64 | |
| | | 2.4 to 2.7 V | | - | - | 16 | |

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.

Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK.

Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 2.22, Clock timing.

**Table 2.18 Operation frequency value in middle-speed operating mode**

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

| Parameter | | | Symbol | Min | Typ | Max*5 | Unit |
|---|---|---|---|---|---|---|---|
| Operation frequency | System clock (ICLK)*4 | 2.7 to 5.5 V | f | 0.032768 | - | 12 | MHz |
| | | 2.4 to 2.7 V | | 0.032768 | - | 12 | |
| | | 1.8 to 2.4 V | | 0.032768 | - | 8 | |
| | Flash interface clock (FCLK)*1, *2, *4 | 2.7 to 5.5 V | | 0.032768 | - | 12 | |
| | | 2.4 to 2.7 V | | 0.032768 | - | 12 | |
| | | 1.8 to 2.4 V | | 0.032768 | - | 8 | |
| | Peripheral module clock (PCLKA)*4 | 2.7 to 5.5 V | | - | - | 12 | |
| | | 2.4 to 2.7 V | | - | - | 12 | |
| | | 1.8 to 2.4 V | | - | - | 8 | |
| | Peripheral module clock (PCLKB)*4 | 2.7 to 5.5 V | | - | - | 12 | |
| | | 2.4 to 2.7 V | | - | - | 12 | |
| | | 1.8 to 2.4 V | | - | - | 8 | |
| | Peripheral module clock (PCLKC)*3, *4 | 2.7 to 5.5 V | | - | - | 12 | |
| | | 2.4 to 2.7 V | | - | - | 12 | |
| | | 1.8 to 2.4 V | | - | - | 8 | |
| | Peripheral module clock (PCLKD)*4 | 2.7 to 5.5 V | | - | - | 12 | |
| | | 2.4 to 2.7 V | | - | - | 12 | |
| | | 1.8 to 2.4 V | | - | - | 8 | |

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 2.22, Clock timing.

**Table 2.19 Operation frequency value in low-speed operating mode**

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

| Parameter | | | Symbol | Min | Typ | Max*4 | Unit |
|---|---|---|---|---|---|---|---|
| Operation frequency | System clock (ICLK)*3 | 1.8 to 5.5 V | f | 0.032768 | - | 1 | MHz |
| | Flash interface clock (FCLK)*1, *3 | 1.8 to 5.5 V | | 0.032768 | - | 1 | |
| | Peripheral module clock (PCLKA)*3 | 1.8 to 5.5 V | | - | - | 1 | |
| | Peripheral module clock (PCLKB)*3 | 1.8 to 5.5 V | | - | - | 1 | |
| | Peripheral module clock (PCLKC)*2, *3 | 1.8 to 5.5 V | | - | - | 1 | |
| | Peripheral module clock (PCLKD)*3 | 1.8 to 5.5 V | | - | - | 1 | |

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory.
Note 2. The lower-limit frequency of PCLKC is 1 MHz when the A/D converter is in use.
Note 3. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 2.22, Clock timing.

**Table 2.20 Operation frequency value in low-voltage operating mode**

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

| Parameter | | | Symbol | Min | Typ | Max*5 | Unit |
|---|---|---|---|---|---|---|---|
| Operation frequency | System clock (ICLK)*4 | 1.6 to 5.5 V | f | 0.032768 | - | 4 | MHz |
| | Flash interface clock (FCLK)*1, *2, *4 | 1.6 to 5.5 V | | 0.032768 | - | 4 | |
| | Peripheral module clock (PCLKA)*4 | 1.6 to 5.5 V | | - | - | 4 | |
| | Peripheral module clock (PCLKB)*4 | 1.6 to 5.5 V | | - | - | 4 | |
| | Peripheral module clock (PCLKC)*3, *4 | 1.6 to 5.5 V | | - | - | 4 | |
| | Peripheral module clock (PCLKD)*4 | 1.6 to 5.5 V | | - | - | 4 | |

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-Bit A/D converter is in use.
Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 2.22, Clock timing.

**Table 2.21 Operation frequency value in Subosc-speed operating mode**

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

| Parameter | | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Operation frequency | System clock (ICLK)*3 | 1.8 to 5.5 V | f | 27.8528 | 32.768 | 37.6832 | kHz |
| | Flash interface clock (FCLK)*1, *3 | 1.8 to 5.5 V | | 27.8528 | 32.768 | 37.6832 | |
| | Peripheral module clock (PCLKA)*3 | 1.8 to 5.5 V | | - | - | 37.6832 | |
| | Peripheral module clock (PCLKB)*3 | 1.8 to 5.5 V | | - | - | 37.6832 | |
| | Peripheral module clock (PCLKC)*2, *3 | 1.8 to 5.5 V | | - | - | 37.6832 | |
| | Peripheral module clock (PCLKD)*3 | 1.8 to 5.5 V | | - | - | 37.6832 | |

Note 1. Programming and erasing the flash memory is not possible.
Note 2. The 14-bit A/D converter cannot be used.
Note 3. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK.

## 2.3.2 Clock Timing

**Table 2.22 Clock timing (1 of 2)**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| EXTAL external clock input cycle time | $t_{Xcyc}$ | 50 | - | - | ns | Figure 2.25 |
| EXTAL external clock input high pulse width | $t_{XH}$ | 20 | - | - | ns | |
| EXTAL external clock input low pulse width | $t_{XL}$ | 20 | - | - | ns | |
| EXTAL external clock rising time | $t_{Xr}$ | - | - | 5 | ns | |
| EXTAL external clock falling time | $t_{Xf}$ | - | - | 5 | ns | |
| EXTAL external clock input wait time*1 | $t_{EXWT}$ | 0.3 | - | - | μs | - |
| EXTAL external clock input frequency | $f_{EXTAL}$ | - | - | 20 | MHz | 2.4 ≤ VCC ≤ 5.5 |
| | | - | - | 8 | | 1.8 ≤ VCC < 2.4 |
| | | - | - | 1 | | 1.6 ≤ VCC < 1.8 |
| Main clock oscillator oscillation frequency | $f_{MAIN}$ | 1 | - | 20 | MHz | 2.4 ≤ VCC ≤ 5.5 |
| | | 1 | - | 8 | | 1.8 ≤ VCC < 2.4 |
| | | 1 | - | 4 | | 1.6 ≤ VCC < 1.8 |
| Main clock oscillation stabilization wait time (crystal)*9 | $t_{MAINOSCWT}$ | - | - | -*9 | ms | - |
| LOCO clock oscillation frequency | $f_{LOCO}$ | 27.8528 | 32.768 | 37.6832 | kHz | - |
| LOCO clock oscillation stabilization time | $t_{LOCO}$ | - | - | 100 | μs | Figure 2.26 |
| IWDT-dedicated clock oscillation frequency | $f_{ILOCO}$ | 12.75 | 15 | 17.25 | kHz | - |
| MOCO clock oscillation frequency | $f_{MOCO}$ | 6.8 | 8 | 9.2 | MHz | - |
| MOCO clock oscillation stabilization time | $t_{MOCO}$ | - | - | 1 | μs | - |

**Table 2.22 Clock timing (2 of 2)**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| HOCO clock oscillation frequency | | $f_{HOCO24}$ | 23.64 | 24 | 24.36 | MHz | $T_a$ = -40 to -20°C<br>1.8 ≤ VCC ≤ 5.5 |
| | | | 22.68 | 24 | 25.32 | | $T_a$ = -40 to 85°C<br>1.6 ≤ VCC < 1.8 |
| | | | 23.76 | 24 | 24.24 | | $T_a$ = -20 to 85°C<br>1.8 ≤ VCC ≤ 5.5 |
| | | | 23.52 | 24 | 24.48 | | $T_a$ = 85 to 105°C<br>2.4 ≤ VCC ≤ 5.5 |
| | | $f_{HOCO32}$ | 31.52 | 32 | 32.48 | | $T_a$ = -40 to -20°C<br>1.8 ≤ VCC ≤ 5.5 |
| | | | 30.24 | 32 | 33.76 | | $T_a$ = -40 to 85°C<br>1.6 ≤ VCC < 1.8 |
| | | | 31.68 | 32 | 32.32 | | $T_a$ = -20 to 85°C<br>1.8 ≤ VCC ≤ 5.5 |
| | | | 31.36 | 32 | 32.64 | | $T_a$ = 85 to 105°C<br>2.4 ≤ VCC ≤ 5.5 |
| | | $f_{HOCO48}$*4 | 47.28 | 48 | 48.72 | | $T_a$ = -40 to -20°C<br>1.8 ≤ VCC ≤ 5.5 |
| | | | 47.52 | 48 | 48.48 | | $T_a$ = -20 to 85°C<br>1.8 ≤ VCC ≤ 5.5 |
| | | | 47.04 | 48 | 48.96 | | $T_a$ = 85 to 105°C<br>2.4 ≤ VCC ≤ 5.5 |
| | | $f_{HOCO64}$*5 | 63.04 | 64 | 64.96 | | $T_a$ = -40 to -20°C<br>2.4 ≤ VCC ≤ 5.5 |
| | | | 63.36 | 64 | 64.64 | | $T_a$ = -20 to 85°C<br>2.4 ≤ VCC ≤ 5.5 |
| | | | 62.72 | 64 | 65.28 | | $T_a$ = 85 to 105°C<br>2.4 ≤ VCC ≤ 5.5 |
| HOCO clock oscillation stabilization time*6, *7 | Except Low-Voltage mode | $t_{HOCO24}$<br>$t_{HOCO32}$ | - | - | 37.1 | μs | Figure 2.27 |
| | | $t_{HOCO48}$ | - | - | 43.3 | | |
| | | $t_{HOCO64}$ | - | - | 80.6 | | |
| | Low-Voltage mode | $t_{HOCO24}$<br>$t_{HOCO32}$<br>$t_{HOCO48}$<br>$t_{HOCO64}$ | - | - | 100.9 | | |
| PLL input frequency*2 | | $f_{PLLIN}$ | 4 | - | 12.5 | MHz | - |
| PLL circuit oscillation frequency*2 | | $f_{PLL}$ | 24 | - | 64 | MHz | - |
| PLL clock oscillation stabilization time*8 | | $t_{PLL}$ | - | - | 55.5 | μs | Figure 2.29 |
| PLL free-running oscillation frequency | | $f_{PLLFR}$ | - | 8 | - | MHz | - |
| Sub-clock oscillator oscillation frequency | | $f_{SUB}$ | - | 32.768 | - | kHz | - |
| Sub-clock oscillation stabilization time*3 | | $t_{SUBOSC}$ | - | - | -*3 | s | Figure 2.30 |

Note 1. Time until the clock can be used after the Main Clock Oscillator Stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.
Note 2. The VCC range that the PLL can be used is 2.4 to 5.5 V.
Note 3. After changing the setting of the SOSCCR.SOSTP bit so that the sub-clock oscillator operates, only start using the sub-clock after the sub-clock oscillation stabilization wait time elapses, that is greater than or equal to the value recommended by the oscillator manufacturer.
Note 4. The 48-MHz HOCO can be used within a VCC range of 1.8 V to 5.5 V.
Note 5. The 64-MHz HOCO can be used within a VCC range of 2.4 V to 5.5 V.
Note 6. This is a characteristic when HOCOCR.HCSTP bit is set to 0 (oscillation) in MOCO stop state.
When HOCOCR.HCSTP bit is set to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1 μs.
Note 7. Whether stabilization time has elapsed can be confirmed by OSCSF.HOCOSF.
Note 8. This is a characteristic when PLLCR.PLLSTP bit is set to 0 (operation) in MOCO stop state.
When PLLCR.PLLSTP bit is set to 0 (operation) during MOCO oscillation, this specification is shortened by 1 μs.
Note 9. When setting up the main clock, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended stabilization time. After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCSF.MOSCSF flag to confirm that it is 1, then start using the main clock.

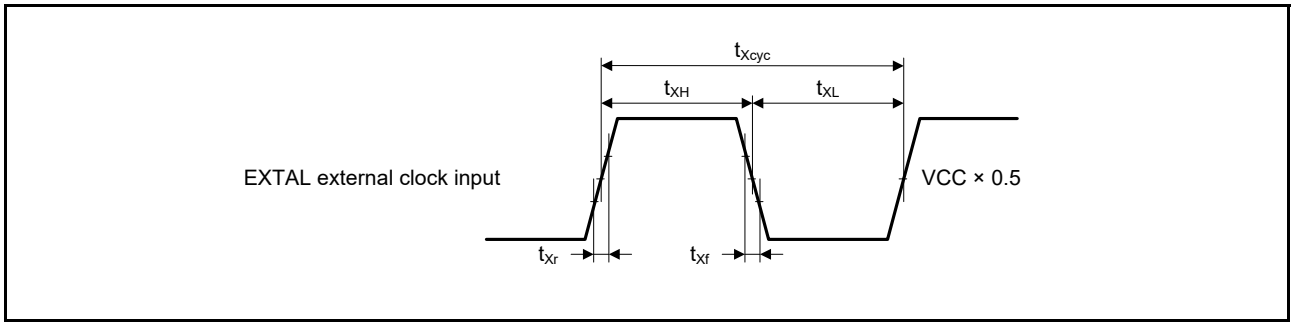



**Figure 2.25 EXTAL external clock input timing**

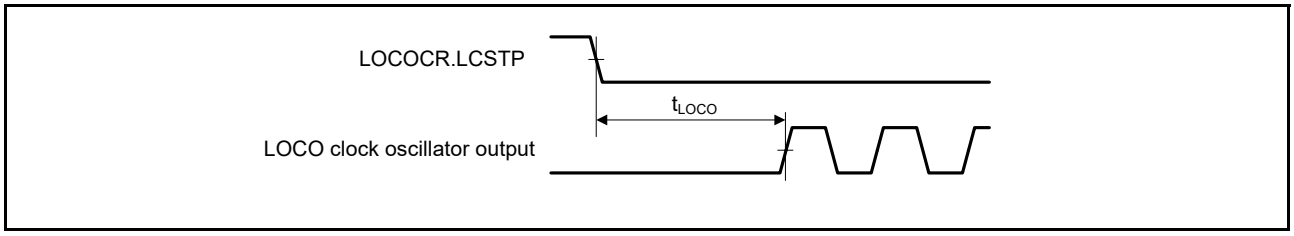
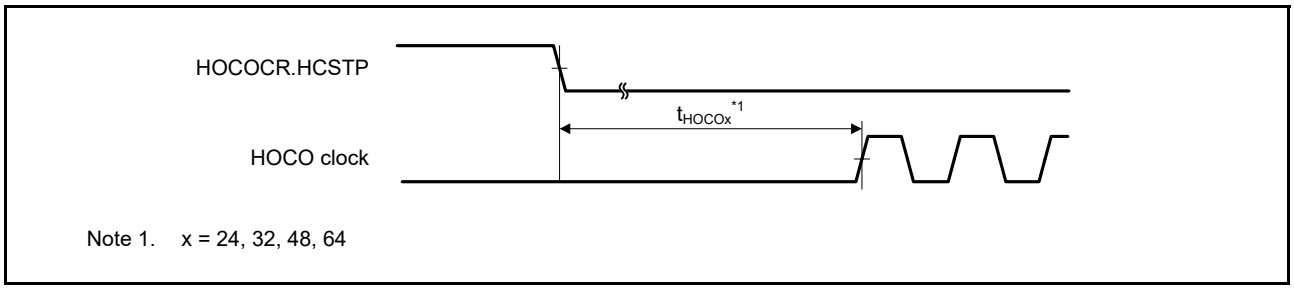



**Figure 2.26 LOCO clock oscillation start timing**




Note 1. x = 24, 32, 48, 64

**Figure 2.27 HOCO clock oscillation start timing (started by setting HOCOCR.HCSTP bit)**

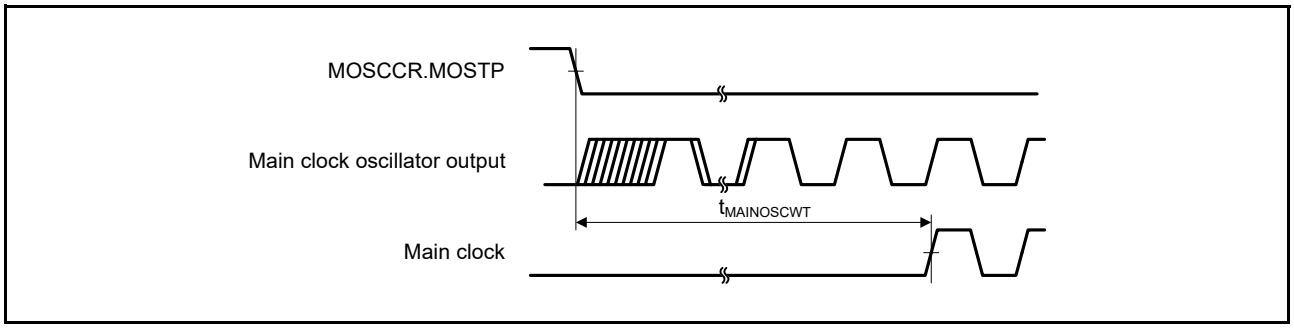



**Figure 2.28 Main clock oscillation start timing**

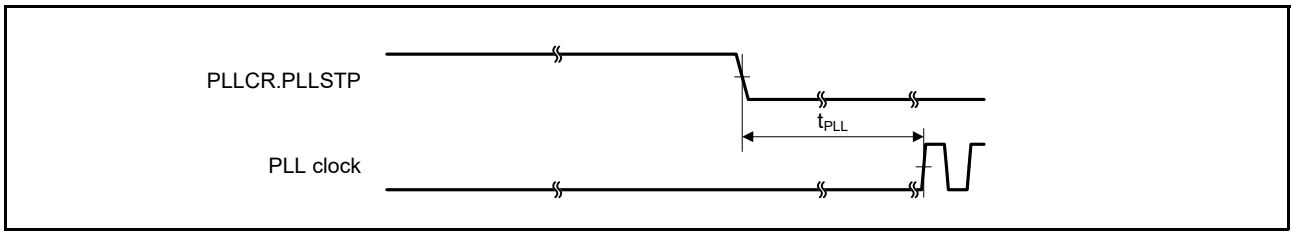



**Figure 2.29 PLL clock oscillation start timing (PLL is operated after main clock oscillation has settled)**

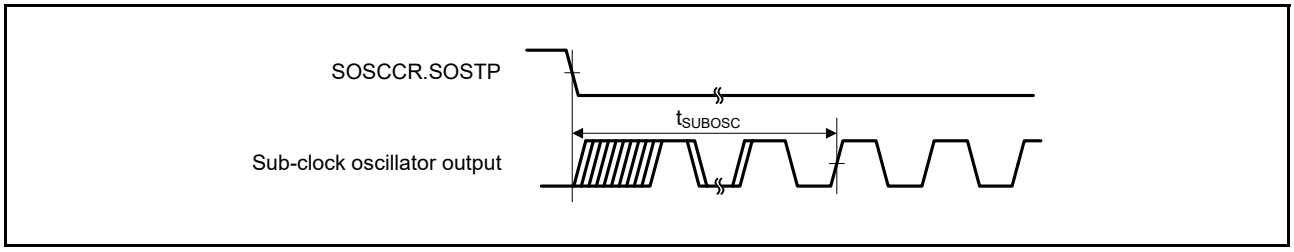



**Figure 2.30 Sub-clock oscillation start timing**

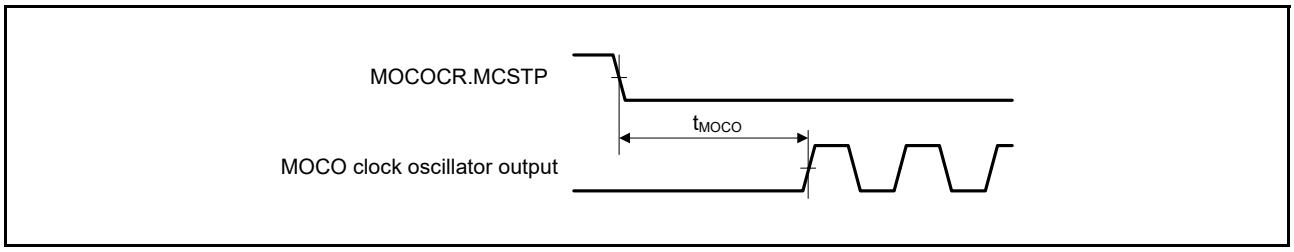



**Figure 2.31 MOCO clock oscillation start timing**

### 2.3.3 Reset Timing

**Table 2.23 Reset timing**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| RES pulse width | At power-on | $t_{RESWP}$ | 3 | - | - | ms | Figure 2.32 |
| | Other than above | $t_{RESW}$ | 30 | - | - | μs | Figure 2.33 |
| Wait time after RES cancellation (at power-on) | LVD0: enable*1 | $t_{RESWT}$ | - | 0.7 | - | ms | Figure 2.32 |
| | LVD0: disable*2 | | - | 0.3 | - | | |
| Wait time after RES cancellation (during powered-on state) | LVD0: enable*1 | $t_{RESWT2}$ | - | 0.5 | - | ms | Figure 2.33 |
| | LVD0: disable*2 | | - | 0.05 | - | | |
| Internal reset cancellation time (Watchdog timer reset, SRAM parity error reset, SRAM ECC error reset, Bus master MPU error reset, Bus slave MPU error reset, Stack pointer error reset, Software reset) | LVD0: enable*1 | $t_{RESWT3}$ | - | 0.6 | - | ms | - |
| | LVD0: disable*2 | | - | 0.15 | - | | |

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.

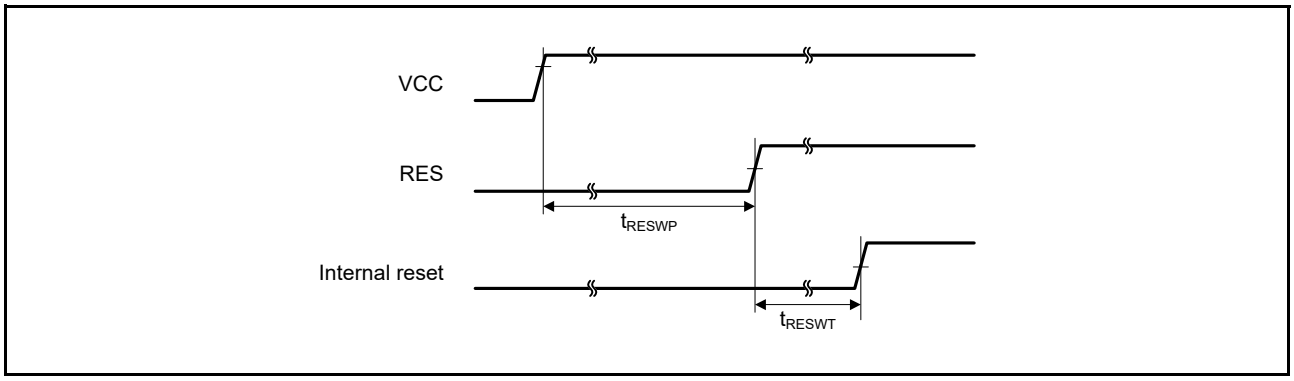



**Figure 2.32 Reset input timing at power-on**

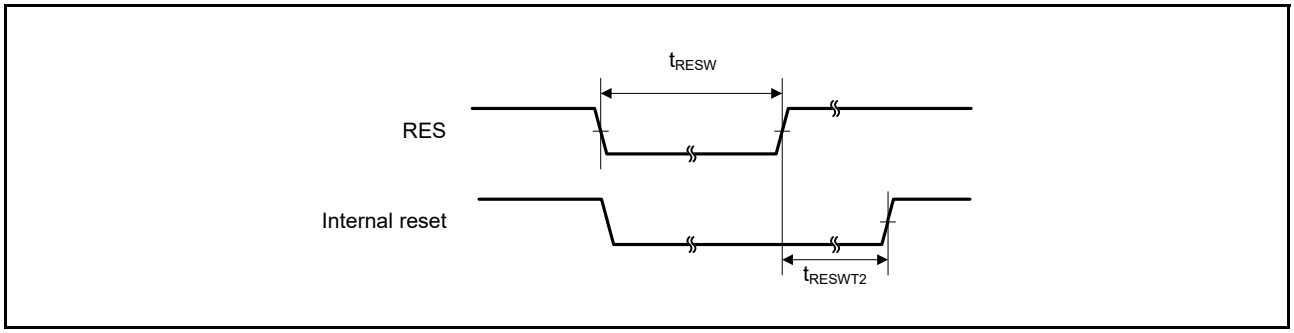



**Figure 2.33 Reset input timing**

### 2.3.4 Wakeup Time

**Table 2.24 Timing of recovery from low power modes (1)**

| Parameter | | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|
| Recovery time from Software Standby mode*1 | High-speed mode | Crystal resonator connected to main clock oscillator | System clock source is main clock oscillator (20 MHz)*2 | $t_{SBYMC}$ | - | 2 | 3 | ms | Figure 2.34 |
| | | | System clock source is PLL (48 MHz) with main clock oscillator*2 | $t_{SBYPC}$ | - | 2 | 3 | ms | |
| | | External clock input to main clock oscillator | System clock source is main clock oscillator (20 MHz)*3 | $t_{SBYEX}$ | - | 14 | 25 | μs | |
| | | | System clock source is PLL (48 MHz) with main clock oscillator*3 | $t_{SBYPE}$ | - | 53 | 76 | μs | |
| | | System clock source is HOCO*4 (HOCO clock is 32 MHz) | | $t_{SBYHO}$ | - | 43 | 52 | μs | |
| | | System clock source is HOCO*4 (HOCO clock is 48 MHz) | | $t_{SBYHO}$ | - | 44 | 52 | μs | |
| | | System clock source is HOCO*5 (HOCO clock is 64 MHz) | | $t_{SBYHO}$ | - | 82 | 110 | μs | |
| | | System clock source is MOCO | | $t_{SBYMO}$ | - | 16 | 25 | μs | |

Note 1. The division ratio of ICK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.
Note 4. The HOCO Clock Wait Control Register (HOCOWTCR) is set to 05h.
Note 5. The HOCO Clock Wait Control Register (HOCOWTCR) is set to 06h.

**Table 2.25 Timing of recovery from low power modes (2)**

| Parameter | | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|
| Recovery time from Software Standby mode*1 | Middle-speed mode | Crystal resonator connected to main clock oscillator | System clock source is main clock oscillator (12 MHz)*2 | $t_{SBYMC}$ | - | 2 | 3 | ms | Figure 2.34 |
| | | | System clock source is PLL (24 MHz) with main clock oscillator*2 | $t_{SBYPC}$ | - | 2 | 3 | ms | |
| | | External clock input to main clock oscillator | System clock source is main clock oscillator (12 MHz)*3 | $t_{SBYEX}$ | - | 2.9 | 10 | μs | |
| | | | System clock source is PLL (24 MHz) with main clock oscillator*3 | $t_{SBYPE}$ | - | 49 | 76 | μs | |
| | | System clock source is HOCO (24 MHz) | | $t_{SBYHO}$ | - | 38 | 50 | μs | |
| | | System clock source is MOCO | | $t_{SBYMO}$ | - | 3.5 | 5.5 | μs | |

Note 1. The division ratio of ICK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

**Table 2.26 Timing of recovery from low power modes (3)**

| Parameter | | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|
| Recovery time from Software Standby mode*1 | Low-speed mode | Crystal resonator connected to main clock oscillator | System clock source is main clock oscillator (1 MHz)*2 | $t_{SBYMC}$ | - | 2 | 3 | ms | Figure 2.34 |
| | | External clock input to main clock oscillator | System clock source is main clock oscillator (1 MHz)*3 | $t_{SBYEX}$ | - | 28 | 50 | μs | |
| | | System clock source is MOCO | | $t_{SBYMO}$ | - | 25 | 35 | μs | |

Note 1. The division ratio of ICK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

**Table 2.27 Timing of recovery from low power modes (4)**

| Parameter | | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|
| Recovery time from Software Standby mode*1 | Low-voltage mode | Crystal resonator connected to main clock oscillator | System clock source is main clock oscillator (4 MHz)*2 | $t_{SBYMC}$ | - | 2 | 3 | ms | Figure 2.34 |
| | | External clock input to main clock oscillator | System clock source is main clock oscillator (4 MHz)*3 | $t_{SBYEX}$ | - | 108 | 130 | μs | |
| | | System clock source is HOCO | | $t_{SBYHO}$ | - | 108 | 130 | μs | |

Note 1. The division ratio of ICK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined by the following expression.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

**Table 2.28 Timing of recovery from low power modes (5)**

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| Recovery time from Software Standby mode*1 | Subosc-speed mode | System clock source is sub-clock oscillator (32.768 kHz) | $t_{SBYSC}$ | - | 0.85 | 1 | ms | Figure 2.34 |
| | | System clock source is LOCO (32.768 kHz) | $t_{SBYLO}$ | - | 0.85 | 1.2 | ms | |

Note 1. The sub-clock oscillator or LOCO itself continues to oscillate in Software Standby mode during Subosc-speed mode.

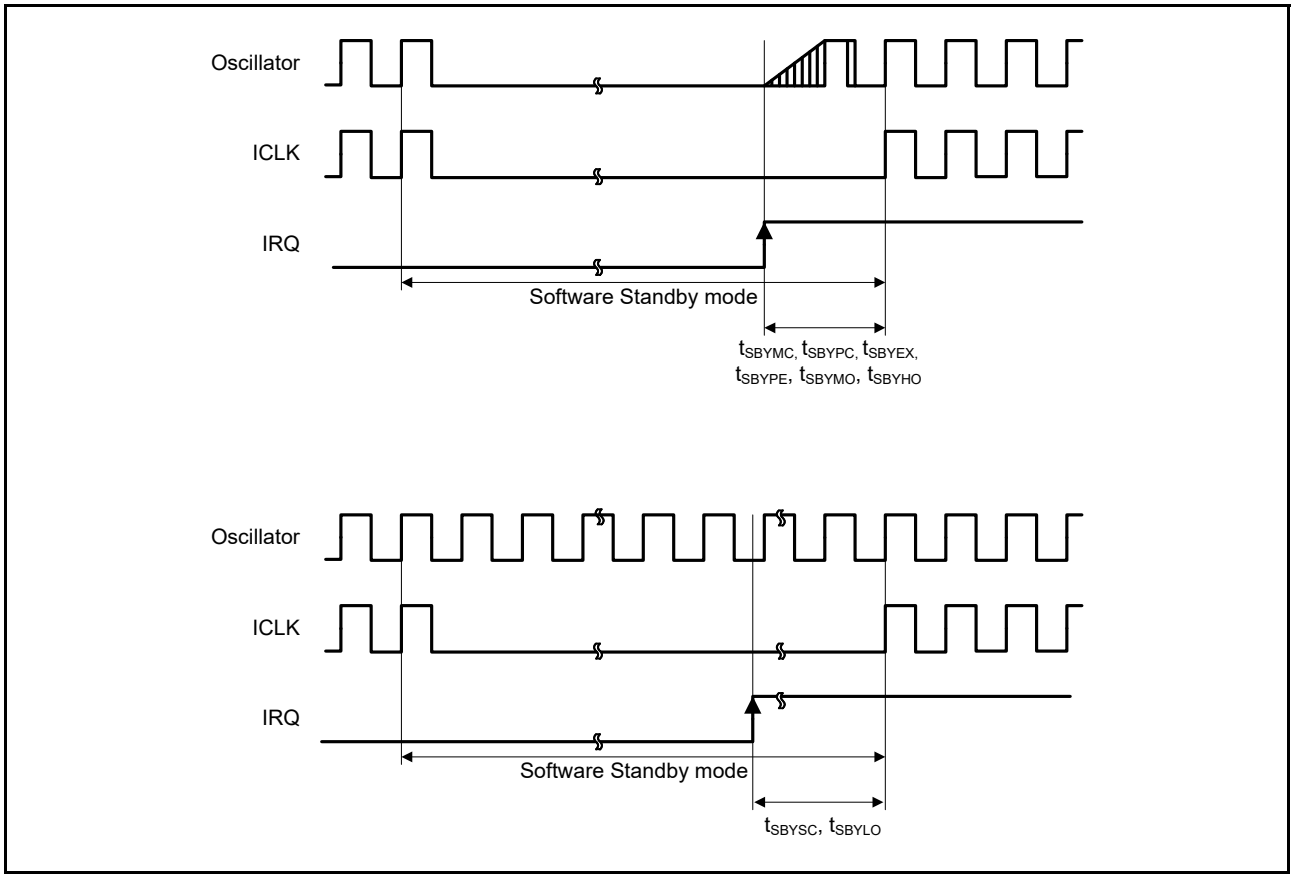
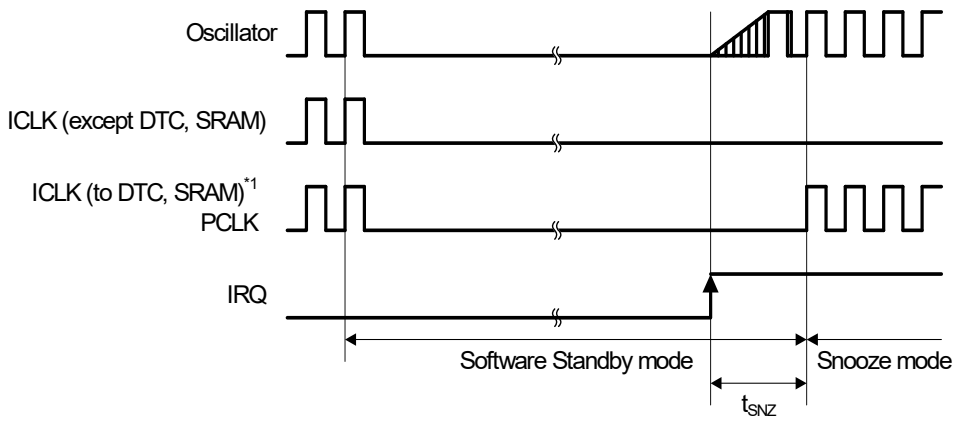



**Figure 2.34 Software Standby mode cancellation timing**

**Table 2.29 Timing of recovery from low power modes (6)**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Recovery time from Software Standby mode to Snooze mode | High-speed mode<br>System clock source is HOCO | $t_{SNZ}$ | - | 36 | 45 | μs | Figure 2.35 |
| | Middle-speed mode<br>System clock source is MOCO | $t_{SNZ}$ | - | 1.3 | 3.6 | μs | |
| | Low-speed mode<br>System clock source is MOCO | $t_{SNZ}$ | - | 10 | 13 | μs | |
| | Low-voltage mode<br>System clock source is HOCO | $t_{SNZ}$ | - | 87 | 110 | μs | |




Note 1. When SNZCR.SNZDTCEN is set to 1, ICLK is supplied to DTC and SRAM.

**Figure 2.35 Software Standby mode to Snooze mode recovery timing**

### 2.3.5 NMI and IRQ Noise Filter

**Table 2.30 NMI and IRQ noise filter**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | |
|---|---|---|---|---|---|---|---|
| NMI pulse width | $t_{NMIW}$ | 200 | - | - | ns | NMI digital filter disabled | $t_{Pcyc} \times 2 \leq 200$ ns |
| | | $t_{Pcyc} \times 2$*1 | - | - | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | - | - | | NMI digital filter enabled | $t_{NMICK} \times 3 \leq 200$ ns |
| | | $t_{NMICK} \times 3.5$*2 | - | - | | | $t_{NMICK} \times 3 > 200$ ns |
| IRQ pulse width | $t_{IRQW}$ | 200 | - | - | ns | IRQ digital filter disabled | $t_{Pcyc} \times 2 \leq 200$ ns |
| | | $t_{Pcyc} \times 2$*1 | - | - | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | - | - | | IRQ digital filter enabled | $t_{IRQCK} \times 3 \leq 200$ ns |
| | | $t_{IRQCK} \times 3.5$*3 | - | - | | | $t_{IRQCK} \times 3 > 200$ ns |

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.
Note 1. $t_{Pcyc}$ indicates the cycle of PCLKB.
Note 2. $t_{NMICK}$ indicates the cycle of the NMI digital filter sampling clock.
Note 3. $t_{IRQCK}$ indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 12, 14, 15).

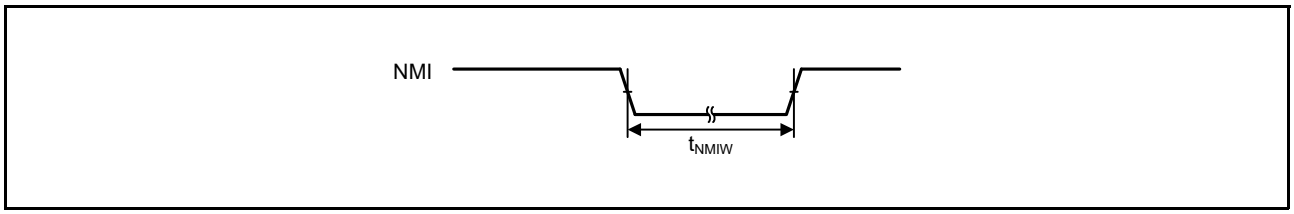



**Figure 2.36 NMI interrupt input timing**

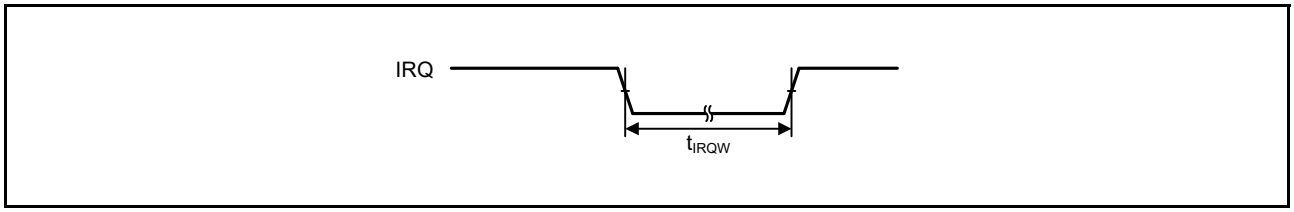



**Figure 2.37 IRQ interrupt input timing**

### 2.3.6 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 Trigger Timing

**Table 2.31 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 trigger timing**

| Parameter | | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| I/O ports | Input data pulse width | | $t_{PRW}$ | 1.5 | - | $t_{Pcyc}$ | Figure 2.38 |
| | Input/output data cycle (P002, P003, P004, P007) | | $t_{POcyc}$ | 10 | - | us | |
| POEG | POEG input trigger pulse width | | $t_{POEW}$ | 3 | - | $t_{Pcyc}$ | Figure 2.39 |
| GPT | Input capture pulse width | Single edge | $t_{GTICW}$ | 1.5 | - | $t_{PDcyc}$ | Figure 2.40 |
| | | Dual edge | | 2.5 | - | | |
| AGT | AGTIO, AGTEE input cycle | 2.7 V ≤ VCC ≤ 5.5 V | $t_{ACYC}$*1 | 250 | - | ns | Figure 2.41 |
| | | 2.4 V ≤ VCC < 2.7 V | | 500 | - | ns | |
| | | 1.8 V ≤ VCC < 2.4 V | | 1000 | - | ns | |
| | | 1.6 V ≤ VCC < 1.8 V | | 2000 | - | ns | |
| | AGTIO, AGTEE input high level width, low-level width | 2.7 V ≤ VCC ≤ 5.5 V | $t_{ACKWH}$, $t_{ACKWL}$ | 100 | - | ns | |
| | | 2.4 V ≤ VCC < 2.7 V | | 200 | - | ns | |
| | | 1.8 V ≤ VCC < 2.4 V | | 400 | - | ns | |
| | | 1.6 V ≤ VCC < 1.8 V | | 800 | - | ns | |
| | AGTIO, AGTO, AGTOA, AGTOB output cycle | 2.7 V ≤ VCC ≤ 5.5 V | $t_{ACYC2}$ | 62.5 | - | ns | Figure 2.41 |
| | | 2.4 V ≤ VCC < 2.7 V | | 125 | - | ns | |
| | | 1.8 V ≤ VCC < 2.4 V | | 250 | - | ns | |
| | | 1.6 V ≤ VCC < 1.8 V | | 500 | - | ns | |
| ADC14 | 14-bit A/D converter trigger input pulse width | | $t_{TRGW}$ | 1.5 | - | $t_{Pcyc}$ | Figure 2.42 |
| KINT | KRn (n = 00 to 07) pulse width | | $t_{KR}$ | 250 | - | ns | Figure 2.43 |

Note 1. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

Note: $t_{Pcyc}$: PCLKB cycle, $t_{PDcyc}$: PCLKD cycle

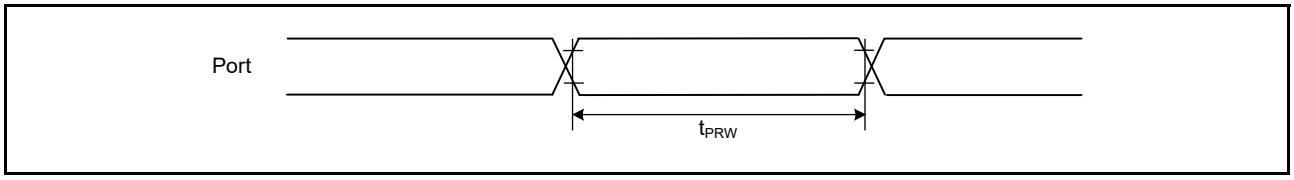



**Figure 2.38 I/O ports input timing**

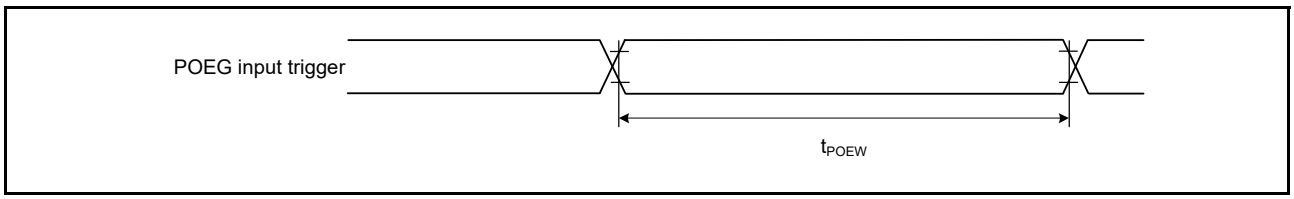



**Figure 2.39 POEG input trigger timing**

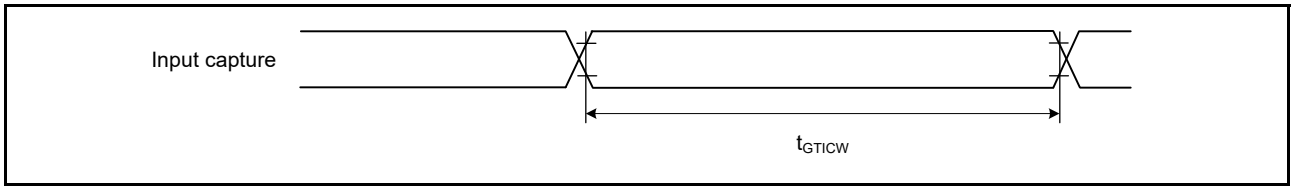



**Figure 2.40 GPT input capture timing**

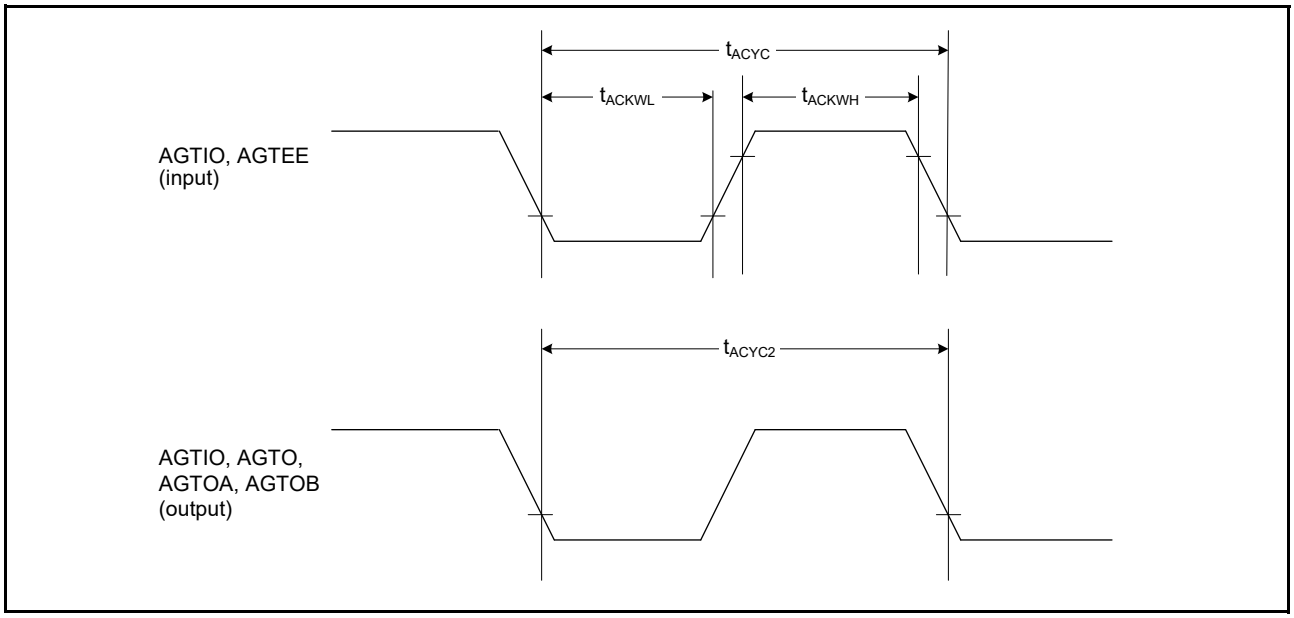



**Figure 2.41 AGT I/O timing**

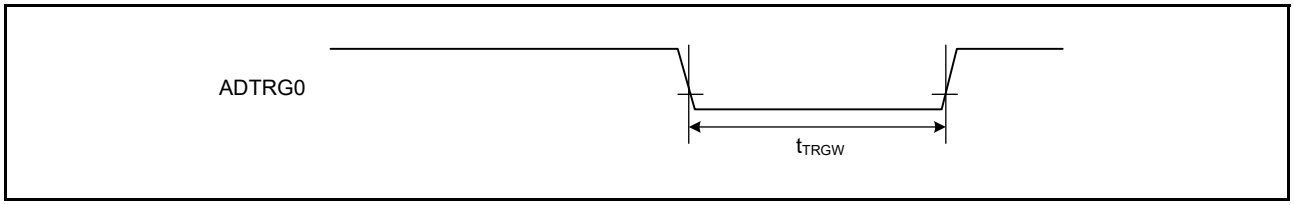



**Figure 2.42 ADC14 trigger input timing**

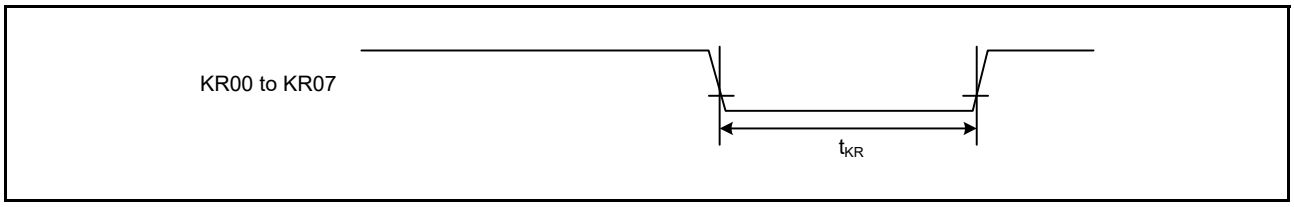



**Figure 2.43 Key interrupt input timing**

## 2.3.7 CAC Timing

**Table 2.32 CAC timing**

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| CAC | CACREF input pulse width | $t_{PBcyc}$*1 ≤ $t_{cac}$*2 | $t_{CACREF}$ | 4.5 × $t_{cac}$ + 3 × $t_{PBcyc}$*1 | - | - | ns | - |
| | | $t_{PBcyc}$*1 > $t_{cac}$*2 | | 5 × $t_{cac}$ + 6.5 × $t_{PBcyc}$*1 | - | - | ns | |

Note 1. $t_{PBcyc}$: PCLKB cycle.
Note 2. $t_{cac}$: CAC count clock source cycle.

## 2.3.8 SCI Timing

**Table 2.33 SCI timing (1)**

| Parameter | | | | Symbol | Min | Max | Unit*1 | Test conditions |
|---|---|---|---|---|---|---|---|---|
| SCI | Input clock cycle | Asynchronous | | $t_{Scyc}$ | 4 | - | $t_{Pcyc}$ | Figure 2.44 |
| | | Clock synchronous | | | 6 | - | | |
| | Input clock pulse width | | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | | $t_{SCKr}$ | - | 20 | ns | |
| | Input clock fall time | | | $t_{SCKf}$ | - | 20 | ns | |
| | Output clock cycle | Asynchronous | | $t_{Scyc}$ | 6 | - | $t_{Pcyc}$ | |
| | | Clock synchronous | | | 4 | - | | |
| | Output clock pulse width | | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | 1.8 V or above | $t_{SCKr}$ | - | 20 | ns | |
| | | | 1.6 V or above | | - | 30 | | |
| | Output clock fall time | | 1.8 V or above | $t_{SCKf}$ | - | 20 | ns | |
| | | | 1.6 V or above | | - | 30 | | |
| | Transmit data delay (master) | Clock synchronous | 1.8 V or above | $t_{TXD}$ | - | 40 | ns | Figure 2.45 |
| | | | 1.6 V or above | | - | 45 | | |
| | Transmit data delay (slave) | Clock synchronous | 2.7 V or above | | - | 55 | ns | |
| | | | 2.4 V or above | | - | 60 | | |
| | | | 1.8 V or above | | - | 100 | | |
| | | | 1.6 V or above | | - | 125 | | |
| | Receive data setup time (master) | Clock synchronous | 2.7 V or above | $t_{RXS}$ | 45 | - | ns | |
| | | | 2.4 V or above | | 55 | - | | |
| | | | 1.8 V or above | | 90 | - | | |
| | | | 1.6 V or above | | 110 | - | | |
| | Receive data setup time (slave) | Clock synchronous | 2.7 V or above | | 40 | - | ns | |
| | | | 1.6 V or above | | 45 | - | | |
| | Receive data hold time (master) | Clock synchronous | | $t_{RXH}$ | 5 | - | ns | |
| | Receive data hold time (slave) | Clock synchronous | | $t_{RXH}$ | 40 | - | ns | |

Note 1. $t_{Pcyc}$: PCLKA cycle.

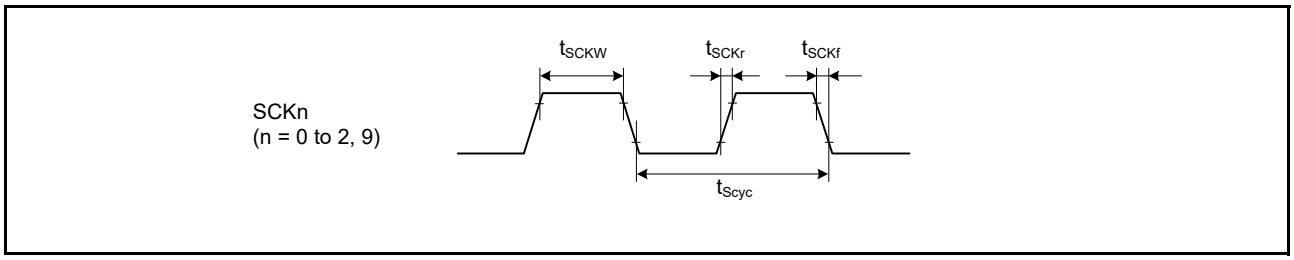



**Figure 2.44 SCK clock input timing**

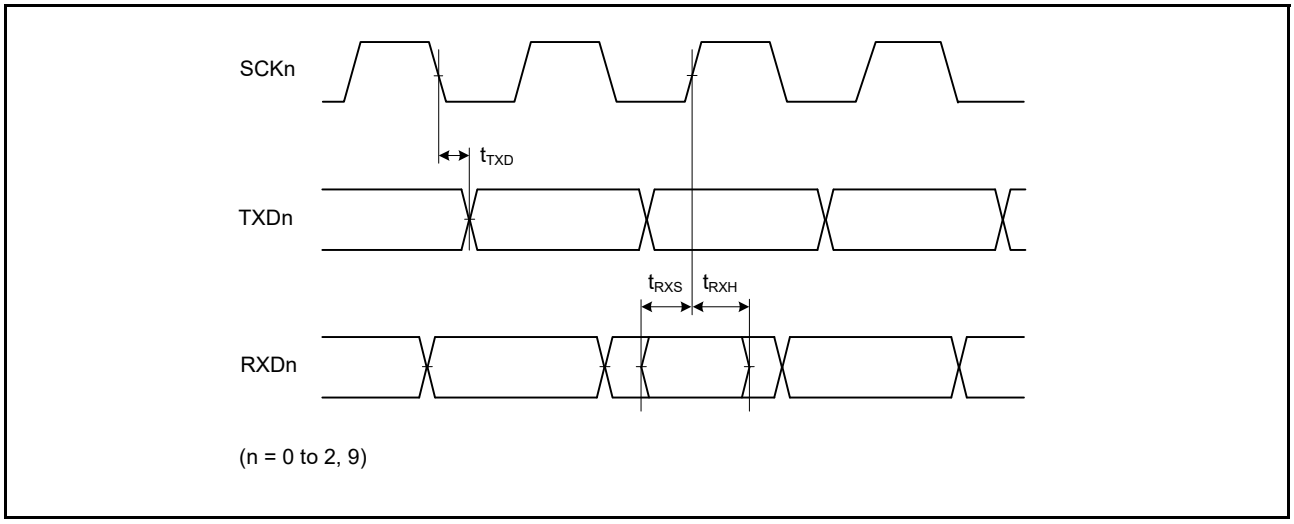



**Figure 2.45 SCI input/output timing in clock synchronous mode**

**Table 2.34 SCI timing (2) (1 of 2)**

| Parameter | | | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| Simple SPI | SCK clock cycle output (master) | | | $t_{SPcyc}$ | 4 | 65,536 | $t_{Pcyc}$ | Figure 2.46 |
| | SCK clock cycle input (slave) | | | | 6 | 65,536 | | |
| | SCK clock high pulse width | | | $t_{SPCKWH}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock low pulse width | | | $t_{SPCKWL}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock rise and fall time | | 1.8 V or above | $t_{SPCKr}$, $t_{SPCKf}$ | - | 20 | ns | |
| | | | 1.6 V or above | | - | 30 | | |
| | Data input setup time | Master | 2.7 V or above | $t_{SU}$ | 45 | - | ns | Figure 2.47 to Figure 2.50 |
| | | | 2.4 V or above | | 55 | - | | |
| | | | 1.8 V or above | | 80 | - | | |
| | | | 1.6 V or above | | 110 | - | | |
| | | Slave | 2.7 V or above | | 40 | - | | |
| | | | 1.6 V or above | | 45 | - | | |
| | Data input hold time | Master | | $t_H$ | 33.3 | - | ns | |
| | | Slave | | | 40 | - | | |
| | SS input setup time | | | $t_{LEAD}$ | 1 | - | $t_{SPcyc}$ | |
| | SS input hold time | | | $t_{LAG}$ | 1 | - | $t_{SPcyc}$ | |
| | Data output delay | Master | 1.8 V or above | $t_{OD}$ | - | 40 | ns | |
| | | | 1.6 V or above | | - | 50 | | |
| | | Slave | 2.4 V or above | | - | 65 | | |
| | | | 1.8 V or above | | - | 100 | | |
| | | | 1.6 V or above | | - | 125 | | |
| | Data output hold time | Master | 2.7 V or above | $t_{OH}$ | -10 | - | ns | |
| | | | 2.4 V or above | | -20 | - | | |
| | | | 1.8 V or above | | -30 | - | | |
| | | | 1.6 V or above | | -40 | - | | |
| | | Slave | | | -10 | - | | |
| | Data rise and fall time | Master | 1.8 V or above | $t_{Dr}$, $t_{Df}$ | - | 20 | ns | |
| | | | 1.6 V or above | | - | 30 | | |
| | | Slave | 1.8 V or above | | - | 20 | | |
| | | | 1.6 V or above | | - | 30 | | |

**Table 2.34 SCI timing (2) (2 of 2)**

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Simple SPI | Slave access time | $t_{SA}$ | - | 10 (PCLKA > 32 MHz), 6 (PCLKA ≤ 32 MHz) | $t_{Pcyc}$ | Figure 2.49 and Figure 2.50 |
| | Slave output release time | $t_{REL}$ | - | 10 (PCLKA > 32 MHz), 6 (PCLKA ≤ 32 MHz) | $t_{Pcyc}$ | |

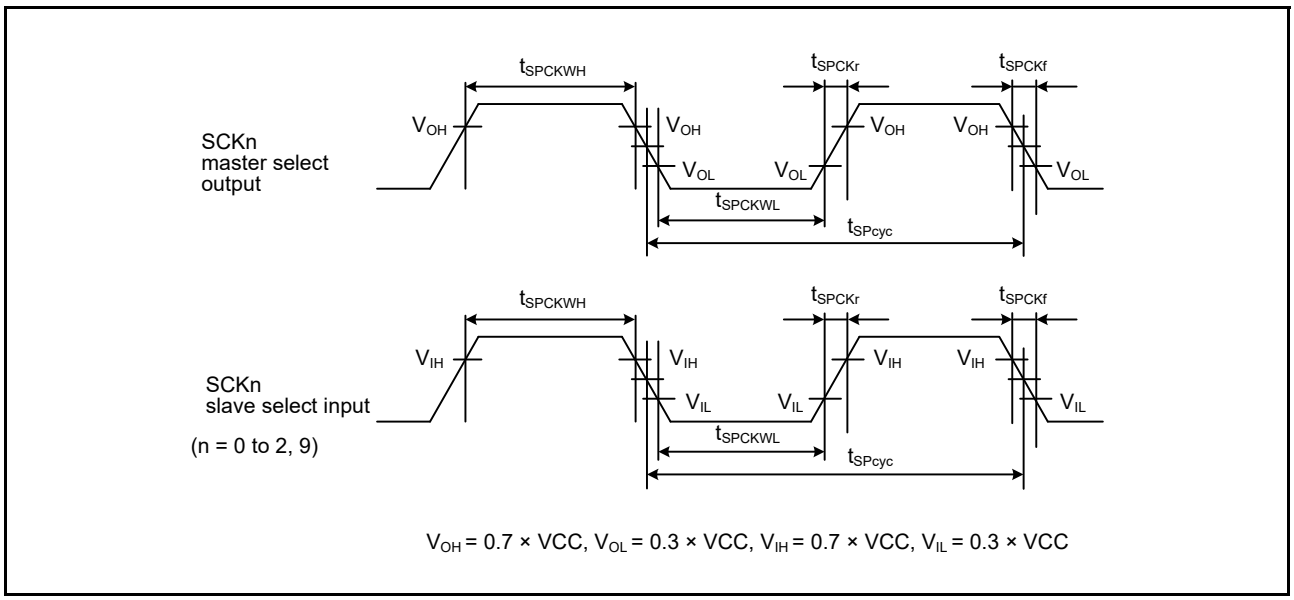



**Figure 2.46 SCI simple SPI mode clock timing**

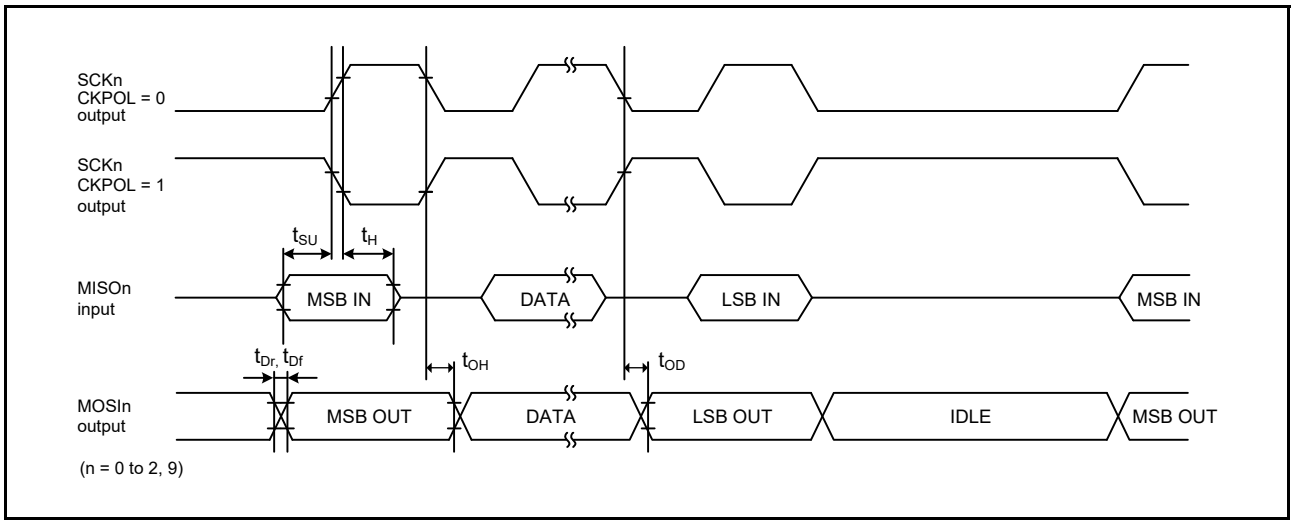



**Figure 2.47 SCI simple SPI mode timing for master when CKPH = 1**

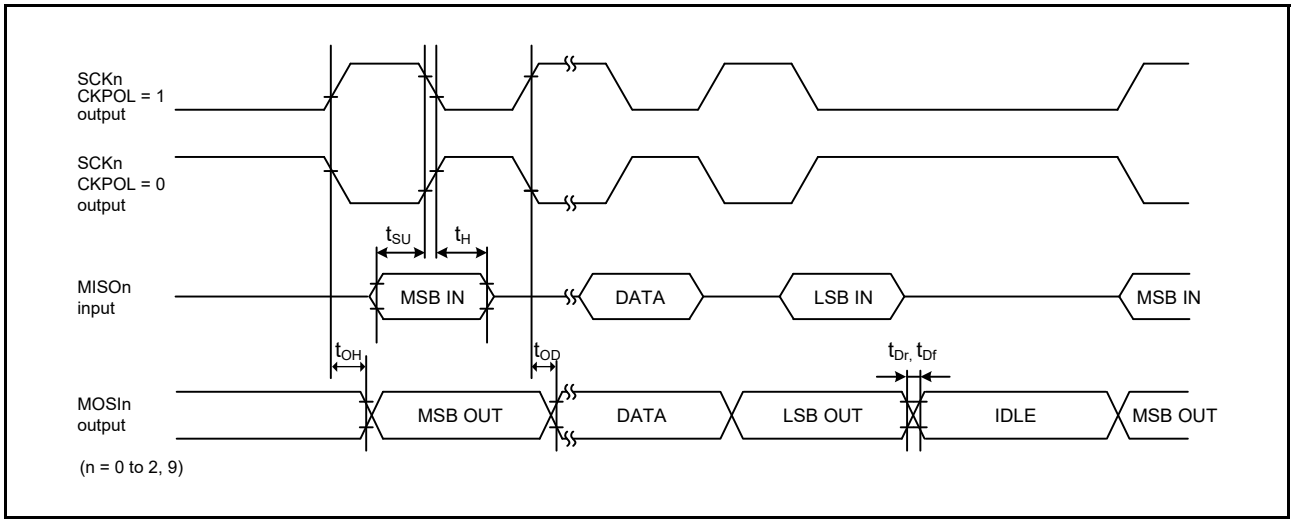



**Figure 2.48 SCI simple SPI mode timing for master when CKPH = 0**

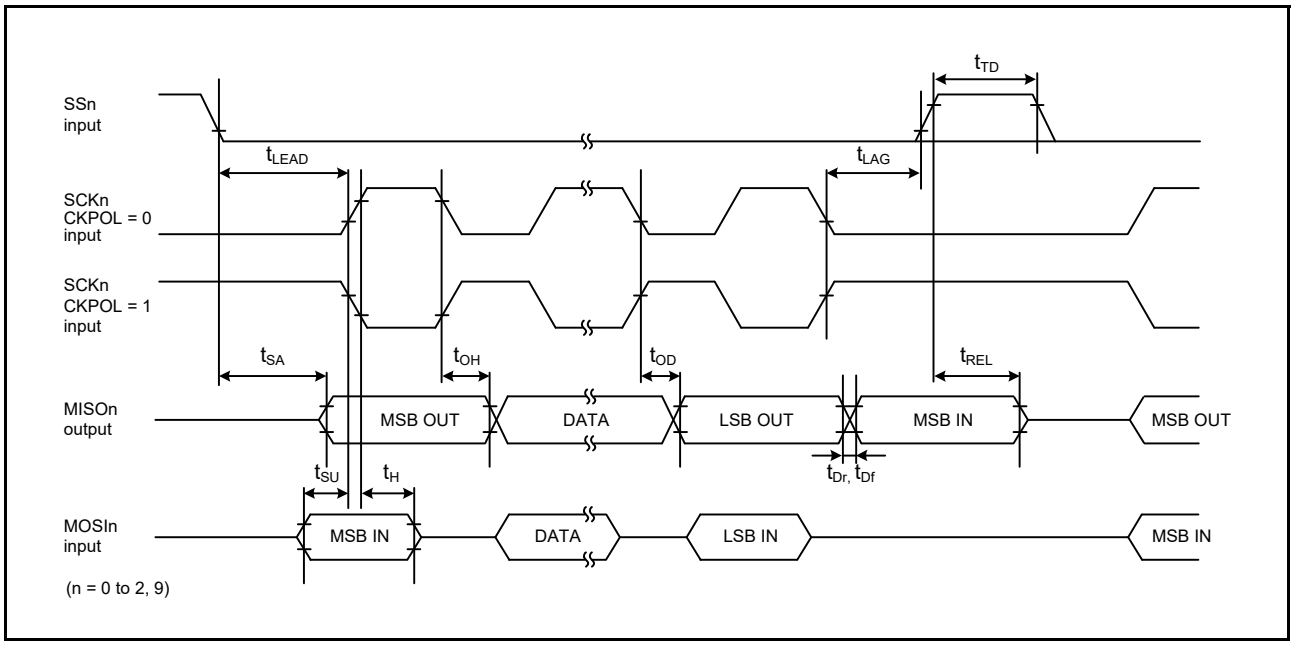



**Figure 2.49 SCI simple SPI mode timing for slave when CKPH = 1**

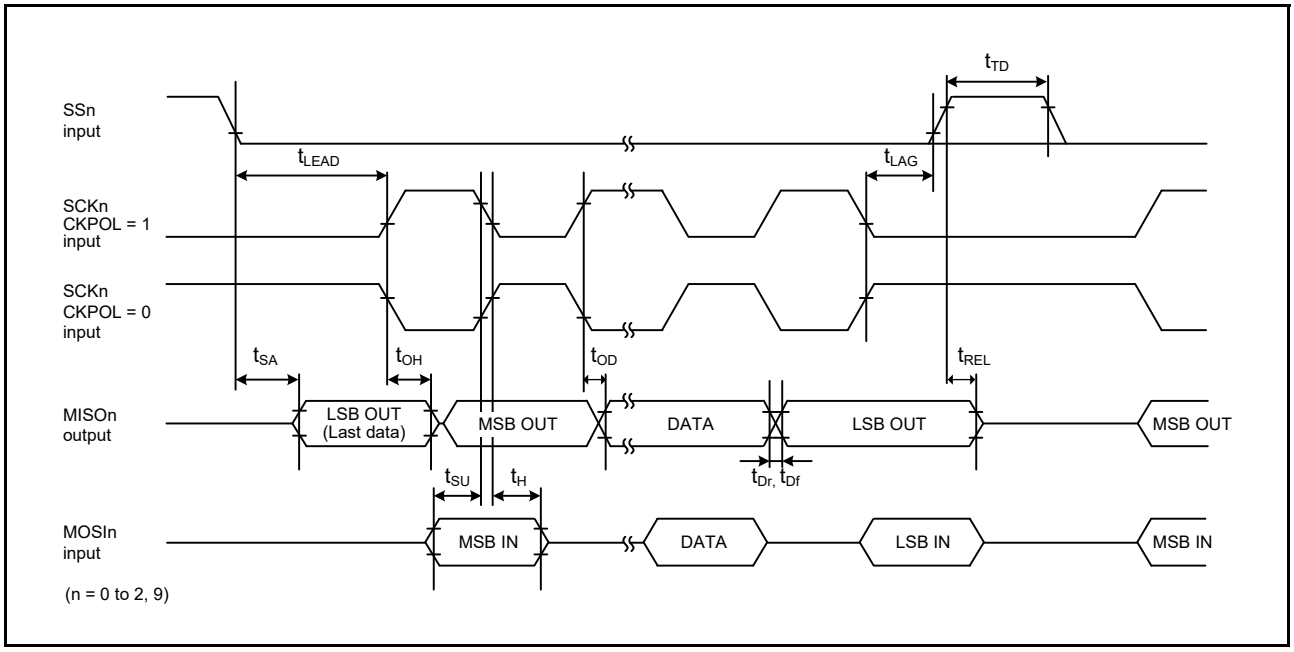


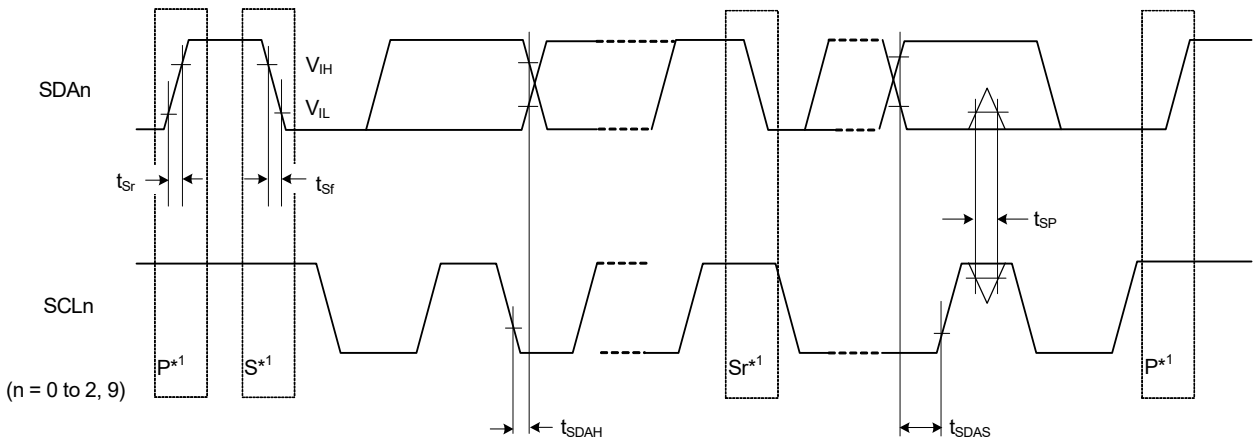

**Figure 2.50 SCI simple SPI mode timing for slave when CKPH = 0**

**Table 2.35 SCI timing (3)**

Conditions: VCC = 2.7 to 5.5 V

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Simple I²C (Standard mode) | SDA input rise time | $t_{Sr}$ | - | 1000 | ns | Figure 2.51 |
| | SDA input fall time | $t_{Sf}$ | - | 300 | ns | |
| | SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{IICcyc}$*1 | ns | |
| | Data input setup time | $t_{SDAS}$ | 250 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$*2 | - | 400 | pF | |
| Simple I²C (Fast mode) | SDA input rise time | $t_{Sr}$ | - | 300 | ns | Figure 2.51 For all ports except P408, use PmnPFS.DSCR of middle drive. For port P408, use PmnPFS.DSCR1 /DSCR of middle drive for IIC fast-mode. |
| | SDA input fall time | $t_{Sf}$ | - | 300 | ns | |
| | SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{IICcyc}$*1 | ns | |
| | Data input setup time | $t_{SDAS}$ | 100 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$*1 | - | 400 | pF | |

Note 1. tIICcyc: Clock cycle selected by the SMR.CKS[1:0] bits.
Note 2. Cb indicates the total capacity of the bus line.




Note 1. S, P, and Sr indicate the following:
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions:
$V_{IH}$ = VCC × 0.7, $V_{IL}$ = VCC × 0.3
$V_{OL}$ = 0.6 V, $I_{OL}$ = 6 mA

**Figure 2.51 SCI simple IIC mode timing**

## 2.3.9 SPI Timing

**Table 2.36 SPI timing (1 of 2)**

Conditions: Middle drive output is selected in the Port Drive Capability bit in PmnPFS register

| Parameter | | | | Symbol | Min | Max | Unit*1 | Test conditions |
|---|---|---|---|---|---|---|---|---|
| SPI | RSPCK clock cycle | Master | | $t_{SPcyc}$ | 2*4 | 4096 | $t_{Pcyc}$ | Figure 2.52 |
| | | Slave | | | 6 | 4096 | | |
| | RSPCK clock high pulse width | Master | | $t_{SPCKWH}$ | ($t_{SPcyc}$ - $t_{SPCKr}$- $t_{SPCKf}$) / 2 - 3 | - | ns | |
| | | Slave | | | 3 × $t_{Pcyc}$ | - | | |
| | RSPCK clock low pulse width | Master | | $t_{SPCKWL}$ | ($t_{SPcyc}$ - $t_{SPCKr}$ - $t_{SPCKf}$) / 2 - 3 | - | ns | |
| | | Slave | | | 3 × $t_{Pcyc}$ | - | | |
| | RSPCK clock rise and fall time | Output | 2.7 V or above | $t_{SPCKr}$, $t_{SPCKf}$ | - | 10 | ns | |
| | | | 2.4 V or above | | - | 15 | | |
| | | | 1.8 V or above | | - | 20 | | |
| | | | 1.6 V or above | | - | 30 | | |
| | | Input | | | - | 1 | μs | |
| | Data input setup time | Master | | $t_{SU}$ | 10 | - | ns | Figure 2.53 to Figure 2.58 |
| | | Slave | 2.4 V or above | | 10 | - | | |
| | | | 1.8 V or above | | 15 | - | | |
| | | | 1.6 V or above | | 20 | - | | |
| | Data input hold time | Master (RSPCK is PCLKA/2) | | $t_{HF}$ | 0 | - | ns | |
| | | Master (RSPCK is other than above.) | | $t_H$ | $t_{Pcyc}$ | - | | |
| | | Slave | | $t_H$ | 20 | - | | |
| | SSL setup time | Master | 1.8 V or above | $t_{LEAD}$ | -30 + N × $t_{Spcyc}$*2 | - | ns | |
| | | | 1.6 V or above | | -50 + N × $t_{Spcyc}$*2 | - | | |
| | | Slave | | | 6 × $t_{Pcyc}$ | - | | |
| | SSL hold time | Master | | $t_{LAG}$ | -30 + N × $t_{Spcyc}$*3 | - | | |
| | | Slave | | | 6 × $t_{Pcyc}$ | - | | |

**Table 2.36 SPI timing (2 of 2)**

Conditions: Middle drive output is selected in the Port Drive Capability bit in PmnPFS register

| Parameter | | | | Symbol | Min | Max | Unit*1 | Test conditions |
|---|---|---|---|---|---|---|---|---|
| SPI | Data output delay | Master | 2.7 V or above | $t_{OD}$ | - | 14 | ns | Figure 2.53 to Figure 2.58 |
| | | | 2.4 V or above | | - | 20 | | |
| | | | 1.8 V or above | | - | 25 | | |
| | | | 1.6 V or above | | - | 30 | | |
| | | Slave | 2.7 V or above | | - | 50 | | |
| | | | 2.4 V or above | | - | 60 | | |
| | | | 1.8 V or above | | - | 85 | | |
| | | | 1.6 V or above | | - | 110 | | |
| | Data output hold time | Master | | $t_{OH}$ | 0 | - | ns | |
| | | Slave | | | 0 | - | | |
| | Successive transmission delay | Master | | $t_{TD}$ | $t_{SPcyc} + 2 \times t_{Pcyc}$ | $8 \times t_{SPcyc} + 2 \times t_{Pcyc}$ | ns | |
| | | Slave | | | $6 \times t_{Pcyc}$ | - | | |
| | MOSI and MISO rise and fall time | Output | 2.7 V or above | $t_{Dr}$, $t_{Df}$ | - | 10 | ns | |
| | | | 2.4 V or above | | - | 15 | | |
| | | | 1.8 V or above | | - | 20 | | |
| | | | 1.6 V or above | | - | 30 | | |
| | | Input | | | - | 1 | μs | |
| | SSL rise and fall time | Output | 2.7 V or above | $t_{SSLr}$, $t_{SSLf}$ | - | 10 | ns | |
| | | | 2.4 V or above | | - | 15 | | |
| | | | 1.8 V or above | | - | 20 | | |
| | | | 1.6 V or above | | - | 30 | | |
| | | Input | | | - | 1 | μs | |
| | Slave access time | | 2.4 V or above | $t_{SA}$ | - | $2 \times t_{Pcyc} + 100$ | ns | Figure 2.57 and Figure 2.58 |
| | | | 1.8 V or above | | - | $2 \times t_{Pcyc} + 140$ | | |
| | | | 1.6 V or above | | - | $2 \times t_{Pcyc} + 180$ | | |
| | Slave output release time | | 2.4 V or above | $t_{REL}$ | - | $2 \times t_{Pcyc} + 100$ | ns | |
| | | | 1.8 V or above | | - | $2 \times t_{Pcyc} + 140$ | | |
| | | | 1.6 V or above | | - | $2 \times t_{Pcyc} + 180$ | | |

Note 1. $t_{Pcyc}$: PCLKA cycle.
Note 2. N is set as an integer from 1 to 8 by the SPCKD register.
Note 3. N is set as an integer from 1 to 8 by the SSLND register.
Note 4. The upper limit of RSPCK is 16 MHz.

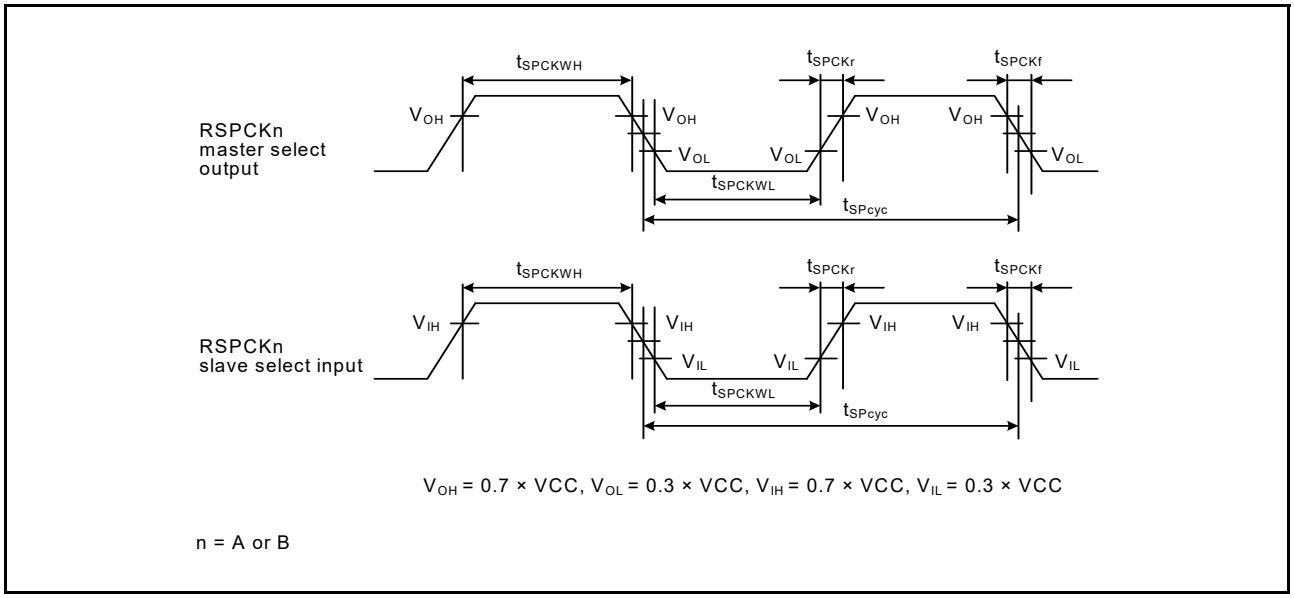



**Figure 2.52 SPI clock timing**

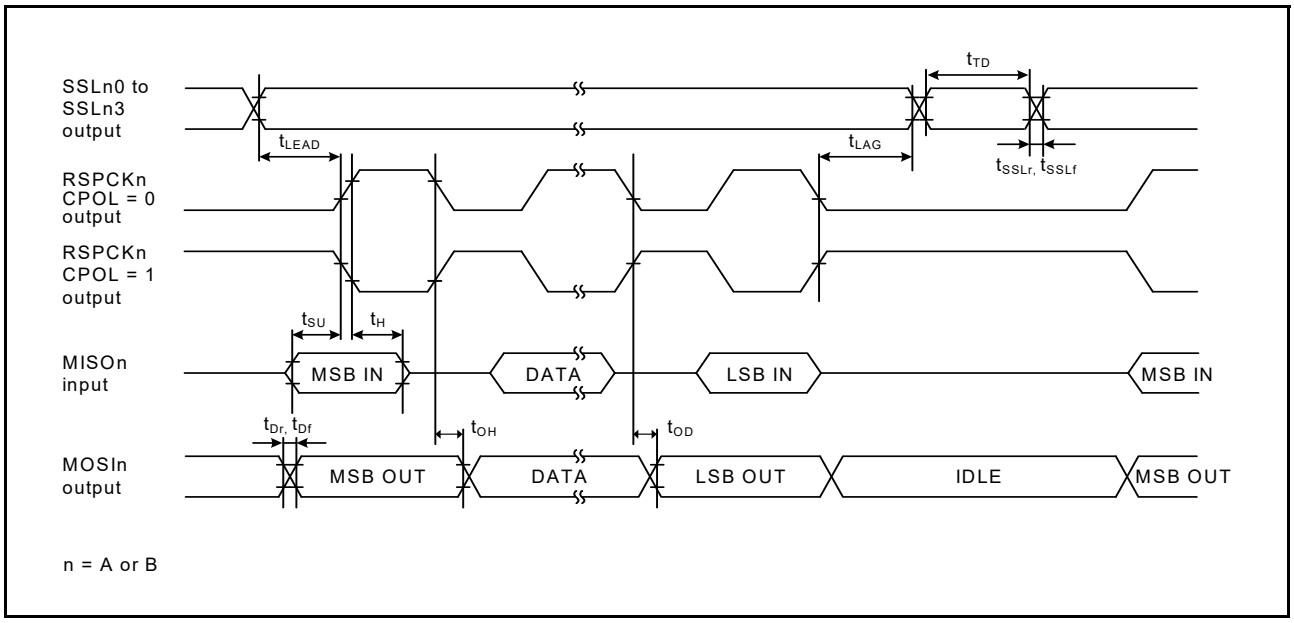



**Figure 2.53 SPI timing for master when CPHA = 0 and the bit rate is set to any value other than PCLKA/2**

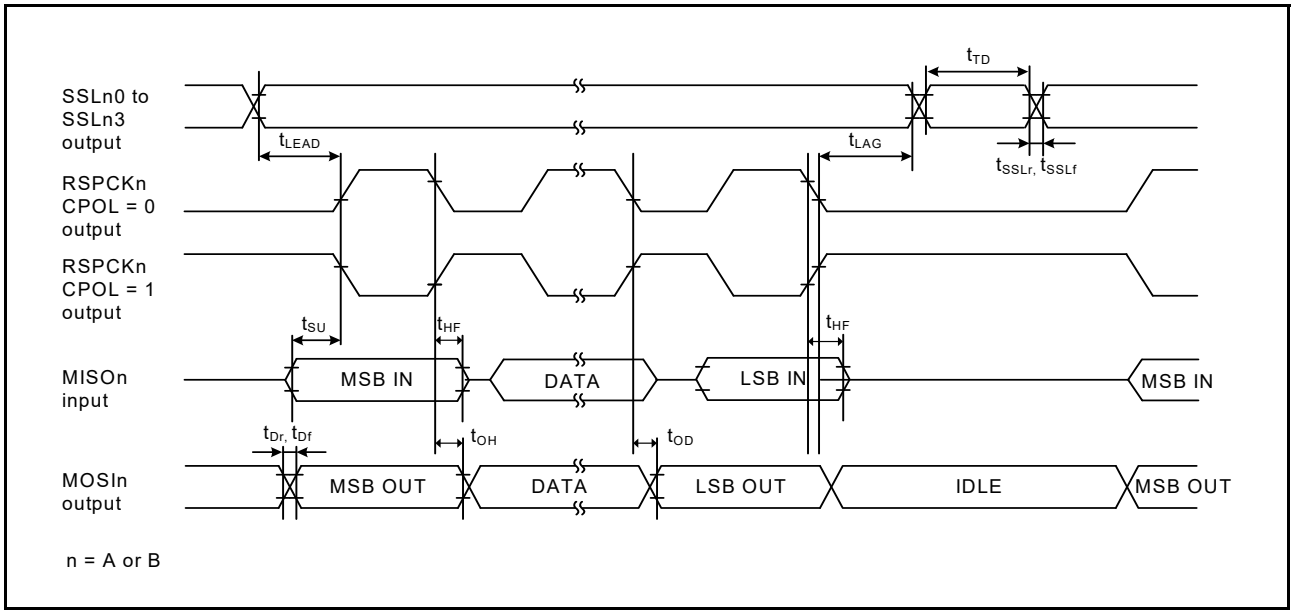



**Figure 2.54 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2**

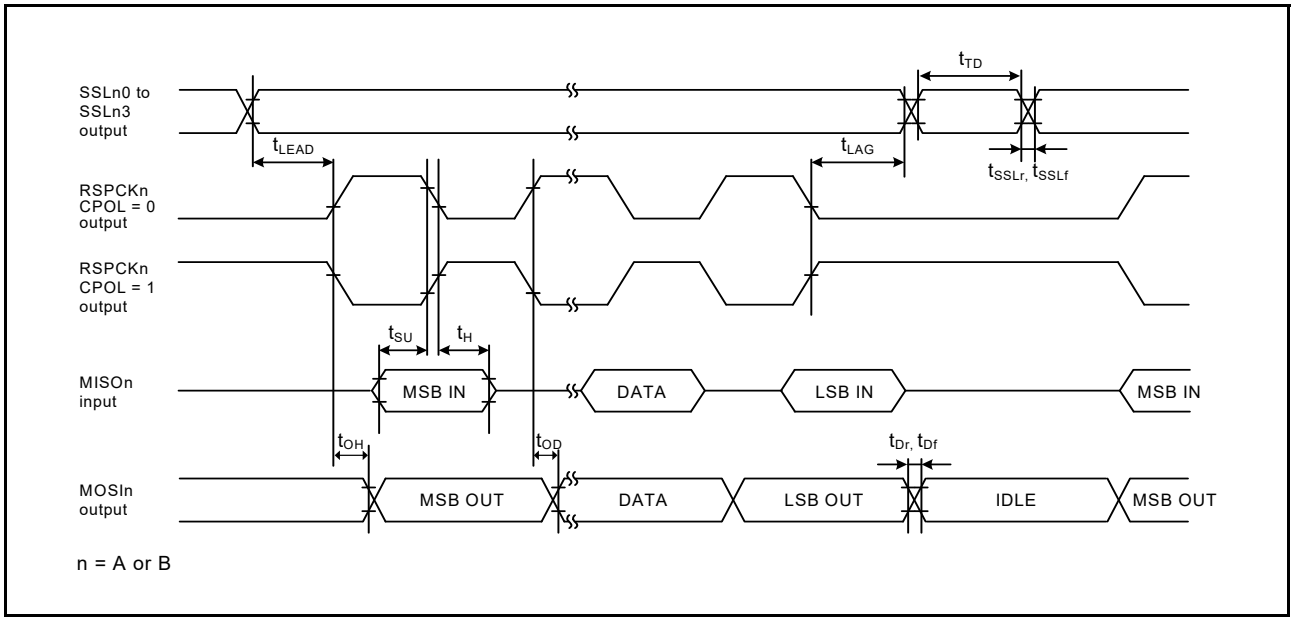



**Figure 2.55 SPI timing for master when CPHA = 1 and the bit rate is set to any value other than PCLKA/2**

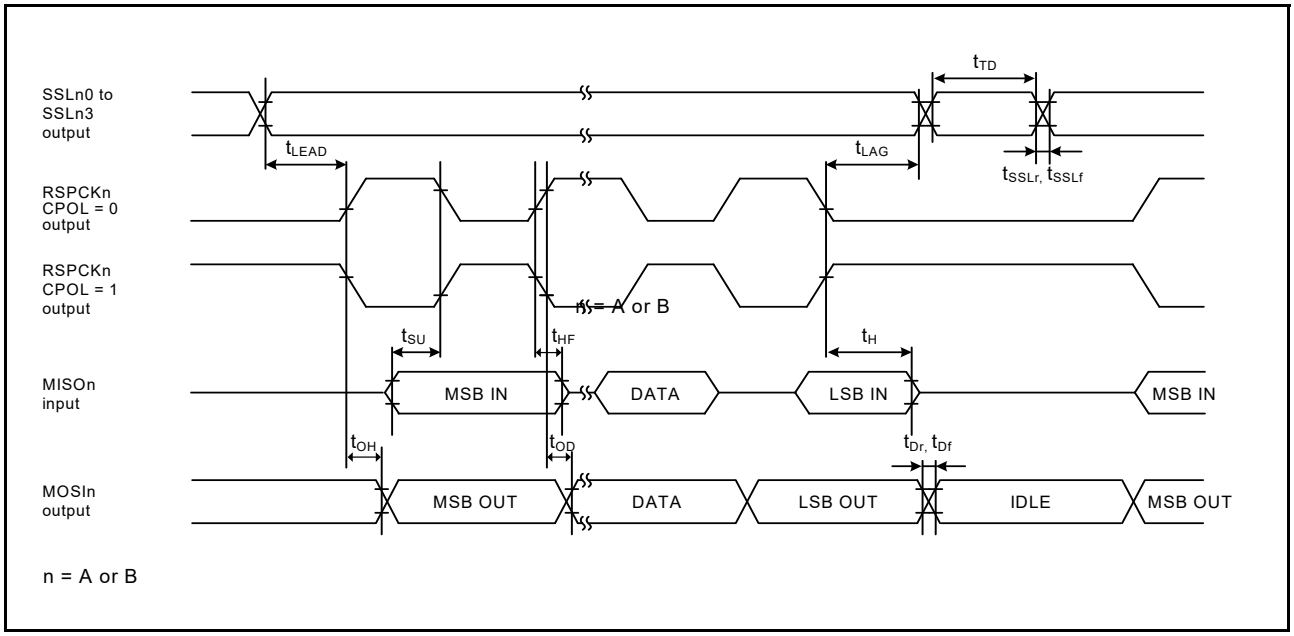



**Figure 2.56 SPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2**

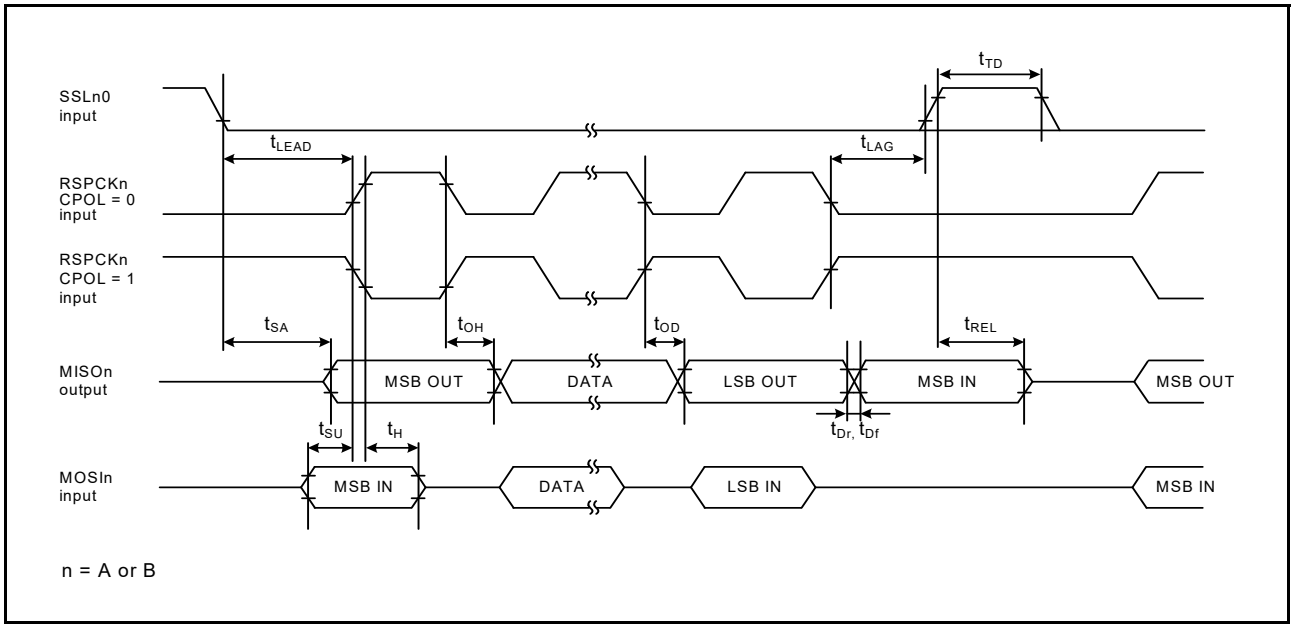



**Figure 2.57 SPI timing for slave when CPHA = 0**

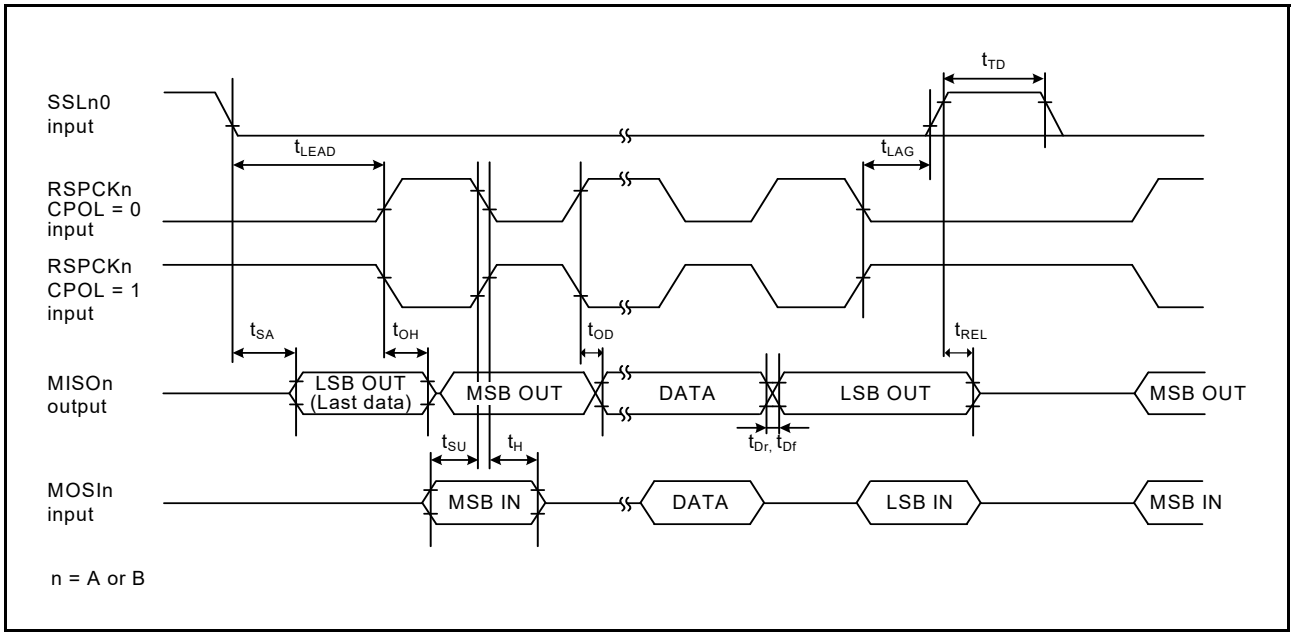



**Figure 2.58 SPI timing for slave when CPHA = 1**

## 2.3.10 IIC Timing

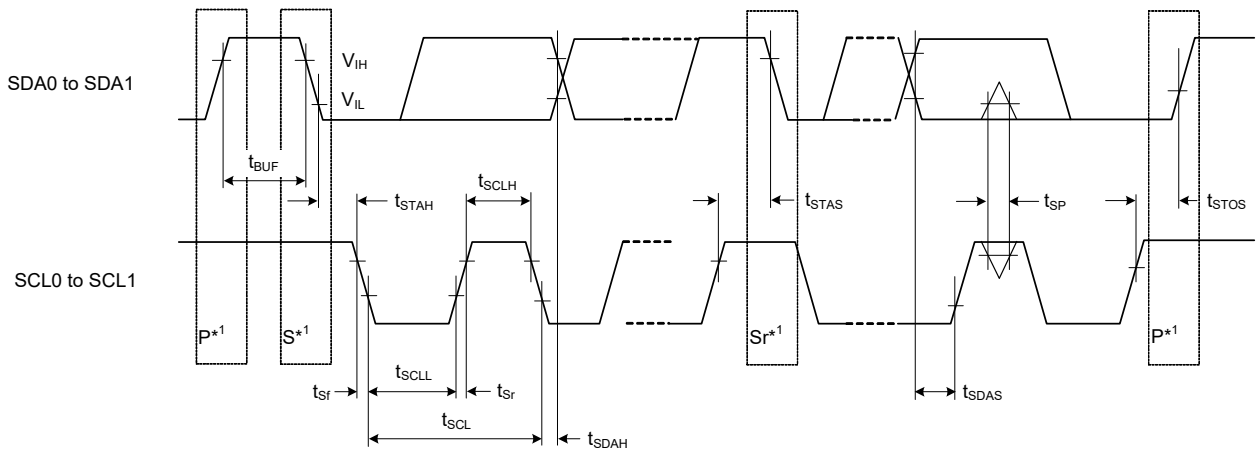
**Table 2.37 IIC timing (1 of 2)**
Conditions: VCC = 2.7 to 5.5 V

| Parameter | | Symbol | Min*1 | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| IIC (standard mode, SMBus) | SCL input cycle time | $t_{SCL}$ | 6 (12) × $t_{IICcyc}$ + 1300 | - | ns | Figure 2.59 |
| | SCL input high pulse width | $t_{SCLH}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | - | 1,000 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | - | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1 (4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time (When wakeup function is disabled) | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SDA input bus free time (When wakeup function is enabled) | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 4 × $t_{Pcyc}$ + 300 | - | ns | |
| | START condition input hold time (When wakeup function is disabled) | $t_{STAH}$ | $t_{IICcyc}$ + 300 | - | ns | |
| | START condition input hold time (When wakeup function is enabled) | $t_{STAH}$ | 1 (5) × $t_{IICcyc}$ + $t_{Pcyc}$ + 300 | - | ns | |
| | Repeated START condition input setup time | $t_{STAS}$ | 1,000 | - | ns | |
| | STOP condition input setup time | $t_{STOS}$ | 1,000 | - | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$ | - | 400 | pF | |

**Table 2.37 IIC timing (2 of 2)**
Conditions: VCC = 2.7 to 5.5 V

| Parameter | | Symbol | Min*1 | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| IIC (Fast mode) | SCL input cycle time | $t_{SCL}$ | 6 (12) × $t_{IICcyc}$ + 600 | - | ns | Figure 2.59 For all ports except P408, use PmnPFS.DSCR of middle drive. For port P408, use PmnPFS.DSCR1/DSCR of middle drive for IIC fast-mode. |
| | SCL input high pulse width | $t_{SCLH}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | - | 300 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | - | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1 (4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time (When wakeup function is disabled) | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SDA input bus free time (When wakeup function is enabled) | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 4 × $t_{Pcyc}$ + 300 | - | ns | |
| | START condition input hold time (When wakeup function is disabled) | $t_{STAH}$ | $t_{IICcyc}$ + 300 | - | ns | |
| | START condition input hold time (When wakeup function is enabled) | $t_{STAH}$ | 1(5) × $t_{IICcyc}$ + $t_{Pcyc}$ + 300 | - | ns | |
| | Repeated START condition input setup time | $t_{STAS}$ | 300 | - | ns | |
| | STOP condition input setup time | $t_{STOS}$ | 300 | - | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$ | - | 400 | pF | |

Note: $t_{IICcyc}$: IIC internal reference clock (IICφ) cycle, $t_{Pcyc}$: PCLKB cycle
Note 1. The value in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.




Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition.

**Figure 2.59 IIC bus interface input/output timing**

### 2.3.11 SSIE Timing

**Table 2.38 SSIE timing**
Conditions: VCC = 1.6 to 5.5 V

| Parameter | | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| SSIE | AUDIO_CLK input frequency | 2.7 V or above | $t_{AUDIO}$ | - | 25 | MHz | - |
| | | 1.6 V or above | | - | 4 | | |
| | Output clock period | | $t_O$ | 250 | - | ns | Figure 2.60 |
| | Input clock period | | $t_I$ | 250 | - | ns | |
| | Clock high pulse width | 1.8 V or above | $t_{HC}$ | 100 | - | ns | |
| | | 1.6 V or above | | 200 | - | | |
| | Clock low pulse width | 1.8 V or above | $t_{LC}$ | 100 | - | ns | |
| | | 1.6 V or above | | 200 | - | | |
| | Clock rise time | | $t_{RC}$ | - | 25 | ns | |
| | Data delay | 2.7 V or above | $t_{DTR}$ | - | 65 | ns | Figure 2.61, Figure 2.62 |
| | | 1.8 V or above | | - | 105 | | |
| | | 1.6 V or above | | - | 140 | | |
| | Set-up time | 2.7 V or above | $t_{SR}$ | 65 | - | ns | |
| | | 1.8 V or above | | 90 | - | | |
| | | 1.6 V or above | | 140 | - | | |
| | Hold time | | $t_{HTR}$ | 40 | - | ns | |
| | SSITXD0 output delay from SSILRCK0/SSIFS0 change time | 1.8 V or above | $T_{DTRW}$ | - | 105 | ns | Figure 2.63 |
| | | 1.6 V or above | | - | 140 | | |

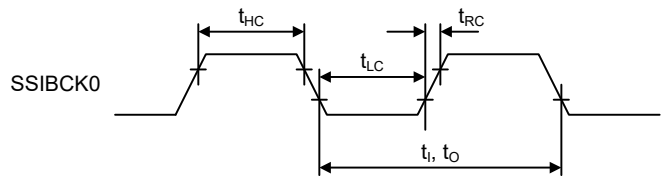



**Figure 2.60 SSIE clock input/output timing**

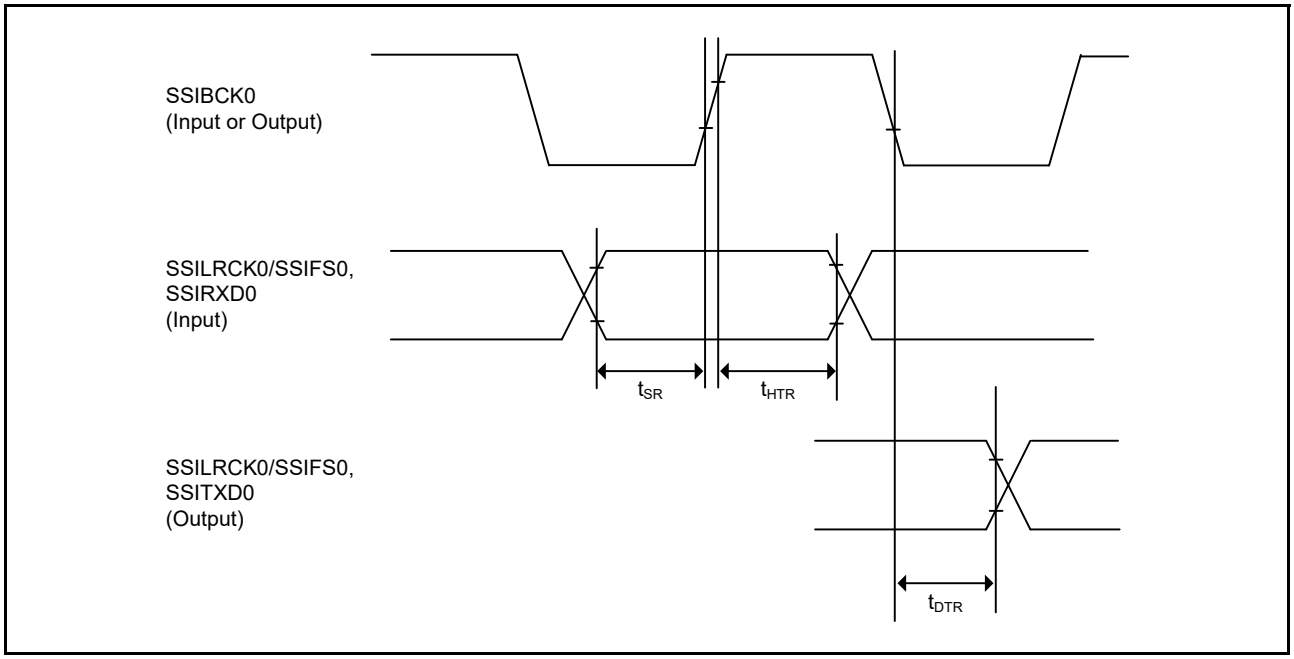



**Figure 2.61 SSIE data transmit/receive timing (SSICR.BCKP = 0)**

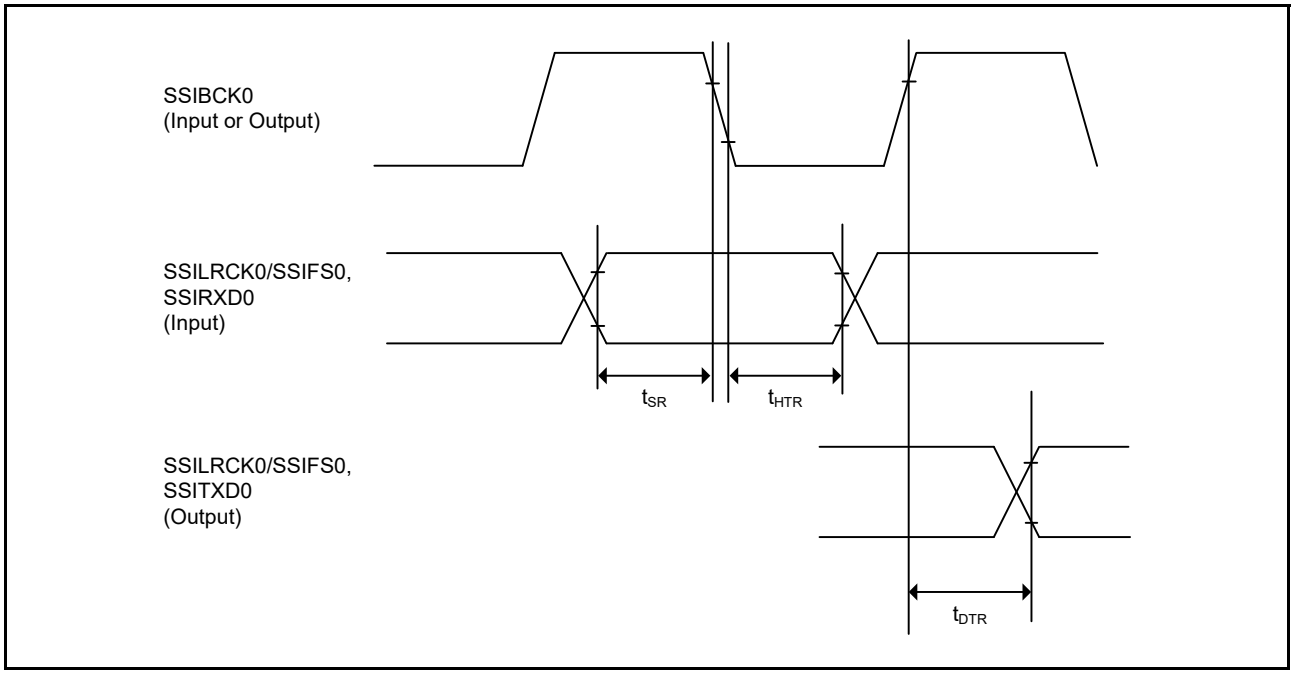
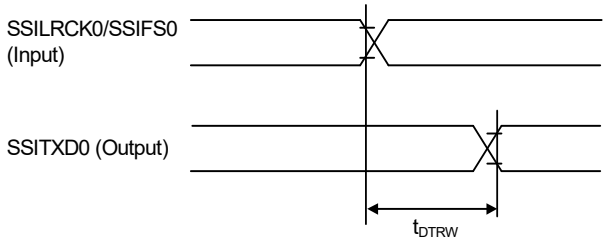



**Figure 2.62 SSIE data transmit/receive timing (SSICR.BCKP = 1)**




MSB bit output delay from SSILRCK0/SSIFS0 change time for
slave transmitter when DEL = 1, SDTA = 0 or DEL = 1, SDTA = 1, SWL[2:0] = DWL[2:0]

**Figure 2.63 SSIE data output delay from SSILRCK0/SSIFS0 change time**

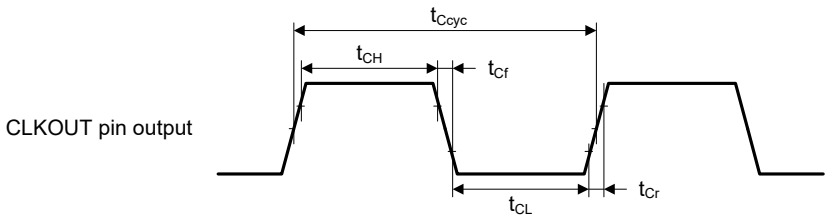
## 2.3.12 CLKOUT Timing

**Table 2.39 CLKOUT timing**

| Parameter | | | Symbol | Min | Max | Unit*1 | Test conditions |
|---|---|---|---|---|---|---|---|
| CLKOUT | CLKOUT pin output cycle*1 | VCC = 2.7 V or above | $t_{Ccyc}$ | 62.5 | - | ns | Figure 2.64 |
| | | VCC = 1.8 V or above | | 125 | - | | |
| | | VCC = 1.6 V or above | | 250 | - | | |
| | CLKOUT pin high pulse width*2 | VCC = 2.7 V or above | $t_{CH}$ | 15 | - | ns | |
| | | VCC = 1.8 V or above | | 30 | - | | |
| | | VCC = 1.6 V or above | | 150 | - | | |
| | CLKOUT pin low pulse width*2 | VCC = 2.7 V or above | $t_{CL}$ | 15 | - | ns | |
| | | VCC = 1.8 V or above | | 30 | - | | |
| | | VCC = 1.6 V or above | | 150 | - | | |
| | CLKOUT pin output rise time | VCC = 2.7 V or above | $t_{Cr}$ | - | 12 | ns | |
| | | VCC = 1.8 V or above | | - | 25 | | |
| | | VCC = 1.6 V or above | | - | 50 | | |
| | CLKOUT pin output fall time | VCC = 2.7 V or above | $t_{Cf}$ | - | 12 | ns | |
| | | VCC = 1.8 V or above | | - | 25 | | |
| | | VCC = 1.6 V or above | | - | 50 | | |

Note 1. When the EXTAL external clock input or an oscillator is used with division by 1 (the CKOCR.CKOSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

Note 2. When the MOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 001b), set the clock output division ratio selection to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).




Test conditions: $V_{OH}$ = VCC × 0.7, $V_{OL}$ = VCC × 0.3, $I_{OH}$ = -1.0 mA, $I_{OL}$ = 1.0 mA, C = 30 pF

**Figure 2.64 CLKOUT output timing**

## 2.4 USB Characteristics

### 2.4.1 USBFS Timing

**Table 2.40 USB characteristics**

Conditions: VCC = VCC_USB = 3.0 to 3.6 V, $T_a$ = -20 to +85°C (USBCLKSEL = 1), $T_a$ = -40 to +105°C (USBCLKSEL = 0)

| Parameter | | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Input characteristics | Input high level voltage | | $V_{IH}$ | 2.0 | - | V | - |
| | Input low level voltage | | $V_{IL}$ | - | 0.8 | V | - |
| | Differential input sensitivity | | $V_{DI}$ | 0.2 | - | V | \|USB_DP - USB_DM \| |
| | Differential common mode range | | $V_{CM}$ | 0.8 | 2.5 | V | - |
| Output characteristics | Output high level voltage | | $V_{OH}$ | 2.8 | VCC_USB | V | $I_{OH}$ = -200 μA |
| | Output low level voltage | | $V_{OL}$ | 0.0 | 0.3 | V | $I_{OL}$ = 2 mA |
| | Cross-over voltage | | $V_{CRS}$ | 1.3 | 2.0 | V | Figure 2.65, Figure 2.66, Figure 2.67 |
| | Rise time | FS | $t_r$ | 4 | 20 | ns | |
| | | LS | | 75 | 300 | | |
| | Fall time | FS | $t_f$ | 4 | 20 | ns | |
| | | LS | | 75 | 300 | | |
| | Rise/fall time ratio | FS | $t_r/t_f$ | 90 | 111.11 | % | |
| | | LS | | 80 | 125 | | |
| | Output resistance | | $Z_{DRV}$ | 28 | 44 | Ω | (Adjusting the resistance of external elements is not necessary.) |
| VBUS characteristics | VBUS input voltage | | $V_{IH}$ | VCC × 0.8 | - | V | - |
| | | | $V_{IL}$ | - | VCC × 0.2 | V | - |
| Pull-up, pull-down | Pull-down resistor | | $R_{PD}$ | 14.25 | 24.80 | kΩ | - |
| | Pull-up resistor | | $R_{PUI}$ | 0.9 | 1.575 | kΩ | During idle state |
| | | | $R_{PUA}$ | 1.425 | 3.09 | kΩ | During reception |
| Battery Charging Specification Ver 1.2 | D + sink current | | $I_{DP_SINK}$ | 25 | 175 | μA | - |
| | D - sink current | | $I_{DM_SINK}$ | 25 | 175 | μA | - |
| | DCD source current | | $I_{DP_SRC}$ | 7 | 13 | μA | - |
| | Data detection voltage | | $V_{DAT_REF}$ | 0.25 | 0.4 | V | - |
| | D + source voltage | | $V_{DP_SRC}$ | 0.5 | 0.7 | V | Output current = 250 μA |
| | D - source voltage | | $V_{DM_SRC}$ | 0.5 | 0.7 | V | Output current = 250 μA |

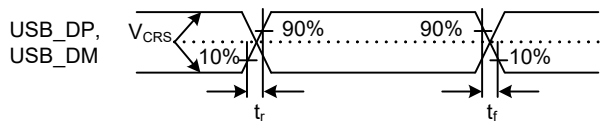



**Figure 2.65 USB_DP and USB_DM output timing**

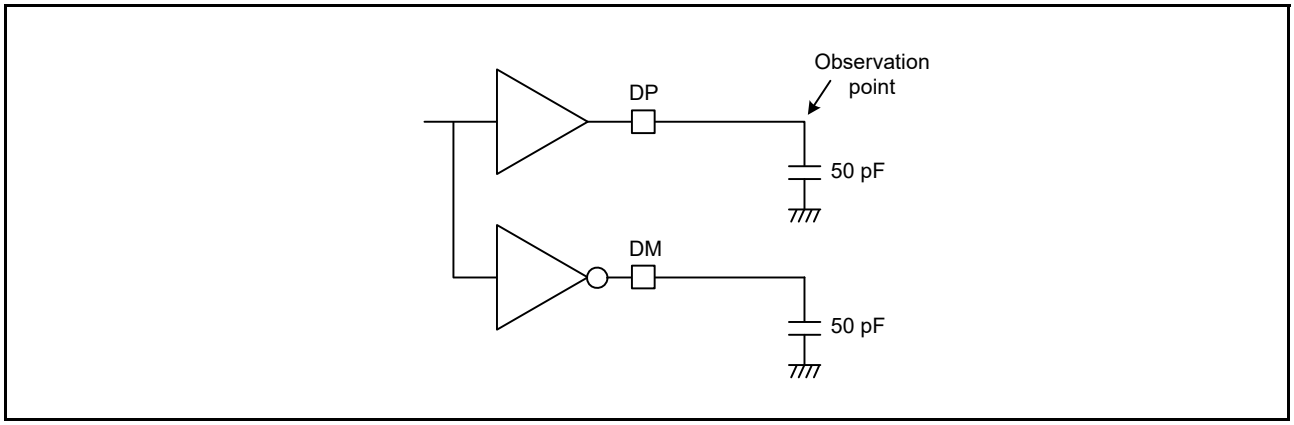



**Figure 2.66 Test circuit for Full-Speed (FS) connection**

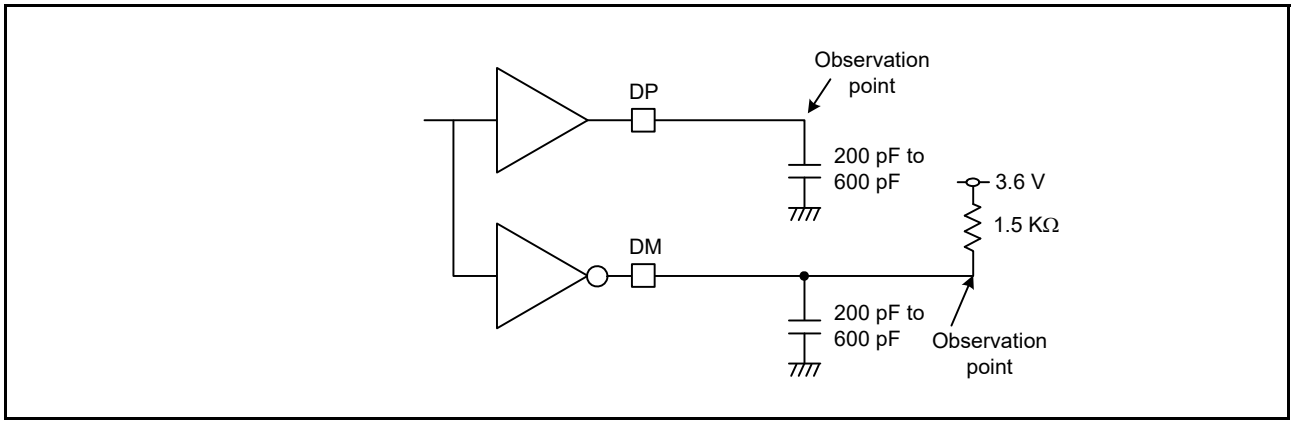



**Figure 2.67 Test circuit for Low-Speed (LS) connection**

## 2.4.2 USB External Supply

**Table 2.41 USB regulator**

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| VCC_USB supply current | VCC_USB_LDO ≥ 3.8V | - | - | 50 | mA | - |
| | VCC_USB_LDO ≥ 4.5V | - | - | 100 | mA | - |
| VCC_USB supply voltage | | 3.0 | - | 3.6 | V | - |

## 2.5 ADC14 Characteristics

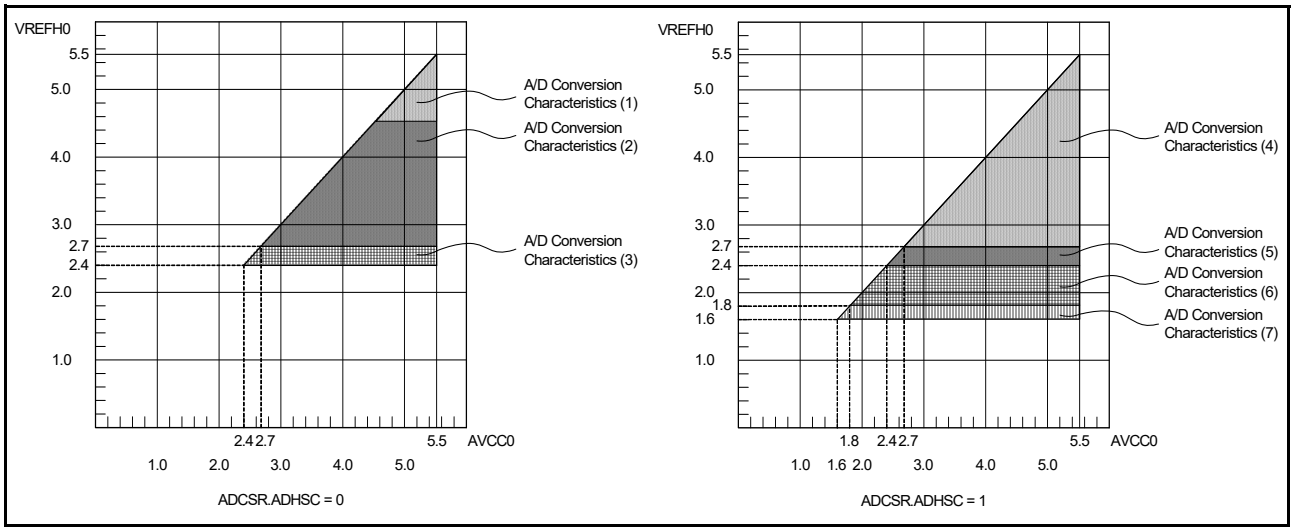



**Figure 2.68 AVCC0 to VREFH0 voltage range**

**Table 2.42 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)**

Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Frequency | | 1 | - | 64 | MHz | - |
| Analog input capacitance*2 | Cs | - | - | 8 (reference data) | pF | High-precision channel |
| | | - | - | 9 (reference data) | pF | Normal-precision channel |
| Analog input resistance | Rs | - | - | 2.5 (reference data) | kΩ | High-precision channel |
| | | - | - | 6.7 (reference data) | kΩ | Normal-precision channel |
| Analog input voltage range | Ain | 0 | - | VREFH0 | V | - |
| 12-bit mode | | | | | | |
| Resolution | | - | - | 12 | Bit | - |
| Conversion time*1 (Operation at PCLKC = 64 MHz) | Permissible signal source impedance Max. = 0.3 kΩ | 0.70 | - | - | μs | High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh |
| | | 1.13 | - | - | μs | Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±0.5 | ±4.5 | LSB | High-precision channel |
| | | | | ±6.0 | LSB | Other than above |
| Full-scale error | | - | ±0.75 | ±4.5 | LSB | High-precision channel |
| | | | | ±6.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±1.25 | ±5.0 | LSB | High-precision channel |
| | | | | ±8.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±1.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±1.0 | ±3.0 | LSB | - |
| 14-bit mode | | | | | | |
| Resolution | | - | - | 14 | Bit | - |

**Table 2.42 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)**

Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Conversion time*1 (Operation at PCLKC = 64 MHz) | Permissible signal source impedance Max. = 0.3 kΩ | 0.80 | - | - | μs | High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh |
| | | 1.22 | - | - | μs | Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±2.0 | ±18 | LSB | High-precision channel |
| | | | | ±24.0 | LSB | Other than above |
| Full-scale error | | - | ±3.0 | ±18 | LSB | High-precision channel |
| | | | | ±24.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±5.0 | ±20 | LSB | High-precision channel |
| | | | | ±32.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±4.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±4.0 | ±12.0 | LSB | - |

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance ($C_{in}$), see section 2.2.4, I/O $V_{OH}$, $V_{OL}$, and Other Characteristics.

**Table 2.43 A/D conversion characteristics (2) in high-speed A/D conversion mode (1 of 2)**

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Frequency | | 1 | - | 48 | MHz | - |
| Analog input capacitance*2 | Cs | - | - | 8 (reference data) | pF | High-precision channel |
| | | - | - | 9 (reference data) | pF | Normal-precision channel |
| Analog input resistance | Rs | - | - | 2.5 (reference data) | kΩ | High-precision channel |
| | | - | - | 6.7 (reference data) | kΩ | Normal-precision channel |
| Analog input voltage range | Ain | 0 | - | VREFH0 | V | - |
| 12-bit mode | | | | | | |
| Resolution | | - | - | 12 | Bit | - |
| Conversion time*1 (Operation at PCLKC = 48 MHz) | Permissible signal source impedance Max. = 0.3 kΩ | 0.94 | - | - | μs | High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh |
| | | 1.50 | - | - | μs | Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±0.5 | ±4.5 | LSB | High-precision channel |
| | | | | ±6.0 | LSB | Other than above |
| Full-scale error | | - | ±0.75 | ±4.5 | LSB | High-precision channel |
| | | | | ±6.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±1.25 | ±5.0 | LSB | High-precision channel |
| | | | | ±8.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±1.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±1.0 | ±3.0 | LSB | - |

**Table 2.43 A/D conversion characteristics (2) in high-speed A/D conversion mode (2 of 2)**

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| 14-bit mode | | | | | | |
| Resolution | | - | - | 14 | Bit | - |
| Conversion time*1 (Operation at PCLKC = 48 MHz) | Permissible signal source impedance Max. = 0.3 kΩ | 1.06 | - | - | μs | High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh |
| | | 1.63 | - | - | μs | Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±2.0 | ±18 | LSB | High-precision channel |
| | | | | ±24.0 | LSB | Other than above |
| Full-scale error | | - | ±3.0 | ±18 | LSB | High-precision channel |
| | | | | ±24.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±5.0 | ±20 | LSB | High-precision channel |
| | | | | ±32.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±4.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±4.0 | ±12.0 | LSB | - |

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance ($C_{in}$), see section 2.2.4, I/O $V_{OH}$, $V_{OL}$, and Other Characteristics.

**Table 2.44 A/D conversion characteristics (3) in high-speed A/D conversion mode (1 of 2)**

Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Frequency | | 1 | - | 32 | MHz | - |
| Analog input capacitance*2 | Cs | - | - | 8 (reference data) | pF | High-precision channel |
| | | - | - | 9 (reference data) | pF | Normal-precision channel |
| Analog input resistance | Rs | - | - | 2.5 (reference data) | kΩ | High-precision channel |
| | | - | - | 6.7 (reference data) | kΩ | Normal-precision channel |
| Analog input voltage range | Ain | 0 | - | VREFH0 | V | - |
| 12-bit mode | | | | | | |
| Resolution | | - | - | 12 | Bit | - |
| Conversion time*1 (Operation at PCLKC = 32 MHz) | Permissible signal source impedance Max. = 1.3 kΩ | 1.41 | - | - | μs | High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh |
| | | 2.25 | - | - | μs | Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±0.5 | ±4.5 | LSB | High-precision channel |
| | | | | ±6.0 | LSB | Other than above |
| Full-scale error | | - | ±0.75 | ±4.5 | LSB | High-precision channel |
| | | | | ±6.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±1.25 | ±5.0 | LSB | High-precision channel |
| | | | | ±8.0 | LSB | Other than above |

**Table 2.44 A/D conversion characteristics (3) in high-speed A/D conversion mode (2 of 2)**

Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| DNL differential nonlinearity error | | - | ±1.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±1.0 | ±3.0 | LSB | - |
| 14-bit mode | | | | | | |
| Resolution | | - | - | 14 | Bit | - |
| Conversion time*1 (Operation at PCLKC = 32 MHz) | Permissible signal source impedance Max. = 1.3 kΩ | 1.59 | - | - | μs | High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh |
| | | 2.44 | - | - | μs | Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±2.0 | ±18 | LSB | High-precision channel |
| | | | | ±24.0 | LSB | Other than above |
| Full-scale error | | - | ±3.0 | ±18 | LSB | High-precision channel |
| | | | | ±24.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±5.0 | ±20 | LSB | High-precision channel |
| | | | | ±32.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±4.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±4.0 | ±12.0 | LSB | - |

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance ($C_{in}$), see section 2.2.4, I/O $V_{OH}$, $V_{OL}$, and Other Characteristics.

**Table 2.45 A/D conversion characteristics (4) in low power A/D conversion mode (1 of 2)**

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Frequency | | 1 | - | 24 | MHz | - |
| Analog input capacitance*2 | Cs | - | - | 8 (reference data) | pF | High-precision channel |
| | | - | - | 9 (reference data) | pF | Normal-precision channel |
| Analog input resistance | Rs | - | - | 2.5 (reference data) | kΩ | High-precision channel |
| | | - | - | 6.7 (reference data) | kΩ | Normal-precision channel |
| Analog input voltage range | Ain | 0 | - | VREFH0 | V | - |
| 12-bit mode | | | | | | |
| Resolution | | - | - | 12 | Bit | - |
| Conversion time*1 (Operation at PCLKC = 24 MHz) | Permissible signal source impedance Max. = 1.1 kΩ | 2.25 | - | - | μs | High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh |
| | | 3.38 | - | - | μs | Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±0.5 | ±4.5 | LSB | High-precision channel |
| | | | | ±6.0 | LSB | Other than above |
| Full-scale error | | - | ±0.75 | ±4.5 | LSB | High-precision channel |
| | | | | ±6.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |

**Table 2.45 A/D conversion characteristics (4) in low power A/D conversion mode (2 of 2)**

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Absolute accuracy | | - | ±1.25 | ±5.0 | LSB | High-precision channel |
| | | | | ±8.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±1.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±1.0 | ±3.0 | LSB | - |
| 14-bit mode | | | | | | |
| Resolution | | - | - | 14 | Bit | - |
| Conversion time*1 (Operation at PCLKC = 24 MHz) | Permissible signal source impedance Max. = 1.1 kΩ | 2.50 | - | - | μs | High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh |
| | | 3.63 | - | - | μs | Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±2.0 | ±18 | LSB | High-precision channel |
| | | | | ±24.0 | LSB | Other than above |
| Full-scale error | | - | ±3.0 | ±18 | LSB | High-precision channel |
| | | | | ±24.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±5.0 | ±20 | LSB | High-precision channel |
| | | | | ±32.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±4.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±4.0 | ±12.0 | LSB | - |

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance ($C_{in}$), see section 2.2.4, I/O $V_{OH}$, $V_{OL}$, and Other Characteristics.

**Table 2.46 A/D conversion characteristics (5) in low power A/D conversion mode (1 of 2)**

Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Frequency | | 1 | - | 16 | MHz | - |
| Analog input capacitance*2 | Cs | - | - | 8 (reference data) | pF | High-precision channel |
| | | - | - | 9 (reference data) | pF | Normal-precision channel |
| Analog input resistance | Rs | - | - | 2.5 (reference data) | kΩ | High-precision channel |
| | | - | - | 6.7 (reference data) | kΩ | Normal-precision channel |
| Analog input voltage range | Ain | 0 | - | VREFH0 | V | - |
| 12-bit mode | | | | | | |
| Resolution | | - | - | 12 | Bit | - |
| Conversion time*1 (Operation at PCLKC = 16 MHz) | Permissible signal source impedance Max. = 2.2 kΩ | 3.38 | - | - | μs | High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh |
| | | 5.06 | - | - | μs | Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±0.5 | ±4.5 | LSB | High-precision channel |
| | | | | ±6.0 | LSB | Other than above |

**Table 2.46 A/D conversion characteristics (5) in low power A/D conversion mode (2 of 2)**

Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Full-scale error | | - | ±0.75 | ±4.5 | LSB | High-precision channel |
| | | | | ±6.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±1.25 | ±5.0 | LSB | High-precision channel |
| | | | | ±8.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±1.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±1.0 | ±3.0 | LSB | - |
| 14-bit mode | | | | | | |
| Resolution | | - | - | 14 | Bit | - |
| Conversion time*1 (Operation at PCLKC = 16 MHz) | Permissible signal source impedance Max. = 2.2 kΩ | 3.75 | - | - | μs | High-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 0Dh |
| | | 5.44 | - | - | μs | Normal-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±2.0 | ±18 | LSB | High-precision channel |
| | | | | ±24.0 | LSB | Other than above |
| Full-scale error | | - | ±3.0 | ±18 | LSB | High-precision channel |
| | | | | ±24.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±5.0 | ±20 | LSB | High-precision channel |
| | | | | ±32.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±4.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±4.0 | ±12.0 | LSB | - |

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance ($C_{in}$), see section 2.2.4, I/O $V_{OH}$, $V_{OL}$, and Other Characteristics.

**Table 2.47 A/D conversion characteristics (6) in low power A/D conversion mode (1 of 2)**

Conditions: VCC = AVCC0 = 1.8 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.8 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Frequency | | 1 | - | 8 | MHz | - |
| Analog input capacitance*2 | Cs | - | - | 8 (reference data) | pF | High-precision channel |
| | | - | - | 9 (reference data) | pF | Normal-precision channel |
| Analog input resistance | Rs | - | - | 3.8 (reference data) | kΩ | High-precision channel |
| | | - | - | 8.2 (reference data) | kΩ | Normal-precision channel |
| Analog input voltage range | Ain | 0 | - | VREFH0 | V | - |
| 12-bit mode | | | | | | |
| Resolution | | - | - | 12 | Bit | - |
| Conversion time*1 (Operation at PCLKC = 8 MHz) | Permissible signal source impedance Max. = 5 kΩ | 6.75 | - | - | μs | High-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 0Dh |
| | | 10.13 | - | - | μs | Normal-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 28h |

**Table 2.47 A/D conversion characteristics (6) in low power A/D conversion mode (2 of 2)**

Conditions: VCC = AVCC0 = 1.8 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.8 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Offset error | | - | ±1.0 | ±7.5 | LSB | High-precision channel |
| | | | | ±10.0 | LSB | Other than above |
| Full-scale error | | - | ±1.5 | ±7.5 | LSB | High-precision channel |
| | | | | ±10.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±3.0 | ±8.0 | LSB | High-precision channel |
| | | | | ±12.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±1.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±1.0 | ±3.0 | LSB | - |
| 14-bit mode | | | | | | |
| Resolution | | - | - | 14 | Bit | - |
| Conversion time*1 (Operation at PCLKC = 8 MHz) | Permissible signal source impedance Max. = 5 kΩ | 7.50 | - | - | μs | High-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 0Dh |
| | | 10.88 | - | - | μs | Normal-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±4.0 | ±30.0 | LSB | High-precision channel |
| | | | | ±40.0 | LSB | Other than above |
| Full-scale error | | - | ±6.0 | ±30.0 | LSB | High-precision channel |
| | | | | ±40.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±12.0 | ±32.0 | LSB | High-precision channel |
| | | | | ±48.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±4.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±4.0 | ±12.0 | LSB | - |

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance ($C_{in}$), see section 2.2.4, I/O $V_{OH}$, $V_{OL}$, and Other Characteristics.

**Table 2.48 A/D conversion characteristics (7) in low power A/D conversion mode (1 of 2)**

Conditions: VCC = AVCC0 = 1.6 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.6 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Frequency | | 1 | - | 4 | MHz | - |
| Analog input capacitance*2 | Cs | - | - | 8 (reference data) | pF | High-precision channel |
| | | - | - | 9 (reference data) | pF | Normal-precision channel |
| Analog input resistance | Rs | - | - | 13.1 (reference data) | kΩ | High-precision channel |
| | | - | - | 14.3 (reference data) | kΩ | Normal-precision channel |
| Analog input voltage range | Ain | 0 | - | VREFH0 | V | - |
| 12-bit mode | | | | | | |
| Resolution | | - | - | 12 | Bit | - |

**Table 2.48 A/D conversion characteristics (7) in low power A/D conversion mode (2 of 2)**

Conditions: VCC = AVCC0 = 1.6 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.6 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Conversion time*1 (Operation at PCLKC = 4 MHz) | Permissible signal source impedance Max. = 9.9 kΩ | 13.5 | - | - | μs | High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh |
| | | 20.25 | - | - | μs | Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±1.0 | ±7.5 | LSB | High-precision channel |
| | | | | ±10.0 | LSB | Other than above |
| Full-scale error | | - | ±1.5 | ±7.5 | LSB | High-precision channel |
| | | | | ±10.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±3.0 | ±8.0 | LSB | High-precision channel |
| | | | | ±12.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±1.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±1.0 | ±3.0 | LSB | - |
| 14-bit mode | | | | | | |
| Resolution | | - | - | 14 | Bit | - |
| Conversion time*1 (Operation at PCLKC = 4 MHz) | Permissible signal source impedance Max. = 9.9 kΩ | 15.0 | - | - | μs | High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh |
| | | 21.75 | - | - | μs | Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±4.0 | ±30.0 | LSB | High-precision channel |
| | | | | ±40.0 | LSB | Other than above |
| Full-scale error | | - | ±6.0 | ±30.0 | LSB | High-precision channel |
| | | | | ±40.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±12.0 | ±32.0 | LSB | High-precision channel |
| | | | | ±48.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±4.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±4.0 | ±12.0 | LSB | - |

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance ($C_{in}$), see section 2.2.4, I/O $V_{OH}$, $V_{OL}$, and Other Characteristics.

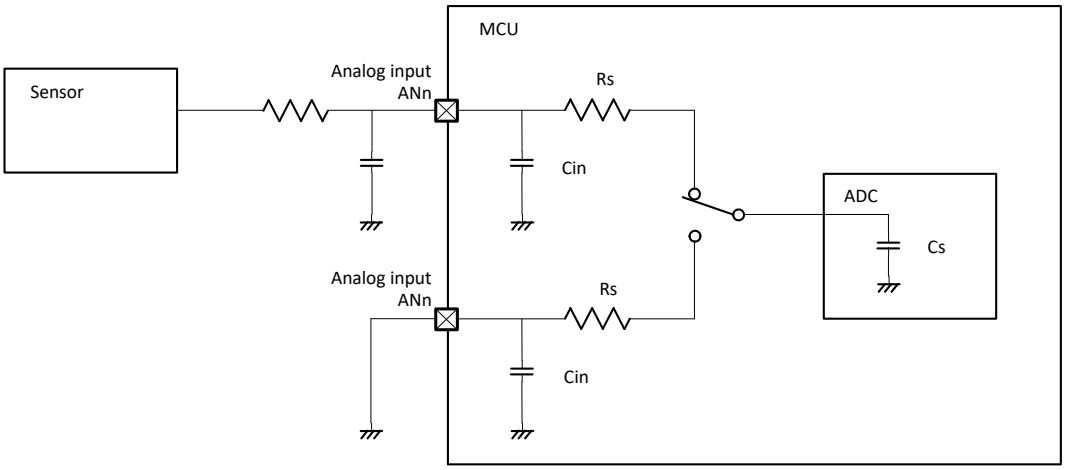



**Figure 2.69 Equivalent circuit for analog input**

**Table 2.49 14-Bit A/D converter channel classification**

| Classification | Channel | Conditions | Remarks |
|---|---|---|---|
| High-precision channel | AN000 to AN014 | AVCC0 = 1.6 to 5.5 V | Pins AN000 to AN014 cannot be used as general I/O, IRQ2, IRQ3 inputs, and TS transmission, when the A/D converter is in use |
| Normal-precision channel | AN016 to AN025 | | |
| Internal reference voltage input channel | Internal reference voltage | AVCC0 = 2.0 to 5.5 V | - |
| Temperature sensor input channel | Temperature sensor output | AVCC0 = 2.0 to 5.5 V | - |

**Table 2.50 A/D internal reference voltage characteristics**

Conditions: VCC = AVCC0 = VREFH0 = 2.0 to 5.5 V*1

| Parameter | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Internal reference voltage input channel*2 | 1.36 | 1.43 | 1.50 | V | - |
| Frequency*3 | 1 | - | 2 | MHz | - |
| Sampling time*4 | 5.0 | - | - | μs | - |

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 < 2.0 V.
Note 2. The 14-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 14-bit A/D converter.
Note 3. This is a parameter for ADC14 when the internal reference voltage is used as the high-potential reference voltage.
Note 4. This is a parameter for ADC14 when the internal reference voltage is selected for an analog input channel in ADC14.

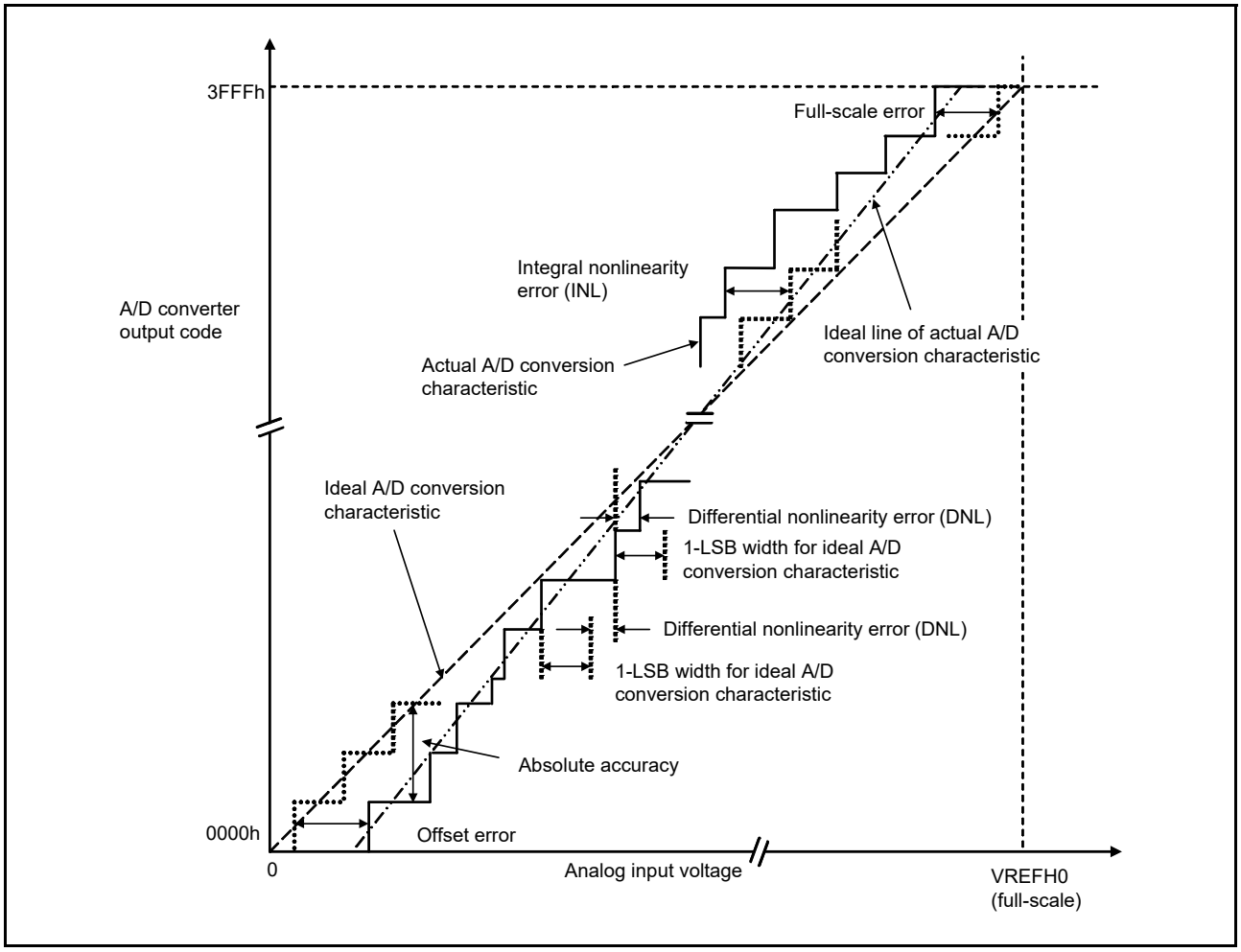



**Figure 2.70 Illustration of 14-bit A/D converter characteristic terms**

### Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

### Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

### Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

### Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

### Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

## 2.6 DAC12 Characteristics

**Table 2.51 D/A conversion characteristics (1)**
Conditions: VCC = AVCC0 = 1.8 to 5.5 V
Reference voltage = VREFH or VREFL selected

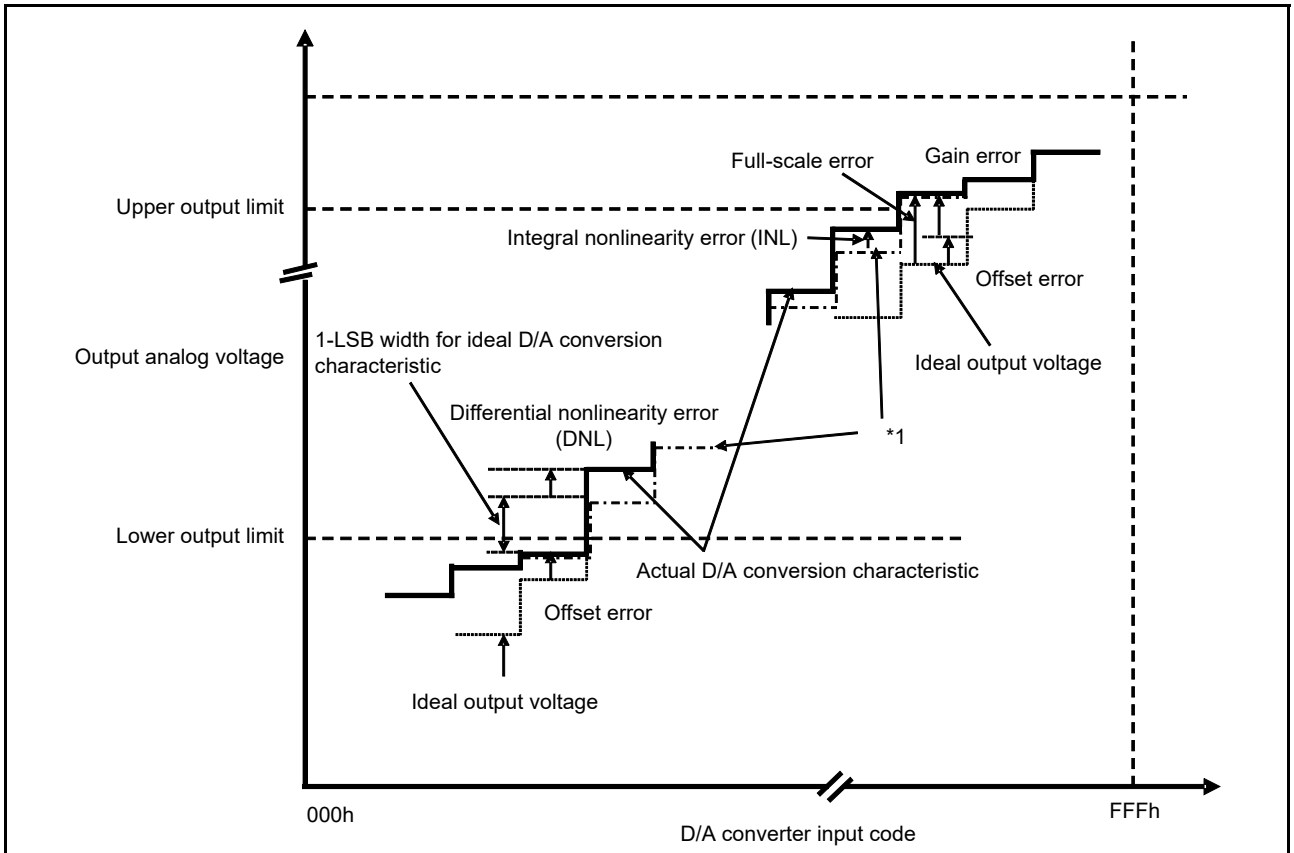
| Parameter | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Resolution | - | - | 12 | bit | - |
| Resistive load | 30 | - | - | kΩ | - |
| Load capacitance | - | - | 50 | pF | - |
| Output voltage range | 0.35 | - | AVCC0 - 0.47 | V | - |
| DNL differential nonlinearity error | - | ±0.5 | ±1.0 | LSB | - |
| INL integral nonlinearity error | - | ±2.0 | ±8.0 | LSB | - |
| Offset error | - | - | ±20 | mV | - |
| Full-scale error | - | - | ±20 | mV | - |
| Output impedance | - | 5 | - | Ω | - |
| Conversion time | - | - | 30 | μs | - |

**Table 2.52 D/A conversion characteristics (2)**
Conditions: VCC = AVCC0 = 1.8 to 5.5 V
Reference voltage = AVCC0 or AVSS0 selected

| Parameter | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Resolution | - | - | 12 | bit | - |
| Resistive load | 30 | - | - | kΩ | - |
| Load capacitance | - | - | 50 | pF | - |
| Output voltage range | 0.35 | - | AVCC0 - 0.47 | V | - |
| DNL differential nonlinearity error | - | ±0.5 | ±2.0 | LSB | - |
| INL integral nonlinearity error | - | ±2.0 | ±8.0 | LSB | - |
| Offset error | - | - | ±30 | mV | - |
| Full-scale error | - | - | ±30 | mV | - |
| Output impedance | - | 5 | - | Ω | - |
| Conversion time | - | - | 30 | μs | - |

**Table 2.53 D/A conversion characteristics (3)**
Conditions: VCC = AVCC0 = 1.8 to 5.5 V
Reference voltage = internal reference voltage selected

| Parameter | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Resolution | - | - | 12 | bit | - |
| Internal reference voltage (Vbgr) | 1.36 | 1.43 | 1.50 | V | - |
| Resistive load | 30 | - | - | kΩ | - |
| Load capacitance | - | - | 50 | pF | - |
| Output voltage range | 0.35 | - | Vbgr | V | - |
| DNL differential nonlinearity error | - | ±2.0 | ±16.0 | LSB | - |
| INL integral nonlinearity error | - | ±8.0 | ±16.0 | LSB | - |
| Offset error | - | - | ±30 | mV | - |
| Output impedance | - | 5 | - | Ω | - |
| Conversion time | - | - | 30 | μs | - |




Note 1. Ideal D/A conversion output voltage that is adjusted so that offset and full scale errors are zeroed.

**Figure 2.71 Illustration of D/A converter characteristic terms**

### Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal output voltage based on the ideal conversion characteristic when the measured offset and full-scale errors are zeroed, and the actual output voltage.

### Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB voltage width based on the ideal D/A conversion characteristics and the width of the actual output voltage.

### Offset error

Offset error is the difference between the highest actual output voltage that falls below the lower output limit and the ideal output voltage based on the input code.

### Full-scale error

Full-scale error is the difference between the lowest actual output voltage that exceeds the upper output limit and the ideal output voltage based on the input code.

## 2.7 TSN Characteristics

**Table 2.54 TSN characteristics**

Conditions: VCC = AVCC0 = 2.0 to 5.5 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Relative accuracy | - | - | ±1.5 | - | °C | 2.4 V or above |
| | - | - | ±2.0 | - | °C | Below 2.4 V |
| Temperature slope | - | - | -3.65 | - | mV/°C | - |
| Output voltage (at 25°C) | - | - | 1.05 | - | V | VCC = 3.3 V |
| Temperature sensor start time | $t_{START}$ | - | - | 5 | μs | - |
| Sampling time | - | 5 | - | - | μs | - |

## 2.8 OSC Stop Detect Characteristics

**Table 2.55 Oscillation stop detection circuit characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Detection time | $t_{dr}$ | - | - | 1 | ms | Figure 2.72 |

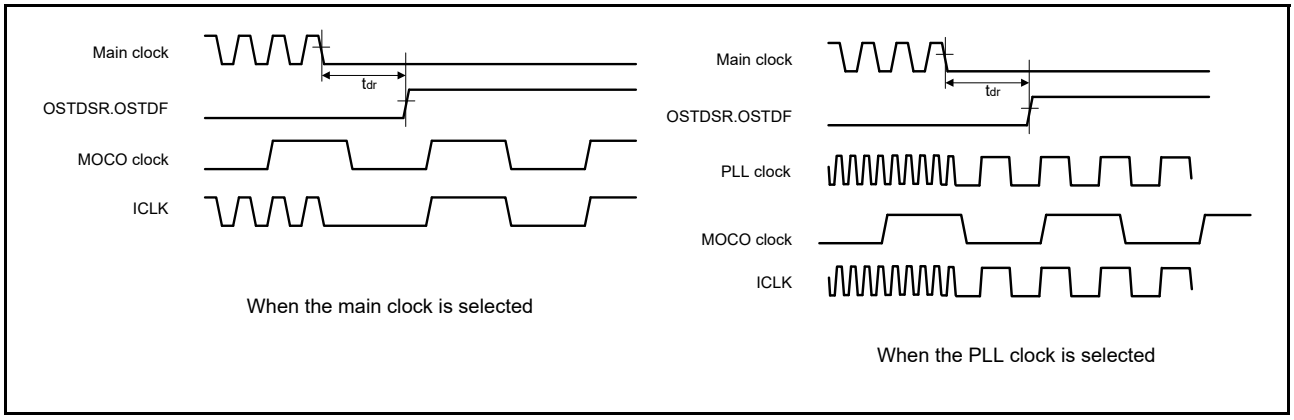



**Figure 2.72 Oscillation stop detection timing**

## 2.9 POR and LVD Characteristics

**Table 2.56 Power-on reset circuit and voltage detection circuit characteristics (1)**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Voltage detection level*1 | Power-on reset (POR) | $V_{POR}$ | 1.27 | 1.42 | 1.57 | V | Figure 2.73, Figure 2.74 |
| | Voltage detection circuit (LVD0)*2 | $V_{det0_0}$ | 3.68 | 3.85 | 4.00 | V | Figure 2.75 At falling edge VCC |
| | | $V_{det0_1}$ | 2.68 | 2.85 | 2.96 | | |
| | | $V_{det0_2}$ | 2.38 | 2.53 | 2.64 | | |
| | | $V_{det0_3}$ | 1.78 | 1.90 | 2.02 | | |
| | | $V_{det0_4}$ | 1.60 | 1.69 | 1.82 | | |
| | Voltage detection circuit (LVD1)*3 | $V_{det1_0}$ | 4.13 | 4.29 | 4.45 | V | Figure 2.76 At falling edge VCC |
| | | $V_{det1_1}$ | 3.98 | 4.16 | 4.30 | | |
| | | $V_{det1_2}$ | 3.86 | 4.03 | 4.18 | | |
| | | $V_{det1_3}$ | 3.68 | 3.86 | 4.00 | | |
| | | $V_{det1_4}$ | 2.98 | 3.10 | 3.22 | | |
| | | $V_{det1_5}$ | 2.89 | 3.00 | 3.11 | | |
| | | $V_{det1_6}$ | 2.79 | 2.90 | 3.01 | | |
| | | $V_{det1_7}$ | 2.68 | 2.79 | 2.90 | | |
| | | $V_{det1_8}$ | 2.58 | 2.68 | 2.78 | | |
| | | $V_{det1_9}$ | 2.48 | 2.58 | 2.68 | | |
| | | $V_{det1_A}$ | 2.38 | 2.48 | 2.58 | | |
| | | $V_{det1_B}$ | 2.10 | 2.20 | 2.30 | | |
| | | $V_{det1_C}$ | 1.84 | 1.96 | 2.05 | | |
| | | $V_{det1_D}$ | 1.74 | 1.86 | 1.95 | | |
| | | $V_{det1_E}$ | 1.63 | 1.75 | 1.84 | | |
| | | $V_{det1_F}$ | 1.60 | 1.65 | 1.73 | | |
| | Voltage detection circuit (LVD2)*4 | $V_{det2_0}$ | 4.11 | 4.31 | 4.48 | V | Figure 2.77 At falling edge VCC |
| | | $V_{det2_1}$ | 3.97 | 4.17 | 4.34 | | |
| | | $V_{det2_2}$ | 3.83 | 4.03 | 4.20 | | |
| | | $V_{det2_3}$ | 3.64 | 3.84 | 4.01 | | |

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit, it cannot be specified whether LVD1 or LVD2 is used for voltage detection.

Note 2. # in the symbol $V_{det0_\#}$ denotes the value of the OFS1.VDSEL1[2:0] bits.

Note 3. # in the symbol $V_{det1_\#}$ denotes the value of the LVDLVLR.LVD1LVL[4:0] bits.

Note 4. # in the symbol $V_{det2_\#}$ denotes the value of the LVDLVLR.LVD2LVL[2:0] bits.

**Table 2.57 Power-on reset circuit and voltage detection circuit characteristics (2)**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Wait time after power-on reset cancellation | LVD0:enable | $t_{POR}$ | - | 1.7 | - | ms | - |
| | LVD0:disable | $t_{POR}$ | - | 1.3 | - | ms | - |
| Wait time after voltage monitor 0,1,2 reset cancellation | LVD0:enable*1 | $t_{LVD0,1,2}$ | - | 0.6 | - | ms | - |
| | LVD0:disable*2 | $t_{LVD1,2}$ | - | 0.2 | - | ms | - |
| Response delay*3 | | $t_{det}$ | - | - | 350 | μs | Figure 2.73, Figure 2.74 |
| Minimum VCC down time | | $t_{VOFF}$ | 450 | - | - | μs | Figure 2.73, VCC = 1.0 V or above |
| Power-on reset enable time | | $t_{W\ (POR)}$ | 1 | - | - | ms | Figure 2.74, VCC = below 1.0 V |
| LVD operation stabilization time (after LVD is enabled) | | $T_{d\ (E-A)}$ | - | - | 300 | μs | Figure 2.76, Figure 2.77 |
| Hysteresis width (POR) | | $V_{PORH}$ | - | 110 | - | mV | - |
| Hysteresis width (LVD0, LVD1 and LVD2) | | $V_{LVH}$ | - | 60 | - | mV | LVD0 selected |
| | | | - | 100 | - | mV | $V_{det1_0}$ to $V_{det1_2}$ selected. |
| | | | - | 60 | - | | $V_{det1_3}$ to $V_{det1_9}$ selected. |
| | | | - | 50 | - | | $V_{det1_A}$ or $V_{det1_B}$ selected. |
| | | | - | 40 | - | | $V_{det1_C}$ or $V_{det1_F}$ selected. |
| | | | - | 60 | - | | LVD2 selected |

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels $V_{POR}$, $V_{det0}$, $V_{det1}$, and $V_{det2}$ for the POR/LVD.

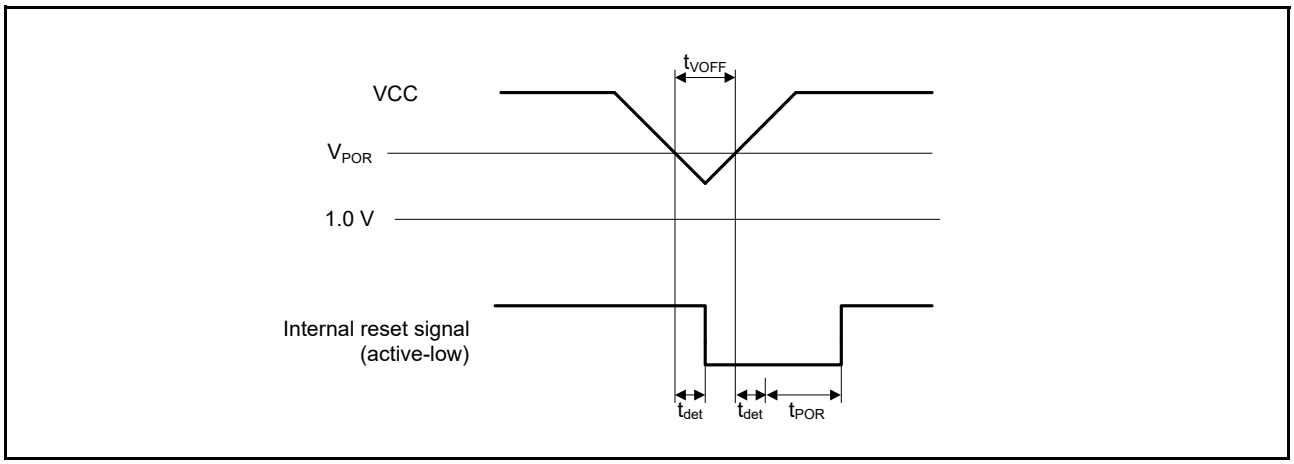
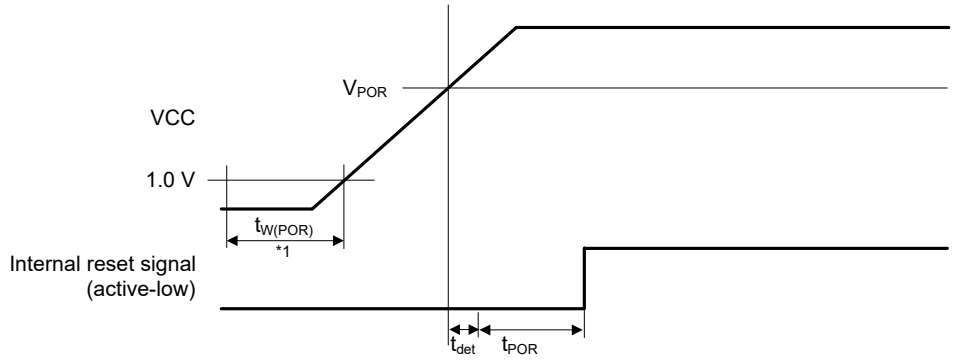



**Figure 2.73 Voltage detection reset timing**




Note: $t_{W(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{W(POR)}$ for 1.0 ms or more.

**Figure 2.74 Power-on reset timing**

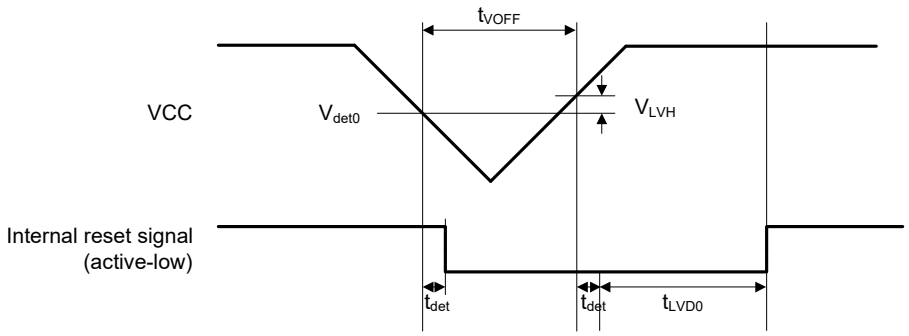



**Figure 2.75 Voltage detection circuit timing ($V_{det0}$)**

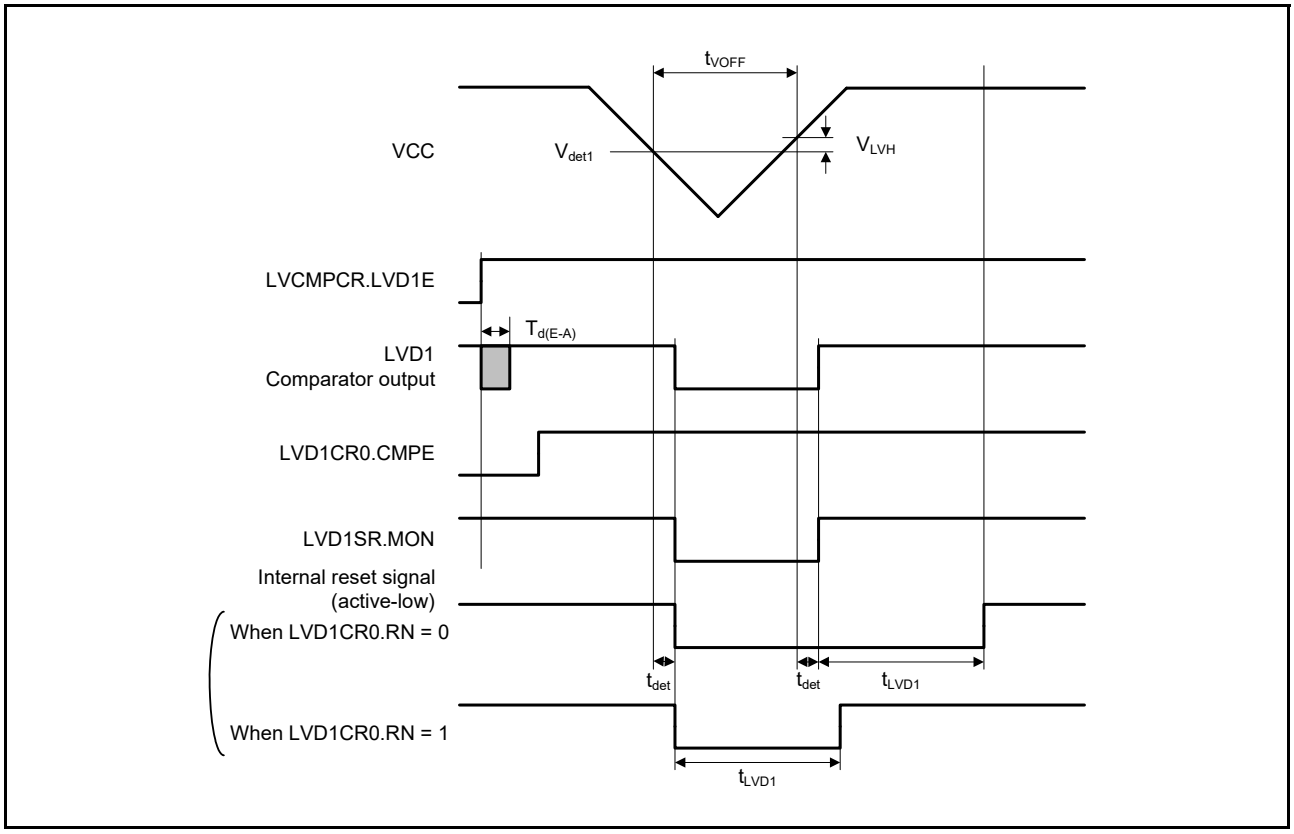



**Figure 2.76 Voltage detection circuit timing ($V_{det1}$)**

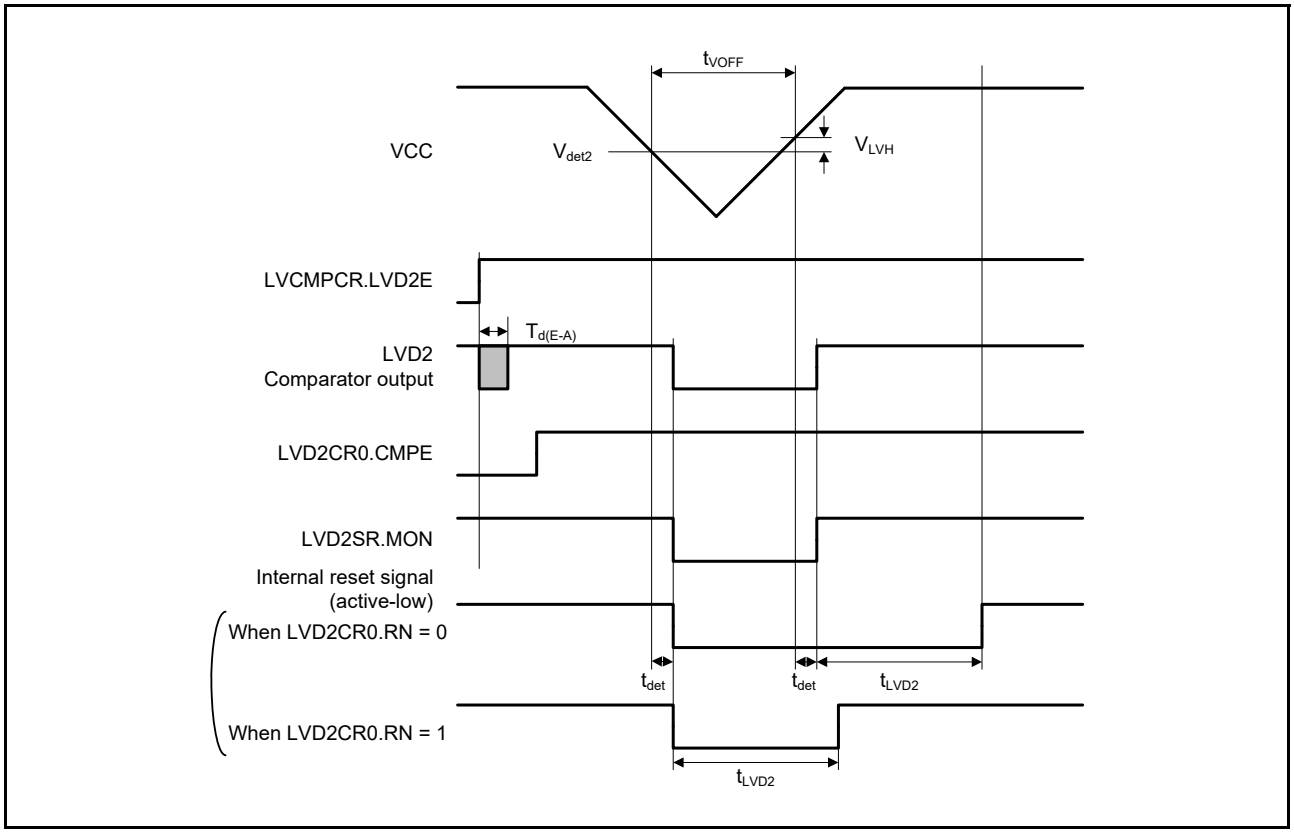



**Figure 2.77 Voltage detection circuit timing ($V_{det2}$)**

## 2.10 VBATT Characteristics

**Table 2.58 Battery backup function characteristics**

Conditions: VCC = AVCC0 = 1.6V to 5.5V, VBATT = 1.6 to 3.6 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Voltage level for switching to battery backup (falling) | | $V_{DETBATT}$ | 1.99 | 2.09 | 2.19 | V | Figure 2.78, Figure 2.79 |
| Hysteresis width for switching to battery back up | | $V_{VBATTH}$ | - | 100 | - | mV | |
| VCC-off period for starting power supply switching | | $t_{VOFFBATT}$ | 300 | - | - | μs | - |
| Voltage detection level VBATT_Power-on reset (VBATT_POR) | | $V_{VBATPOR}$ | 1.30 | 1.40 | 1.50 | V | Figure 2.78, Figure 2.79 |
| Wait time after VBATT_POR reset time cancellation | | $t_{VBATPOR}$ | - | - | 3 | mS | - |
| Level for detection of voltage drop on the VBATT pin (falling) | VBTLVDLVL[1:0] = 10b | $V_{DETBATLVD}$ | 2.11 | 2.2 | 2.29 | V | Figure 2.80 |
| | VBTLVDLVL[1:0] = 11b | | 1.92 | 2 | 2.08 | V | |
| Hysteresis width for VBATT pin LVD | | $V_{VBATLVDTH}$ | - | 50 | - | mV | |
| VBATT pin LVD operation stabilization time | | $t_{d_vbat}$ | - | - | 300 | μs | Figure 2.80 |
| VBATT pin LVD response delay time | | $t_{det_vbat}$ | - | - | 350 | μs | |
| Allowable voltage change rising/falling gradient | | dt/dVCC | 1.0 | - | - | ms/V | - |
| VCC voltage level for access to the VBATT backup registers | | $V_{_BKBATT}$ | 1.8 | - | - | V | - |

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

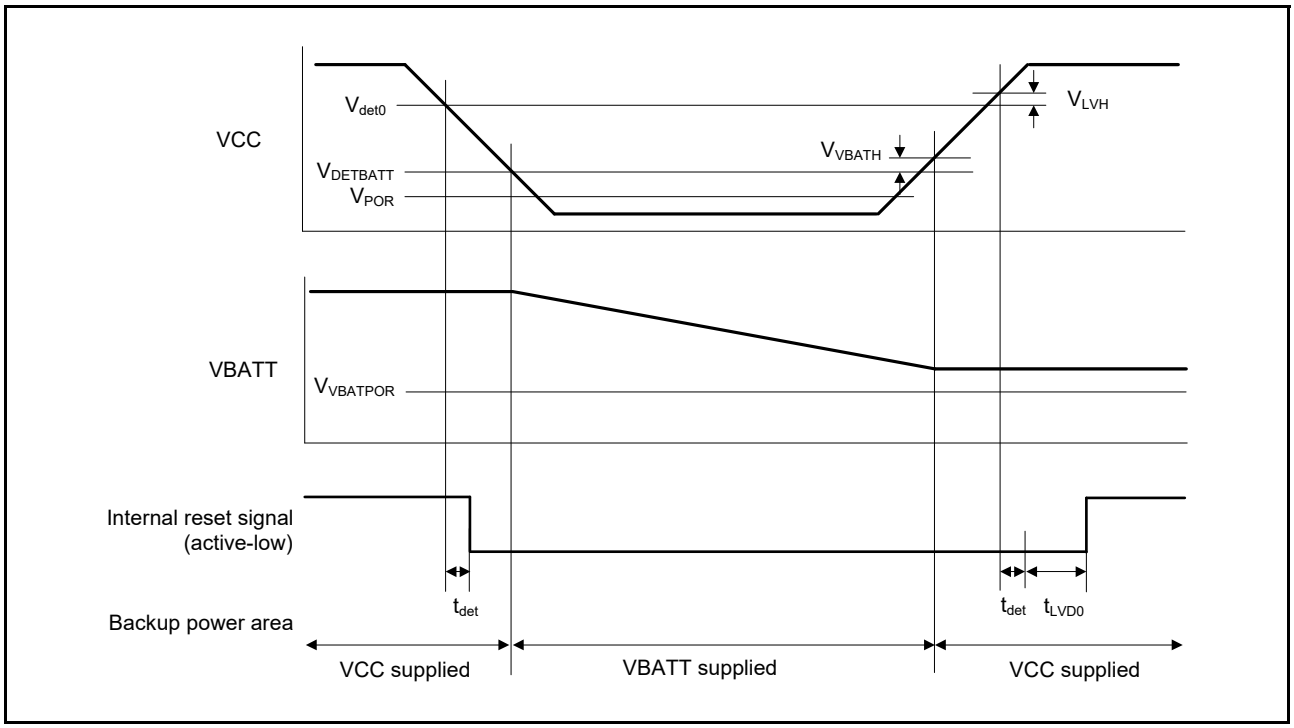



**Figure 2.78 Power supply switching and LVD0 reset timing**

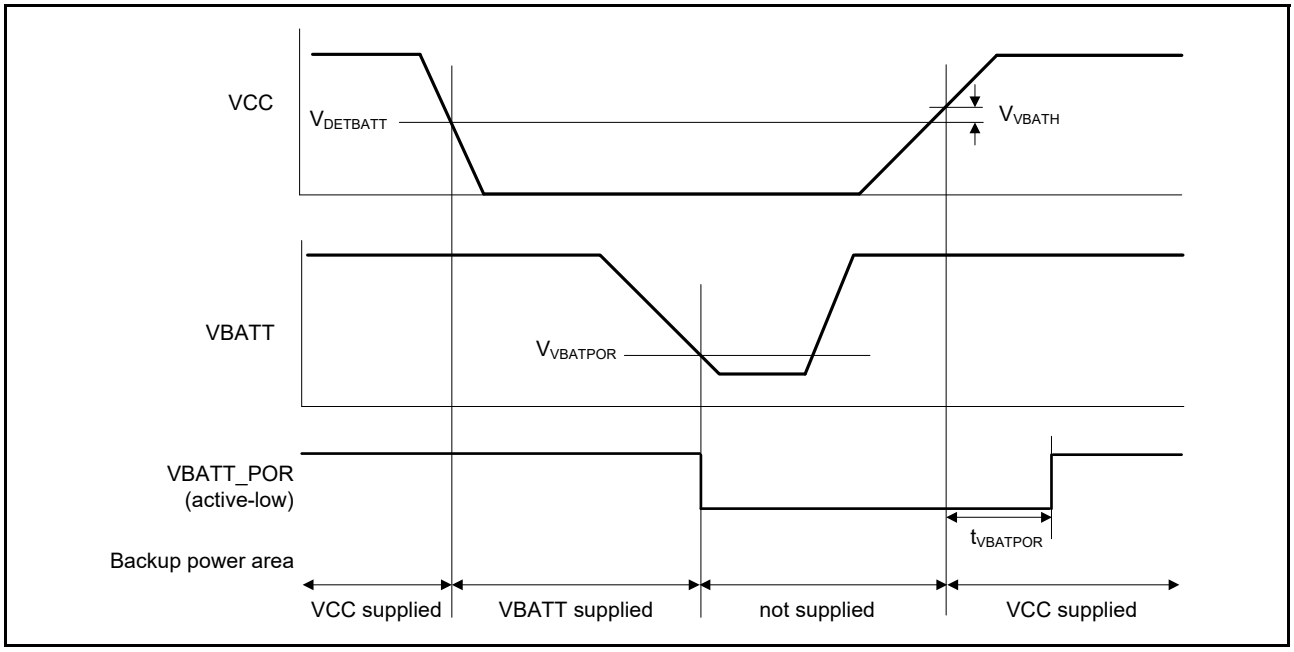



**Figure 2.79 VBATT_POR reset timing**

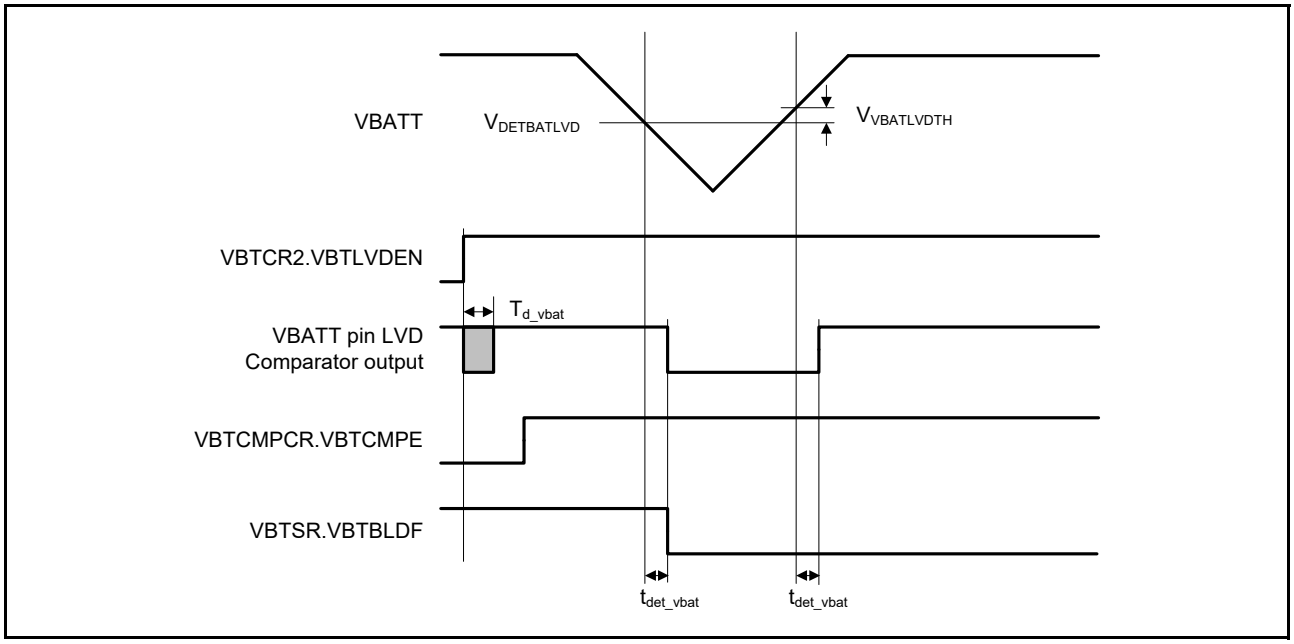



**Figure 2.80 VBATT pin voltage detection circuit timing**

**Table 2.59 VBATT-I/O characteristics**

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| VBATWIOn I/O output characteristics (n = 0 to 2) | VCC > $V_{DETBATT}$ | VCC = 4.0 to 5.5 V | $V_{OH}$ | VCC - 0.8 | - | - | V | $I_{OH}$ = -200 μA |
| | | | $V_{OL}$ | - | - | 0.8 | | $I_{OL}$ = 200 μA |
| | | VCC = 2.7 to 4.0 V | $V_{OH}$ | VCC - 0.5 | - | - | | $I_{OH}$ = -100 μA |
| | | | $V_{OL}$ | - | - | 0.5 | | $I_{OL}$ = 100 μA |
| | | VCC = $V_{DETBATT}$ to 2.7 V | $V_{OH}$ | VCC - 0.3 | - | - | | $I_{OH}$ = -50 μA |
| | | | $V_{OL}$ | - | - | 0.3 | | $I_{OL}$ = 50 μA |
| | VCC < $V_{DETBATT}$ | VBATT = 2.7 to 3.6 V | $V_{OH}$ | $V_{BATT}$ - 0.5 | - | - | | $I_{OH}$ = -100 μA |
| | | | $V_{OL}$ | - | - | 0.5 | | $I_{OL}$ = 100 μA |
| | | VBATT = 1.6 to 2.7 V | $V_{OH}$ | $V_{BATT}$ - 0.3 | - | - | | $I_{OH}$ = -50 μA |
| | | | $V_{OL}$ | - | - | 0.3 | | $I_{OL}$ = 50 μA |

## 2.11 CTSU Characteristics

**Table 2.60 CTSU characteristics**

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| External capacitance connected to TSCAP pin | $C_{tscap}$ | 9 | 10 | 11 | nF | - |
| TS pin capacitive load | $C_{base}$ | - | - | 50 | pF | - |
| Permissible output high current | ΣIoH | - | - | -24 | mA | When the mutual capacitance method is applied |

## 2.12 Segment LCD Controller Characteristics

### 2.12.1 Resistance Division Method

[Static Display Mode]

**Table 2.61 Resistance division method LCD characteristics (1)**

Conditions: VL4 ≤ VCC ≤ 5.5 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| LCD drive voltage | $V_{L4}$ | 2.0 | - | VCC | V | - |

[1/2 Bias Method, 1/4 Bias Method]

**Table 2.62 Resistance division method LCD characteristics (2)**

Conditions: VL4 ≤ VCC ≤ 5.5 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| LCD drive voltage | $V_{L4}$ | 2.7 | - | VCC | V | - |

[1/3 Bias Method]

**Table 2.63 Resistance division method LCD characteristics (3)**

Conditions: VL4 ≤ VCC ≤ 5.5 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| LCD drive voltage | $V_{L4}$ | 2.5 | - | VCC | V | - |

### 2.12.2 Internal Voltage Boosting Method

[1/3 Bias Method]

**Table 2.64 Internal voltage boosting method LCD characteristics**

Conditions: VCC = 1.8 V to 5.5 V

| Parameter | Symbol | Conditions | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| LCD output voltage variation range | $V_{L1}$ | C1 to C4*1 = 0.47 μF | VLCD = 04h | 0.90 | 1.0 | 1.08 | V | - |
| | | | VLCD = 05h | 0.95 | 1.05 | 1.13 | V | - |
| | | | VLCD = 06h | 1.00 | 1.10 | 1.18 | V | - |
| | | | VLCD = 07h | 1.05 | 1.15 | 1.23 | V | - |
| | | | VLCD = 08h | 1.10 | 1.20 | 1.28 | V | - |
| | | | VLCD = 09h | 1.15 | 1.25 | 1.33 | V | - |
| | | | VLCD = 0Ah | 1.20 | 1.30 | 1.38 | V | - |
| | | | VLCD = 0Bh | 1.25 | 1.35 | 1.43 | V | - |
| | | | VLCD = 0Ch | 1.30 | 1.40 | 1.48 | V | - |
| | | | VLCD = 0Dh | 1.35 | 1.45 | 1.53 | V | - |
| | | | VLCD = 0Eh | 1.40 | 1.50 | 1.58 | V | - |
| | | | VLCD = 0Fh | 1.45 | 1.55 | 1.63 | V | - |
| | | | VLCD = 10h | 1.50 | 1.60 | 1.68 | V | - |
| | | | VLCD = 11h | 1.55 | 1.65 | 1.73 | V | - |
| | | | VLCD = 12h | 1.60 | 1.70 | 1.78 | V | - |
| | | | VLCD = 13h | 1.65 | 1.75 | 1.83 | V | - |
| Doubler output voltage | $V_{L2}$ | C1 to C4*1 = 0.47 μF | | $2 \times V_{L1} - 0.1$ | $2 \times V_{L1}$ | $2 \times V_{L1}$ | V | - |
| Tripler output voltage | $V_{L4}$ | C1 to C4*1 = 0.47 μF | | $3 \times V_{L1} - 0.15$ | $3 \times V_{L1}$ | $3 \times V_{L1}$ | V | - |
| Reference voltage setup time*2 | $t_{VL1S}$ | | | 5 | - | - | ms | Figure 2.81 |
| LCD output voltage variation range*3 | $t_{VLWT}$ | C1 to C4*1 = 0.47 μF | | 500 | - | - | ms | |

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between VL1 and GND
C3: A capacitor connected between VL2 and GND
C4: A capacitor connected between VL4 and GND
C1 = C2 = C3 = C4 = 0.47 μF ±30%.

Note 2. This is the time required to wait from when the reference voltage is specified using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET[1:0] bits in the LCDM0 register to 01b) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

[1/4 Bias Method]

**Table 2.65 Internal voltage boosting method LCD characteristics**

Conditions: VCC = 1.8 V to 5.5 V

| Parameter | Symbol | Conditions | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| LCD output voltage variation range | $V_{L1}$ | C1 to C5*1 = 0.47 μF | VLCD = 04h | 0.90 | 1.0 | 1.08 | V | - |
| | | | VLCD = 05h | 0.95 | 1.05 | 1.13 | V | - |
| | | | VLCD = 06h | 1.00 | 1.10 | 1.18 | V | - |
| | | | VLCD = 07h | 1.05 | 1.15 | 1.23 | V | - |
| | | | VLCD = 08h | 1.10 | 1.20 | 1.28 | V | - |
| | | | VLCD = 09h | 1.15 | 1.25 | 1.33 | V | - |
| | | | VLCD = 0Ah | 1.20 | 1.30 | 1.38 | V | - |
| | | | VLCD = 0Bh | 1.25 | 1.35 | 1.43 | V | - |
| | | | VLCD = 0Ch | 1.30 | 1.40 | 1.48 | V | - |
| Doubler output voltage | $V_{L2}$ | C1 to C5*1 = 0.47 μF | | $2V_{L1}$ - 0.08 | $2V_{L1}$ | $2V_{L1}$ | V | - |
| Tripler output voltage | $V_{L3}$ | C1 to C5*1 = 0.47 μF | | $3V_{L1}$ - 0.12 | $3V_{L1}$ | $3V_{L1}$ | V | - |
| Quadruply output voltage | $V_{L4}$*4 | C1 to C5*1 = 0.47 μF | | $4V_{L1}$ - 0.16 | $4V_{L1}$ | $4V_{L1}$ | V | - |
| Reference voltage setup time*2 | $t_{VL1S}$ | | | 5 | - | - | ms | Figure 2.81 |
| LCD output voltage variation range*3 | $t_{VLWT}$ | C1 to C5*1 = 0.47 μF | | 500 | - | - | ms | |

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between $V_{L1}$ and GND
C3: A capacitor connected between $V_{L2}$ and GND
C4: A capacitor connected between $V_{L3}$ and GND
C5: A capacitor connected between $V_{L4}$ and GND
C1 = C2 = C3 = C4 = C5 = 0.47 μF ± 30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits in the LCDM0 register to 01b) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 4. $V_{L4}$ must be 5.5 V or lower.

### 2.12.3 Capacitor Split Method

[1/3 Bias Method]

**Table 2.66 Internal voltage boosting method LCD characteristics**

Conditions: VCC = 2.2 V to 5.5 V

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| VL4 voltage*1 | $V_{L4}$ | C1 to C4 = 0.47 μF*2 | - | VCC | - | V | - |
| VL2 voltage*1 | $V_{L2}$ | C1 to C4 = 0.47 μF*2 | 2/3 × $V_{L4}$ - 0.07 | 2/3 × $V_{L4}$ | 2/3 × $V_{L4}$ + 0.07 | V | - |
| VL1 voltage*1 | $V_{L1}$ | C1 to C4 = 0.47 μF*2 | 1/3 × $V_{L4}$ - 0.08 | 1/3 × $V_{L4}$ | 1/3 × $V_{L4}$ + 0.08 | V | - |
| Capacitor split wait time*1 | $t_{WAIT}$ | | 100 | - | - | ms | Figure 2.81 |

Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 2. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between $V_{L1}$ and GND
C3: A capacitor connected between $V_{L2}$ and GND
C4: A capacitor connected between $V_{L4}$ and GND
C1 = C2 = C3 = C4 = 0.47 μF ± 30%.

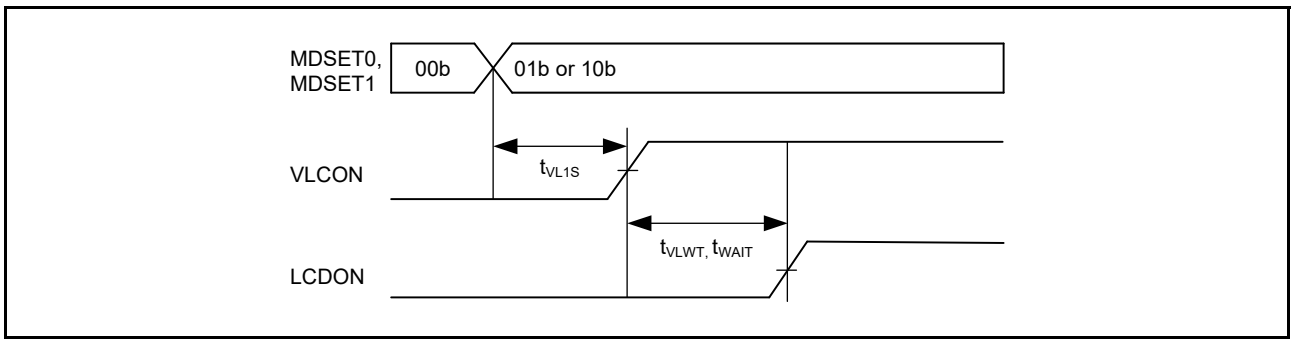



**Figure 2.81 LCD reference voltage setup time, voltage boosting wait time, and capacitor split wait time**

## 2.13 Comparator Characteristics

**Table 2.67 ACMPLP characteristics**

Conditions: VCC = 1.8 to 5.5 V

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| Reference voltage range | Standard mode | IVREFn (n= 0,1) | VREF | 0 | - | VCC-1.4 | V | - |
| | Window mode*2 | IVREF1 | VREFH | 1.4 | - | VCC | V | - |
| | | IVREF0 | VREFL | 0 | - | VCC-1.4 | V | - |
| Input voltage range | | | VI | 0 | - | VCC | V | - |
| Internal reference voltage | | | - | 1.36 | 1.44 | 1.50 | V | - |
| Output delay | High-speed mode | | Td | - | - | 1.2 | μs | VCC = 3.0<br>Slew rate of input signal > 50 mV/μs |
| | Low-speed mode | | | - | - | 5 | μs | |
| | Window mode | | | - | - | 2 | μs | |
| Offset voltage*1 | High-speed mode | | - | - | - | 50 | mV | - |
| | Low-speed mode | | - | - | - | 40 | mV | - |
| | Window mode | | - | - | - | 60 | mV | - |
| Operation stabilization wait time | | | $T_{cmp}$ | 100 | - | - | μs | - |

Note 1. When 8-bit DAC output is used as the reference voltage, the offset voltage increases up to 2.5 x VCC/256.

Note 2. In window mode, be sure to satisfy the following condition: IVREF1 - IVREF0 ≥ 0.2 V.

## 2.14 OPAMP Characteristics

**Table 2.68 OPAMP characteristics**

Conditions: VCC = AVCC0 = 1.8 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V)

| Parameter | Symbol | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Common mode input range | Vicm1 | Low power mode | | 0.2 | - | AVCC0 - 0.5 | V |
| | Vicm2 | High-speed mode | | 0.3 | - | AVCC0 - 0.6 | V |
| Output voltage range | Vo1 | Low power mode | | 0.1 | - | AVCC0 - 0.1 | V |
| | Vo2 | High-speed mode | | 0.1 | - | AVCC0 - 0.1 | V |
| Input offset voltage | Vioff | 3σ | | -10 | - | 10 | mV |
| Open gain | Av | | | 60 | 120 | - | dB |
| Gain-bandwidth (GB) product | GBW1 | Low power mode | | - | 0.04 | - | MHz |
| | GBW2 | High-speed mode | | - | 1.7 | - | MHz |
| Phase margin | PM | CL = 20 pF | | 50 | - | - | deg |
| Gain margin | GM | CL = 20 pF | | 10 | - | - | dB |
| Equivalent input noise | Vnoise1 | f = 1 kHz | Low power mode | - | 230 | - | nV/√Hz |
| | Vnoise2 | f = 10 kHz | | - | 200 | - | nV/√Hz |
| | Vnoise3 | f = 1 kHz | High-speed mode | - | 90 | - | nV/√Hz |
| | Vnoise4 | f = 2 kHz | | - | 70 | - | nV/√Hz |
| Power supply reduction ratio | PSRR | | | - | 90 | - | dB |
| Common mode signal reduction ratio | CMRR | | | - | 90 | - | dB |
| Stabilization wait time | Tstd1 | CL = 20 pF<br>Only operational amplifier is activated *1 | Low power mode | 650 | - | - | μs |
| | Tstd2 | | High-speed mode | 13 | - | - | μs |
| | Tstd3 | CL = 20 pF<br>Operational amplifier and reference current circuit are activated simultaneously | Low power mode | 650 | - | - | μs |
| | Tstd4 | | High-speed mode | 13 | - | - | μs |
| Settling time | Tset1 | CL = 20 pF | Low power mode | - | - | 750 | μs |
| | Tset2 | | High-speed mode | - | - | 13 | μs |
| Slew rate | Tslew1 | CL = 20 pF | Low power mode | - | 0.02 | - | V/μs |
| | Tslew2 | | High-speed mode | - | 1.1 | - | V/μs |
| Load current | Iload1 | Low-power mode | | -100 | - | 100 | μA |
| | Iload2 | High-speed mode | | -100 | - | 100 | μA |
| Load capacitance | CL | | | - | - | 20 | pF |

Note 1. When the operational amplifier reference current circuit is activated in advance.

## 2.15 Flash Memory Characteristics

### 2.15.1 Code Flash Memory Characteristics

**Table 2.69 Code flash characteristics (1)**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Reprogramming/erasure cycle*1 | | $N_{PEC}$ | 1000 | - | - | Times | - |
| Data hold time | After 1000 times of $N_{PEC}$ | $t_{DRP}$ | 20*2, *3 | - | - | Year | $T_a$ = +85°C |

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be done n times for each block. For instance, when 8-byte programming is performed 256 times for different addresses in 2-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. This result is obtained from reliability testing.

**Table 2.70 Code flash characteristics (2)**
High-speed operating mode
Conditions: VCC = 2.7 to 5.5 V

| Parameter | | Symbol | FCLK = 1 MHz | | | FCLK = 32 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Programming time | 8-byte | $t_{P8}$ | - | 116 | 998 | - | 54 | 506 | μs |
| Erasure time | 2-KB | $t_{E2K}$ | - | 9.03 | 287 | - | 5.67 | 222 | ms |
| Blank check time | 8-byte | $t_{BC8}$ | - | - | 56.8 | - | - | 16.6 | μs |
| | 2-KB | $t_{BC2K}$ | - | - | 1899 | - | - | 140 | μs |
| Erase suspended time | | $t_{SED}$ | - | - | 22.5 | - | - | 10.7 | μs |
| Startup area switching setting time | | $t_{SAS}$ | - | 21.7 | 585 | - | 12.1 | 447 | ms |
| Access window time | | $t_{AWS}$ | - | 21.7 | 585 | - | 12.1 | 447 | ms |
| OCD/serial programmer ID setting time | | $t_{OSIS}$ | - | 21.7 | 585 | - | 12.1 | 447 | ms |
| Flash memory mode transition wait time 1 | | $t_{DIS}$ | 2 | - | - | 2 | - | - | μs |
| Flash memory mode transition wait time 2 | | $t_{MS}$ | 5 | - | - | 5 | - | - | μs |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

**Table 2.71 Code flash characteristics (3)**

Middle-speed operating mode

Conditions: VCC = 1.8 to 5.5 V, $T_a$ = -40 to +85°C

| Parameter | | Symbol | FCLK = 1 MHz | | | FCLK = 8 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Programming time | 8-byte | $t_{P8}$ | - | 157 | 1411 | - | 101 | 966 | μs |
| Erasure time | 2-KB | $t_{E2K}$ | - | 9.10 | 289 | - | 6.10 | 228 | ms |
| Blank check time | 8-byte | $t_{BC8}$ | - | - | 87.7 | - | - | 52.5 | μs |
| | 2-KB | $t_{BC2K}$ | - | - | 1930 | - | - | 414 | μs |
| Erase suspended time | | $t_{SED}$ | - | - | 32.7 | - | - | 21.6 | μs |
| Startup area switching setting time | | $t_{SAS}$ | - | 22.5 | 592 | - | 14.0 | 464 | ms |
| Access window time | | $t_{AWS}$ | - | 22.5 | 592 | - | 14.0 | 464 | ms |
| OCD/serial programmer ID setting time | | $t_{OSIS}$ | - | 22.5 | 592 | - | 14.0 | 464 | ms |
| Flash memory mode transition wait time 1 | | $t_{DIS}$ | 2 | - | - | 2 | - | - | μs |
| Flash memory mode transition wait time 2 | | $t_{MS}$ | 720 | - | - | 720 | - | - | ns |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

## 2.15.2 Data Flash Memory Characteristics

**Table 2.72 Data flash characteristics (1)**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Reprogramming/erasure cycle*1 | | $N_{DPEC}$ | 100,000 | 1,000,000 | - | Times | - |
| Data hold time | After 10,000 times of $N_{DPEC}$ | $t_{DDRP}$ | 20*2, *3 | - | - | Year | $T_a$ = +85°C |
| | After 100,000 times of $N_{DPEC}$ | | 5*2, *3 | - | - | Year | |
| | After 1,000,000 times of $N_{DPEC}$ | | - | 1*2, *3 | - | Year | $T_a$ = +25°C |

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,000 times for different addresses in 1-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. Overwriting is prohibited.

Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. These results are obtained from reliability testing.

**Table 2.73 Data flash characteristics (2)**

High-speed operating mode

Conditions: VCC = 2.7 to 5.5 V

| Parameter | | Symbol | FCLK = 4 MHz | | | FCLK = 32 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Programming time | 1-byte | $t_{DP1}$ | - | 52.4 | 463 | - | 42.1 | 387 | μs |
| Erasure time | 1-KB | $t_{DE1K}$ | - | 8.98 | 286 | - | 6.42 | 237 | ms |
| Blank check time | 1-byte | $t_{DBC1}$ | - | - | 24.3 | - | - | 16.6 | μs |
| | 1-KB | $t_{DBC1K}$ | - | - | 1872 | - | - | 512 | μs |
| Suspended time during erasing | | $t_{DSED}$ | - | - | 13.0 | - | - | 10.7 | μs |
| Data flash STOP recovery time | | $t_{DSTOP}$ | 5 | - | - | 5 | - | - | μs |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

**Table 2.74 Data flash characteristics (3)**
Middle-speed operating mode
Conditions: VCC = 1.8 to 5.5 V, $T_a$ = -40 to +85°C

| Parameter | | Symbol | FCLK = 4 MHz | | | FCLK = 8 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Programming time | 1-byte | $t_{DP1}$ | - | 94.7 | 886 | - | 89.3 | 849 | μs |
| Erasure time | 1-KB | $t_{DE1K}$ | - | 9.59 | 299 | - | 8.29 | 273 | ms |
| Blank check time | 1-byte | $t_{DBC1}$ | - | - | 56.2 | - | - | 52.5 | μs |
| | 1-KB | $t_{DBC1K}$ | - | - | 2.17 | - | - | 1.51 | ms |
| Suspended time during erasing | | $t_{DSED}$ | - | - | 23.0 | - | - | 21.7 | μs |
| Data flash STOP recovery time | | $t_{DSTOP}$ | 720 | - | - | 720 | - | - | ns |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

## 2.16 Boundary Scan

**Table 2.75 Boundary scan**
Conditions: VCC = AVCC0 = 2.4 to 5.5 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| TCK clock cycle time | $t_{TCKcyc}$ | 100 | - | - | ns | Figure 2.82 |
| TCK clock high pulse width | $t_{TCKH}$ | 45 | - | - | ns | |
| TCK clock low pulse width | $t_{TCKL}$ | 45 | - | - | ns | |
| TCK clock rise time | $t_{TCKr}$ | - | - | 5 | ns | |
| TCK clock fall time | $t_{TCKf}$ | - | - | 5 | ns | |
| TMS setup time | $t_{TMSS}$ | 20 | - | - | ns | Figure 2.83 |
| TMS hold time | $t_{TMSH}$ | 20 | - | - | ns | |
| TDI setup time | $t_{TDIS}$ | 20 | - | - | ns | |
| TDI hold time | $t_{TDIH}$ | 20 | - | - | ns | |
| TDO data delay | $t_{TDOD}$ | - | - | 70 | ns | |
| Boundary Scan circuit start up time*1 | $t_{BSSTUP}$ | $t_{RESWP}$ | - | - | - | Figure 2.84 |

Note 1. Boundary scan does not function until power-on-reset becomes negative.

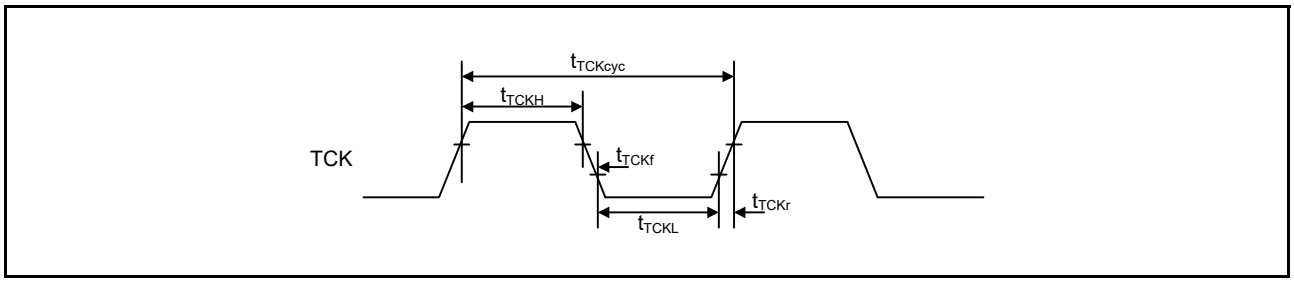



**Figure 2.82 Boundary scan TCK timing**

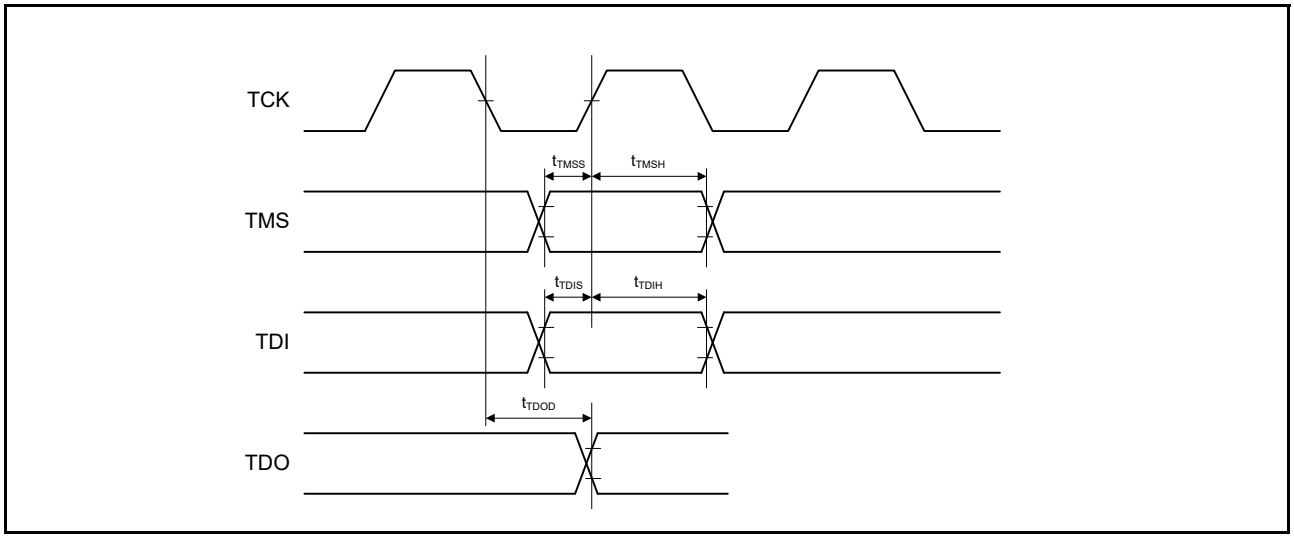



**Figure 2.83 Boundary scan input/output timing**

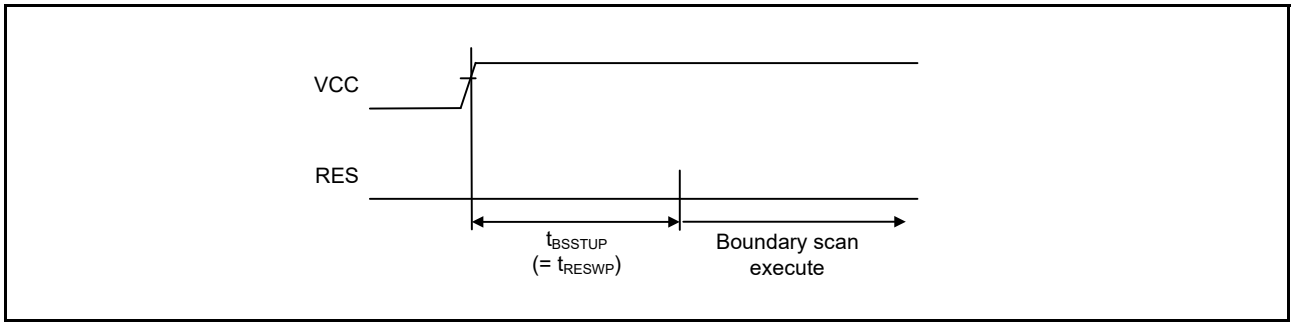



**Figure 2.84 Boundary scan circuit start up timing**

## 2.17 Joint Test Action Group (JTAG)

**Table 2.76 JTAG (debug) characteristics (1)**

Conditions: VCC = 2.4 to 5.5 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| TCK clock cycle time | $t_{TCKcyc}$ | 80 | - | - | ns | Figure 2.85 |
| TCK clock high pulse width | $t_{TCKH}$ | 35 | - | - | ns | |
| TCK clock low pulse width | $t_{TCKL}$ | 35 | - | - | ns | |
| TCK clock rise time | $t_{TCKr}$ | - | - | 5 | ns | |
| TCK clock fall time | $t_{TCKf}$ | - | - | 5 | ns | |
| TMS setup time | $t_{TMSS}$ | 16 | - | - | ns | Figure 2.86 |
| TMS hold time | $t_{TMSH}$ | 16 | - | - | ns | |
| TDI setup time | $t_{TDIS}$ | 16 | - | - | ns | |
| TDI hold time | $t_{TDIH}$ | 16 | - | - | ns | |
| TDO data delay time | $t_{TDOD}$ | - | - | 70 | ns | |

**Table 2.77 JTAG (debug) characteristics (2)**
Conditions: VCC = 1.6 to 2.4 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| TCK clock cycle time | $t_{TCKcyc}$ | 250 | - | - | ns | Figure 2.85 |
| TCK clock high pulse width | $t_{TCKH}$ | 120 | - | - | ns | |
| TCK clock low pulse width | $t_{TCKL}$ | 120 | - | - | ns | |
| TCK clock rise time | $t_{TCKr}$ | - | - | 5 | ns | |
| TCK clock fall time | $t_{TCKf}$ | - | - | 5 | ns | |
| TMS setup time | $t_{TMSS}$ | 50 | - | - | ns | Figure 2.86 |
| TMS hold time | $t_{TMSH}$ | 50 | - | - | ns | |
| TDI setup time | $t_{TDIS}$ | 50 | - | - | ns | |
| TDI hold time | $t_{TDIH}$ | 50 | - | - | ns | |
| TDO data delay time | $t_{TDOD}$ | - | - | 150 | ns | |

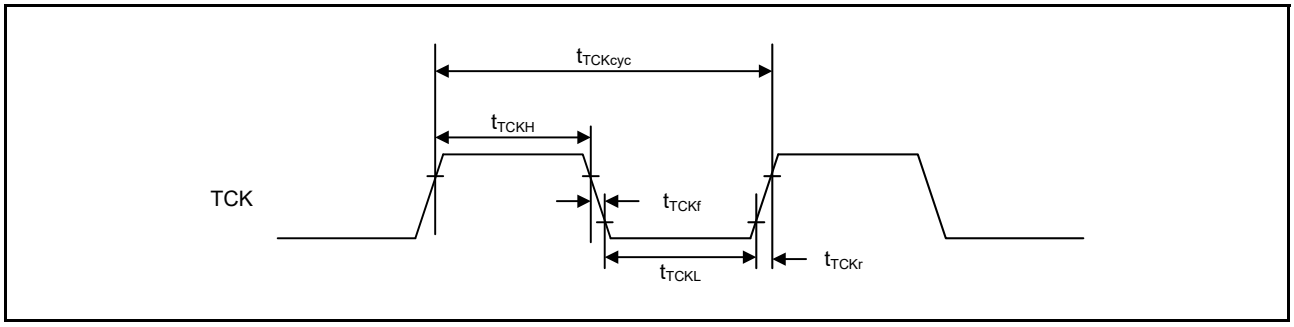



**Figure 2.85 JTAG TCK timing**

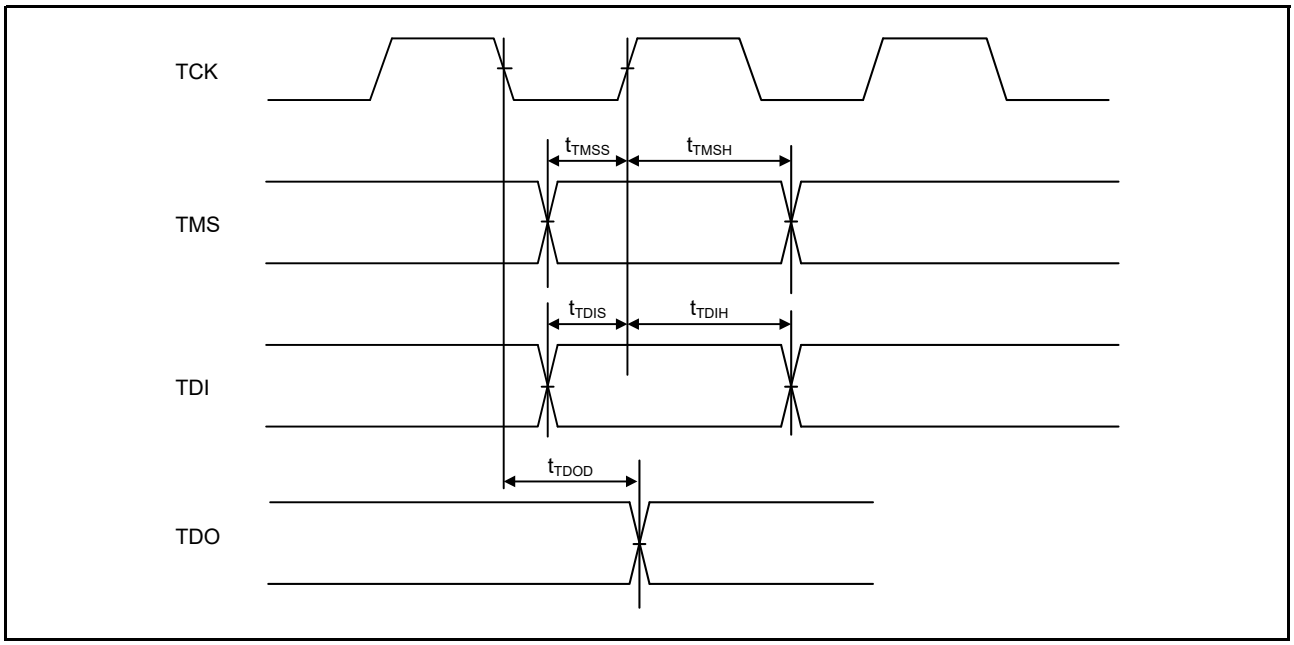



**Figure 2.86 JTAG input/output timing**

### 2.17.1 Serial Wire Debug (SWD)

**Table 2.78 SWD characteristics (1)**
Conditions: VCC = 2.4 to 5.5 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| SWCLK clock cycle time | $t_{SWCKcyc}$ | 80 | - | - | ns | Figure 2.87 |
| SWCLK clock high pulse width | $t_{SWCKH}$ | 35 | - | - | ns | |
| SWCLK clock low pulse width | $t_{SWCKL}$ | 35 | - | - | ns | |
| SWCLK clock rise time | $t_{SWCKr}$ | - | - | 5 | ns | |
| SWCLK clock fall time | $t_{SWCKf}$ | - | - | 5 | ns | |
| SWDIO setup time | $t_{SWDS}$ | 16 | - | - | ns | Figure 2.88 |
| SWDIO hold time | $t_{SWDH}$ | 16 | - | - | ns | |
| SWDIO data delay time | $t_{SWDD}$ | 2 | - | 70 | ns | |

**Table 2.79 SWD characteristics (2)**
Conditions: VCC = 1.6 to 2.4 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| SWCLK clock cycle time | $t_{SWCKcyc}$ | 250 | - | - | ns | Figure 2.87 |
| SWCLK clock high pulse width | $t_{SWCKH}$ | 120 | - | - | ns | |
| SWCLK clock low pulse width | $t_{SWCKL}$ | 120 | - | - | ns | |
| SWCLK clock rise time | $t_{SWCKr}$ | - | - | 5 | ns | |
| SWCLK clock fall time | $t_{SWCKf}$ | - | - | 5 | ns | |
| SWDIO setup time | $t_{SWDS}$ | 50 | - | - | ns | Figure 2.88 |
| SWDIO hold time | $t_{SWDH}$ | 50 | - | - | ns | |
| SWDIO data delay time | $t_{SWDD}$ | 2 | - | 150 | ns | |

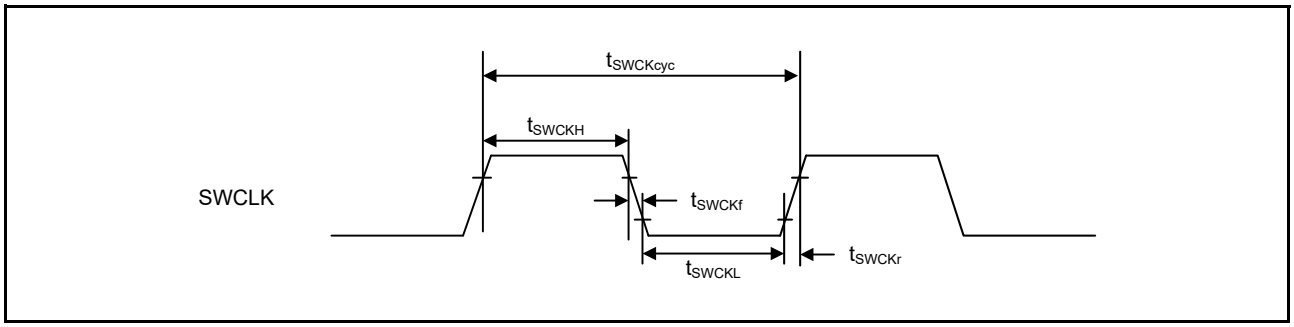



**Figure 2.87 SWD SWCLK timing**

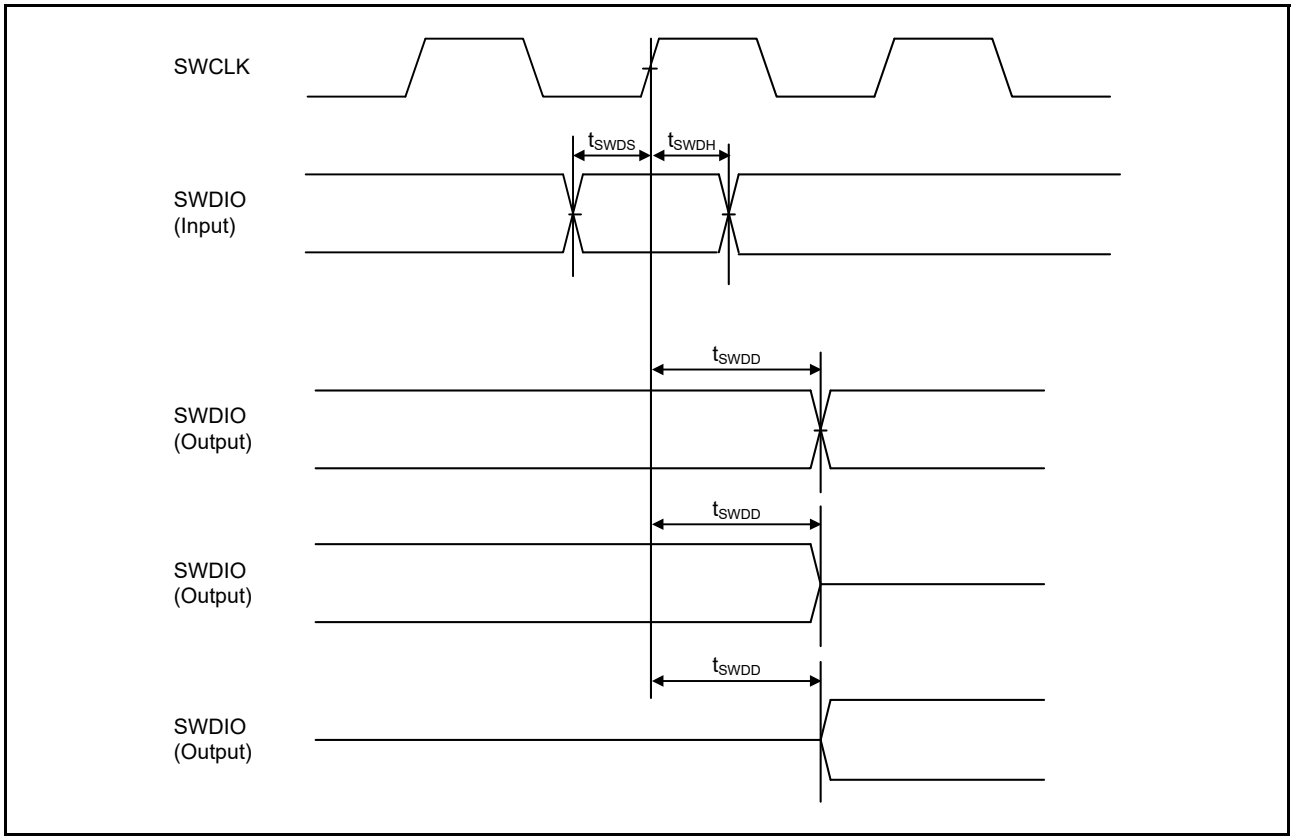
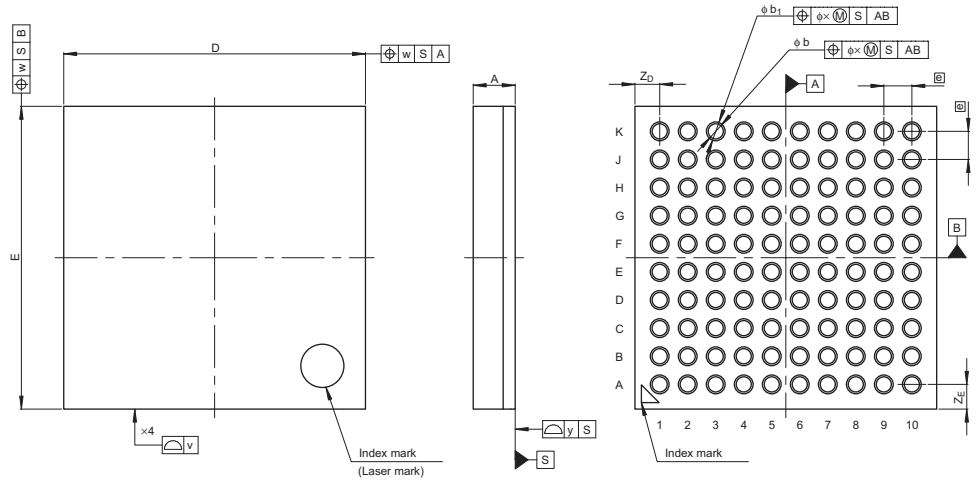



**Figure 2.88 SWD input/output timing**

# Appendix 1.Package Dimensions

Information on the latest version of the package dimensions or mountings is shown in “Packages” on the Renesas Electronics Corporation website.

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TFLGA100-7x7-0.65 | PTLG0100JA-A | 100F0G | 0.1g |

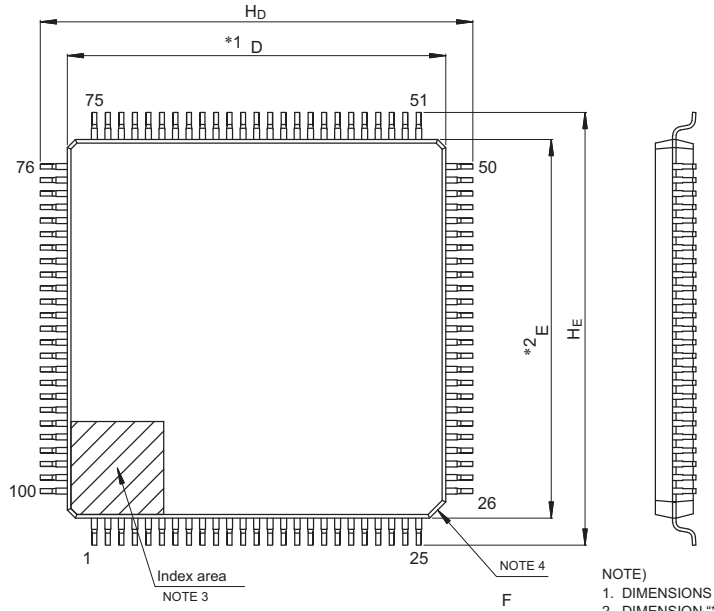



| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 7.0 | — |
| E | — | 7.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.05 |
| e | — | 0.65 | — |
| b | 0.31 | 0.35 | 0.39 |
| $b_1$ | 0.385 | 0.435 | 0.485 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.575 | — |
| $Z_E$ | — | 0.575 | — |

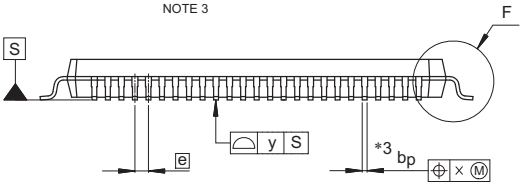
**Figure 1.1 100-pin LGA**

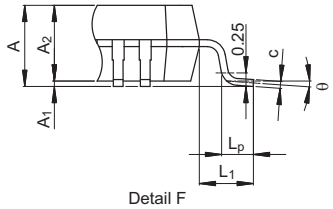
| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP100-14x14-0.50 | PLQP0100KB-B | — | 0.6 |

Unit: mm






NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

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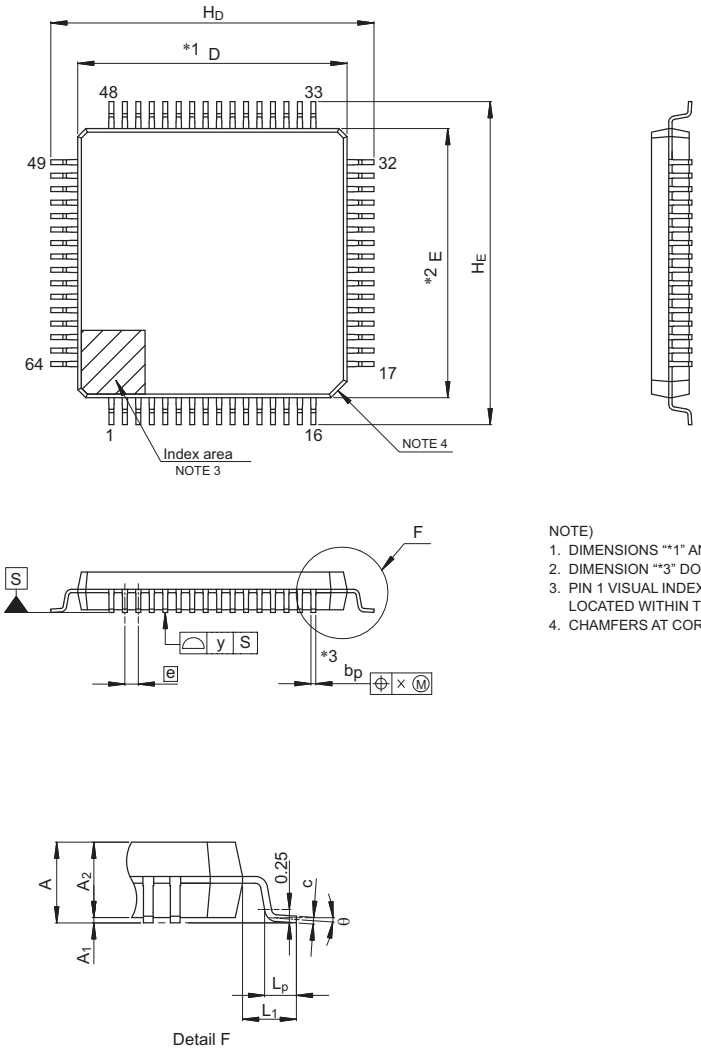
**Figure 1.2 100-pin LQFP**

| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP64-10x10-0.50 | PLQP0064KB-C | — | 0.3 |

Unit: mm




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 11.8 | 12.0 | 12.2 |
| $H_E$ | 11.8 | 12.0 | 12.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

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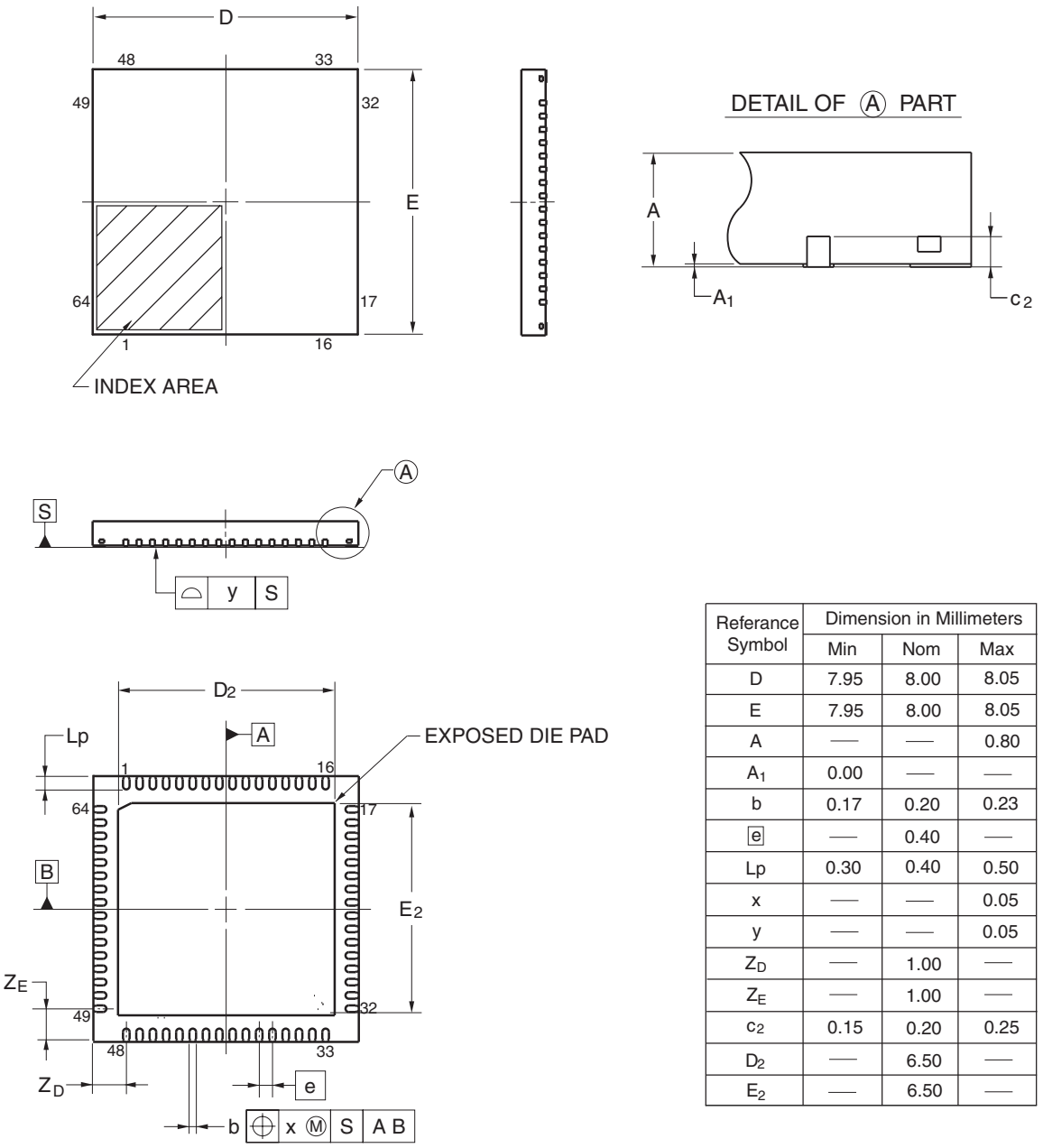
**Figure 1.3 64-pin LQFP**

| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|---|---|---|---|
| P-HWQFN64-8x8-0.40 | PWQN0064LA-A | P64K8-40-9B5-3 | 0.16 |




| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 7.95 | 8.00 | 8.05 |
| E | 7.95 | 8.00 | 8.05 |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | — | — |
| b | 0.17 | 0.20 | 0.23 |
| e | — | 0.40 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $Z_D$ | — | 1.00 | — |
| $Z_E$ | — | 1.00 | — |
| $c_2$ | 0.15 | 0.20 | 0.25 |
| $D_2$ | — | 6.50 | — |
| $E_2$ | — | 6.50 | — |

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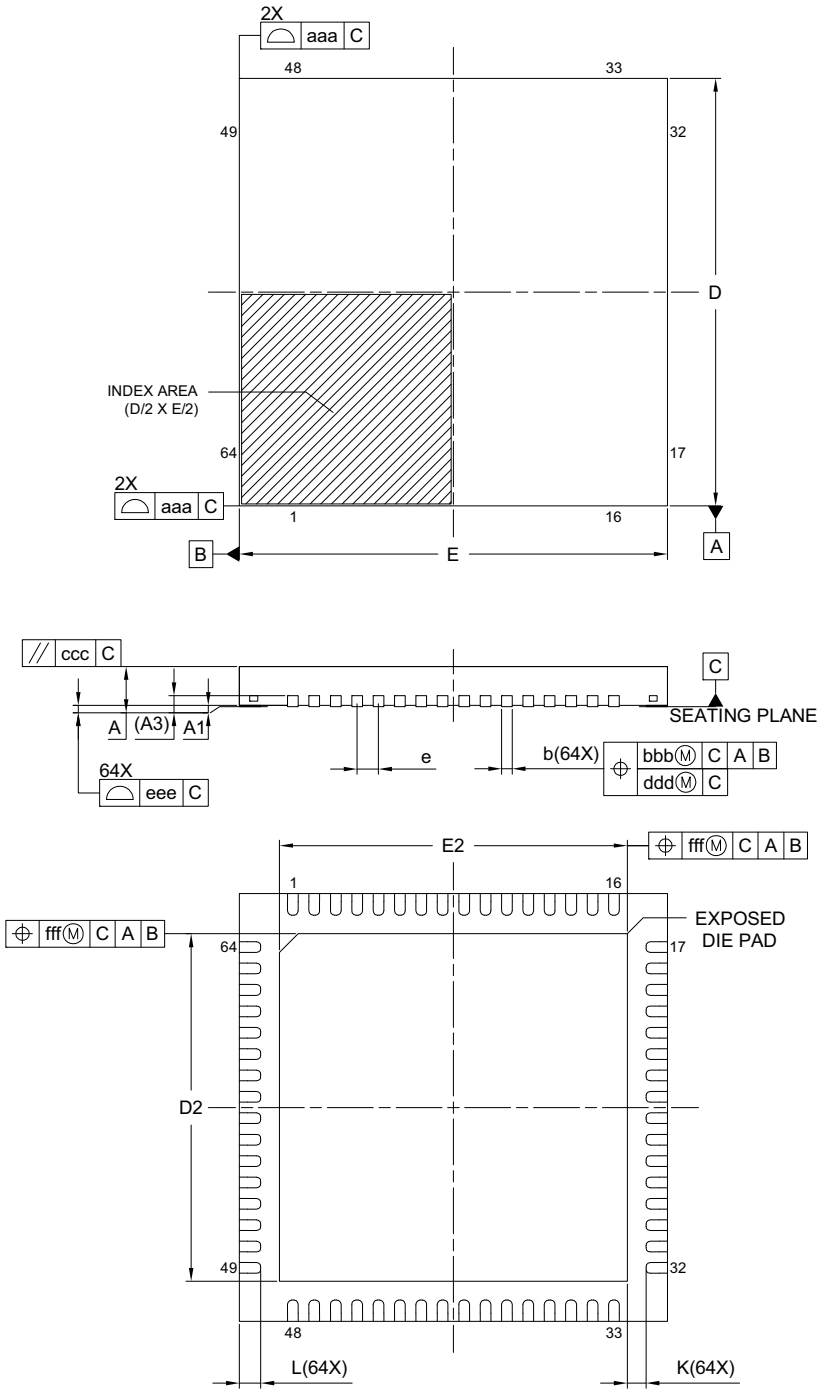
**Figure 1.4 64-pin QFN (1)**

| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
|---|---|---|
| P-HWQFN064-8x8-0.40 | PWQN0064LB-B | 0.14 |

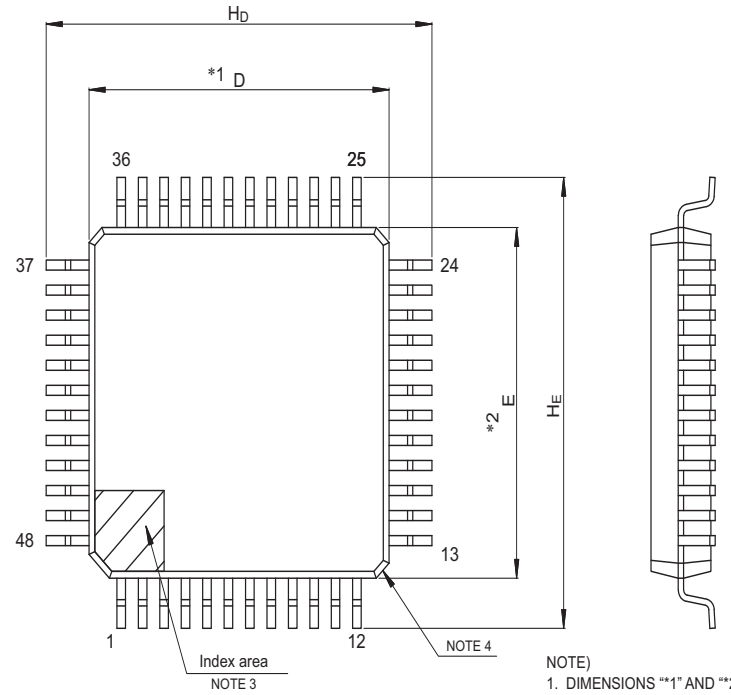



| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | 0.02 | 0.05 |
| $A_3$ | 0.203 REF. | | |
| b | 0.15 | 0.20 | 0.25 |
| D | 8.00 BSC | | |
| E | 8.00 BSC | | |
| e | 0.40 BSC | | |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.20 | — | — |
| $D_2$ | 6.40 | 6.50 | 6.60 |
| $E_2$ | 6.40 | 6.50 | 6.60 |
| aaa | 0.10 | | |
| bbb | 0.07 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

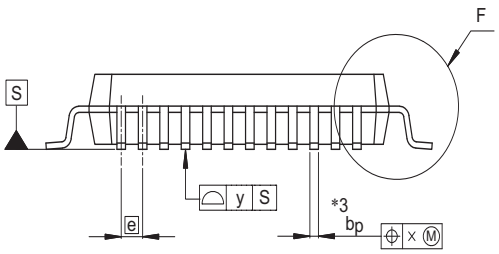
**Figure 1.5 64-pin QFN (2)**

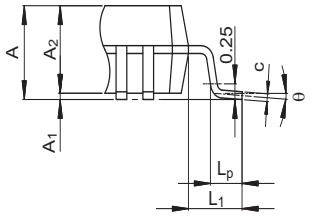
| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP48-7x7-0.50 | PLQP0048KB-B | — | 0.2 |

Unit: mm




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.



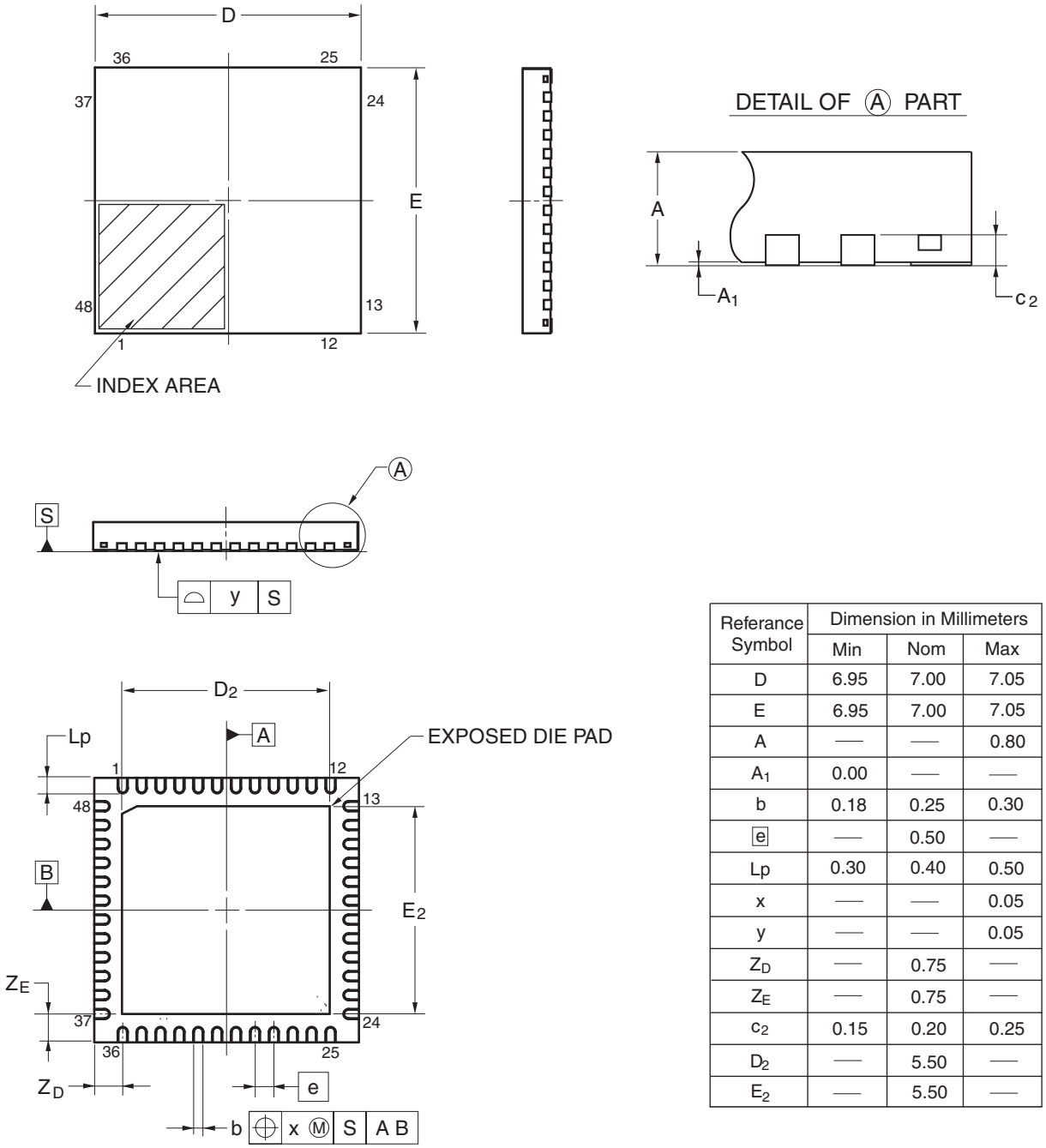




Detail F

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.9 | 7.0 | 7.1 |
| E | 6.9 | 7.0 | 7.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 8.8 | 9.0 | 9.2 |
| $H_E$ | 8.8 | 9.0 | 9.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.17 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

**Figure 1.6 48-pin LQFP**

| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|---|---|---|---|
| P-HWQFN48-7x7-0.50 | PWQN0048KB-A | 48PJN-A<br>P48K8-50-5B4-6 | 0.13 |




| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.95 | 7.00 | 7.05 |
| E | 6.95 | 7.00 | 7.05 |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | — | — |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $Z_D$ | — | 0.75 | — |
| $Z_E$ | — | 0.75 | — |
| $c_2$ | 0.15 | 0.20 | 0.25 |
| $D_2$ | — | 5.50 | — |
| $E_2$ | — | 5.50 | — |

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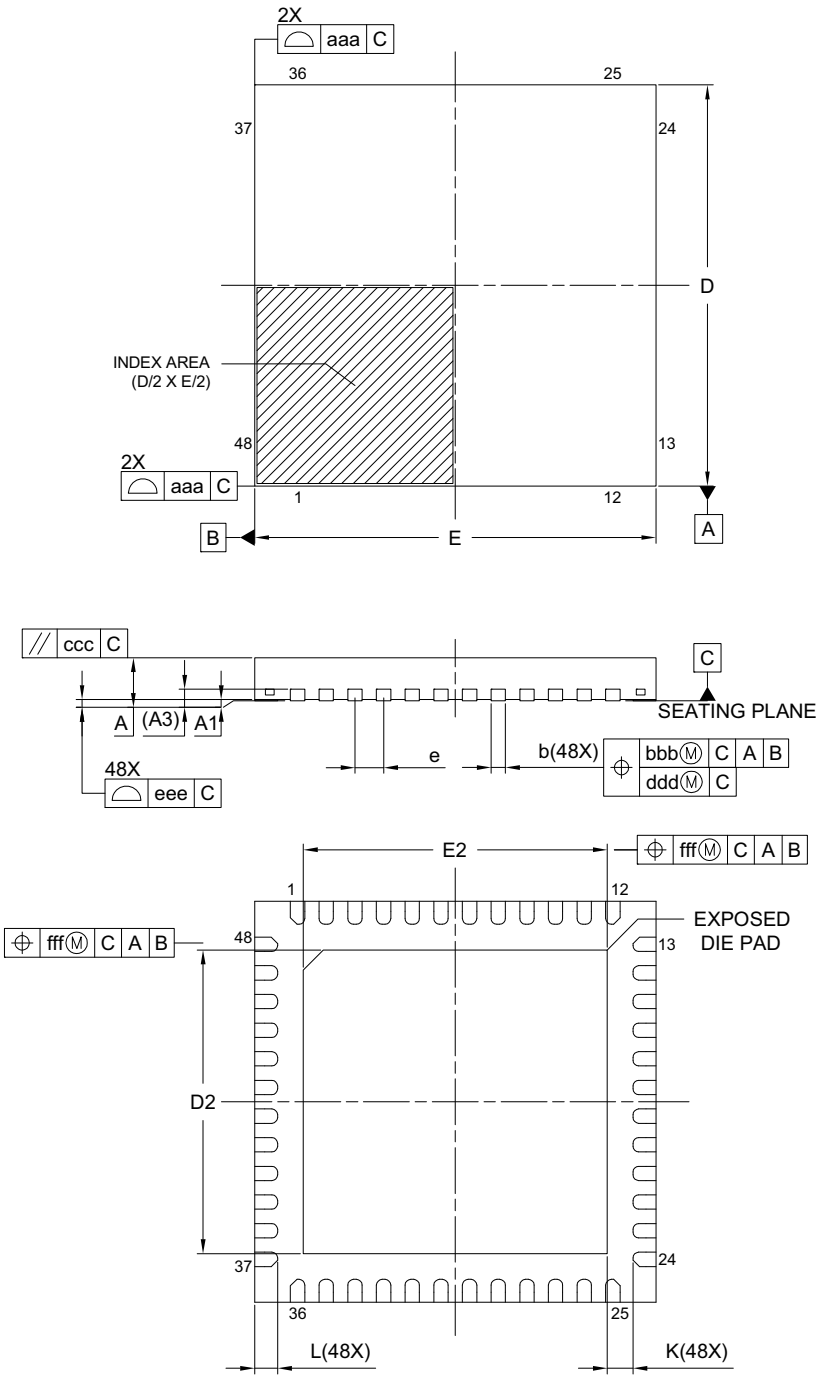
**Figure 1.7 48-pin QFN (1)**

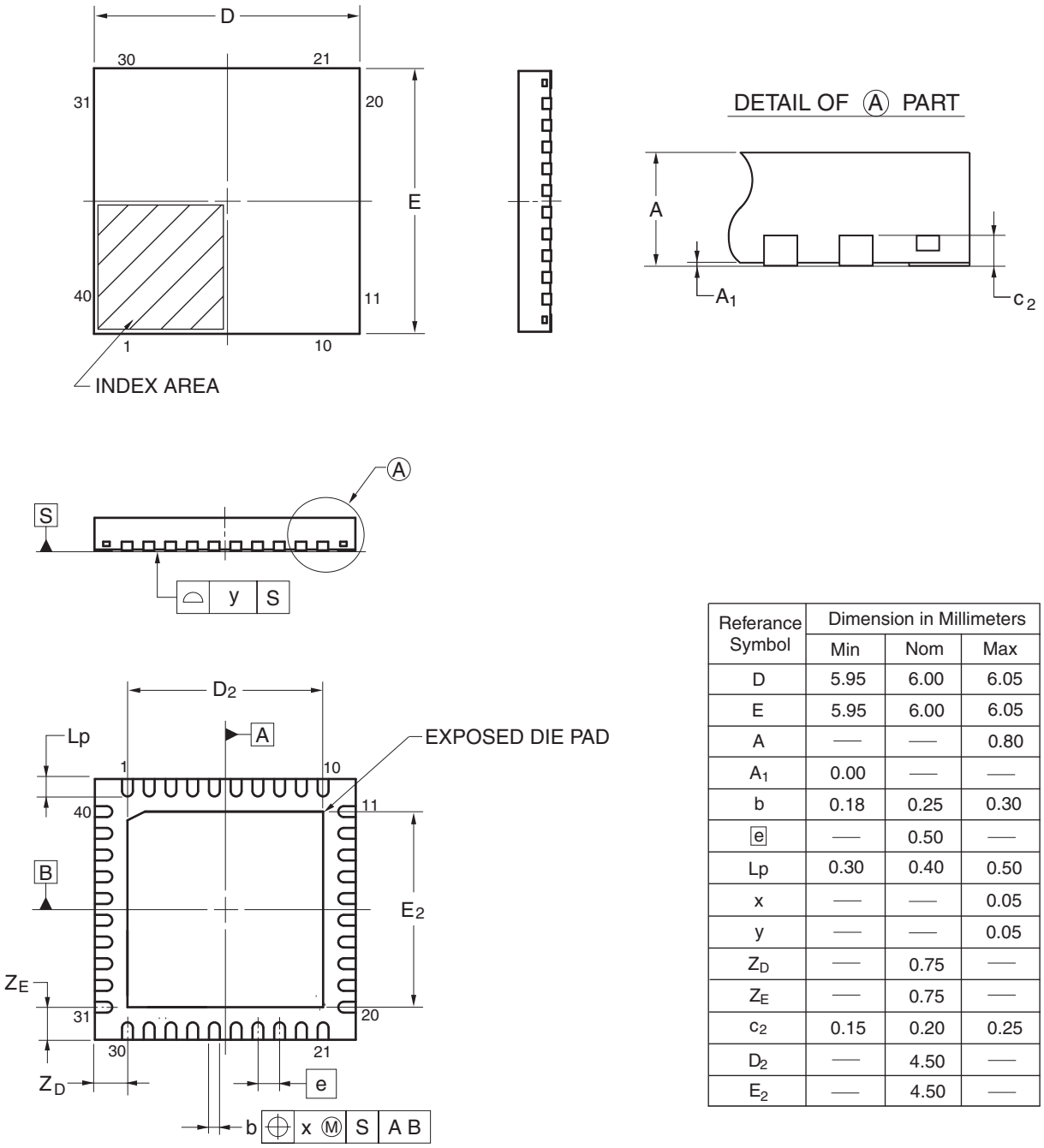
| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
|---|---|---|
| P-HWQFN048-7x7-0.50 | PWQN0048KC-A | 0.13 g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | 0.02 | 0.05 |
| $A_3$ | 0.203 REF. | | |
| b | 0.20 | 0.25 | 0.30 |
| D | 7.00 BSC | | |
| E | 7.00 BSC | | |
| e | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | — | — |
| $D_2$ | 5.25 | 5.30 | 5.35 |
| $E_2$ | 5.25 | 5.30 | 5.35 |
| aaa | 0.15 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

**Figure 1.8 48-pin QFN (2)**

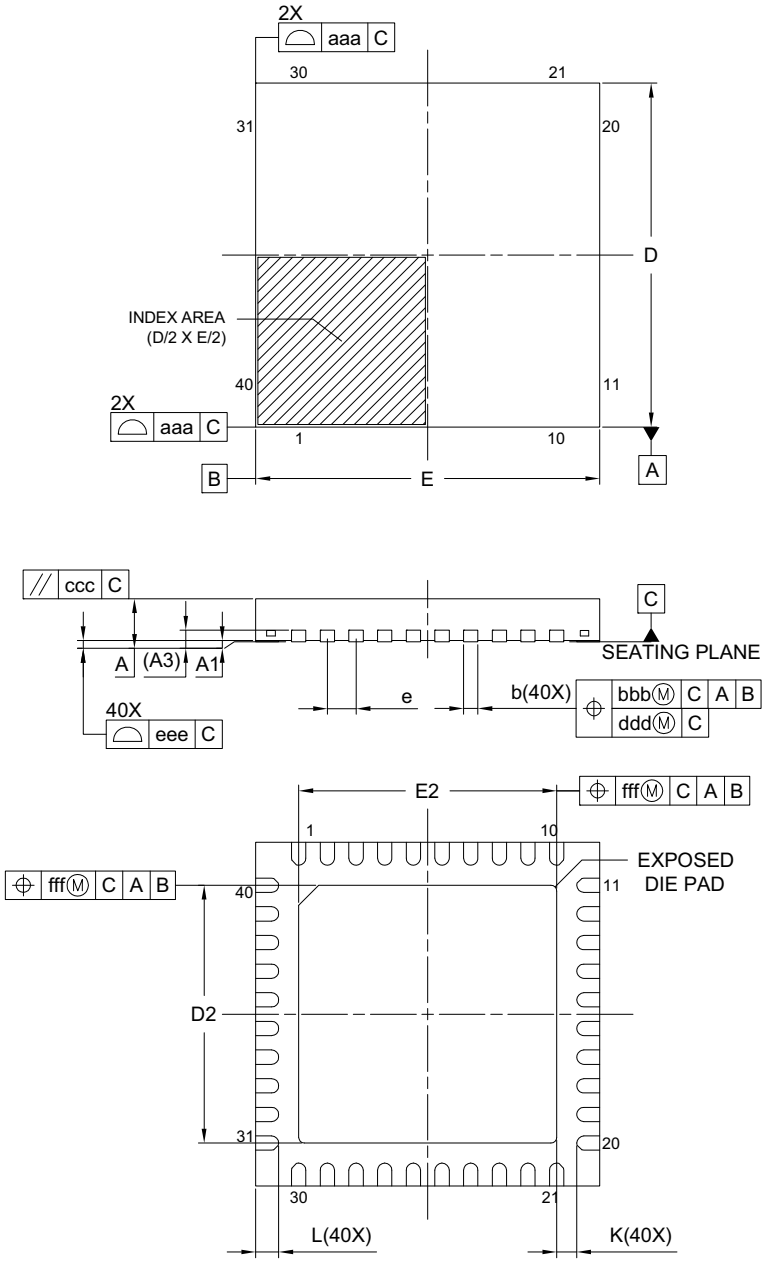
| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|---|---|---|---|
| P-HWQFN40-6x6-0.50 | PWQN0040KC-A | P40K8-50-4B4-5 | 0.09 |




| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 5.95 | 6.00 | 6.05 |
| E | 5.95 | 6.00 | 6.05 |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | — | — |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $Z_D$ | — | 0.75 | — |
| $Z_E$ | — | 0.75 | — |
| $c_2$ | 0.15 | 0.20 | 0.25 |
| $D_2$ | — | 4.50 | — |
| $E_2$ | — | 4.50 | — |

**Figure 1.9 40-pin QFN (1)**

| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
|---|---|---|
| P-HWQFN040-6x6-0.50 | PWQN0040KD-A | 0.08 |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | 0.02 | 0.05 |
| $A_3$ | 0.203 REF. | | |
| b | 0.18 | 0.25 | 0.30 |
| D | 6.00 BSC | | |
| E | 6.00 BSC | | |
| e | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | — | — |
| $D_2$ | 4.45 | 4.50 | 4.55 |
| $E_2$ | 4.45 | 4.50 | 4.55 |
| aaa | 0.15 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

**Figure 1.10 40-pin QFN (2)**

| Revision History | RA4M1 Group Datasheet |
|---|---|

| Rev. | Date | Chapter | Summary |
|---|---|---|---|
| 1.00 | Oct 8, 2019 | — | First Edition issued |
| 1.10 | Sep 29, 2023 | — | Second Edition issued |

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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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