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# INA3221 26V, Triple Channel, 13-Bit, I<sup>2</sup>C Output Current and Voltage Monitor With Alerts

## 1 Features

- Senses bus voltages from 0V to 26V
- Reports shunt and bus voltage
- High accuracy:
  - Offset voltage:  $\pm 80\mu\text{V}$  (maximum)
  - Gain error: 0.25% (maximum)
- Configurable averaging options
- Four programmable addresses
- Programmable alert and warning outputs
- Power-supply operation: 2.7V to 5.5V

## 2 Applications

- [Computers](#)
- [Power management](#)
- [Telecom equipment](#)
- [Battery chargers](#)
- [Power supplies](#)
- [Test equipment](#)
- [Data Centers](#)

## 3 Description

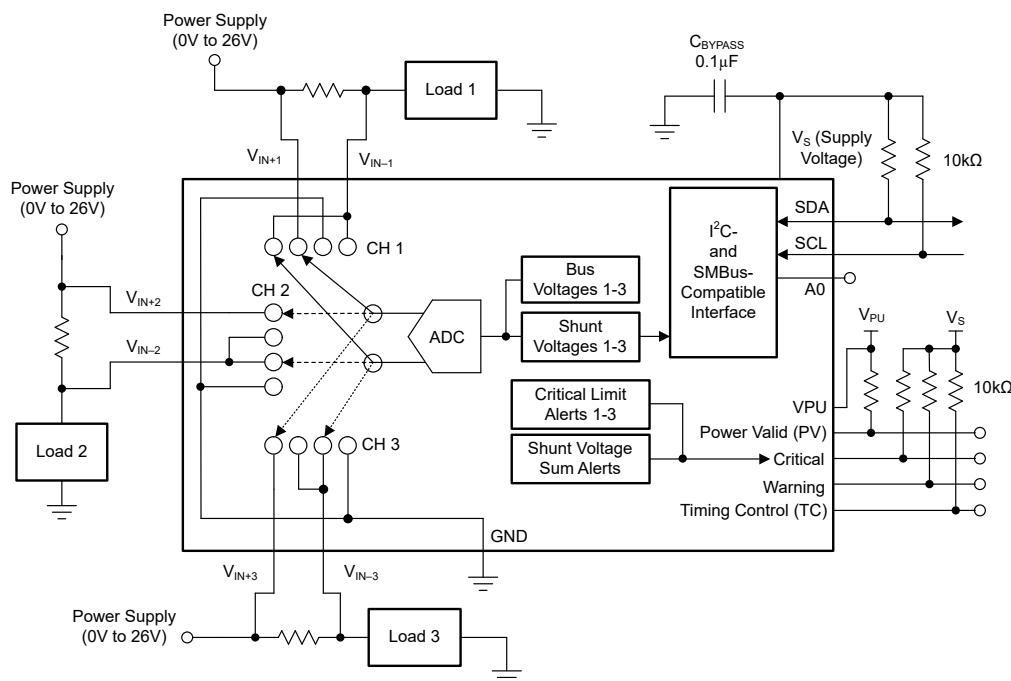
The INA3221 is a three-channel, high-side current and bus voltage monitor with an I<sup>2</sup>C- and SMBUS-compatible interface. The INA3221 monitors both shunt voltage drops and bus supply voltages, in addition to having programmable conversion times and averaging modes for these signals. The INA3221 offers both critical and warning alerts to detect multiple programmable out-of-range conditions for each channel.

The INA3221 senses current on buses that can vary from 0V to 26V. The device is powered from a single 2.7V to 5.5V supply, and draws 350 $\mu\text{A}$  (typ) of supply current. The INA3221 is specified over the operating temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . The I<sup>2</sup>C- and SMBUS-compatible interface features four programmable addresses.

### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------|------------------------|-----------------------------|
| INA3221     | RGV (VQFN, 16)         | 4.00mm × 4.00mm             |

- (1) For all available packages, see the package option addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



**Typical Application**



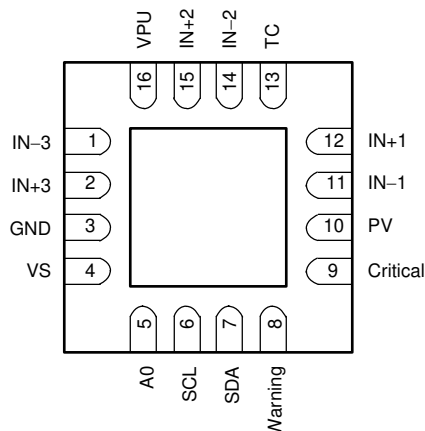
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## 4 Device Comparison Table

| DEVICE                                 | DESCRIPTION                                                                                                           |
|----------------------------------------|-----------------------------------------------------------------------------------------------------------------------|
| INA226                                 | 36V, Bidirectional, Ultrahigh Accuracy, Low- or High-Side, I <sup>2</sup> C Out, Current and Power Monitor With Alert |
| INA219                                 | 26V, Bidirectional, Zero-Drift, High-Side, I <sup>2</sup> C Out, Current and Power Monitor                            |
| INA209                                 | 26V, Bidirectional, Low- or High-Side, I <sup>2</sup> C Out, Current and Power Monitor and High-Speed Comparator      |
| INA210, INA211, INA212, INA213, INA214 | 26V, Bidirectional, Zero-Drift, High-Accuracy, Low- or High-Side, Voltage Out, Current Shunt Monitor                  |

## 5 Pin Configuration and Functions



**Figure 5-1. RGV Package 16-Pin VQFN Top View**

**Table 5-1. Pin Functions**

| PIN         |     | Type           | DESCRIPTION                                                                                                                          |
|-------------|-----|----------------|--------------------------------------------------------------------------------------------------------------------------------------|
| NAME        | NO. |                |                                                                                                                                      |
| A0          | 5   | Digital input  | Address pin. Connect to GND, SCL, SDA, or V <sub>S</sub> . <a href="#">Table 7-1</a> shows pin settings and corresponding addresses. |
| Critical    | 9   | Digital output | Conversion-triggered critical alert; open-drain output.                                                                              |
| GND         | 3   | Analog         | Ground                                                                                                                               |
| IN-1        | 11  | Analog input   | Connect to load side of the channel 1 shunt resistor. Bus voltage is the measurement from this pin to ground.                        |
| IN+1        | 12  | Analog input   | Connect to supply side of the channel 1 shunt resistor.                                                                              |
| IN-2        | 14  | Analog input   | Connect to load side of the channel 2 shunt resistor. Bus voltage is the measurement from this pin to ground.                        |
| IN+2        | 15  | Analog input   | Connect to supply side of the channel 2 shunt resistor.                                                                              |
| IN-3        | 1   | Analog input   | Connect to load side of the channel 3 shunt resistor. Bus voltage is the measurement from this pin to ground.                        |
| IN+3        | 2   | Analog input   | Connect to supply side of the channel 3 shunt resistor.                                                                              |
| PV          | 10  | Digital output | Power valid alert; open-drain output.                                                                                                |
| SCL         | 6   | Digital input  | Serial bus clock line; open-drain input.                                                                                             |
| SDA         | 7   | Digital I/O    | Serial bus data line; open-drain input/output.                                                                                       |
| TC          | 13  | Digital output | Timing control alert; open-drain output.                                                                                             |
| VPU         | 16  | Analog input   | Pull-up supply voltage used to bias power valid output circuitry.                                                                    |
| VS          | 4   | Analog         | Power supply, 2.7V to 5.5V.                                                                                                          |
| Warning     | 8   | Digital output | Averaged measurement warning alert; open-drain output.                                                                               |
| Thermal Pad | -   | -              | This pad must be connected to ground or left floating.                                                                               |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                |                                                     | MIN         | MAX             | UNIT |
|-----------------|--------------------------------|-----------------------------------------------------|-------------|-----------------|------|
| Voltage         | Supply, $V_S$                  |                                                     |             | 6               | V    |
| Analog inputs   | IN+, IN–                       | Differential ( $V_{IN+} - V_{IN-}$ ) <sup>(2)</sup> | –26         | 26              | V    |
|                 |                                | Common-mode ( $V_{IN+} + V_{IN-} / 2$ )             | –0.3        | 26              |      |
|                 | VPU                            |                                                     |             | 26              |      |
| Digital outputs | Critical, warning, power valid |                                                     |             | 6               | V    |
|                 | Timing control                 |                                                     |             | 26              |      |
| Serial bus      | Data line, SDA                 |                                                     | (GND – 0.3) | 6               | V    |
|                 | Clock line, SCL                |                                                     | (GND – 0.3) | ( $V_S + 0.3$ ) |      |
| Current         | Input, into any pin            |                                                     |             | 5               | mA   |
|                 | Open-drain, digital output     |                                                     |             | 10              |      |
| Temperature     | Operating, $T_A$               |                                                     | –40         | 125             | °C   |
|                 | Junction, $T_J$                |                                                     |             | 150             |      |
|                 | Storage, $T_{stg}$             |                                                     | –65         | 150             |      |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2)  $V_{IN+}$  and  $V_{IN-}$  can have a differential voltage of –26V to +26V; however, the voltage at these pins must not exceed the range of –0.3V to +26V.

### 6.2 ESD Ratings

|             |                         |                                                                                | VALUE | UNIT |
|-------------|-------------------------|--------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2500 | V    |
|             |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |      |
|             |                         | Machine model                                                                  | ±200  |      |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                              | MIN | NOM | MAX | UNIT |
|------------------------------|-----|-----|-----|------|
| Operating supply voltage     | 2.7 |     | 5.5 | V    |
| Operating temperature, $T_A$ | –40 |     | 125 | °C   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | INA3221    | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | RGV (VQFN) |      |
|                               |                                              | 16 PINS    |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 36.5       | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 42.7       | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 14.7       | °C/W |
| $\psi_{JT}$                   | Junction-to-top characterization parameter   | 0.5        | °C/W |
| $\psi_{JB}$                   | Junction-to-board characterization parameter | 14.8       | °C/W |

| THERMAL METRIC <sup>(1)</sup>                                     | UNIT                  |
|-------------------------------------------------------------------|-----------------------|
|                                                                   | INA3221               |
|                                                                   | RGV (VQFN)<br>16 PINS |
| $R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance | 3.3 °C/W              |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

## 6.5 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 3.3\text{V}$ ,  $V_{IN+} = 12\text{V}$ ,  $V_{SHUNT} = (V_{IN+}) - (V_{IN-}) = 0\text{mV}$ , and  $V_{BUS} = V_{IN-} = 12\text{V}$  (unless otherwise noted)

| PARAMETER            |                                          |                            | TEST CONDITIONS                                 | MIN                   | TYP | MAX                   | UNIT     |
|----------------------|------------------------------------------|----------------------------|-------------------------------------------------|-----------------------|-----|-----------------------|----------|
| INPUT                |                                          |                            |                                                 |                       |     |                       |          |
| V <sub>SHUNT</sub>   | Shunt voltage input                      |                            |                                                 | −163.84               |     | 163.8                 | mV       |
| V <sub>BUS</sub>     | Bus voltage input                        |                            |                                                 | 0                     |     | 26                    | V        |
| CMR                  | Common-mode rejection                    |                            | V <sub>IN+</sub> = 0V to +26V                   | 110                   | 120 |                       | dB       |
| V <sub>OS</sub>      | Shunt offset voltage, RTI <sup>(1)</sup> |                            |                                                 | ±40                   |     | ±80                   | μV       |
|                      |                                          |                            | T <sub>A</sub> = −40°C to +125°C                |                       | 0.1 | 0.5                   | μV/°C    |
| PSRR                 |                                          |                            | vs power supply, V <sub>S</sub> = 2.7V to 5.5V  | 15                    |     |                       | μV/V     |
| V <sub>OS</sub>      | Bus offset voltage, RTI <sup>(1)</sup>   |                            |                                                 | ±8                    |     | ±16                   | mV       |
|                      |                                          |                            | T <sub>A</sub> = −40°C to +125°C                |                       | 80  |                       | μV/°C    |
| PSRR                 |                                          |                            | vs power supply                                 | 0.5                   |     |                       | mV/V     |
| I <sub>IN+</sub>     | Input bias current at IN+                |                            |                                                 | 10                    |     |                       | μA       |
| I <sub>IN−</sub>     | Input bias current at IN−                |                            |                                                 | 10    670             |     |                       | μA    kΩ |
|                      | Input leakage <sup>(2)</sup>             |                            | (IN+ pin) + (IN− pin), power-down mode          | 0.1                   |     | 0.5                   | μA       |
| DC ACCURACY          |                                          |                            |                                                 |                       |     |                       |          |
|                      | ADC native resolution                    |                            |                                                 | 13                    |     |                       | Bits     |
|                      | 1LSB step size                           |                            | Shunt voltage                                   | 40                    |     |                       | μV       |
|                      |                                          |                            | Bus voltage                                     | 8                     |     |                       | mV       |
|                      | Shunt voltage gain error                 |                            |                                                 | 0.1%                  |     | 0.25%                 |          |
|                      |                                          |                            | T <sub>A</sub> = −40°C to +125°C                |                       | 10  | 50                    | ppm/°C   |
|                      | Bus voltage gain error                   |                            |                                                 | 0.1%                  |     | 0.25%                 |          |
|                      |                                          |                            | T <sub>A</sub> = −40°C to +125°C                |                       | 10  | 50                    | ppm/°C   |
| DNL                  | Differential nonlinearity                |                            |                                                 | ±0.1                  |     |                       | LSB      |
| t <sub>CONVERT</sub> | ADC conversion time                      |                            | CT bit = 000                                    | 140                   |     | 154                   | μs       |
|                      |                                          |                            | CT bit = 001                                    | 204                   |     | 224                   |          |
|                      |                                          |                            | CT bit = 010                                    | 332                   |     | 365                   |          |
|                      |                                          |                            | CT bit = 011                                    | 588                   |     | 646                   |          |
|                      |                                          |                            | CT bit = 100                                    | 1.1                   |     | 1.21                  | ms       |
|                      |                                          |                            | CT bit = 101                                    | 2.116                 |     | 2.328                 |          |
|                      |                                          |                            | CT bit = 110                                    | 4.156                 |     | 4.572                 |          |
|                      |                                          |                            | CT bit = 111                                    | 8.244                 |     | 9.068                 |          |
| SMBus                |                                          |                            |                                                 |                       |     |                       |          |
|                      | SMBus timeout <sup>(3)</sup>             |                            |                                                 | 28                    |     | 35                    | ms       |
| DIGITAL INPUT/OUTPUT |                                          |                            |                                                 |                       |     |                       |          |
| C <sub>I</sub>       | Input capacitance                        |                            |                                                 | 3                     |     |                       | pF       |
|                      | Leakage input current                    |                            | 0V ≤ V <sub>IN</sub> ≤ V <sub>S</sub>           | 0.1                   |     | 1                     | μA       |
| V <sub>IH</sub>      | High-level input voltage                 |                            |                                                 | 0.7 (V <sub>S</sub> ) |     | 6                     | V        |
| V <sub>IL</sub>      | Low-level input voltage                  |                            |                                                 | −0.5                  |     | 0.3 (V <sub>S</sub> ) | V        |
| V <sub>OL</sub>      | Low-level output voltage                 | SDA, critical, warning, PV | V <sub>S</sub> > +2.7V, I <sub>OL</sub> = 3mA   | 0                     |     | 0.4                   | V        |
|                      |                                          | TC                         | V <sub>S</sub> > +2.7V, I <sub>OL</sub> = 1.2mA | 0                     |     | 0.4                   |          |
| V <sub>hys</sub>     | Hysteresis voltage                       |                            |                                                 | 500                   |     |                       | mV       |
| POWER SUPPLY         |                                          |                            |                                                 |                       |     |                       |          |

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 3.3\text{V}$ ,  $V_{IN+} = 12\text{V}$ ,  $V_{SHUNT} = (V_{IN+}) - (V_{IN-}) = 0\text{mV}$ , and  $V_{BUS} = V_{IN-} = 12\text{V}$  (unless otherwise noted)

| PARAMETER                | TEST CONDITIONS | MIN | TYP | MAX | UNIT          |
|--------------------------|-----------------|-----|-----|-----|---------------|
| Quiescent current        |                 |     | 350 | 450 | $\mu\text{A}$ |
|                          | Power-down mode |     | 0.5 | 2   |               |
| Power-on reset threshold |                 |     | 2   |     | V             |

- (1) RTI = Referred-to-input.
- (2) Input leakage is positive (current flows into the pin) for the conditions shown at the top of this table. Negative leakage currents can occur under different input conditions.
- (3) SMBus timeouts in the INA3221 reset the interface whenever SCL is low for more than 28ms.

## 6.6 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 3.3\text{V}$ ,  $V_{IN+} = 12\text{V}$ ,  $V_{SHUNT} = (V_{IN+}) - (V_{IN-}) = 0\text{mV}$ , and  $V_{BUS} = V_{IN-} = 12\text{V}$  (unless otherwise noted)

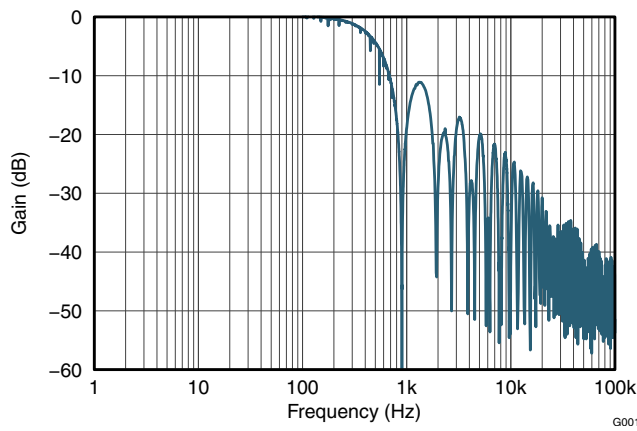


Figure 6-1. Frequency Response

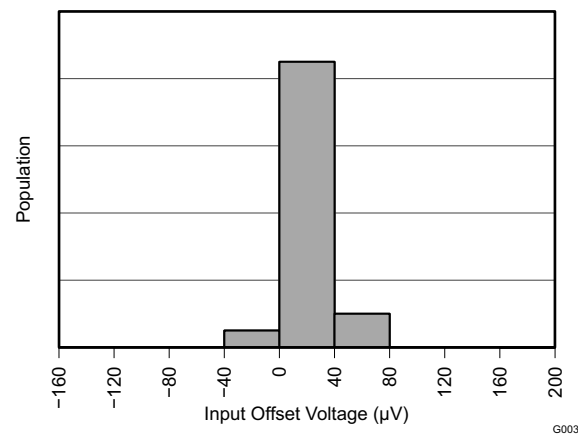


Figure 6-2. Shunt Input Offset Voltage Production Distribution

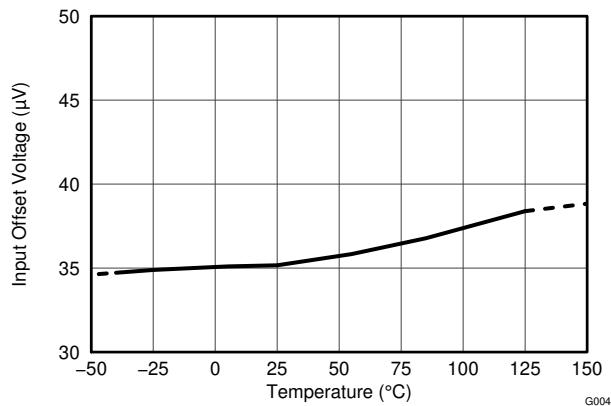


Figure 6-3. Shunt Input Offset Voltage vs. Temperature

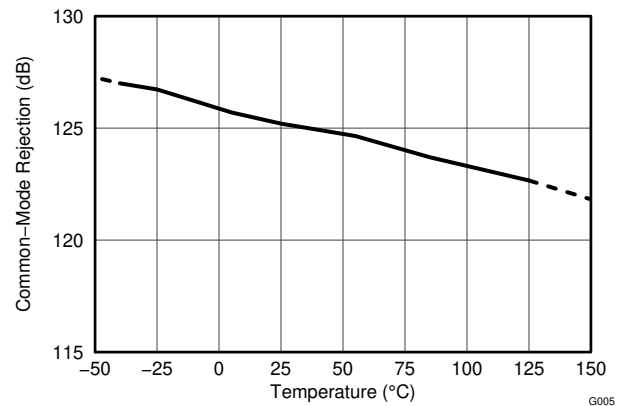


Figure 6-4. Shunt Input Common-Mode Rejection Ratio vs. Temperature

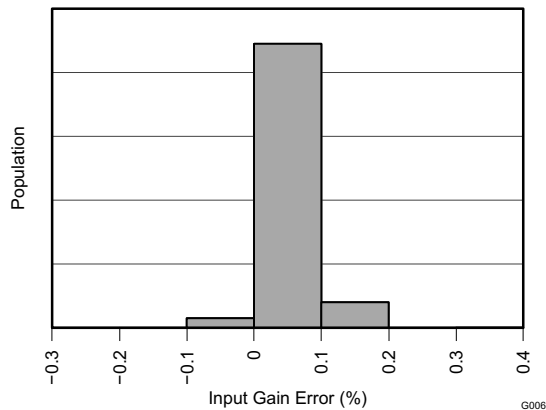


Figure 6-5. Shunt Input Gain Error Production Distribution

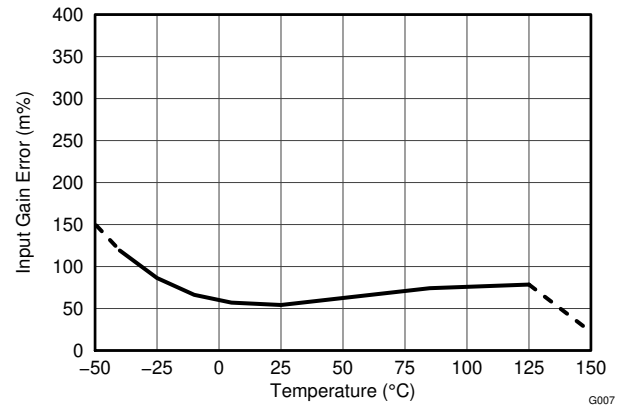


Figure 6-6. Shunt Input Gain Error vs. Temperature



## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 3.3\text{V}$ ,  $V_{IN+} = 12\text{V}$ ,  $V_{SHUNT} = (V_{IN+}) - (V_{IN-}) = 0\text{mV}$ , and  $V_{BUS} = V_{IN-} = 12\text{V}$  (unless otherwise noted)

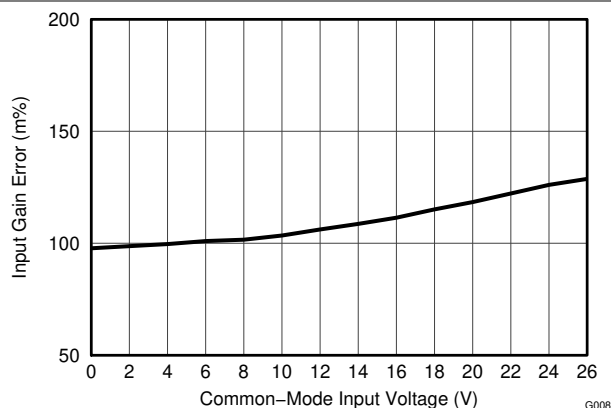


Figure 6-7. Shunt Input Gain Error vs. Common-Mode Voltage

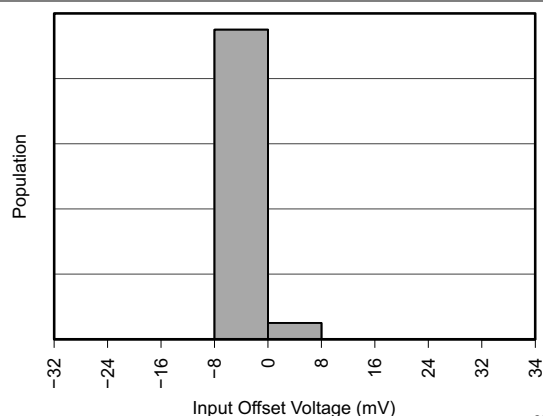


Figure 6-8. Bus Input Offset Voltage Production Distribution

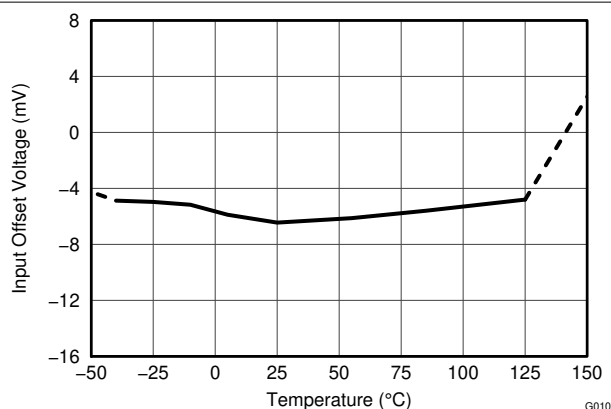


Figure 6-9. Bus Input Offset Voltage vs. Temperature

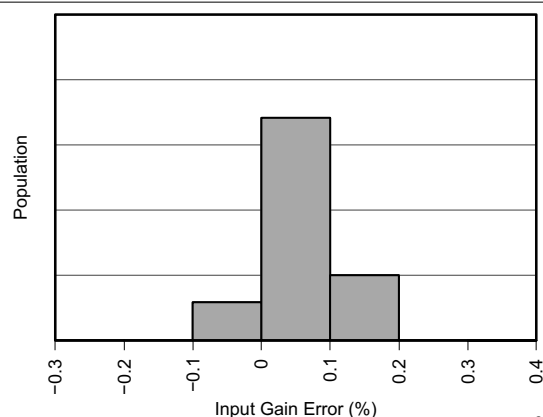


Figure 6-10. Bus Input Gain Error Production Distribution

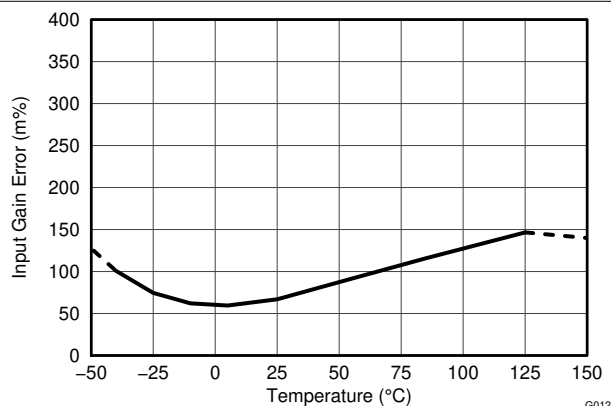


Figure 6-11. Bus Input Gain Error vs. Temperature

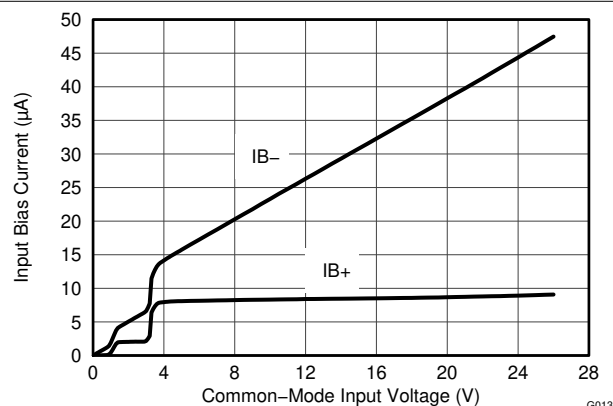
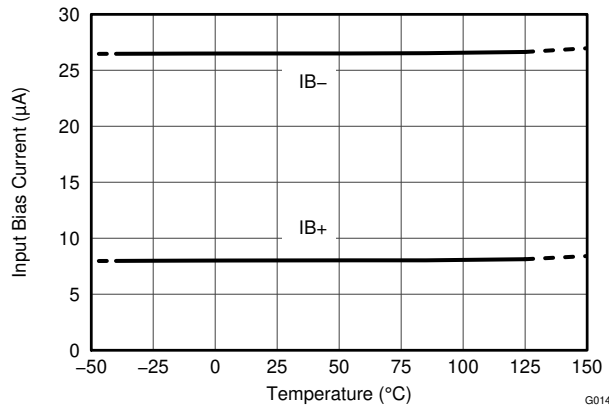


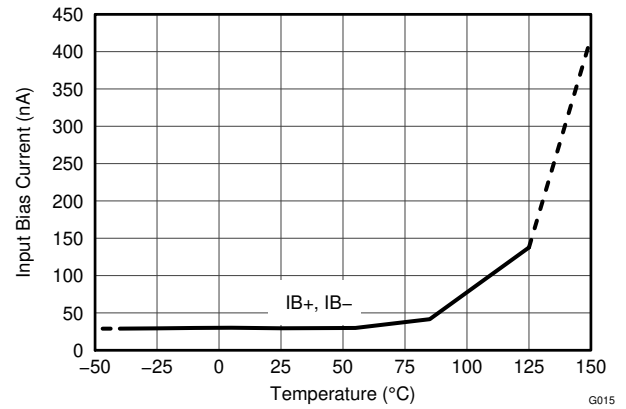
Figure 6-12. Input Bias Current vs. Common-Mode Voltage

## 6.6 Typical Characteristics (continued)

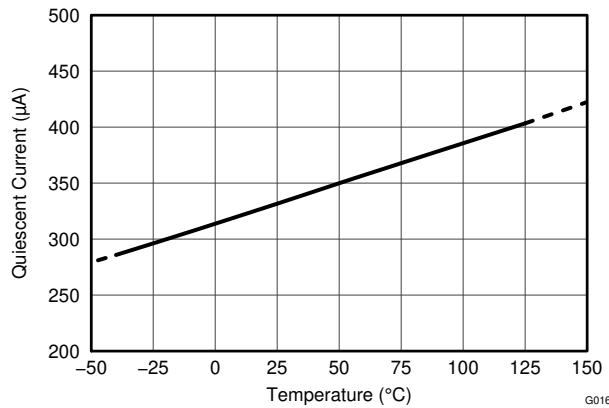
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 3.3\text{V}$ ,  $V_{IN+} = 12\text{V}$ ,  $V_{SHUNT} = (V_{IN+}) - (V_{IN-}) = 0\text{mV}$ , and  $V_{BUS} = V_{IN-} = 12\text{V}$  (unless otherwise noted)



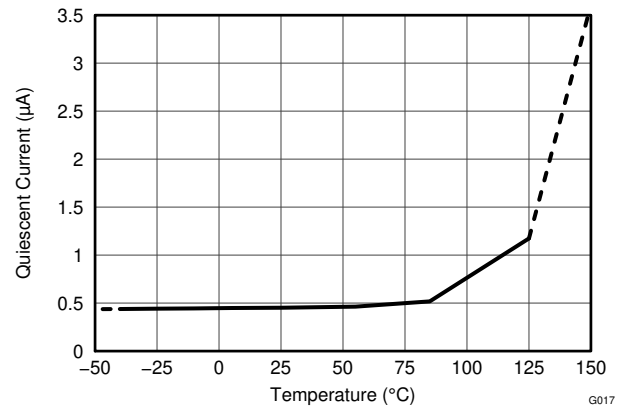
**Figure 6-13. Input Bias Current vs. Temperature**



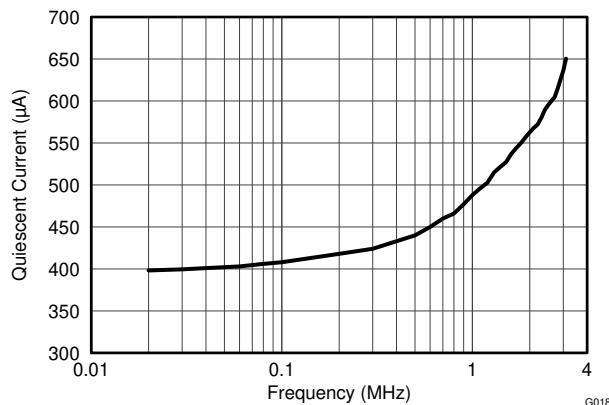
**Figure 6-14. Input Bias Current vs. Temperature (Shutdown)**



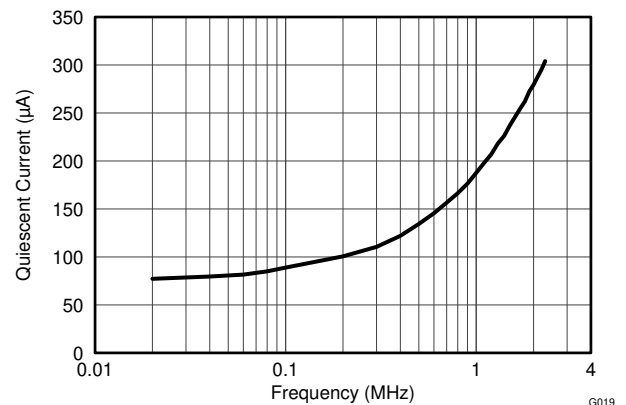
**Figure 6-15. Active  $I_Q$  vs. Temperature**



**Figure 6-16. Shutdown  $I_Q$  vs. Temperature**



**Figure 6-17. Active  $I_Q$  vs.  $I^2C$  Clock Frequency**



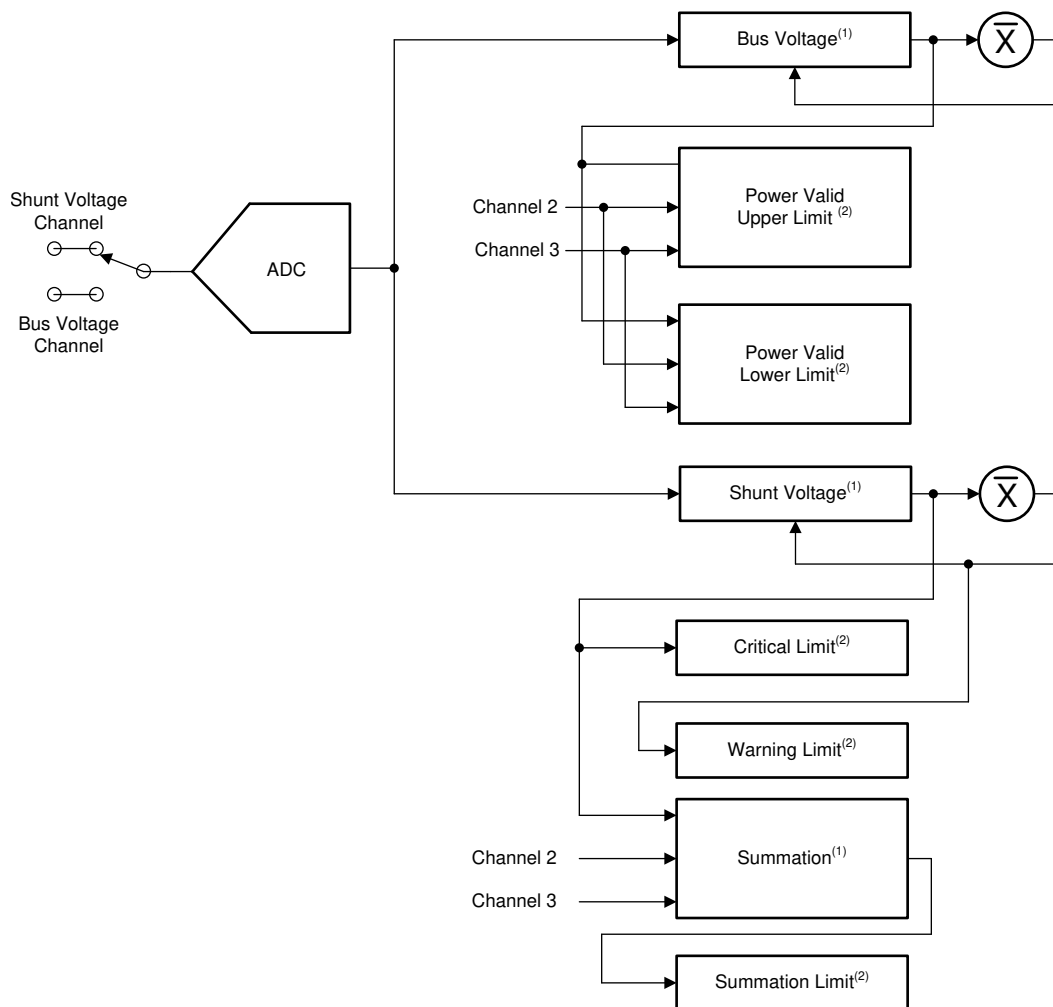
**Figure 6-18. Shutdown  $I_Q$  vs.  $I^2C$  Clock Frequency**

## 7 Detailed Description

### 7.1 Overview

The INA3221 is a current-shunt and bus voltage monitor that communicates over an I<sup>2</sup>C- and SMBus-compatible interface. The INA3221 provides digital shunt and bus voltage readings necessary for accurate decision making in precisely-controlled systems, and also monitors multiple rails to maintain compliance voltages. Programmable registers offer flexible configuration for measurement precision, and continuous versus single-shot operation. The [Register Maps](#) section provides details of the INA3221 registers, beginning with [Table 7-3](#).

### 7.2 Functional Block Diagram



- A. Read-only.
- B. Read/write.

## 7.3 Feature Description

### 7.3.1 Basic ADC Functions

The INA3221 performs two measurements on up to three power supplies of interest. The voltage developed from the load current passing through a shunt resistor creates a shunt voltage that is measured between the IN+ and IN– pins. The device also internally measures the power-supply bus voltage at the IN– pin for each channel. The differential shunt voltage is measured with respect to the IN– pin, and the bus voltage is measured with respect to ground.

The INA3221 is typically powered by a separate power supply that ranges from 2.7V to 5.5V. The monitored supply buses range from 0V to 26V.

#### CAUTION

Based on the fixed 8mV bus-voltage register LSB (for any channel), a full-scale register value results in 32.76V. However, the actual voltage applied to the INA3221 input pins must not exceed 26V.

There are no special power-supply sequencing considerations between the common-mode input ranges and the device power-supply voltage because each are independent of the other; therefore, the bus voltages can be present with the supply voltage off and reciprocally.

The INA3221 takes two measurements for each channel: one for shunt voltage and one for bus voltage. Each measurement can be independently or sequentially measured, based on the mode setting (bits 2-0 in the Configuration register). When the INA3221 is in normal operating mode (that is, the MODE bits of the Configuration register are set to 111), the device continuously converts a shunt-voltage reading followed by a bus-voltage reading. This procedure converts one channel, and then continues to the shunt voltage reading of the next enabled channel, followed by the bus-voltage reading for that channel, and so on, until all enabled channels have been measured. The programmed Configuration register mode setting applies to all channels. Any channels that are not enabled are bypassed in the measurement sequence, regardless of mode setting.

The INA3221 has two operating modes, continuous and single-shot, that determine the internal ADC operation after these conversions complete. When the INA3221 is set to continuous mode (using the MODE bit settings), the device continues to cycle through all enabled channels until a new configuration setting is programmed.

The Configuration register MODE control bits also enable modes to be selected that convert only the shunt or bus voltage. This feature further allows the device to fit specific application requirements.

In single-shot (triggered) mode, setting any single-shot convert mode to the Configuration register (that is, the Configuration register MODE bits set to 001, 010, or 011) triggers a single-shot conversion. This action produces a single set of measurements for all enabled channels. To trigger another single-shot conversion, write to the Configuration register a second time, even if the mode does not change. When a single-shot conversion is initiated, all enabled channels are measured one time and then the device enters a power-down state. The INA3221 registers can be read at any time, even while in power-down. The data present in these registers are from the last completed conversion results for the corresponding register. The conversion ready flag bit (Mask/Enable register, CVRF bit) helps coordinate single-shot conversions, and is especially helpful during longer conversion time settings. The CVRF bit is set after all conversions are complete. The CVRF bit clears under the following conditions:

1. Writing to the Configuration register, except when configuring the MODE bits for power-down mode; or
2. Reading the Mask/Enable register.

In addition to the two operating modes (continuous and single-shot), the INA3221 also has a separate selectable power-down mode that reduces the quiescent current and turns off current into the INA3221 inputs. Power-down mode reduces the impact of supply drain when the device is not used. Full recovery from power-down mode requires 40μs. The INA3221 registers can be written to and read from while the device is in power-down mode. The device remains in power-down mode until one of the active MODE settings are written to the Configuration register.

### 7.3.2 Alert Monitoring

The INA3221 allows programmable thresholds that make sure the intended application operates within the desired operating conditions. Multiple monitoring functions are available using four alert pins: Critical, Warning, PV (power valid), and TC (timing control). These alert pins are open-drain connections.

#### 7.3.2.1 Critical Alert

The critical-alert feature monitors functions based on individual conversions of each shunt-voltage channel. The critical-alert limit feature compares the shunt-voltage conversion for each shunt-voltage channel to the value programmed into the corresponding limit register, to determine if the measured value exceeds the intended limit. Exceeding the programmed limit indicates that the current through the shunt resistor is too high.

At power-up, the default critical-alert limit value for each channel is set to the positive full-scale value, effectively disabling the alert. Program the corresponding limit registers at any time to begin monitoring for out-of-range conditions. The Critical alert pin pulls low if any channel measurement exceeds the limit present in the corresponding-channel critical-alert limit register. When the Critical alert pulls low, read the Mask/Enable register to determine which channel caused the critical alert flag indicator bit (CF1-3) to assert (= 1).

##### 7.3.2.1.1 Summation Control Function

The INA3221 also allows the Critical alert pin to be controlled by the summation control function. This function adds the single shunt-voltage conversions for the desired channels (set by SCC1-3 in the Mask/Enable register) to compare the combined sum to the programmed limit.

The SCC bits either disable the summation control function or allow the summation control function to switch between including two or three channels in the Shunt-Voltage Sum register. The Shunt-Voltage Sum Limit register contains the programmed value that is compared to the value in the Shunt-Voltage Sum register to determine if the total summed limit is exceeded. If the shunt-voltage sum limit value is exceeded, the Critical alert pin pulls low. Either the summation alert flag indicator bit (SF) or the individual critical alert limit bits (CF1-3) in the Mask/Enable register determine the source of the alert when the Critical alert pin pulls low.

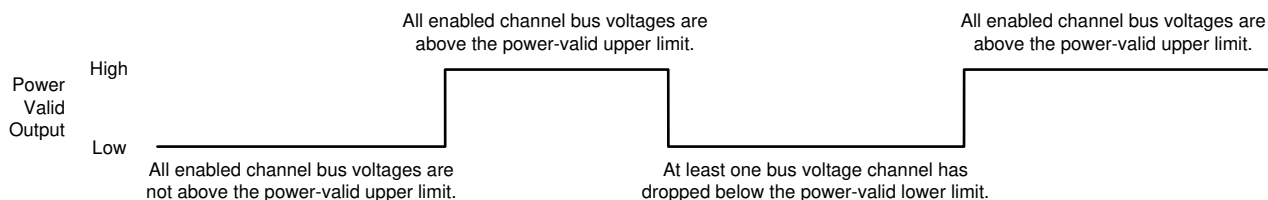
For the summation limit to have a meaningful value, use the same shunt-resistor value on all included channels. Unless equal shunt-resistor values are used for each channel, do not use this function to add the individual conversion values directly together in the Shunt-Voltage Sum register to report the total current.

#### 7.3.2.2 Warning Alert

The warning alert monitors the averaged value of each shunt-voltage channel. The averaged value of each shunt-voltage channel is based on the number of averages set with the averaging mode bits (AVG1-3) in the Configuration register. The average value updates in the shunt-voltage output register each time there is a conversion on the corresponding channel. The device compares the averaged value to the value programmed in the corresponding-channel Warning Alert Limit register to determine if the averaged value has been exceeded, indicating whether the average current is too high. At power-up, the default warning-alert limit value for each channel is set to the positive full-scale value, effectively disabling the alert. The corresponding limit registers can be programmed at any time to begin monitoring for out-of-range conditions. The Warning alert pin pulls low if any channel measurements exceed the limit present in the corresponding-channel Warning Alert Limit register. When the Warning alert pin pulls low, read the Mask/Enable register to determine which channel warning alert flag indicator bit (WF1-3) is asserted (= 1).

### 7.3.2.3 Power-Valid Alert

The power-valid alert verifies if all power rails are above the required levels. This feature manages power sequencing, and validates the reported measurements based on system configuration. Power-valid mode starts at power-up, and detects when each channel exceeds a 10V threshold. This 10V level is the default value programmed into the Power-Valid Upper-Limit register. This value can be reprogrammed when the INA3221 is powered up to a valid supply-voltage level of at least 2.7V. When all three bus-voltage measurements reach the programmed value loaded to the Power-Valid Upper-Limit register, the power-valid (PV) alert pin pulls high. PV powers up in a low state, and does not pull high until the power-valid conditions are met, indicating all bus-voltage rails are above the power-valid upper-limit value. This sequence is shown in [Figure 7-1](#).



**Figure 7-1. Power-Valid State Diagram**

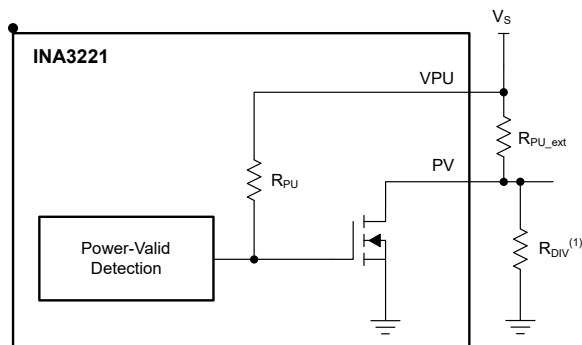
When the power-valid conditions are met, and the PV pin pulls high, the INA3221 monitors if any bus-voltage measurements drop below 9V. This 9V level is the default value programmed into the Power-Valid Lower-Limit register. This value can also be reprogrammed when the INA3221 powers up to a supply voltage of at least 2.7V. If any bus-voltage measurement on the three channels drops below the Power-Valid Lower-Limit register value, the PV pin goes low, indicating that the power-valid condition is no longer met. At this point, the INA3221 resumes monitoring the power rails for a power-valid condition set in the Power-Valid Upper-Limit register.

The power-valid alert function is based on the power-valid conditions requirement that all three channels reach the intended Power-Valid Upper-Limit register value. If all three channels are not used, connect the unused-channel IN<sup>-</sup> pin externally to one of the used channels to use the power-valid alert function. If the unused channel is not connected to a valid rail, the power-valid alert function cannot detect if all three channels reach the power-valid level. Float the unused channel IN<sup>+</sup> pin.

The power-valid function also requires that bus-voltage measurements are monitored. To detect changes in the power-valid state, enable bus-voltage measurements through one of the corresponding MODE-bit settings in the Configuration register. The single-shot bus-voltage mode periodically cycles between the bus-voltage measurements to make sure that the power-valid conditions are met.

When all three bus-voltage measurements are completed, the device compares the results to the power-valid threshold values to determine the power-valid state. The bus-voltage measurement values remain in the corresponding channel output registers until the bus-voltage measurements are taken again, thus updating the output registers. When the output registers are updated, the values are again compared to the power-valid thresholds. Without taking periodic bus-voltage measurements, the INA3221 is unable to determine if the power-valid conditions are maintained.

The PV pin allows for a 0V output that indicates a power-invalid condition. An output equal to the pull-up supply voltage connected to the VPU pin indicates a power-valid condition, as shown in Figure 7-2. Dividing down the high power-valid pull-up voltage by adding a resistor to ground at the PV output is also possible, thus allowing this function to interface with lower-voltage circuitry, if needed.

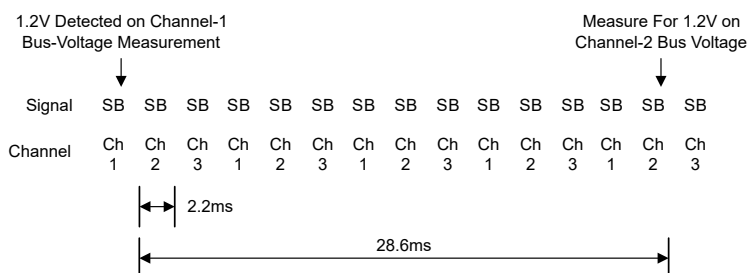


A.  $R_{DIV}$  can be used to level-shift the PV output high.

**Figure 7-2. Power-Valid Output Structure**

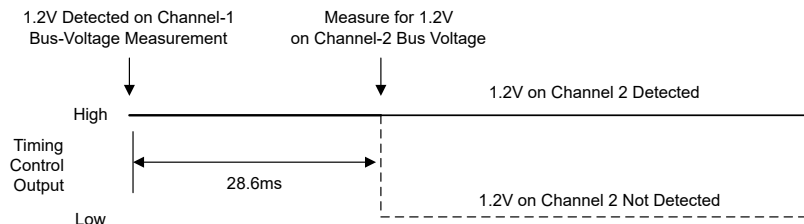
### 7.3.2.4 Timing-Control Alert

The INA3221 timing-control alert function helps verify proper power-supply sequencing. At power-up, the default INA3221 setting is continuous shunt- and bus-voltage conversion mode, and the INA3221 internally begins comparing the channel-1 bus voltage to determine when a 1.2V level is reached. This comparison is made each time the sequence returns to the channel-1 bus-voltage measurement. When a 1.2V level is detected on the channel-1 bus-voltage measurement, the INA3221 begins checking for a 1.2V level present on the channel-2 bus-voltage measurement. After a 1.2V level is detected on channel 1, if the INA3221 does not detect a 1.2V value or greater on the bus voltage measurement following four complete cycles of all three channels, the timing control (TC) alert pin pulls low to indicate that the INA3221 has not detected a valid power rail on channel 2. As shown in Figure 7-3, this sequence allows for approximately 28.6ms from the time 1.2V is detected on channel 1 for a valid voltage to be detected on channel 2. Figure 7-4 illustrates the state diagram for the TC alert pin.



NOTE: The signal refers to the corresponding shunt (S) and bus (B) voltage measurement for each channel.

**Figure 7-3. Timing Control Timing Diagram**



**Figure 7-4. Timing Control State Diagram**

The timing control alert function is only monitored at power-up or when a software reset is issued by setting the reset bit (RST, bit 15) in the Configuration register. The timing control alert function timing is based on the default device settings at power-up. Writing to the Configuration register before the timing control alert function completes the full sequence results in disabling the timing control alert until power is cycled or a software reset is issued.

#### **7.3.2.5 Default Settings**

The default register power-up states are listed in the [Register Maps](#) section. These registers are volatile; if programmed to a value other than the default values shown in [Table 7-3](#), the registers must be reprogrammed every time the device powers up.

#### **7.3.3 Software Reset**

The INA3221 features a software reset that reinitializes the device and register settings to default power-up values without having to cycle power to the device. Use bit 15 (RST) of the Configuration register to perform a software reset. Setting RST reinitializes all registers and settings to the default power state with the exception of the power-valid output state.

If a software reset is issued, the INA3221 holds the output of the PV pin until the power-valid detection sequence completes. The Power-Valid Upper Limit and Power-Valid Lower limit registers return to the default state when the software reset has been issued. Therefore, any reprogrammed limit registers are reset, resulting in the original power-valid thresholds validating the power-valid conditions. This architecture prevents interruption to circuitry connected to the power valid output during a software reset event.



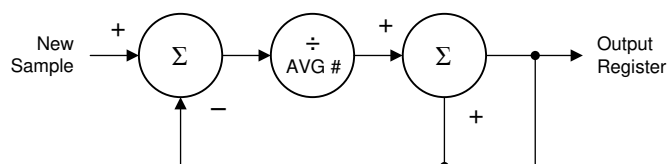
## 7.4 Device Functional Modes

### 7.4.1 Averaging Function

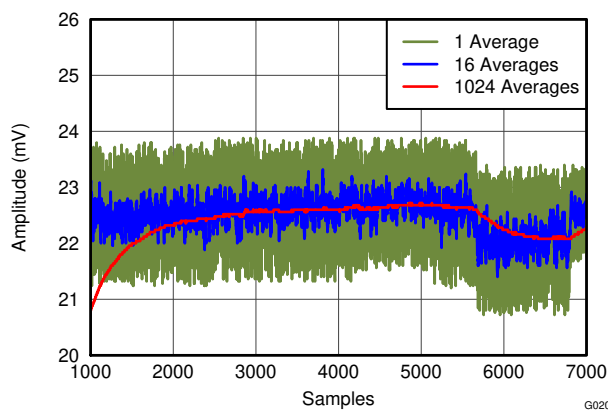
The INA3221 includes three channels to monitor up to three independent supply buses; however, multichannel monitoring sometimes results in poor shunt-resistor placement. Ideally, shunt resistors are placed as close as possible to the corresponding channel input pins. However, because of system layout and multiple power-supply rails, one or more shunt resistors can require being located further away, thus presenting potentially larger measurement errors. These errors result from additional trace inductance and other parasitic impedances between the shunt resistor and input pins. Longer traces also create an additional potential for coupling noise into the signal if the traces are routed near noise-generating sections of the board.

The INA3221 averaging function mitigates this potential problem by limiting the impact that any single measurement has on the averaged value of each measured signal. This limitation reduces the influence that noise has on the averaged value, thereby effectively creating an input-signal filter.

The averaging function is illustrated in Figure 7-5. Operation begins by first measuring the shunt input signal on channel 1. This value is then subtracted from the previous value that was present in the corresponding data output register. This difference is then divided by the value programmed by the averaging mode setting (AVG2-0, Configuration register bits 11-9) and stored in an internal accumulation register. The computed result is then added to the previously-loaded data output register value, and the resulting value is loaded to the corresponding data output register. After the update, the next signal to be measured follows the same process. The larger the value selected for the averaging mode setting, the less impact or influence any new conversion has on the average value, as shown in Figure 7-6. This averaging feature functions as a filter to reduce input noise from the averaged measurement value.



**Figure 7-5. Averaging Function Block Diagram**



**Figure 7-6. Average Setting Example**

### 7.4.2 Multiple Channel Monitoring

The INA3221 monitors shunt and voltage measurements for up to three unique power-supply rails, and measures up to six different signals. Adjust the number of channels and signals being measured by setting the channel enable (CH1<sub>en</sub> to CH3<sub>en</sub>) and mode (MODE3-1) bits in the Configuration register. This adjustment allows the device to be optimized based on application requirements for the system in use.

#### 7.4.2.1 Channel Configuration

If all three channels must be monitored at power-up, but only one channel must be monitored after the system has stabilized, disable the other two channels after power-up. This configuration allows the INA3221 to only monitor the power-supply rail of interest. Disable unused channels to help improve system response time by more quickly returning to sampling the channel of interest. The INA3221 linearly monitors the enabled channels. That is, if all three channels are enabled for both shunt- and bus-voltage measurements, an additional five conversions complete after a signal is measured before the device returns to that particular signal to begin another conversion. To reduce this requirement down to two conversions before the device begins a new conversion on a particular channel again, change the operating mode to monitor only the shunt voltage.

A timing aspect is also involved in reducing the measured signals. The amount of time to complete an all-channel, shunt- and bus-voltage sequence is equal to the sum of the shunt-voltage conversion time and the bus-voltage conversion time (programmed by the CT bits in the Configuration register) multiplied by the three channels. The conversion times for the shunt- and bus-voltage measurements are programmed independently; however, the selected shunt- and bus-voltage conversion times apply to all channels.

Enable a single channel with only one signal measured to allow for that particular signal to be monitored solely. This setting enables the fastest response over time to changes in that specific input signal because there is no delay from the end of one conversion before the next conversion begins on that channel. Conversion time is not affected by enabling or disabling other channels. Selecting both the shunt- and bus-voltage settings, as well as enabling additional channels, extends the time from the end of one conversion on a signal before the beginning of the next conversion of that signal.

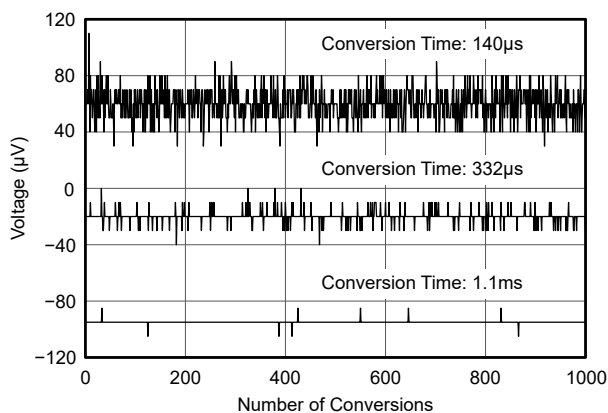
#### 7.4.2.2 Averaging and Conversion-Time Considerations

The INA3221 has programmable conversion times for both the shunt- and bus-voltage measurements. The selectable conversion times for these measurements range from 140 $\mu$ s to 8.244ms. The conversion-time settings, along with the programmable-averaging mode, enable the INA3221 to optimize available timing requirements in a given application. For example, if a system requires data to be read every 2ms with all three channels monitored, configure the INA3221 with the conversion times for the shunt- and bus-voltage measurements set to 332 $\mu$ s.

The INA3221 can also be configured with a different conversion-time setting for the shunt- and bus-voltage measurements. This approach is common in applications where the bus voltage tends to be relatively stable, and allows for the time focused on the bus voltage measurement to be reduced relative to the shunt-voltage measurement. For example, the shunt-voltage conversion time can be set to 4.156ms with the bus-voltage conversion time set to 588 $\mu$ s for a 5ms update time.

There are trade-offs associated with the conversion-time and averaging-mode settings. The averaging feature significantly improves the measurement accuracy by effectively filtering the signal. This approach allows the INA3221 to reduce the amount of noise in the measurement caused by noise coupling into the signal. A greater number of averages allows the INA3221 to be more effective in reducing the measurement noise component. The trade-off to this noise reduction is that the averaged value has a longer response time to input-signal changes. This aspect of the averaging feature is mitigated to some extent with the critical-alert feature that compares each single conversion to determine if a measured signal (with noise component) has exceeded the maximum acceptable level.

The selected conversion times also have an impact on measurement accuracy. This effect can be seen in [Figure 7-7](#). The multiple conversion times shown in [Figure 7-7](#) illustrate the impact of noise on measurement. These curves shown do not use averaging. To achieve the highest-accuracy measurement possible, use a combination of the longest allowable conversion times and highest number of averages, based on system timing requirements.

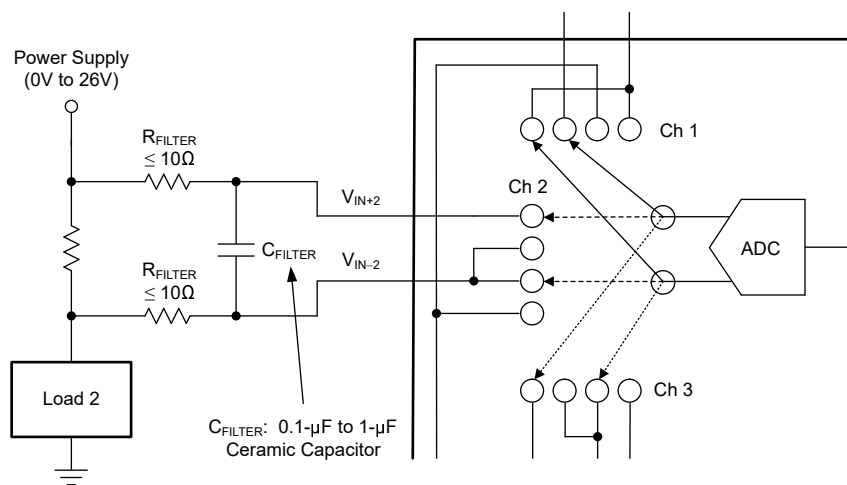


**Figure 7-7. Noise Versus Conversion Time**

### 7.4.3 Filtering and Input Considerations

Measuring current is often noisy, and such noise can be difficult to define. The INA3221 offers several filtering options by allowing conversion times and the number of averages to be selected independently in the Configuration register. The conversion times can be set independently for the shunt- and bus-voltage measurements as well, for added flexibility in configuring power-supply bus monitoring.

The internal ADC is based on a delta-sigma ( $\Delta\Sigma$ ) front-end with a 500kHz ( $\pm 30\%$ ) typical sampling rate. This architecture has good inherent noise rejection; however, transients that occur at or very close to the sampling-rate harmonics can cause problems. These transient signals are at 1MHz and higher; therefore, the signals are managed by incorporating filtering at the INA3221 input. High-frequency signals allow for the use of low-value series resistors on the filter, with negligible effects on measurement accuracy. In general, filtering the INA3221 input is only necessary if there are transients at exact harmonics of the 500kHz ( $\pm 30\%$ ) sampling rate that are greater than 1MHz. Filter using the lowest-possible series resistance (typically 10 $\Omega$  or less) and a ceramic capacitor. Recommended capacitor values are 0.1 $\mu$ F to 1.0 $\mu$ F. Figure 7-8 shows the INA3221 with an additional filter added at the input.



**Figure 7-8. INA3221 With Input Filtering**

The INA3221 inputs are specified to tolerate 26V across the inputs. However, overload conditions are another consideration for the INA3221 inputs. For example, a large differential-input scenario can be a short to ground on the load side of the shunt. This type of event results in the full power-supply voltage applied across the shunt, if supported by the power supply or energy-storage capacitors. Keep in mind that removing a short to ground can result in inductive kickbacks that can exceed the 26V differential and common-mode rating of the INA3221. Inductive kickback voltages are best controlled by zener-type transient-absorbing devices (commonly called *transzorbs*) combined with sufficient energy-storage capacitance.

In applications that do not have large energy-storage electrolytic capacitors on one or both sides of the shunt, an input overstress condition can result from an excessive dV/dt of the voltage applied to the input. A hard physical short is the most likely cause of this event, particularly in applications without large electrolytic capacitors present. This problem occurs because an excessive dV/dt can activate the INA3221 ESD protection in systems where large currents are available. Testing has demonstrated that the addition of 10 $\Omega$  resistors in series with each INA3221 input sufficiently protects the inputs against this dV/dt failure up to the 26V device rating.

## 7.5 Programming

### 7.5.1 Bus Overview

The INA3221 offers compatibility with both I<sup>2</sup>C and SMBus interfaces. The I<sup>2</sup>C and SMBus protocols are essentially compatible with one another.

The I<sup>2</sup>C interface is used throughout this data sheet as the primary example, with the SMBus protocol specified only when a difference between the two systems is discussed. Two I/O lines, the serial clock (SCL) and data signal line (SDA), connect the INA3221 to the bus. Both SCL and SDA are open-drain connections.

The device that initiates a data transfer is called a *controller*, and the devices controlled by the controller are *targets*. The bus must be controlled by the controller device that generates the SCL, controls the bus access, and generates start and stop conditions.

To address a specific device, the controller initiates a start condition by pulling SDA from a high to a low logic level while SCL is high. All targets on the bus shift in the target address byte on the SCL rising edge, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the target being addressed responds to the controller by generating an *acknowledge* bit and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition.

After all data are transferred, the controller generates a stop condition by pulling SDA from low to high while SCL is high. The INA3221 includes a 28ms timeout on the interface to prevent locking up the bus.

#### 7.5.1.1 Serial Bus Address

To communicate with the INA3221, the controller must first address target devices with a target address byte. This byte consists of seven address bits and a direction bit to indicate whether the intended action is a read or write operation.

The INA3221 has one address pin, A0. [Table 7-1](#) describes the pin logic levels for each of the four possible addresses. The state of the A0 pin is sampled on every bus communication and must be set before any activity on the interface occurs.

**Table 7-1. Address Pins and Target Addresses**

| A0  | TARGET ADDRESS |
|-----|----------------|
| GND | 1000000        |
| VS  | 1000001        |
| SDA | 1000010        |
| SCL | 1000011        |

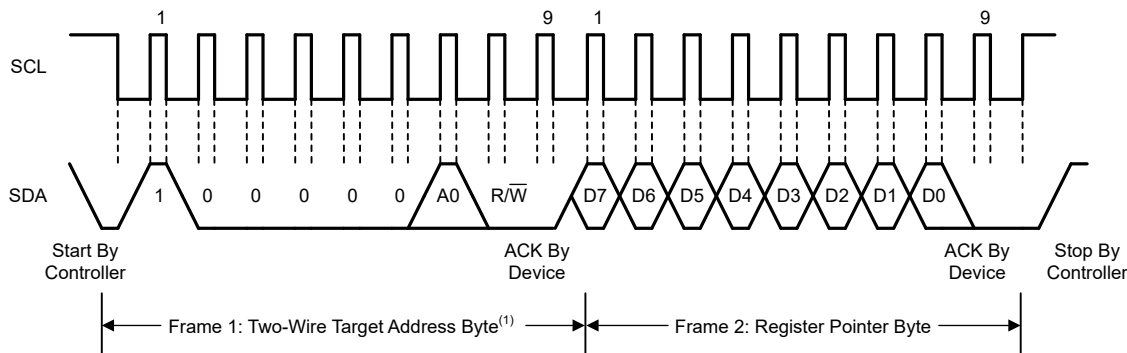
#### 7.5.1.2 Serial Interface

The INA3221 only operates as a target device on the I<sup>2</sup>C bus and SMBus. Bus connections are made using the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. While there is spike suppression integrated into the digital I/O lines, use proper layout to minimize the amount of coupling into the communication lines. Noise introduction occurs from capacitively coupling signal edges between the two communication lines themselves, or from other switching noise sources present in the system. Routing traces in parallel with ground between layers on a printed circuit board (PCB) typically reduces the effects of coupling between the communication lines. Shield communication lines to reduce the possibility of unintended noise coupling into the digital I/O lines that can be incorrectly interpreted as start or stop commands.

The INA3221 supports a transmission protocol for Fast (1kHz to 400kHz) and High-speed (1kHz to 2.44MHz) modes. All data bytes are transmitted MSB first.

## 7.5.2 Writing To and Reading From the INA3221

To access a specific INA3221 register, write the appropriate value to the register pointer. See [Table 7-3](#) for a complete list of registers and corresponding addresses. The value for the register pointer, as shown in [Figure 7-9](#), is the first byte transferred after the target address byte with the R/  $\overline{W}$  bit low. Every write operation to the INA3221 requires a register pointer value.



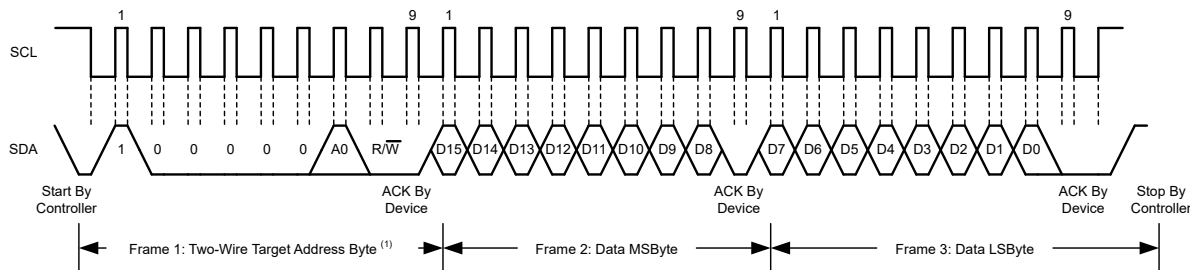
A. The value of the Target Address Byte is determined by the A0 pin setting; see [Table 7-1](#).

**Figure 7-9. Typical Register Pointer Set**

Register writes begin with the first byte transmitted by the controller. This byte is the target address, with the R/  $\overline{W}$  bit low. The INA3221 then acknowledges receipt of a valid address. The next byte transmitted by the controller is the register address that data are written to. This register address value updates the register pointer to the desired register. The next two bytes are written to the register addressed by the register pointer. The INA3221 acknowledges receipt of each data byte. The controller terminates data transfer by generating a start or stop condition.

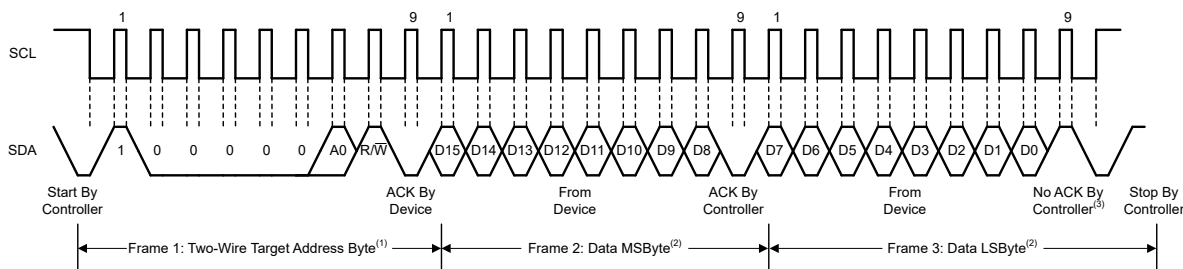
When reading from the INA3221, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, write a new value to the register pointer. This write is accomplished by issuing a target address byte with the R/  $\overline{W}$  bit low, followed by the register pointer byte. No additional data are required. The controller then generates a start condition and sends the target address byte with the R/  $\overline{W}$  bit high to initiate the read command. The next byte is transmitted by the target and is the most significant byte of the register indicated by the register pointer. This byte is followed by an acknowledge from the controller; then the target transmits the least significant byte. The controller acknowledges receipt of the data byte. The controller terminates data transfer by generating a *not-acknowledge* after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the INA3221 retains the register pointer value until the value is changed by the next write operation.

[Figure 7-10](#) and [Figure 7-11](#) show the write and read operation timing diagrams, respectively. Note that register bytes are sent most-significant byte first, followed by the least significant byte.



A. The value of the target address byte is determined by the A0 pin setting; see [Table 7-1](#).

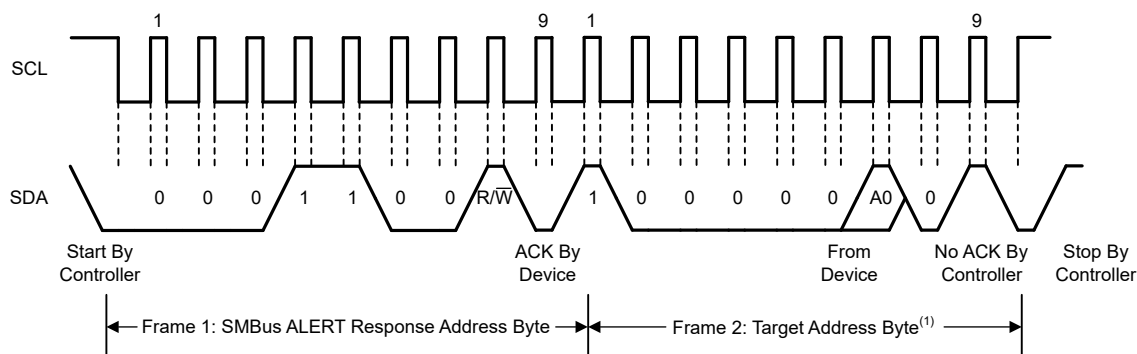
**Figure 7-10. Timing Diagram for Write Word Format**



- A. The value of the target address byte is determined by the A0 pin setting; see [Table 7-1](#).
- B. Read data are from the last register pointer location. If a new register is desired, the register pointer must be updated. See [Figure 7-9](#).
- C. The controller can also send an ACK.

### Figure 7-11. Timing Diagram for Read Word Format

Figure 7-12 shows the timing diagram for the SMBus Alert response operation.



- A. The value of the Target Address Byte is determined by the A0 pin setting; see [Table 7-1](#).

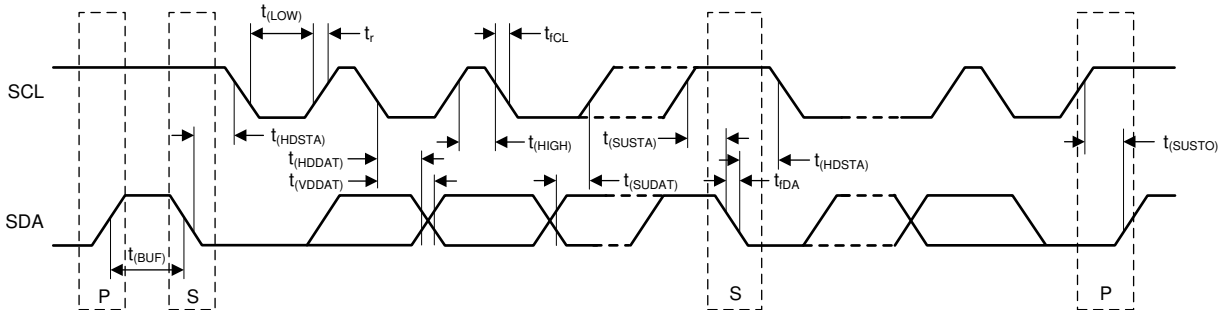
### Figure 7-12. Timing Diagram for SMBus Alert

### 7.5.2.1 High-Speed I<sup>2</sup>C Mode

When the bus is idle, the SDA and SCL lines are pulled high by the pull-up resistors. The controller generates a start condition followed by a valid serial byte with the high-speed (Hs) controller code `00001XXX`. This transmission is made in fast (400kHz) or standard (100kHz) (F/S) mode at no more than 400kHz. The INA3221 does not acknowledge the Hs controller code, but does recognize the code and switches the internal filters to support 2.44MHz operation.

The controller then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.44MHz are allowed. Instead of using a stop condition, the controller uses a repeated start conditions to secure the bus in Hs mode. A stop condition ends the Hs mode, and switches all internal INA3221 filters to support F/S mode.

Figure 7-13 shows the bus timing, and Table 7-2 lists the bus timing definitions.



**Figure 7-13. Bus Timing**

**Table 7-2. Bus Timing Definitions <sup>(1)</sup>**

| PARAMETER     |                                                                                            | FAST MODE |      | HIGH-SPEED MODE |      | UNIT |
|---------------|--------------------------------------------------------------------------------------------|-----------|------|-----------------|------|------|
|               |                                                                                            | MIN       | MAX  | MIN             | MAX  |      |
| $f_{(SCL)}$   | SCL operating frequency                                                                    | 0.001     | 0.4  | 0.001           | 2.44 | MHz  |
| $t_{(BUF)}$   | Bus free time between stop and start conditions                                            | 1300      |      | 160             |      | ns   |
| $t_{(HDSTA)}$ | Hold time after repeated START condition. After this period, the first clock is generated. | 600       |      | 160             |      | ns   |
| $t_{(SUSTA)}$ | Repeated start condition setup time                                                        | 600       |      | 160             |      | ns   |
| $t_{(SUSTO)}$ | STOP condition setup time                                                                  | 600       |      | 160             |      | ns   |
| $t_{(HDDAT)}$ | Data hold time                                                                             | 0         |      | 0               |      | ns   |
| $t_{(VDDAT)}$ | Data valid time                                                                            |           | 1200 |                 | 260  | ns   |
| $t_{(SUDAT)}$ | Data setup time                                                                            | 100       |      | 10              |      | ns   |
| $t_{(LOW)}$   | SCL clock low period                                                                       | 1300      |      | 270             |      | ns   |
| $t_{(HIGH)}$  | SCL clock high period                                                                      | 600       |      | 60              |      | ns   |
| $t_{fDA}$     | Data fall time                                                                             |           | 500  |                 | 150  | ns   |
| $t_{fCL}$     | Clock fall time                                                                            |           | 300  |                 | 40   | ns   |
| $t_r$         | Clock rise time                                                                            |           | 300  |                 | 40   | ns   |
|               | Clock rise time for SCLK $\leq$ 100kHz                                                     |           | 1000 |                 |      | ns   |

(1) Values based on a statistical analysis of a one-time sample of devices. Minimum and maximum values are not production tested.  
A0 = A1 = 0.

### 7.5.3 SMBus Alert Response

The INA3221 responds to the SMBus alert response address. The SMBus alert response provides a quick fault identification for simple target devices. When an alert occurs, the controller broadcasts the alert response target address (0001 100) with the R/  $\bar{W}$  bit set high. Following this alert response, any target devices that generated an alert self-identifies by acknowledging the alert response, and sending the respective address on the bus.

The alert response can activate several different target devices simultaneously, similar to the I<sup>2</sup>C general call. If more than one target attempts to respond, bus arbitration rules apply. The losing device does not generate an acknowledge, and continues to hold the alert line low until the interrupt is cleared. Alerts must be in Latch mode to function.



## 7.6 Register Maps

The INA3221 uses a bank of registers for holding configuration settings, measurement results, minimum and maximum limits, and status information. [Table 7-3](#) summarizes the INA3221 registers; see the [Functional Block Diagram](#) section for an illustration of the registers.

### 7.6.1 Summary of Register Set

**Table 7-3. Summary of Register Set**

| POINTER ADDRESS (Hex) | REGISTER NAME                  | DESCRIPTION                                                                                                                               | POWER-ON RESET    |      | TYPE <sup>(1)</sup> |
|-----------------------|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|-------------------|------|---------------------|
|                       |                                |                                                                                                                                           | BINARY            | HEX  |                     |
| 0                     | Configuration                  | All-register reset, shunt and bus voltage ADC conversion times and averaging, operating mode.                                             | 01110001 00100111 | 7127 | R/ $\bar{W}$        |
| 1                     | Channel-1 Shunt Voltage        | Averaged shunt voltage value.                                                                                                             | 00000000 00000000 | 0000 | R                   |
| 2                     | Channel-1 Bus Voltage          | Averaged bus voltage value.                                                                                                               | 00000000 00000000 | 0000 | R                   |
| 3                     | Channel-2 Shunt Voltage        | Averaged shunt voltage value.                                                                                                             | 00000000 00000000 | 0000 | R                   |
| 4                     | Channel-2 Bus Voltage          | Averaged bus voltage value.                                                                                                               | 00000000 00000000 | 0000 | R                   |
| 5                     | Channel-3 Shunt Voltage        | Averaged shunt voltage value.                                                                                                             | 00000000 00000000 | 0000 | R                   |
| 6                     | Channel-3 Bus Voltage          | Averaged bus voltage value.                                                                                                               | 00000000 00000000 | 0000 | R                   |
| 7                     | Channel-1 Critical Alert Limit | Contains limit value to compare each conversion value to determine if the corresponding limit has been exceeded.                          | 01111111 11111000 | 7FF8 | R/ $\bar{W}$        |
| 8                     | Channel-1 Warning Alert Limit  | Contains limit value to compare to averaged measurement to determine if the corresponding limit has been exceeded.                        | 01111111 11111000 | 7FF8 | R/ $\bar{W}$        |
| 9                     | Channel-2 Critical Alert Limit | Contains limit value to compare each conversion value to determine if the corresponding limit has been exceeded.                          | 01111111 11111000 | 7FF8 | R/ $\bar{W}$        |
| A                     | Channel-2 Warning Alert Limit  | Contains limit value to compare to averaged measurement to determine if the corresponding limit has been exceeded.                        | 01111111 11111000 | 7FF8 | R/ $\bar{W}$        |
| B                     | Channel-3 Critical Alert Limit | Contains limit value to compare each conversion value to determine if the corresponding limit has been exceeded.                          | 01111111 11111000 | 7FF8 | R/ $\bar{W}$        |
| C                     | Channel-3 Warning Alert Limit  | Contains limit value to compare to averaged measurement to determine if the corresponding limit has been exceeded.                        | 01111111 11111000 | 7FF8 | R/ $\bar{W}$        |
| D                     | Shunt-Voltage Sum              | Contains the summed value of the each of the selected shunt voltage conversions.                                                          | 00000000 00000000 | 0000 | R                   |
| E                     | Shunt-Voltage Sum Limit        | Contains limit value to compare to the Shunt Voltage Sum register to determine if the corresponding limit has been exceeded.              | 01111111 11111110 | 7FFE | R/ $\bar{W}$        |
| F                     | Mask/Enable                    | Alert configuration, alert status indication, summation control and status.                                                               | 00000000 00000010 | 0002 | R/ $\bar{W}$        |
| 10                    | Power-Valid Upper Limit        | Contains limit value to compare all bus voltage conversions to determine if the Power Valid level has been reached.                       | 00100111 00010000 | 2710 | R/ $\bar{W}$        |
| 11                    | Power-Valid Lower Limit        | Contains limit value to compare all bus voltage conversions to determine if the any voltage rail has dropped below the Power Valid range. | 00100011 00101000 | 2328 | R/ $\bar{W}$        |
| FE                    | Manufacturer ID                | Contains unique manufacturer identification number.                                                                                       | 01010100 01001001 | 5449 | R                   |
| FF                    | Die ID                         | Contains unique die identification number.                                                                                                | 00110010 00100000 | 3220 | R                   |

(1) Type: R = read-only, R/  $\bar{W}$  = read/write.

## 7.6.2 Register Descriptions

All 16-bit INA3221 registers are two 8-bit bytes via the I<sup>2</sup>C interface. [Table 7-4](#) shows a register map for the INA3221.

**Table 7-4. Register Map**

| REGISTER                       | ADDRESS<br>(Hex) | D15   | D14               | D13               | D12               | D11   | D10  | D9   | D8                   | D7                   | D6                   | D5                  | D4                  | D3                  | D2    | D1    | D0    |
|--------------------------------|------------------|-------|-------------------|-------------------|-------------------|-------|------|------|----------------------|----------------------|----------------------|---------------------|---------------------|---------------------|-------|-------|-------|
| Configuration                  | 00               | RST   | CH1 <sub>en</sub> | CH2 <sub>en</sub> | CH3 <sub>en</sub> | AVG2  | AVG1 | AVG0 | V <sub>BUS</sub> CT2 | V <sub>BUS</sub> CT1 | V <sub>BUS</sub> CT0 | V <sub>SH</sub> CT2 | V <sub>SH</sub> CT1 | V <sub>SH</sub> CT0 | MODE3 | MODE2 | MODE1 |
| Channel-1 Shunt Voltage        | 01               | SIGN  | SD11              | SD10              | SD9               | SD8   | SD7  | SD6  | SD5                  | SD4                  | SD3                  | SD2                 | SD1                 | SD0                 | —     | —     | —     |
| Channel-1 Bus Voltage          | 02               | SIGN  | BD11              | BD10              | BD9               | BD8   | BD7  | BD6  | BD5                  | BD4                  | BD3                  | BD2                 | BD1                 | BD0                 | —     | —     | —     |
| Channel-2 Shunt Voltage        | 03               | SIGN  | SD11              | SD10              | SD9               | SD8   | SD7  | SD6  | SD5                  | SD4                  | SD3                  | SD2                 | SD1                 | SD0                 | —     | —     | —     |
| Channel-2 Bus Voltage          | 04               | SIGN  | BD11              | BD10              | BD9               | BD8   | BD7  | BD6  | BD5                  | BD4                  | BD3                  | BD2                 | BD1                 | BD0                 | —     | —     | —     |
| Channel-3 Shunt Voltage        | 05               | SIGN  | SD11              | SD10              | SD9               | SD8   | SD7  | SD6  | SD5                  | SD4                  | SD3                  | SD2                 | SD1                 | SD0                 | —     | —     | —     |
| Channel-3 Bus Voltage          | 06               | SIGN  | BD11              | BD10              | BD9               | BD8   | BD7  | BD6  | BD5                  | BD4                  | BD3                  | BD2                 | BD1                 | BD0                 | —     | —     | —     |
| Channel-1 Critical-Alert Limit | 07               | C1L12 | C1L11             | C1L10             | C1L9              | C1L8  | C1L7 | C1L6 | C1L5                 | C1L4                 | C1L3                 | C1L2                | C1L1                | C1L0                | —     | —     | —     |
| Channel-1 Warning-Alert Limit  | 08               | W1L12 | W1L11             | W1L10             | W1L9              | W1L8  | W1L7 | W1L6 | W1L5                 | W1L4                 | W1L3                 | W1L2                | W1L1                | W1L0                | —     | —     | —     |
| Channel-2 Critical-Alert Limit | 09               | C2L12 | C2L11             | C2L10             | C2L9              | C2L8  | C2L7 | C2L6 | C2L5                 | C2L4                 | C2L3                 | C2L2                | C2L1                | C2L0                | —     | —     | —     |
| Channel-2 Warning-Alert Limit  | 0A               | W2L12 | W2L11             | W2L10             | W2L9              | W2L8  | W2L7 | W2L6 | W2L5                 | W2L4                 | W2L3                 | W2L2                | W2L1                | W2L0                | —     | —     | —     |
| Channel-3 Critical-Alert Limit | 0B               | C3L12 | C3L11             | C3L10             | C3L9              | C3L8  | C3L7 | C3L6 | C3L5                 | C3L4                 | C3L3                 | C3L2                | C3L1                | C3L0                | —     | —     | —     |
| Channel-3 Warning-Alert Limit  | 0C               | W3L12 | W3L11             | W3L10             | W3L9              | W3L8  | W3L7 | W3L6 | W3L5                 | W3L4                 | W3L3                 | W3L2                | W3L1                | W3L0                | —     | —     | —     |
| Shunt-Voltage Sum              | 0D               | SIGN  | SV13              | SV12              | SV11              | SV10  | SV9  | SV8  | SV7                  | SV6                  | SV5                  | SV4                 | SV3                 | SV2                 | SV1   | SV0   | —     |
| Shunt-Voltage Sum Limit        | 0E               | SIGN  | SVL13             | SVL12             | SVL11             | SVL10 | SVL9 | SVL8 | SVL7                 | SVL6                 | SVL5                 | SVL4                | SVL3                | SVL2                | SVL1  | SVL0  | —     |
| Mask/Enable                    | 0F               | —     | SCC1              | SCC2              | SCC3              | WEN   | CEN  | CF1  | CF2                  | CF3                  | SF                   | WF1                 | WF2                 | WF3                 | PVF   | TCF   | CVRF  |
| Power-Valid Upper Limit        | 10               | SIGN  | PVU11             | PVU10             | PVU9              | PVU8  | PVU7 | PVU6 | PVU5                 | PVU4                 | PVU3                 | PVU2                | PVU1                | PVU0                | —     | —     | —     |
| Power-Valid Lower Limit        | 11               | SIGN  | PVL11             | PVL10             | PVL9              | PVL8  | PVL7 | PVL6 | PVL5                 | PVL4                 | PVL3                 | PVL2                | PVL1                | PVL0                | —     | —     | —     |
| Manufacturer ID                | FE               | 0     | 1                 | 0                 | 1                 | 0     | 1    | 0    | 0                    | 0                    | 1                    | 0                   | 0                   | 1                   | 0     | 0     | 1     |
| Die ID                         | FF               | 0     | 0                 | 1                 | 1                 | 0     | 0    | 1    | 0                    | 0                    | 0                    | 1                   | 0                   | 0                   | 0     | 0     | 0     |

### 7.6.2.1 Configuration Register (address = 00h) [reset = 7127h]

The Configuration register settings control the operating modes for the shunt- and bus-voltage measurements for the three input channels. This register controls the conversion time settings for both the shunt- and bus-voltage measurements and the averaging mode used. The Configuration register is used to independently enable or disable each channel, as well as select the operating mode that controls which signals are selected to be measured.

This register can be read from at any time without impacting or affecting either device settings or conversions in progress. Writing to this register halts any conversion in progress until the write sequence is completed, resulting in a new conversion starting, based on the new Configuration register contents. This architecture prevents any uncertainty in the conditions used for the next completed conversion.

**Table 7-5. Configuration Register**

| 15   | 14                | 13                | 12                | 11   | 10   | 9    | 8                    | 7                    | 6                    | 5                   | 4                   | 3                   | 2      | 1      | 0      |
|------|-------------------|-------------------|-------------------|------|------|------|----------------------|----------------------|----------------------|---------------------|---------------------|---------------------|--------|--------|--------|
| RST  | CH1 <sub>en</sub> | CH2 <sub>en</sub> | CH3 <sub>en</sub> | AVG2 | AVG1 | AVG0 | V <sub>BUS</sub> CT2 | V <sub>BUS</sub> CT1 | V <sub>BUS</sub> CT0 | V <sub>SH</sub> CT2 | V <sub>SH</sub> CT1 | V <sub>SH</sub> CT0 | MODE 3 | MODE 2 | MODE 1 |
| RW-0 | RW-1              | RW-1              | RW-1              | RW-0 | RW-0 | RW-0 | RW-1                 | RW-0                 | RW-0                 | RW-1                | RW-0                | RW-0                | RW-1   | RW-1   | RW-1   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-6. Configuration Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                                                                                                                                                                                      |
|------|------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | RST                    | R/W  | 0h    | Reset bit. Set this bit = 1 to generate a system reset that is the same as a power-on reset (POR). This bit resets all registers to default values and self-clears.                                                                              |
| 14   | CH1 <sub>en</sub>      | R/W  | 7h    | Channel enable mode. These bits allow each channel to be independently enabled or disabled.<br>0 = Channel disable<br>1 = Channel enable (default)                                                                                               |
| 13   | CH2 <sub>en</sub>      |      |       |                                                                                                                                                                                                                                                  |
| 12   | CH3 <sub>en</sub>      |      |       |                                                                                                                                                                                                                                                  |
| 11-9 | AVG2-0                 | R/W  | 0h    | Averaging mode. These bits set the number of samples that are collected and averaged together.<br>000 = 1 (default)<br>001 = 4<br>010 = 16<br>011 = 64<br>100 = 128<br>101 = 256<br>110 = 512<br>111 = 1024                                      |
| 8-6  | V <sub>BUS</sub> CT2-0 | R/W  | 4h    | Bus-voltage conversion time. These bits set the conversion time for the bus-voltage measurement.<br>000 = 140μs<br>001 = 204μs<br>010 = 332μs<br>011 = 588μs<br>100 = 1.1ms (default)<br>101 = 2.116ms<br>110 = 4.156ms<br>111 = 8.244ms         |
| 5-3  | V <sub>SH</sub> CT2-0  | R/W  | 4h    | Shunt-voltage conversion time. These bits set the conversion time for the shunt-voltage measurement.<br>The conversion-time bit settings for V <sub>SH</sub> CT2-0 are the same as V <sub>BUS</sub> CT2-0 (bits 8-6) listed in the previous row. |

**Table 7-6. Configuration Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-----|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2-0 | MODE3-1 | R/W  | 7h    | <p>Operating mode. These bits select continuous, single-shot (triggered), or power-down mode of operation. These bits default to continuous shunt and bus mode.</p> <p>000 = Power-down<br/>           001 = Shunt voltage, single-shot (triggered)<br/>           010 = Bus voltage, single-shot (triggered)<br/>           011 = Shunt and bus, single-shot (triggered)<br/>           100 = Power-down<br/>           101 = Shunt voltage, continuous<br/>           110 = Bus voltage, continuous<br/>           111 = Shunt and bus, continuous (default)</p> |

### 7.6.2.2 Channel-1 Shunt-Voltage Register (address = 01h), [reset = 00h]

This register contains the averaged shunt-voltage measurement for channel 1. This register stores the current shunt-voltage reading,  $V_{SHUNT}$ , for channel 1. Negative numbers are represented in twos complement format. Generate the twos complement of a negative number by complementing the absolute value binary number and adding 1. Extend the sign, denoting a negative number by setting MSB = 1.

Full-scale range = 163.8mV (decimal = 7FF8); LSB (SD0): 40 $\mu$ V.

Example: For a value of  $V_{SHUNT} = -80$ mV:

1. Take the absolute value: 80mV
2. Translate this number to a whole decimal number (80mV / 40 $\mu$ V) = 2000
3. Convert this number to binary = 011 1110 1000 0\_\_\_ (last three bits are set to 0)
4. Complement the binary result = 100 0001 0111 1111
5. Add 1 to the complement to create the twos complement result = 100 0001 1000 0000
6. Extend the sign and create the 16-bit word: 1100 0001 1000 0000 = C180h

**Table 7-7. Channel-1 Shunt-Voltage Register**

| 15   | 14   | 13   | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| SIGN | SD11 | SD10 | SD9 | SD8 | SD7 | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 | —   | —   | —   |
| R-0  | R-0  | R-0  | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-8. Channel-1 Shunt-Voltage Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                       |
|------|----------|------|-------|-----------------------------------------------------------------------------------|
| 15   | SIGN     | R    | 0h    | Sign bit.<br>0 = positive number<br>1 = negative number in twos complement format |
| 14-3 | SD11-0   | R    | 0h    | Channel-1 shunt-voltage data bits                                                 |
| 2-0  | Reserved | R    | 0h    | Reserved                                                                          |

### 7.6.2.3 Channel-1 Bus-Voltage Register (address = 02h) [reset = 00h]

This register stores the bus voltage reading,  $V_{BUS}$ , for channel 1. Full-scale range = 32.76V (decimal = 7FF8); LSB (BD0) = 8mV. Although the input range is 26V, the full-scale range of the ADC scaling is 32.76V. Do not apply more than 26V.

**Table 7-9. Channel-1 Bus-Voltage Register**

| 15   | 14   | 13   | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| SIGN | BD11 | BD10 | BD9 | BD8 | BD7 | BD6 | BD5 | BD4 | BD3 | BD2 | BD1 | BD0 | —   | —   | —   |
| R-0  | R-0  | R-0  | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-10. Channel-1 Bus-Voltage Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                        |
|------|----------|------|-------|------------------------------------------------------------------------------------|
| 15   | SIGN     | R    | 0h    | Sign bit.<br>0 = positive number<br>1 = negative number in twos complement format. |
| 14-3 | BD11-0   | R    | 0h    | Channel-1 bus-voltage data bits                                                    |
| 2-0  | Reserved | R    | 0h    | Reserved                                                                           |

#### 7.6.2.4 Channel-2 Shunt-Voltage Register (address = 03h) [reset = 00h]

This register contains the averaged shunt voltage measurement for channel 2. Full-scale range = 163.8mV (decimal = 7FF8); LSB (SD0): 40μV. Although the input range is 26V, the full-scale range of the ADC scaling is 32.76V. Do not apply more than 26V.

**Table 7-11. Channel-2 Shunt-Voltage Register**

| 15   | 14   | 13   | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| SIGN | SD11 | SD10 | SD9 | SD8 | SD7 | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 | —   | —   | —   |
| R-0  | R-0  | R-0  | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-12. Channel-2 Shunt-Voltage Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                       |
|------|----------|------|-------|-----------------------------------------------------------------------------------|
| 15   | SIGN     | R    | 0h    | Sign bit.<br>0 = positive number<br>1 = negative number in twos complement format |
| 14-3 | SD11-0   | R    | 0h    | Channel-2 shunt-voltage data bits                                                 |
| 2-0  | Reserved | R    | 0h    | Reserved                                                                          |

#### 7.6.2.5 Channel-2 Bus-Voltage Register (address = 04h) [reset = 00h]

This register stores the bus voltage reading,  $V_{BUS}$ , for channel 2. Full-scale range = 32.76V (decimal = 7FF8); LSB (BD0) = 8mV. Although the input range is 26V, the full-scale range of the ADC scaling is 32.76V. Do not apply more than 26V.

**Table 7-13. Channel-2 Bus-Voltage Register**

| 15   | 14   | 13   | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| SIGN | BD11 | BD10 | BD9 | BD8 | BD7 | BD6 | BD5 | BD4 | BD3 | BD2 | BD1 | BD0 | —   | —   | —   |
| R-0  | R-0  | R-0  | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-14. Channel-2 Bus-Voltage Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                       |
|------|----------|------|-------|-----------------------------------------------------------------------------------|
| 15   | SIGN     | R    | 0h    | Sign bit.<br>0 = positive number<br>1 = negative number in twos complement format |
| 14-3 | BD11-0   | R    | 0h    | Channel-2 bus-voltage data bits                                                   |
| 2-0  | Reserved | R    | 0h    | Reserved                                                                          |

### 7.6.2.6 Channel-3 Shunt-Voltage Register (address = 05h) [reset = 00h]

This register contains the averaged shunt voltage measurement for channel 3. Full-scale range = 163.8mV (decimal = 7FF8); LSB (SD0): 40μV.

**Table 7-15. Channel-3 Shunt-Voltage Register**

| 15   | 14   | 13   | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| SIGN | SD11 | SD10 | SD9 | SD8 | SD7 | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 | —   | —   | —   |
| R-0  | R-0  | R-0  | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-16. Channel-3 Shunt-Voltage Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                       |
|------|----------|------|-------|-----------------------------------------------------------------------------------|
| 15   | SIGN     | R    | 0h    | Sign bit.<br>0 = positive number<br>1 = negative number in twos complement format |
| 14-3 | SD11-0   | R    | 0h    | Channel-3 shunt-voltage data bits                                                 |
| 2-0  | Reserved | R    | 0h    | Reserved                                                                          |

### 7.6.2.7 Channel-3 Bus-Voltage Register (address = 06h) [reset = 00h]

This register stores the bus voltage reading,  $V_{BUS}$ , for channel 3. Full-scale range = 32.76V (decimal = 7FF8); LSB (BD0) = 8mV. Although the input range is 26V, the full-scale range of the ADC scaling is 32.76V. Do not apply more than 26V.

**Table 7-17. Channel-3 Bus-Voltage Register**

| 15   | 14   | 13   | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| SIGN | BD11 | BD10 | BD9 | BD8 | BD7 | BD6 | BD5 | BD4 | BD3 | BD2 | BD1 | BD0 | —   | —   | —   |
| R-0  | R-0  | R-0  | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-18. Channel-3 Bus-Voltage Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                       |
|------|----------|------|-------|-----------------------------------------------------------------------------------|
| 15   | SIGN     | R    | 0h    | Sign bit.<br>0 = positive number<br>1 = negative number in twos complement format |
| 14-3 | BD11-0   | R    | 0h    | Channel-3 bus-voltage data bits                                                   |
| 2-0  | Reserved | R    | 0h    | Reserved                                                                          |

#### 7.6.2.8 Channel-1 Critical-Alert Limit Register (address = 07h) [reset = 7FF8h]

This register contains the value used to compare to each shunt voltage conversion on channel 1 to detect fast overcurrent events.

**Table 7-19. Channel-1 Critical-Alert Limit Register**

| 15    | 14    | 13    | 12   | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| C1L12 | C1L11 | C1L10 | C1L9 | C1L8 | C1L7 | C1L6 | C1L5 | C1L4 | C1L3 | C1L2 | C1L1 | C1L0 | —    | —    | —    |
| RW-0  | RW-1  | RW-1  | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-0 | RW-0 | RW-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-20. Channel-1 Critical-Alert Limit Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                              |
|------|----------|------|-------|------------------------------------------|
| 15-3 | C1L12-0  | R/W  | FFFh  | Channel-1 critical-alert-limit data bits |
| 2-0  | Reserved | R/W  | 0h    | Reserved                                 |

#### 7.6.2.9 Warning-Alert Channel-1 Limit Register (address = 08h) [reset = 7FF8h]

This register contains the value used to compare to the averaged shunt voltage value of channel 1 to detect a longer duration overcurrent event.

**Table 7-21. Channel-1 Warning-Alert Limit Register**

| 15    | 14    | 13    | 12   | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| W1L12 | W1L11 | W1L10 | W1L9 | W1L8 | W1L7 | W1L6 | W1L5 | W1L4 | W1L3 | W1L2 | W1L1 | W1L0 | —    | —    | —    |
| RW-0  | RW-1  | RW-1  | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-0 | RW-0 | RW-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-22. Channel-1 Warning-Alert Limit Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                             |
|------|----------|------|-------|-----------------------------------------|
| 15-3 | W1L12-0  | R/W  | FFFh  | Channel-1 warning-alert-limit data bits |
| 2-0  | Reserved | R/W  | 0h    | Reserved                                |

#### 7.6.2.10 Channel-2 Critical-Alert Limit Register (address = 09h) [reset = 7FF8h]

This register contains the value used to compare to each shunt voltage conversion on channel 2 to detect fast overcurrent events.

**Table 7-23. Channel-2 Critical-Alert Limit Register**

| 15    | 14    | 13    | 12   | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| C2L12 | C2L11 | C2L10 | C2L9 | C2L8 | C2L7 | C2L6 | C2L5 | C2L4 | C2L3 | C2L2 | C2L1 | C2L0 | —    | —    | —    |
| RW-0  | RW-1  | RW-1  | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-0 | RW-0 | RW-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-24. Channel-2 Critical-Alert Limit Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                              |
|------|----------|------|-------|------------------------------------------|
| 15-3 | C2L12-0  | R/W  | FFFh  | Channel-2 critical-alert-limit data bits |
| 2-0  | Reserved | R/W  | 0h    | Reserved                                 |



### 7.6.2.11 Channel-2 Warning-Alert Limit Register (address = 0Ah) [reset = 7FF8h]

This register contains the value used to compare to the averaged shunt voltage value of channel 2 to detect a longer duration overcurrent event.

**Table 7-25. Channel-2 Warning-Alert Limit Register**

| 15    | 14    | 13    | 12   | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| W2L12 | W2L11 | W2L10 | W2L9 | W2L8 | W2L7 | W2L6 | W2L5 | W2L4 | W2L3 | W2L2 | W2L1 | W2L0 | —    | —    | —    |
| RW-0  | RW-1  | RW-1  | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-0 | RW-0 | RW-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-26. Channel-2 Warning-Alert Limit Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                             |
|------|----------|------|-------|-----------------------------------------|
| 15-3 | W2L12-0  | R/W  | FFFh  | Channel-2 warning-alert-limit data bits |
| 2-0  | Reserved | R/W  | 0h    | Reserved                                |

### 7.6.2.12 Channel-3 Critical-Alert Limit Register (address = 0Bh) [reset = 7FF8h]

This register contains the value used to compare to each shunt voltage conversion on channel 3 to detect fast overcurrent events.

**Table 7-27. Channel-3 Critical-Alert Limit Register**

| 15    | 14    | 13    | 12   | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| C3L12 | C3L11 | C3L10 | C3L9 | C3L8 | C3L7 | C3L6 | C3L5 | C3L4 | C3L3 | C3L2 | C3L1 | C3L0 | —    | —    | —    |
| RW-0  | RW-1  | RW-1  | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-0 | RW-0 | RW-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-28. Channel-3 Critical-Alert Limit Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                              |
|------|----------|------|-------|------------------------------------------|
| 15-3 | C3L12-0  | R/W  | FFFh  | Channel-3 critical-alert-limit data bits |
| 2-0  | Reserved | R/W  | 0h    | Reserved                                 |

### 7.6.2.13 Channel-3 Warning-Alert Limit Register (address = 0Ch) [reset = 7FF8h]

This register contains the value used to compare to the averaged shunt voltage value of channel 3 to detect a longer duration overcurrent event.

**Table 7-29. Channel-3 Warning-Alert Limit Register**

| 15    | 14    | 13    | 12   | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| W3L12 | W3L11 | W3L10 | W3L9 | W3L8 | W3L7 | W3L6 | W3L5 | W3L4 | W3L3 | W3L2 | W3L1 | W3L0 | —    | —    | —    |
| RW-0  | RW-1  | RW-1  | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-0 | RW-0 | RW-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-30. Channel-3 Warning-Alert Limit Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                             |
|------|----------|------|-------|-----------------------------------------|
| 15-3 | W3L12-0  | R/W  | FFFh  | Channel-3 warning-alert limit data bits |
| 2-0  | Reserved | R/W  | 0h    | Reserved                                |

#### 7.6.2.14 Shunt-Voltage Sum Register (address = 0Dh) [reset = 00h]

This register contains the sum of the single conversion shunt voltages of the selected channels based on the summation control bits 12, 13, and 14 in the Mask/Enable register.

This register is updated with the most recent sum following each complete cycle of all selected channels. The Shunt-Voltage Sum register LSB value is 40μV.

**Table 7-31. Shunt-Voltage Sum Register**

| 15   | 14   | 13   | 12   | 11   | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| SIGN | SV13 | SV12 | SV11 | SV10 | SV9 | SV8 | SV7 | SV6 | SV5 | SV4 | SV3 | SV2 | SV1 | SV0 | —   |
| R-0  | R-0  | R-0  | R-0  | R-0  | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-32. Shunt-Voltage Sum Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                       |
|------|----------|------|-------|-----------------------------------------------------------------------------------|
| 15   | SIGN     | R    | 0h    | Sign bit.<br>0 = positive number<br>1 = negative number in twos complement format |
| 14-1 | SV13-0   | R    | 0h    | Shunt-voltage sum data bits                                                       |
| 0    | Reserved | R    | 0h    | Reserved                                                                          |

#### 7.6.2.15 Shunt-Voltage Sum-Limit Register (address = 0Eh) [reset = 7FEh]

This register contains the value that is compared to the Shunt-Voltage Sum register value following each completed cycle of all selected channels to detect for system overcurrent events. The Shunt-Voltage Sum-Limit register LSB value is 40μV.

**Table 7-33. Shunt-Voltage Sum-Limit Register**

| 15   | 14    | 13    | 12    | 11    | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|------|
| SIGN | SVL13 | SVL12 | SVL11 | SVL10 | SVL9 | SVL8 | SVL7 | SVL6 | SVL5 | SVL4 | SVL3 | SVL2 | SVL1 | SVL0 | —    |
| RW-0 | RW-1  | RW-1  | RW-1  | RW-1  | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-1 | RW-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-34. Shunt-Voltage Sum-Limit Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                       |
|------|----------|------|-------|-----------------------------------------------------------------------------------|
| 15   | SIGN     | R    | 0h    | Sign bit.<br>0 = positive number<br>1 = negative number in twos complement format |
| 14-1 | SVL13-0  | R    | 0h    | Shunt-voltage sum-limit data bits                                                 |
| 0    | Reserved | R    | 0h    | Reserved                                                                          |

### 7.6.2.16 Mask/Enable Register (address = 0Fh) [reset = 0002h]

This register selects which function is enabled to control the Critical alert and Warning alert pins, and how each warning alert responds to the corresponding channel. Read the Mask/Enable register to clear any flag results present. Writing to this register does not clear the flag bit status. To make sure that there is no uncertainty in the warning function setting that resulted in a flag bit being set, the Mask/Enable register must be read from to clear the flag bit status before changing the warning function setting.

**Table 7-35. Mask/Enable Register**

| 15   | 14   | 13   | 12   | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| —    | SCC1 | SCC2 | SCC3 | WEN  | CEN  | CF1  | CF2  | CF3  | SF   | WF1  | WF2  | WF3  | PVF  | TCF  | CVRF |
| RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-1 | RW-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-36. Mask/Enable Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | Reserved | R/W  | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 14-12 | SCC1-3   | R/W  | 0h    | Summation channel control. These bits determine which shunt voltage measurement channels are enabled to fill the Shunt-Voltage Sum register. The selection of these bits does not impact the individual channel enable or disable status, or the corresponding channel measurements. The corresponding bit is used to select if the channel is used to fill the Shunt-Voltage Sum register.<br>0 = Disabled (default)<br>1 = Enabled |
| 11    | WEN      | R/W  | 0h    | Warning alert latch enable. These bits configure the latching feature of the Warning alert pin.<br>0 = Transparent (default)<br>1 = Latch enabled                                                                                                                                                                                                                                                                                    |
| 10    | CEN      | R/W  | 0h    | Critical alert latch enable. These bits configure the latching feature of the Critical alert pin.<br>0 = Transparent (default)<br>1 = Latch enabled                                                                                                                                                                                                                                                                                  |
| 9-7   | CF1-3    | R/W  | 0h    | Critical-alert flag indicator. These bits are asserted if the corresponding channel measurement has exceeded the critical alert limit resulting in the Critical alert pin being asserted. Read these bits to determine which channel caused the critical alert. The critical alert flag bits are cleared when the Mask/Enable register is read back.                                                                                 |
| 6     | SF       | R/W  | 0h    | Summation-alert flag indicator. This bit is asserted if the Shunt Voltage Sum register exceeds the Shunt Voltage Sum Limit register. If the summation alert flag is asserted, the Critical alert pin is also asserted. The Summation Alert Flag bit is cleared when the Mask/Enable register is read back.                                                                                                                           |
| 5-3   | WF1-3    | R/W  | 0h    | Warning-alert flag indicator. These bits are asserted if the corresponding channel averaged measurement has exceeded the warning alert limit, resulting in the Warning alert pin being asserted. Read these bits to determine which channel caused the warning alert. The Warning Alert Flag bits clear when the Mask/Enable register is read back.                                                                                  |
| 2     | PVF      | R/W  | 0h    | Power-valid-alert flag indicator. This bit can be used to be able to determine if the power valid (PV) alert pin has been asserted through software rather than hardware. The bit setting corresponds to the status of the PV pin. This bit does not clear until the condition that caused the alert is removed, and the PV pin has cleared.                                                                                         |
| 1     | TCF      | R/W  | 11h   | Timing-control-alert flag indicator. Use this bit to determine if the timing control (TC) alert pin has been asserted through software rather than hardware. The bit setting corresponds to the status of the TC pin. This bit does not clear after it has been asserted unless the power is recycled or a software reset is issued. The default state for the timing control alert flag is high.                                    |

**Table 7-36. Mask/Enable Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | CVRF  | R/W  | 0h    | Conversion-ready flag. Although the INA3221 can be read at any time, and the data from the last conversion are available, the conversion ready bit is provided to help coordinate single-shot conversions. The conversion bit is set after all conversions are complete. Conversion ready clears under the following conditions: <ol style="list-style-type: none"> <li>Writing the Configuration register (except for power-down or disable-mode selections).</li> <li>Reading the Mask/Enable register.</li> </ol> |

#### 7.6.2.17 Power-valid Upper-limit Register (address = 10h) [reset = 2710h]

This register contains the value used to determine if the power-valid conditions are met. The power-valid condition is reached when all bus-voltage channels exceed the value set in this limit register. When the power-valid condition is met, the PV alert pin asserts high to indicate that the INA3221 has confirmed all bus voltage channels are above the power-valid upper-limit value. For the power-valid conditions to be monitored, the bus measurements must be enabled through one of the corresponding MODE bits set in the Configuration register. The power-valid upper-limit LSB value is 8mV. Power-on reset value is 2710h = 10.000V.

**Table 7-37. Power-Valid Upper-Limit Register**

| 15   | 14    | 13    | 12   | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|------|-------|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| SIGN | PVU11 | PVU10 | PVU9 | PVU8 | PVU7 | PVU6 | PVU5 | PVU4 | PVU3 | PVU2 | PVU1 | PVU0 | —    | —    | —    |
| R-0  | RW-0  | RW-1  | RW-0 | RW-0 | RW-1 | RW-1 | RW-1 | RW-0 | RW-0 | RW-0 | RW-1 | RW-0 | RW-0 | RW-0 | RW-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-38. Power-Valid Upper-Limit Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                       |
|------|----------|------|-------|-----------------------------------|
| 15   | SIGN     | R    | 0h    | Power-valid upper-limit data bits |
| 14-3 | PVU11-0  | R/W  | 4E2h  | Power-valid upper-limit data bits |
| 2-0  | Reserved | R/W  | 0h    | Reserved                          |

#### 7.6.2.18 Power-Valid Lower-Limit Register (address = 11h) [reset = 2328h]

This register contains the value used to determine if any of the bus-voltage channels drops below the power-valid lower-limit when the power-valid conditions are met. This limit contains the value used to compare all bus-channel readings to verify that all channels remain above the power-valid lower-limit, thus maintaining the power-valid condition. If any bus-voltage channel drops below the power-valid lower-limit, the PV alert pin pulls low to indicate that the INA3221 detects a bus voltage reading below the power-valid lower-limit. For the power-valid condition to be monitored, the bus measurements must be enabled through the mode (MODE3-1) bits set in the Configuration register. The power-valid lower-limit LSB value is 8mV. Power-on reset value is 2328h = 9.000V.

**Table 7-39. Power-Valid Lower-Limit Register**

| 15   | 14    | 13    | 12   | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|------|-------|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| SIGN | PVL11 | PVL10 | PVL9 | PVL8 | PVL7 | PVL6 | PVL5 | PVL4 | PVL3 | PVL2 | PVL1 | PVL0 | —    | —    | —    |
| R-0  | RW-0  | RW-1  | RW-0 | RW-0 | RW-0 | RW-1 | RW-1 | RW-0 | RW-0 | RW-1 | RW-0 | RW-1 | RW-0 | RW-0 | RW-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-40. Power-Valid Lower-Limit Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                       |
|------|---------|------|-------|-----------------------------------|
| 15   | SIGN    | R    | 0h    | Power-valid lower-limit data bits |
| 14-3 | PVL11-0 | R/W  | 465h  | Power-valid lower-limit data bits |

**Table 7-40. Power-Valid Lower-Limit Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 2-0 | Reserved | R/W  | 0h    | Reserved    |

**7.6.2.19 Manufacturer ID Register (address = FEh) [reset = 5449h]**

This register contains a factory-programmable identification value that identifies this device as being manufactured by Texas Instruments. This register distinguishes this device from other devices that are on the same I<sup>2</sup>C bus. The contents of this register are 5449h, or TI in ASCII.

**Table 7-41. Manufacturer ID Register**

|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
| R-0 | R-1 | R-0 | R-1 | R-0 | R-1 | R-0 | R-0 | R-0 | R-1 | R-0 | R-0 | R-1 | R-0 | R-0 | R-1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-42. Manufacturer ID Register Field Descriptions**

| Bit  | Field | Type | Reset | Description          |
|------|-------|------|-------|----------------------|
| 15-0 | D15-0 | R    | 5449h | Manufacturer ID bits |

**7.6.2.20 Die ID Register (address = FFh) [reset = 3220h]**

This register contains a factory-programmable identification value that identifies this device as an INA3221. This register distinguishes this device from other devices that are on the same I<sup>2</sup>C bus. The Die ID for the INA3221 is 3220h.

**Table 7-43. Die ID Register**

|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
| R-0 | R-0 | R-1 | R-1 | R-0 | R-0 | R-1 | R-0 | R-0 | R-0 | R-1 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-44. Die ID Register Field Descriptions**

| Bit  | Field | Type | Reset | Description |
|------|-------|------|-------|-------------|
| 15-0 | D15-0 | R    | 3220h | Die ID bits |

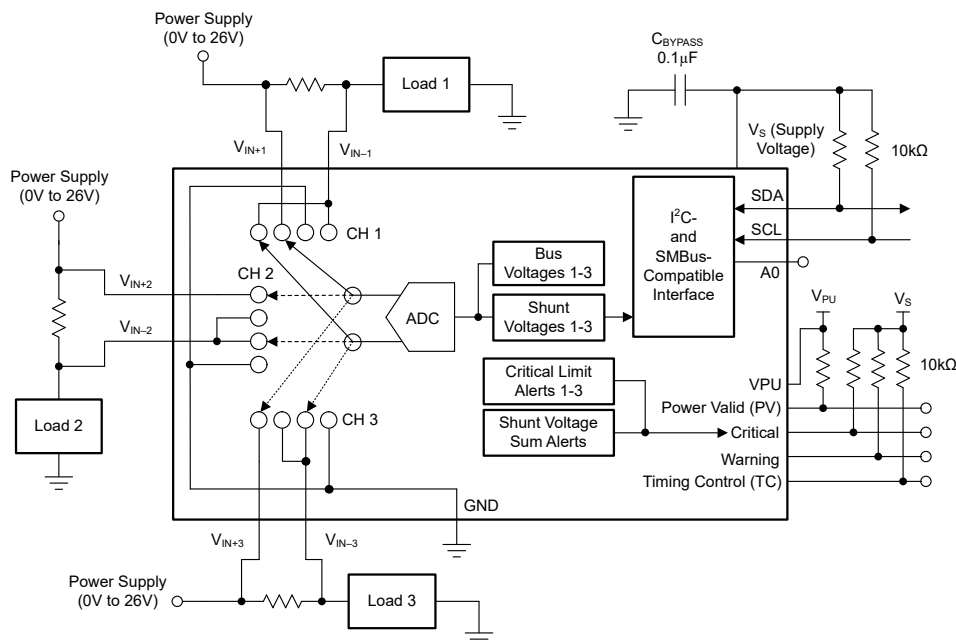
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

INA3221 is a three-channel current and bus voltage monitor with I<sup>2</sup>C/SMBUS-compatible interface. It features programmable conversion times and averaging modes and offers both critical and warning alerts to detect multiple programmable out-of-range conditions for each channel.

The INA3221 measures the voltage developed across a current-sensing resistor when current passes through the resistor. The device also measures the bus supply voltage at the IN- pin. Multiple monitoring functions are supported using four alert pins: Critical, Warning, PV, and TC. Programmable thresholds make sure operation is within desired operating conditions. This design illustrates the ability of the Critical alert pin to respond to a set threshold.

**Figure 8-1** illustrates a typical INA3221 application circuit using all three channels. For best performance, use a 0.1µF ceramic capacitor for power-supply bypassing, placed as close as possible to the supply and ground pins. The digital pins (SCL, SDA, Critical, Warning, TC) are connected to supply through pull-up resistors. The power valid (PV) alert pin is connected to the VPU pin through a pull-up resistor to enable power-valid monitoring.



### Figure 8-1. INA3221 as an Overcurrent Sensor

### 8.2.1 Design Requirements

For this design example, use the input parameters shown in [Table 8-1](#). All other register settings are default.

**Table 8-1. Design Parameters**

| DESIGN PARAMETER                      | EXAMPLE VALUE             |
|---------------------------------------|---------------------------|
| Supply voltage, $V_S$                 | 5V                        |
| Pull-up resistors                     | 10k $\Omega$              |
| Input range                           | -163.84 to +163.8         |
| Enabled channel                       | CH1                       |
| Operating mode                        | Shunt voltage, continuous |
| Average setting                       | 1                         |
| Critical alert limit                  | 80mV                      |
| Critical Alert Limit register setting | 7D0h                      |

### 8.2.2 Detailed Design Procedure

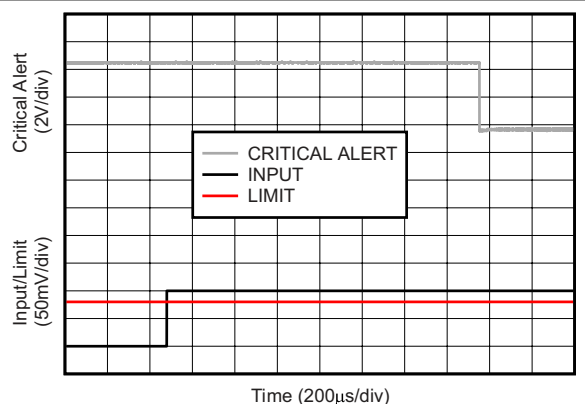
This design shows two shunt voltage conversion times to demonstrate the difference in the alert response times. This design generates a critical-alert response when the input voltage exceeds 80mV on channel 1. See [Table 8-1](#) for all design parameters.

For the first example the shunt voltage conversion time is set to 1.1ms. When the input signal exceeds 80mV, the Critical alert pin pulls low after the conversion cycle completes, indicating an overcurrent condition, as shown in [Figure 8-2](#).

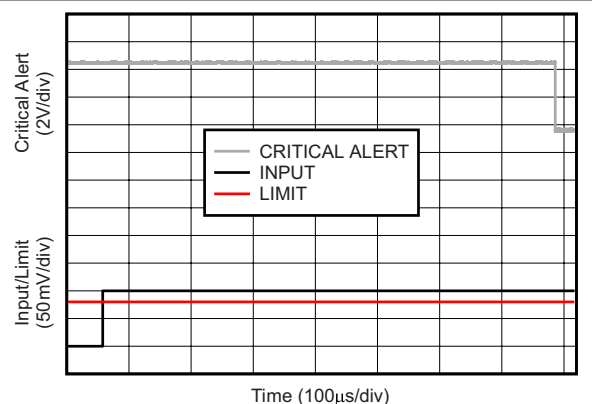
For the second example, the conversion time is set to 588 $\mu$ s, and the response is shown in [Figure 8-3](#).

### 8.2.3 Application Curves

[Figure 8-2](#) shows the Critical alert pin response to a shunt voltage overlimit of 80mV for a conversion time of 1.1ms. [Figure 8-3](#) shows the response for the same limit, but with the conversion time reduced to 588 $\mu$ s.



**Figure 8-2. Critical Alert Response for 1.1ms Conversion Time**



**Figure 8-3. Critical Alert Response for 588 $\mu$ s Conversion Time**

## 8.3 Power Supply Recommendations

The input circuitry of the device can accurately measure signals on common-mode voltages beyond the power supply voltage,  $V_S$ . For example, the voltage applied to the  $V_S$  power supply terminal can be 5V, whereas the load power-supply voltage being monitored (the common-mode voltage) on any one of the three channels can be as high as 26V. Note also that the device can withstand the full 0V to 26V range at the input terminals,

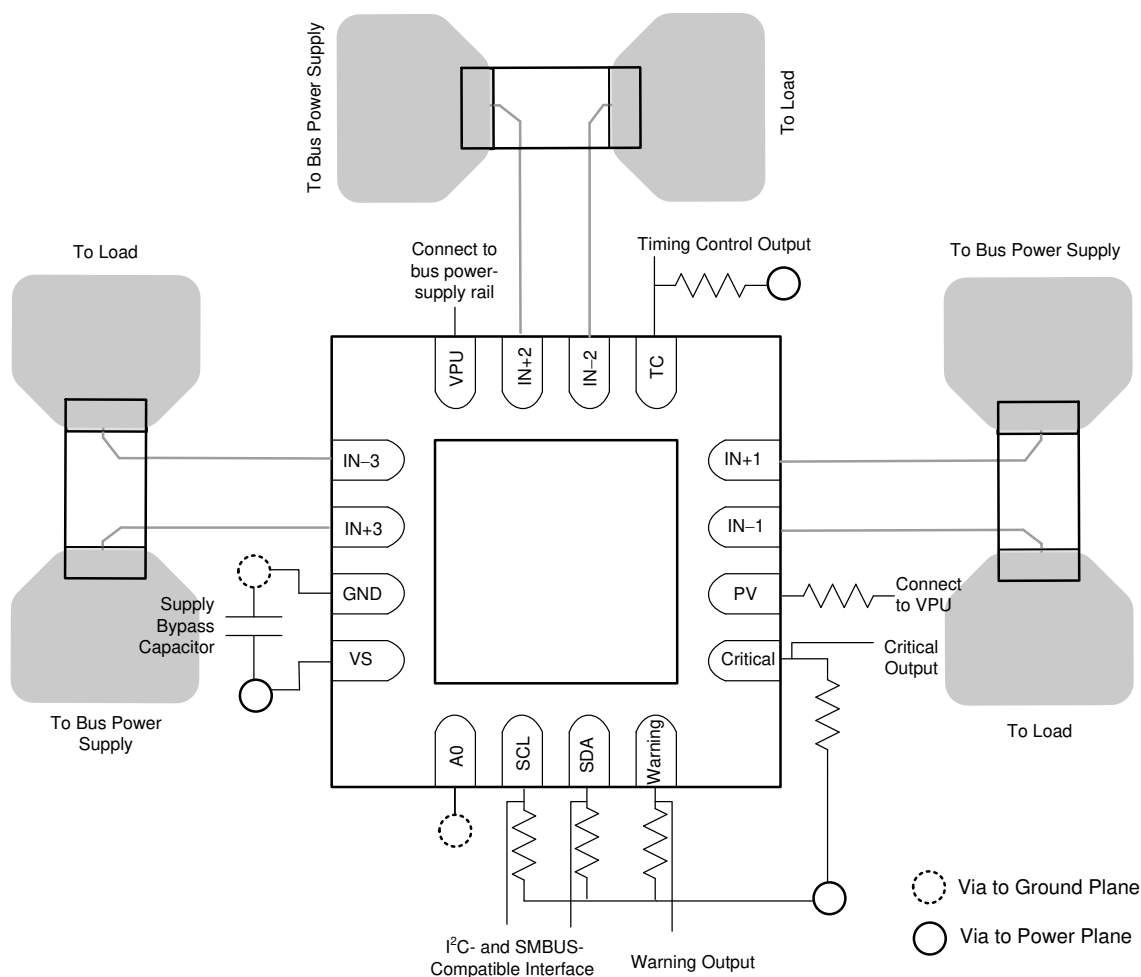
regardless of whether the device has power applied or not. Place the required power-supply bypass capacitors as close as possible to the supply and ground terminals of the device to provide stability. A typical value for this supply bypass capacitor is 0.1μF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

## 8.4 Layout

### 8.4.1 Layout Guidelines

Connect the input pins (IN+ and IN–) of all the used channels to the sensing resistor using a Kelvin connection or a 4-wire connection. These connection techniques verify that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current-sensing resistor, any additional high-current carrying impedance causes significant measurement errors. Place the power-supply bypass capacitor as close as possible to the supply and ground pins.

### 8.4.2 Layout Example



**Figure 8-4. Layout Example**



## 9 Device and Documentation Support

### 9.1 Device Support

#### 9.1.1 Development Support

- For INA3221 evaluation module (EVM), go to [www.ti.com/tool/INA3221EVM](http://www.ti.com/tool/INA3221EVM)

### 9.2 Documentation Support

#### 9.2.1 Related Documentation

- Texas Instruments, [INA3221EVM User Guide](#)

### 9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.5 Trademarks

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### 9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (September 2014) to Revision C (September 2025)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Page                                 |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|
| Changes from Revision A (June 2013) to Revision B (September 2014)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Page                                 |
| <ul style="list-style-type: none"> <li>Added <i>Device Information</i> and <i>ESD Ratings</i> tables, and <i>Feature Description</i>, <i>Device Functional Modes</i>, <i>Application and Implementation</i>, <i>Power Supply Recommendations</i>, <i>Layout</i>, <i>Device and Documentation Support</i>, and <i>Mechanical, Packaging, and Orderable Information</i> sections.....</li> <li>Deleted trace from SDA to SCL, and added missing connector dot to <math>V_S</math> in front-page diagram .....</li> <li>Added <math>(V_{IN+}) + (V_{IN-}) / 2</math> to common-mode analog inputs in the <i>Absolute Maximum Ratings</i> table .....</li> <li>Deleted VBUS from analog inputs in <i>Absolute Maximum Ratings</i> table .....</li> <li>Added operating temperature to <i>Absolute Maximum Ratings</i> table.....</li> <li>Changed all <math>V_{SENSE}</math> to <math>V_{SHUNT}</math> throughout data sheet for consistency.....</li> <li>Changed "Status register" to "Mask/Enable register" to clarify register name in <i>Basic ADC Functions</i> section...</li> </ul> | <br>1<br>1<br>4<br>4<br>4<br>5<br>11 |

|                                                                                                       |    |
|-------------------------------------------------------------------------------------------------------|----|
| • Changed <i>Critical Alert</i> section text for clarity. ....                                        | 12 |
| • Added Summation Control Function section.....                                                       | 12 |
| • Changed external "R <sub>PU</sub> " to "R <sub>PU_ext</sub> " in Figure 20.....                     | 13 |
| • Changed <i>Multiple Channel Monitoring</i> section text for clarity. ....                           | 17 |
| • Added X and Y axis labels to Figure 25.....                                                         | 18 |
| • Changed "bidirectional" to "I/O" in second paragraph of <i>Bus Overview</i> section.....            | 20 |
| • Changed V <sub>S+</sub> to V <sub>S</sub> in Table 1.....                                           | 20 |
| • Changed references in Figure 30 to point to correct notes.....                                      | 21 |
| • Changed Figure 31.....                                                                              | 22 |
| • Changed values in Table 2, <i>Bus Timing Definitions</i> .....                                      | 22 |
| • Added data valid time to Table 2, <i>Bus Timing Definitions</i> .....                               | 22 |
| • Changed fall time to split data and clock times in Table 2, <i>Bus Timing Definitions</i> .....     | 22 |
| • Deleted rise time for data in Table 2, <i>Bus Timing Definitions</i> .....                          | 22 |
| • Deleted trace from SDA to SCL, and added missing connector dot to V <sub>S</sub> in Figure 52 ..... | 37 |

| <b>Changes from Revision * (May 2012) to Revision A (June 2013)</b>                                         | <b>Page</b> |
|-------------------------------------------------------------------------------------------------------------|-------------|
| • Changed <i>Shunt voltage input range</i> parameter values in <i>Electrical Characteristics</i> table..... | 5           |
| • Updated Figure 19.....                                                                                    | 13          |
| • Changed second paragraph of <i>Serial Bus Address</i> section.....                                        | 20          |
| • Updated Figure 27 and note (1).....                                                                       | 21          |
| • Updated Figure 28 and note (1).....                                                                       | 21          |
| • Updated Figure 29 and note (1).....                                                                       | 21          |
| • Updated Figure 30 and note (1).....                                                                       | 21          |
| • Changed bit D15 in Power Valid Upper Limit Register.....                                                  | 35          |
| • Changed bit D15 in Power Valid Lower Limit Register.....                                                  | 35          |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">INA3221AIRGVR</a> | Active        | Production           | VQFN (RGV)   16 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | INA<br>3221         |
| INA3221AIRGVR.B               | Active        | Production           | VQFN (RGV)   16 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | INA<br>3221         |
| INA3221AIRGVRG4               | Active        | Production           | VQFN (RGV)   16 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | INA<br>3221         |
| INA3221AIRGVRG4.B             | Active        | Production           | VQFN (RGV)   16 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | INA<br>3221         |
| <a href="#">INA3221AIRGVT</a> | Obsolete      | Production           | VQFN (RGV)   16 | -                     | -           | Call TI                              | Call TI                           | -40 to 125   | INA<br>3221         |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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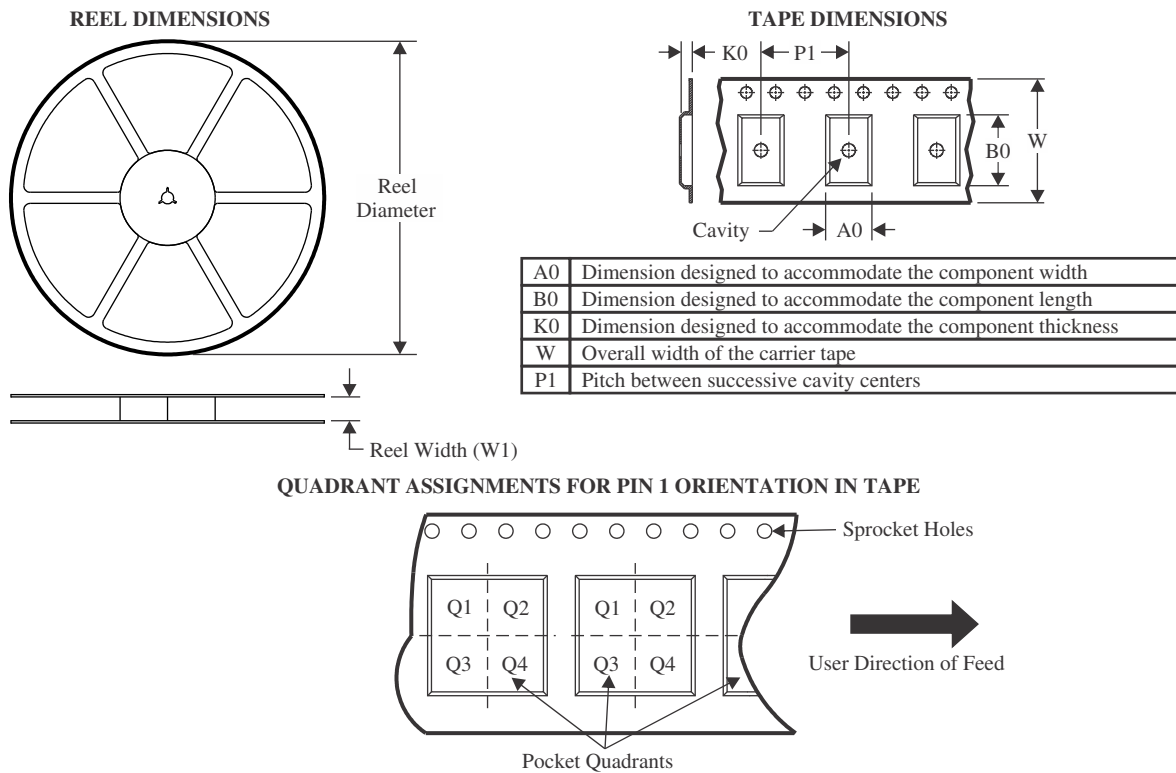
**OTHER QUALIFIED VERSIONS OF INA3221 :**

- Automotive : [INA3221-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

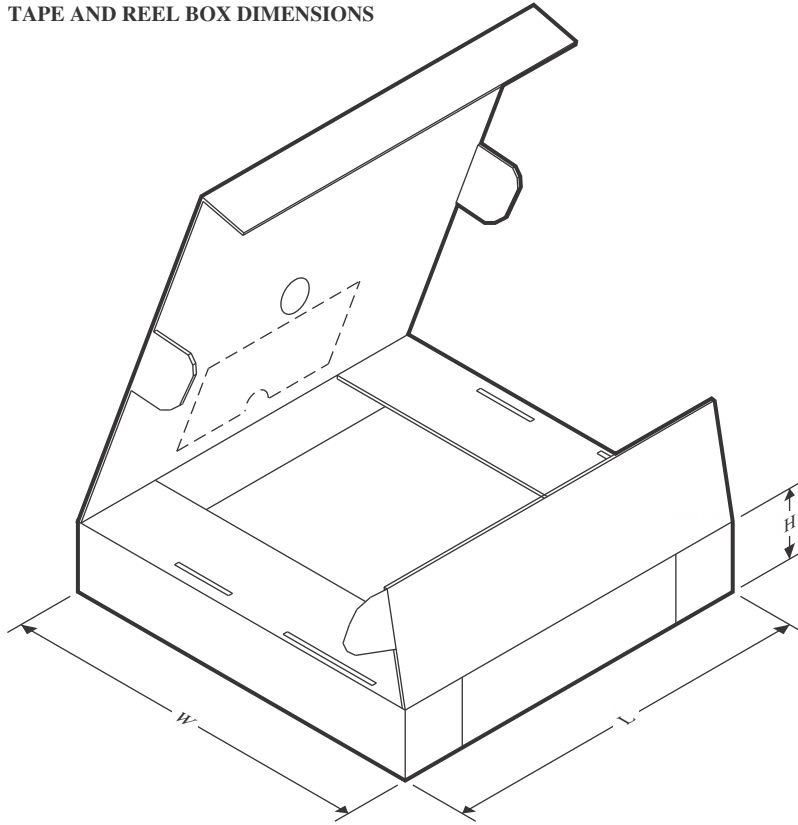
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| INA3221AIRGVR   | VQFN         | RGV             | 16   | 2500 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| INA3221AIRGVRG4 | VQFN         | RGV             | 16   | 2500 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| INA3221AIRGVR   | VQFN         | RGV             | 16   | 2500 | 346.0       | 346.0      | 33.0        |
| INA3221AIRGVRG4 | VQFN         | RGV             | 16   | 2500 | 346.0       | 346.0      | 33.0        |

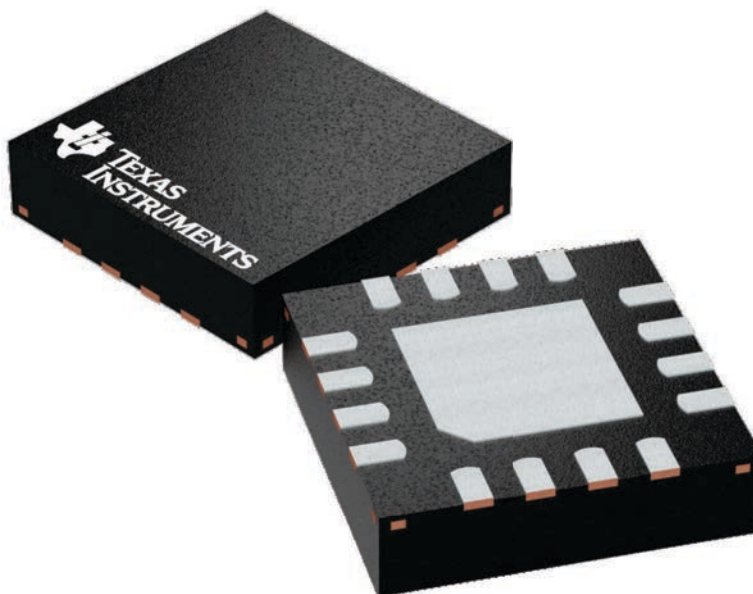
## GENERIC PACKAGE VIEW

**RGV 16**

**VQFN - 1 mm max height**

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224748/A

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

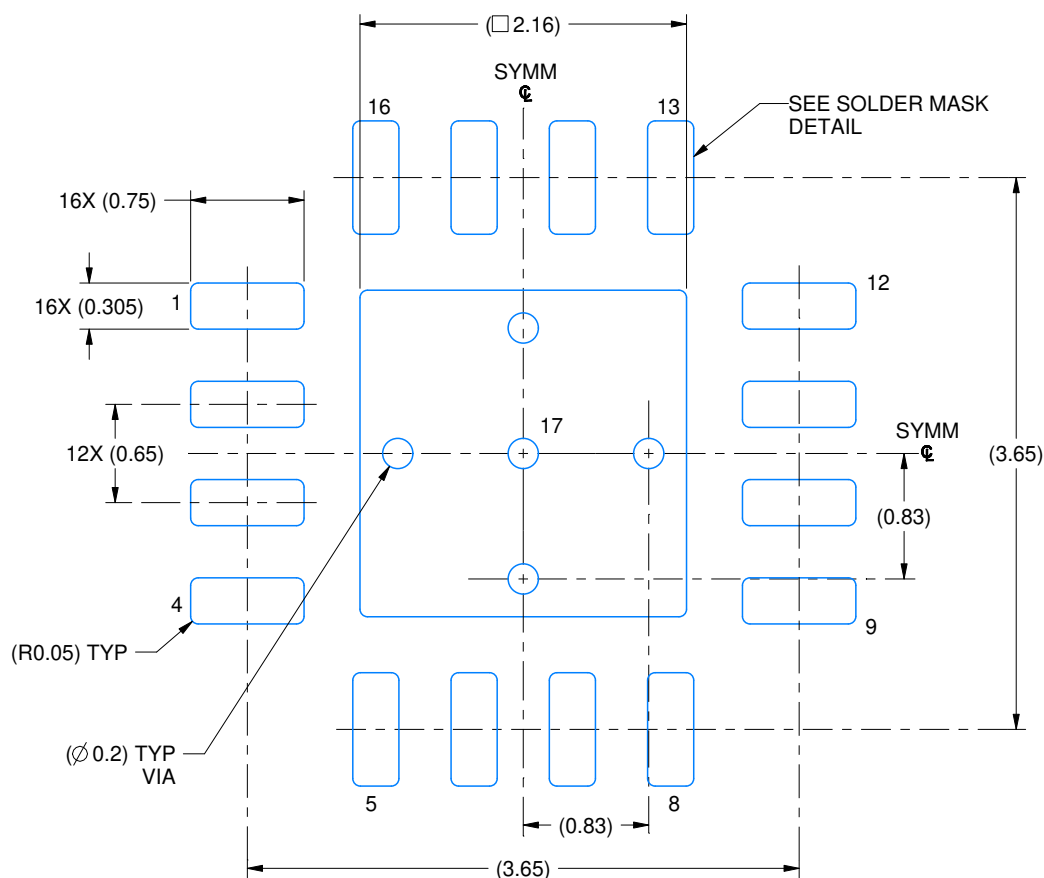


# EXAMPLE BOARD LAYOUT

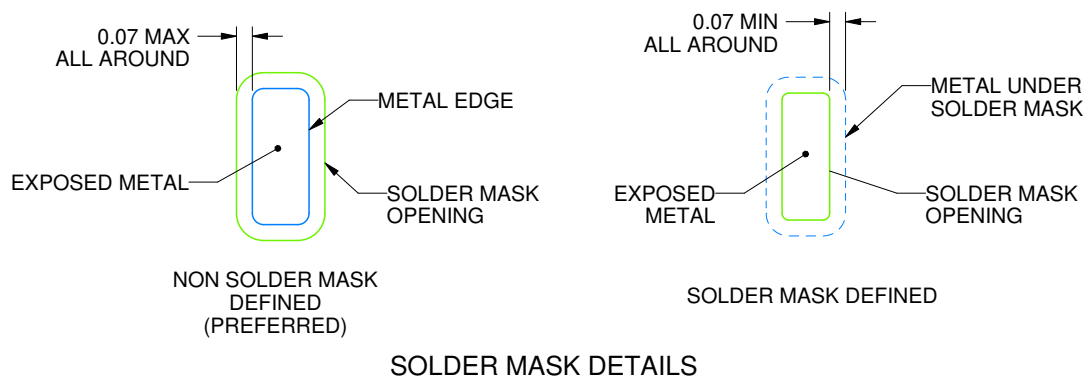
RGV0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4219037/A 06/2019

NOTES: (continued)

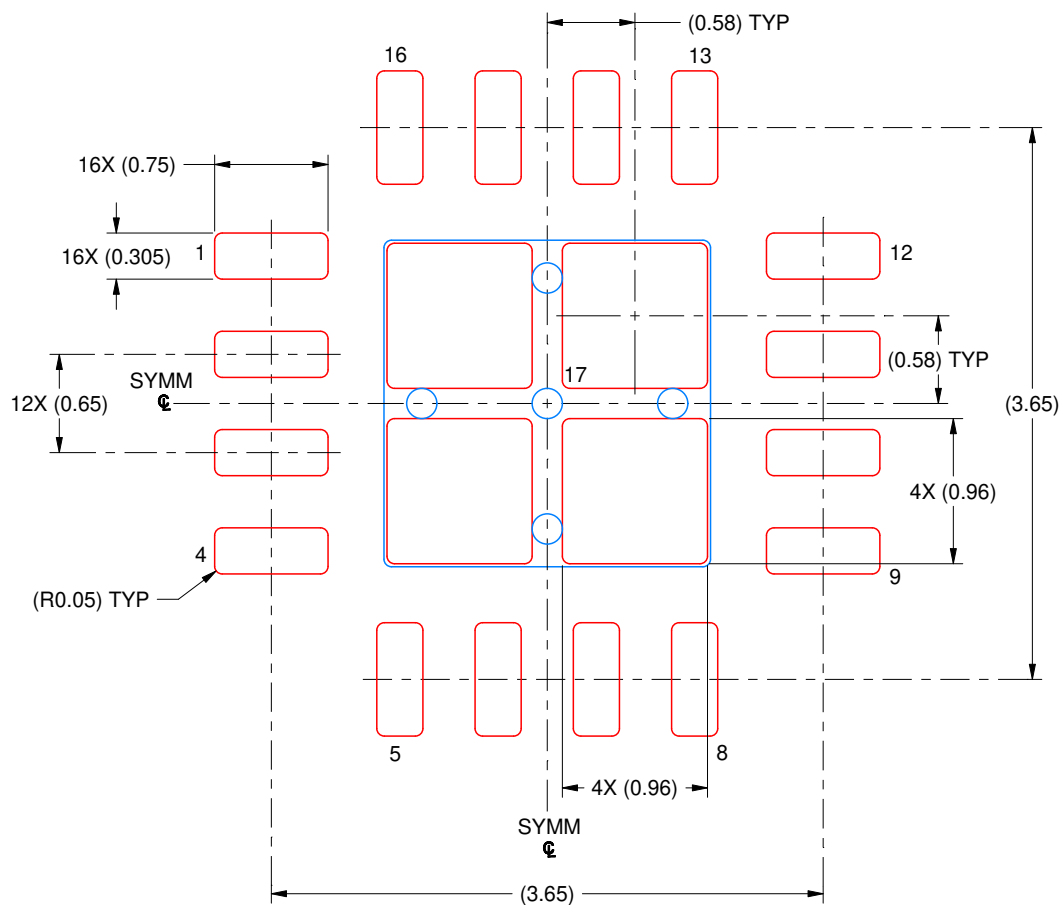
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGV0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 17  
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219037/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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