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P-Channel Enhancement-Mode Lateral MOSFET

Features

- Ultra-Low Threshold
- High Input Impedance
- Low Input Capacitance
- Fast Switching Speeds
- Low On-Resistance
- Freedom from Secondary Breakdown
- Low Input and Output Leakage

Applications

- Logic-Level Interfaces
- Solid-State Relays
- Battery-Operated Systems
- Photovoltaic Drives
- Analog Switches
- General Purpose Line Drivers

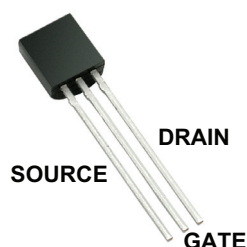
General Description

The LP0701 Enhancement-mode (normally-off) transistor uses a lateral MOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

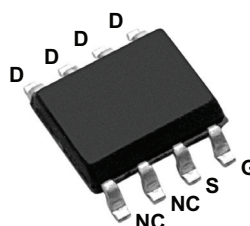
The low threshold voltage and low on-resistance characteristics are ideally suited for handheld and battery-operated applications.

Package Types

3-lead TO-92
(Top view)



8-lead SOIC
(Top view)



See [Table 3-1](#) and [Table 3-2](#) for pin information.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	$\pm 10V$
Operating Ambient Temperature, T_A	$-55^{\circ}C$ to $+150^{\circ}C$
Storage Temperature, T_S	$-55^{\circ}C$ to $+150^{\circ}C$

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $T_A = 25^{\circ}C$ unless otherwise specified. All DC parameters are 100% tested at $25^{\circ}C$ unless otherwise stated. Pulse test: 300 μs pulse, 2% duty cycle

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	-16.5	—	—	V	$V_{GS} = 0V, I_D = -1\text{ mA}$
Gate Threshold Voltage	$V_{GS(th)}$	-0.5	-0.7	-1	V	$V_{GS} = V_{DS}, I_D = -1\text{ mA}$
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	-4	mV/ $^{\circ}C$	$V_{GS} = V_{DS}, I_D = -1\text{ mA}$ (Note 1)
Gate Body Leakage Current	I_{GSS}	—	—	-100	nA	$V_{GS} = \pm 10V, V_{DS} = 0V$
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	-100	nA	$V_{DS} = -15V, V_{GS} = 0V$
		—	—	-1	mA	$V_{DS} = 0.8$ Maximum rating, $V_{GS} = 0V, T_A = 125^{\circ}C$ (Note 1)
On-State Drain Current	$I_{D(ON)}$	—	-0.4	—	A	$V_{GS} = V_{DS} = -2V$
		-0.6	-1	—	A	$V_{GS} = V_{DS} = -3V$
		-1.25	-2.3	—	A	$V_{GS} = V_{DS} = -5V$
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	2	4	Ω	$V_{GS} = -2V, I_D = -50\text{ mA}$
		—	1.7	2	Ω	$V_{GS} = -3V, I_D = -150\text{ mA}$
		—	1.3	1.5	Ω	$V_{GS} = -5V, I_D = -300\text{ mA}$
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	0.75	%/ $^{\circ}C$	$V_{GS} = -5V, I_D = -300\text{ mA}$ (Note 1)

Note 1: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $T_A = 25^\circ\text{C}$ unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G _{FS}	500	700	—	mmho	V _{GS} = −15V, I _D = −1A
Input Capacitance	C _{ISS}	—	120	250	pF	V _{GS} = 0V, V _{DS} = −15V, f = 1 MHz
Common Source Output Capacitance	C _{OSS}	—	100	125	pF	
Reverse Transfer Capacitance	C _{RSS}	—	40	60	pF	
Turn-On Delay Time	t _{d(ON)}	—	—	20	ns	V _{DD} = −15V, I _D = −1.25A, R _{GEN} = 25Ω
Rise Time	t _r	—	—	20	ns	
Turn-Off Delay Time	t _{d(OFF)}	—	—	30	ns	
Fall Time	t _f	—	—	30	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V _{SD}	—	−1.2	−1.5	V	V _{GS} = 0V, I _{SD} = −500 mA (Note 1)

Note 1: Unless otherwise stated, all DC parameters are 100% tested at 25°C . Pulse test: 300 μs pulse, 2% duty cycle.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	-55	—	+150	$^\circ\text{C}$	
Storage Temperature	T_S	-55	—	+150	$^\circ\text{C}$	
PACKAGE THERMAL RESISTANCE						
3-lead TO-92	θ_{JA}	—	132	—	$^\circ\text{C/W}$	
8-lead SOIC	θ_{JA}	—	101	—	$^\circ\text{C/W}$	Note 1

Note 1: Mounted on an FR4 board, 25 mm x 25 mm x 1.57 mm

THERMAL CHARACTERISTICS

Package	I_D (Note 1) (Continuous) (mA)	I_D (Pulsed) (A)	Power Dissipation at $T_A = 25^\circ\text{C}$ (W)	I_{DR} (Note 1) (mA)	I_{DRM} (mA)
3-lead TO-92	-500	-1.25	1	-500	-1.25
8-lead SOIC	-700	-1.25	1.5 (Note 2)	-700	-1.25

Note 1: I_D (continuous) is limited by maximum rated T_J .

2: Mounted on an FR4 board 25 mm x 25 mm x 1.57 mm

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

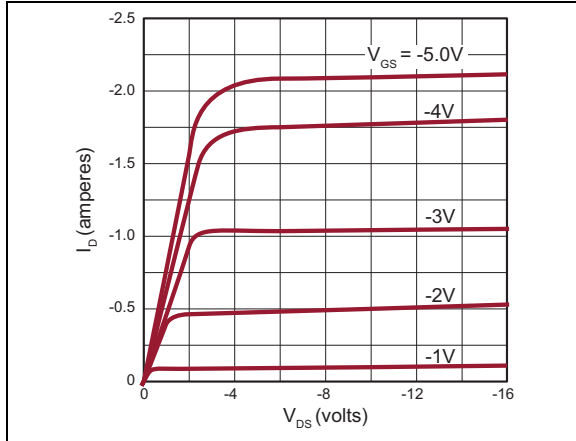


FIGURE 2-1: Output Characteristics.

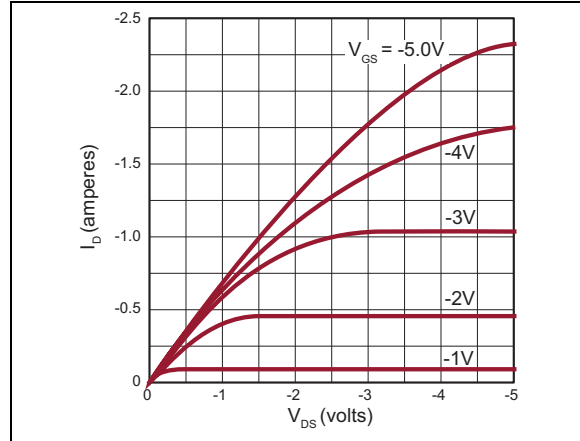


FIGURE 2-4: Saturation Characteristics.

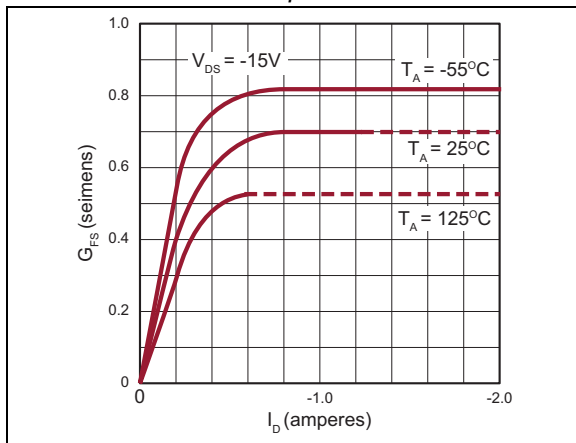


FIGURE 2-2: Transconductance vs. Drain Current.

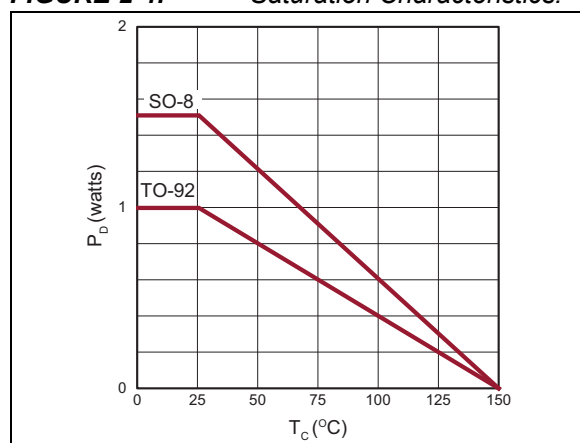


FIGURE 2-5: Power Dissipation vs. Case Temperature.

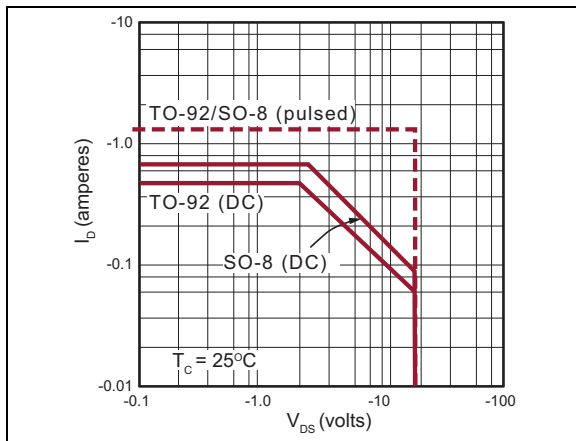


FIGURE 2-3: Maximum Rated Safe Operating Area.

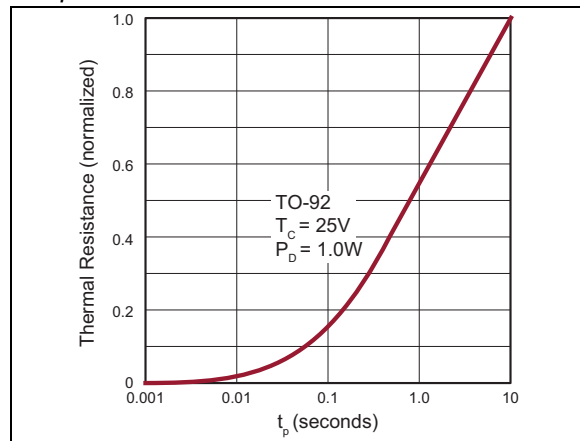


FIGURE 2-6: Thermal Response Characteristics.

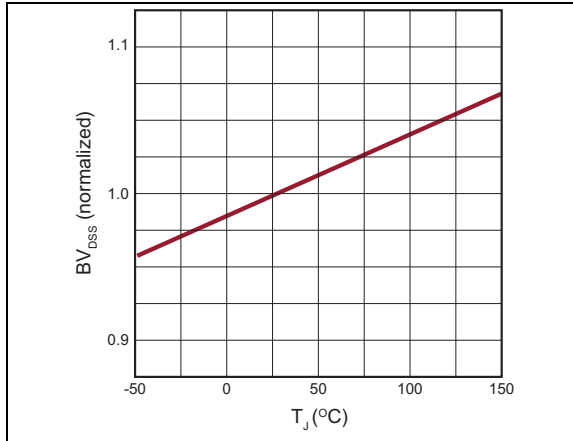


FIGURE 2-7: BV_{DSS} Variation with Temperature.

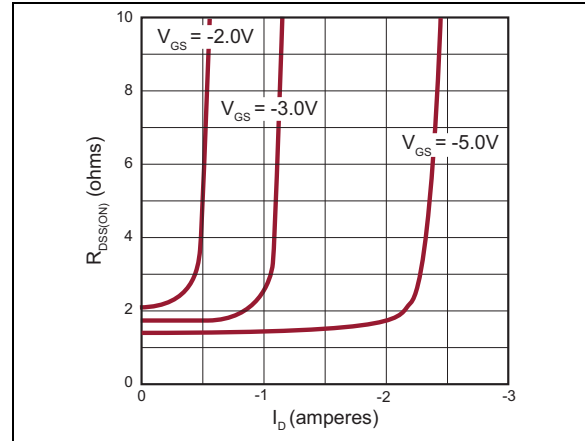


FIGURE 2-10: On-Resistance vs. Drain Current.

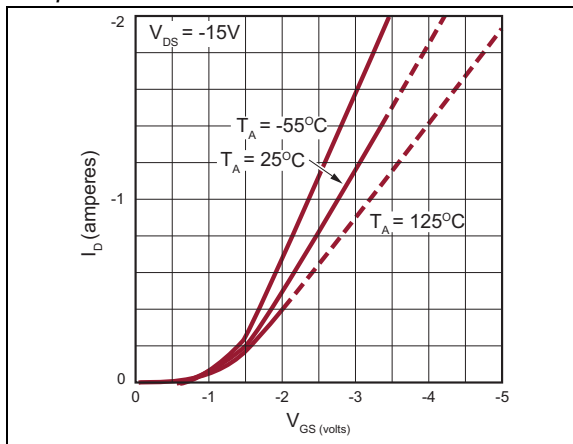


FIGURE 2-8: Transfer Characteristics.

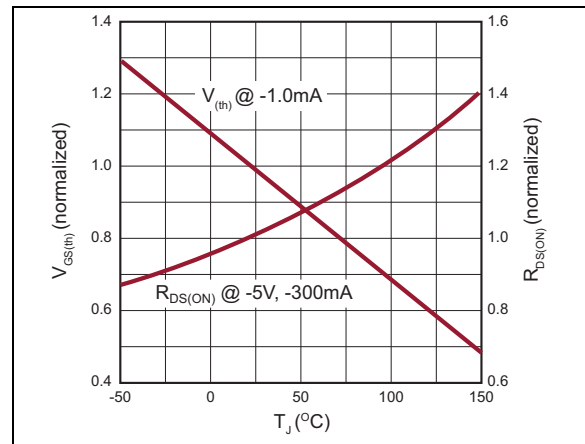


FIGURE 2-11: $V_{(th)}$ and R_{DS} Variation with Temperature.

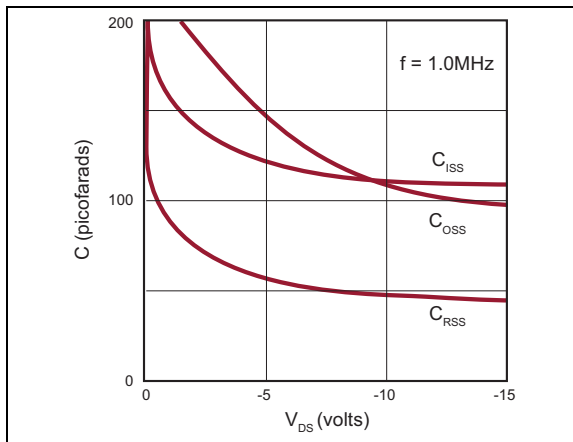


FIGURE 2-9: Capacitance vs. Drain-to-Source Voltage.

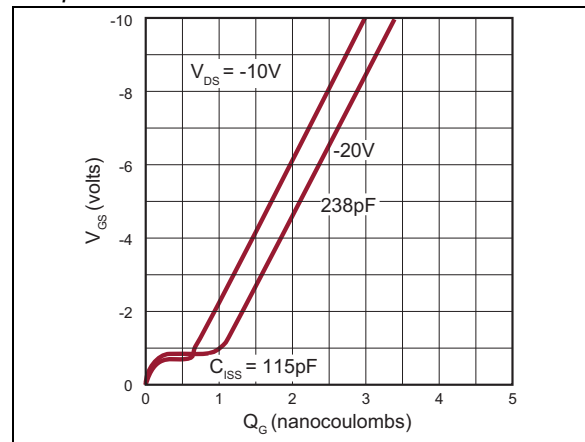


FIGURE 2-12: Gate Drive Dynamic Characteristics.

3.0 PIN DESCRIPTION

The details on the pins of LP0701 3-lead TO-92 and 8-lead SOIC are listed in [Table 3-1](#) and [Table 3-2](#), respectively. Refer to [Package Types](#) for the location of pins.

TABLE 3-1: 3-LEAD TO-92 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Source	Source
2	Gate	Gate
3	Drain	Drain

TABLE 3-2: 8-LEAD SOIC PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	NC	No connection
2	NC	No connection
3	Source	Source
4	Gate	Gate
5	Drain	Drain
6	Drain	Drain
7	Drain	Drain
8	Drain	Drain

4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for LP0701.

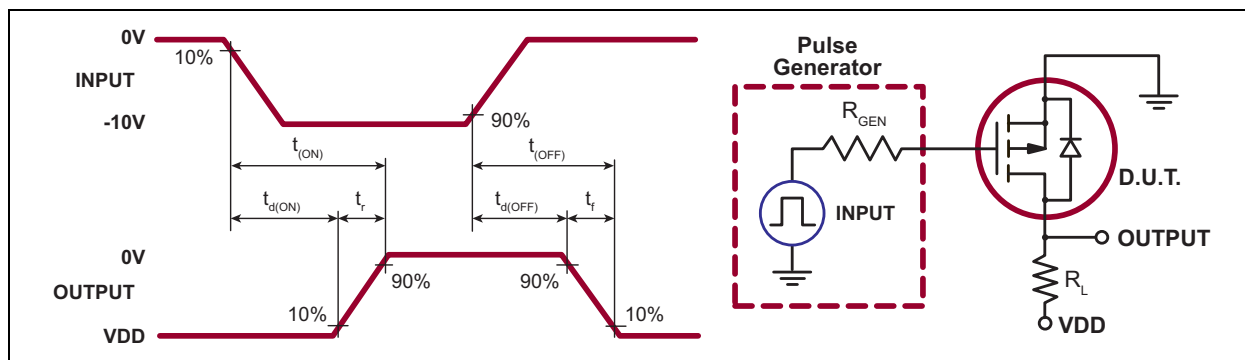
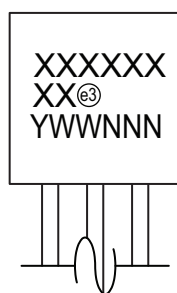


FIGURE 4-1: Switching Waveforms and Test Circuit.

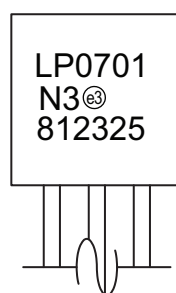
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

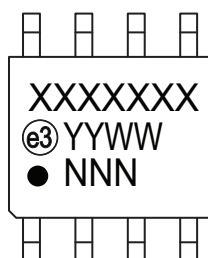
3-lead TO-92



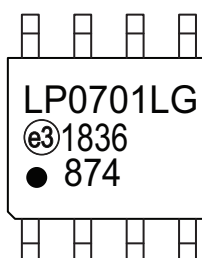
Example



8-lead SOIC



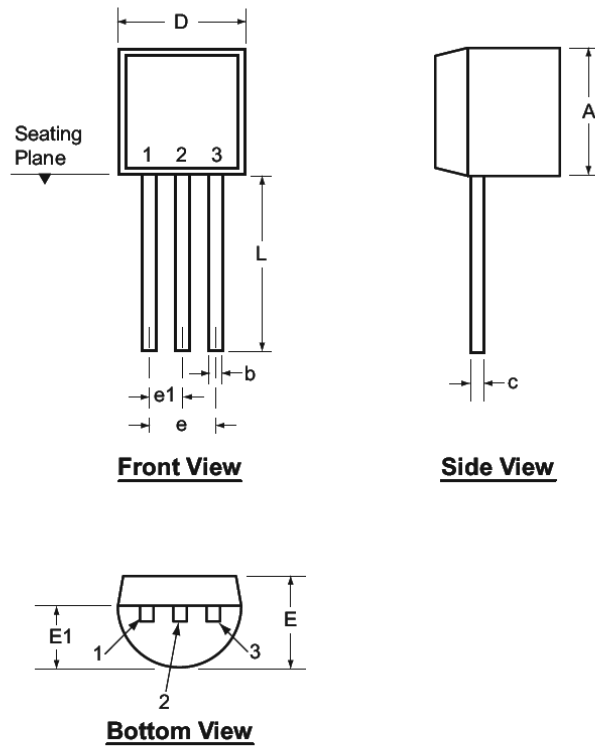
Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

3-Lead TO-92 Package Outline (L/LL/N3)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

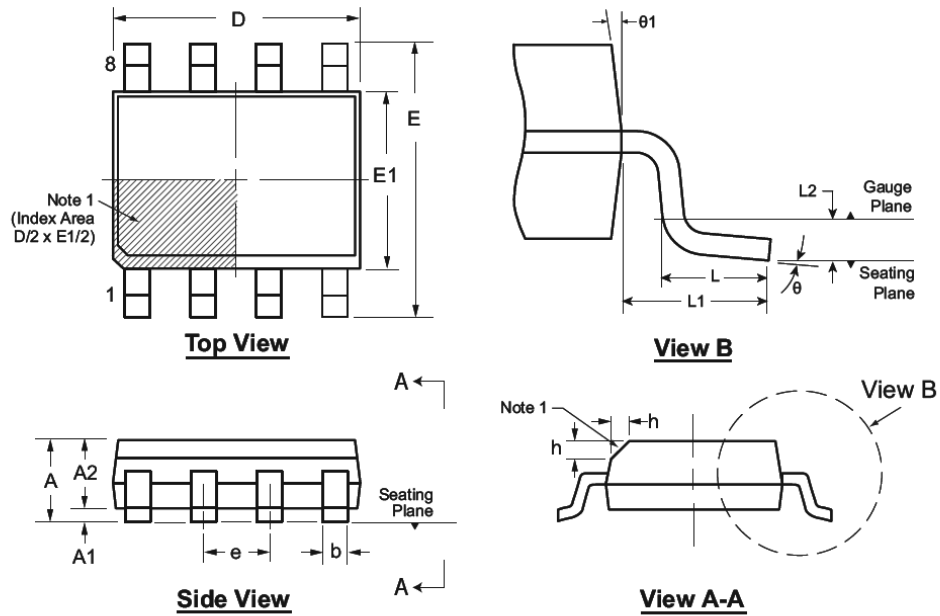
JEDEC Registration TO-92.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

8-Lead SOIC (Narrow Body) Package Outline (LG/TG) 4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

APPENDIX A: REVISION HISTORY

Revision A (October 2018)

- Converted Supertex Doc# DSFP-LP0701 to Microchip DS20005447A
- Changed the package marking format
- Removed the 3-lead TO-92 N3 P002, P003, P005, P013 and P014 media types
- Added some sections to comply with the standard Microchip format
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>				Examples:	
Device	Package Options	Environmental	Media Type	a) LP0701N3-G:	P-Channel Enhancement-Mode Lateral MOSFET, 3-lead TO-92, 1000/Bag
Device:	LP0701	=	P-Channel Enhancement-Mode Lateral MOSFET		
Packages:	N3	=	3-lead TO-92		
	LG	=	8-lead SOIC		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Types:	(blank)	=	1000/Bag for an N3 Package	b) LP0701LG-G:	P-Channel Enhancement-Mode Lateral MOSFET, 8-lead SOIC, 3300/Reel
	(blank)	=	3300/Reel for an LG Package		

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Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820