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TXS0102 2-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Applications

1 Features

- No direction-control signal needed
- Maximum data rates:
  - 24Mbps (push pull)
  - 2Mbps (open drain)
- Available in the Texas Instruments NanoStar™ integrated circuit package
- 1.65V to 3.6V on A port and 2.3V to 5.5V on B port ($V_{CCA} \leq V_{CCB}$)
- V_{CC} isolation feature: if either V_{CC} input is at GND, both ports are in the High-Impedance state
- No power-supply sequencing required: either V_{CCA} or V_{CCB} can be ramped first
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD protection exceeds JESD 22:
  - A port:
    - 2500V Human-Body Model (A114-B)
    - 250V Machine Model (A115-A)
    - 1500V Charged-Device Model (C101)
  - B port:
    - 8kV Human-Body Model (A114-B)
    - 250V Machine Model (A115-A)
    - 1500V Charged-Device Model (C101)

2 Applications

- I^2C / SMBus
- UART
- GPIO

3 Description

This two-bit non-inverting translator is a bidirectional voltage-level translator and can be used to establish digital switching compatibility between mixed-voltage systems. It uses two separate configurable power-supply rails, with the A ports supporting operating voltages from 1.65V to 3.6V while it tracks the V_{CCA} supply, and the B ports supporting operating voltages from 2.3V to 5.5V while it tracks the V_{CCB} supply. This allows the support of both lower and higher logic signal levels while providing bidirectional translation capabilities between any of the 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

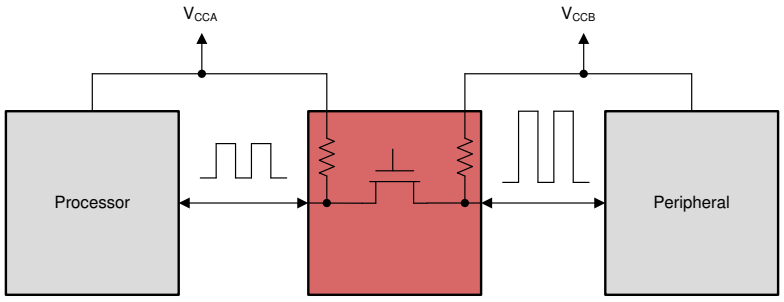
When the output-enable (OE) input is low, all I/Os are placed in the high-impedance state, which significantly reduces the power-supply quiescent current consumption.

To put the device in the high-impedance state during power up or power down, tie OE to GND through a pulldown resistor; the current-sourcing capability of the driver determines the minimum value of the resistor.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TXS0102	DCT (SSOP, 8)	2.95mm × 4mm
	DCU (VSSOP, 8)	2mm × 3.1mm
	DQE (X2SON, 8)	1.4mm × 1mm
	DQM (SON, 8)	1.8mm × 1.2mm
	YZP (DSBGA, 8)	1.9mm x 0.9mm
	DTT (DSBGA, 8)	1.95mm × 1mm

(1) For more information, see Section 11
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Block Diagram for TXS0102

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

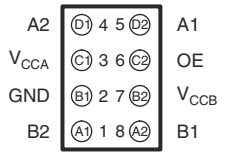


Figure 4-1. YZP Package, 8-Pin DSBGA (Bottom View)

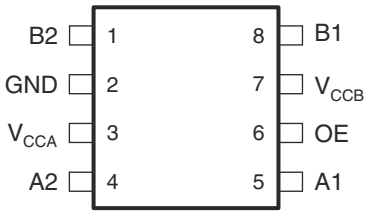


Figure 4-2. DCT or DCU Package, 8-Pin SSOP and VSSOP (Top View)

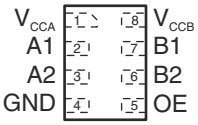


Figure 4-3. DQE or DQM Package, 8-Pin X2SON (Top View)

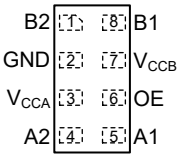


Figure 4-4. DTT Package, 8-Pin SOP (Top View)

Table 4-1. Pin Functions

PIN				TYPE[1]	DESCRIPTION
NAME	NO.				
	DCT, DCU, DTT	DQE, DQM	YZP		
A1	5	2	D2	I/O	Input/output A. Referenced to V_{CCA}.
A2	4	3	D1	I/O	Input/output A. Referenced to V_{CCA}.
B1	8	7	A2	I/O	Input/output B. Referenced to V_{CCB}.
B2	1	6	A1	I/O	Input/output B. Referenced to V_{CCB}.
GND	2	4	B1	—	Ground
OE	6	5	C2	I	Output enable (active High). Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
V_{CCA}	3	1	C1	P	A-port supply voltage. $1.65V \le V_{CCA} \le 3.6V$ and $V_{CCA} \le V_{CCB}$
V_{CCB}	7	8	B2	P	B-port supply voltage. $2.3V \le V_{CCB} \le 5.5V$

(1) I = input, O = output, I/O = input and output, P = power

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	4.6	V
V_{CCB}	Supply voltage B		–0.5	6.5	V
V_I	Input Voltage(2)	A Port	–0.5	4.6	V
		B Port	–0.5	6.5	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port	–0.5	4.6	V
		B Port	–0.5	6.5	
V_O	Voltage applied to any output in the high or low state(2) (3)	A Port	–0.5	V_{CCA} + 0.5	V
		B Port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Section 5.1* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3* Exposure beyond the limits listed in *Section 5.3* may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5V maximum if the output current rating is observed.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	A Port	±2500	V
			B Port	±8000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002	A Port	±1500	
			B Port	±1500	

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3) (4) (5)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage A				1.65	3.6	V
V_{CCB}	Supply voltage B				2.3	5.5	V
V_{IH}	High-level input voltage	A-port I/O's	1.65V to 1.95V	2.3V to 5.5V	V_{CCI} - 0.2	V_{CCI}	V
			2.3V to 3.6V		V_{CCI} - 0.4	V_{CCI}	
		B-port I/O's	1.65V to 3.6V		V_{CCI} - 0.4	V_{CCI}	
		OE Input	1.65V to 3.6V		V_{CCA} x 0.65	5.5	
V_{IL}	Low-level input voltage	A-port I/O's	1.65V to 3.6V	2.3V to 5.5V	0	0.15	V
		B-port I/O's			0	0.15	
		OE Input			0	V_{CCA} x 0.35	
Δt/Δv	Input transition rise and fall time	A-port I/O's	1.65V to 3.6V	2.3V to 5.5V		10	ns/V
		B-port I/O's				10	ns/V
		OE Input				10	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) The maximum V_{IL} value is provided to ensure that a valid V_{OL} is maintaned. The V_{OL} value is V_{IL} plus the voltage drop across the pass-gate transistor.
(4) V_{CCA} must be less than or equal to V_{CCB} , and V_{CCA} must not exceed 3.6V.
(5) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application note, *Implications of Slow or Floating CMOS Inputs*.

5.4 Thermal Information

THERMAL METRIC(1)		TXS0102						UNIT
		DCU	DQE	DCT	DTT	YZP	DQM	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	239.8	229.6	168.5	219.8	105.8	212.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.5	89.1	84.6	139.0	1.6	84.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	151.6	128.0	96.1	122.3	10.8	118.1	°C/W
Y_{JT}	Junction-to-top characterization parameter	30.9	2.8	15.1	17.5	3.1	2.8	°C/W
Y_{JB}	Junction-to-board characterization parameter	150.5	127.7	94.7	122.2	10.8	117.8	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)						UNIT
					25°C			–40°C to 85°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{OHA}	Port A output high voltage	I_{OH} = –20uA $V_{IB} \geq V_{CCB}$ - 0.4V	1.65V to 3.6V	2.3V to 5.5V				V_{CCA} x 0.67			V
V_{OLA}	Port A output low voltage	I_{OL} = 1mA $V_{IB} \leq$ 0.15V	1.65V to 3.6V	2.3V to 5.5V						0.4	
V_{OHB}	Port B output high voltage	I_{OH} = –20uA $V_{IB} \geq V_{CCB}$ - 0.4V	1.65V to 3.6V	2.3V to 5.5V				V_{CCB} x 0.67			
V_{OLB}	Port B output low voltage	I_{OL} = 1mA $V_{IB} \leq$ 0.15V	1.65V to 3.6V	2.3V to 5.5V						0.4	
I_I	Input leakage current	OE $V_I = V_{CC}$ or GND	1.65V to 3.6V	2.3V to 5.5V			±1			±2	μA
I_{off}	Partial power down current	A port	0V	0V to 5.5V			±1			±2	
	Partial power down current	B port	0V to 3.6V	0V			±1			±2	
I_{OZ}	Tri-state output current	A or B Port: $V_I = V_{CCI}$ or GND $V_O = V_{CCO}$ or GND OE = GND	1.65V to 3.6V	2.3V to 5.5V	–1		1	–2		2	μA
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND I_O = 0	1.65V to V_{CCB}	2.3V to 5.5V						2.4	μA
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND I_O = 0	3.6V	0V						2.2	μA
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND I_O = 0	0V	5.5V				–2			μA
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND I_O = 0	1.65V to V_{CCB}	2.3V to 5.5V						12	μA
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND I_O = 0	3.6V	0V				–1			μA
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND I_O = 0	0V	5.5V						3	μA
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND I_O = 0	1.65V to V_{CCB}	2.3V to 5.5V						14.4	μA
C_i	Input Capacitance	OE	3.3V	3.3V		2.5				3.5	pF
C_{io}	Input-to-output internal capacitance	A or B port	3.3V	3.3V		10					pF
C_{io}	Input-to-output internal capacitance	A port	3.3V	3.3V		5			6		pF
C_{io}	Input-to-output internal capacitance	B port	3.3V	3.3V		6			7.5		pF

(1) V_{CCI} is the V_{CC} associated with the input port
(2) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6V.
(3) V_{CCO} is the V_{CC} associated with the output port

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5.6 Switching Characteristics, V_{CCA} = 1.8 ± 0.15V

PARAMETER		FROM	TO	TEST CONDITIONS		B-Port Supply Voltage (V_{CCB})									UNIT
						2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 85°C			5.3			5.4			6.8	ns
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Open-Drain	-40°C to 85°C	2.3		8.8	2.4		9.6	2.6		10	ns
t_{PLH}	Propagation Delay (Low-to-High)	A	B	Push-Pull	-40°C to 85°C			6.8			7.1			7.5	ns
t_{PLH}	Propagation Delay (Low-to-High)	A	B	Open-Drain	-40°C to 85°C	45		260	36		208	27		198	ns
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull	-40°C to 85°C			4.4			4.5			4.7	ns
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Open-Drain	-40°C to 85°C	1.9		5.3	1.1		4.4	1.2		4	ns
t_{PLH}	Propagation Delay (Low-to-High)	B	A	Push-Pull	-40°C to 85°C			5.3			4.5			0.5	ns
t_{PLH}	Propagation Delay (Low-to-High)	B	A	Open-Drain	-40°C to 85°C	45		175	36		140	27		102	ns
t_{en}	Enable Time	OE	A or B		-40°C to 85°C			200			200			200	ns
t_{dis}	Disable Time	OE	A or B		-40°C to 85°C			200			200			200	ns
t_{rA}	Ouput Rise Time	B	A	Push-Pull	-40°C to 85°C	3.2		9.5	2.3		9.3	2		7.6	ns
t_{rA}	Ouput Rise Time	B	A	Open-Drain	-40°C to 85°C	38		165	30		132	22		95	ns
t_{rB}	Ouput Rise Time	A	B	Push-Pull	-40°C to 85°C	4		10.8	2.7		9.1	2.7		7.6	ns
t_{rB}	Ouput Rise Time	A	B	Open-Drain	-40°C to 85°C	34		145	23		106	10		58	ns
t_{fA}	Output Fall Time	B	A	Push-Pull	-40°C to 85°C	2		5.9	1.9		6	1.7		13.3	ns
t_{fA}	Output Fall Time	B	A	Open-Drain	-40°C to 85°C	4.4		6.9	4.3		6.4	4.2		6.1	ns
t_{fB}	Output Fall Time	A	B	Push-Pull	-40°C to 85°C	2.9		13.8	2.8		16.2	2.8		16.2	ns
t_{fB}	Output Fall Time	A	B	Open-Drain	-40°C to 85°C	6.9		13.8	7.5		16.2	7		16.2	ns

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5.7 Switching Characteristics, V_{CCA} = 2.5 ± 0.2V

PARAMETER		FROM	TO	TEST CONDITIONS		B-Port Supply Voltage (V_{CCB})									UNIT
						2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 85°C			3.2			3.7			3.8	ns
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Open-Drain	-40°C to 85°C	1.7		6.3	2		6	2.1		5.8	ns
t_{PLH}	Propagation Delay (Low-to-High)	A	B	Push-Pull	-40°C to 85°C			3.5			4.1			4.4	ns
t_{PLH}	Propagation Delay (Low-to-High)	A	B	Open-Drain	-40°C to 85°C	43		250	36		206	27		190	ns
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull	-40°C to 85°C			3			3.6			4.3	ns
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Open-Drain	-40°C to 85°C	1.8		4.7	2.6		4.2	1.2		4	ns
t_{PLH}	Propagation Delay (Low-to-High)	B	A	Push-Pull	-40°C to 85°C			2.5			1.6			1	ns
t_{PLH}	Propagation Delay (Low-to-High)	B	A	Open-Drain	-40°C to 85°C	44		170	37		140	27		103	ns
t_{en}	Enable Time	OE	A or B		-40°C to 85°C			200			200			200	ns
t_{dis}	Disable Time	OE	A or B		-40°C to 85°C			200			200			200	ns
t_{rA}	Ouput Rise Time	B	A	Push-Pull	-40°C to 85°C	2.8		7.4	2.6		6.6	1.8		5.6	ns
t_{rA}	Ouput Rise Time	B	A	Open-Drain	-40°C to 85°C	3		149	28		121	24		89	ns
t_{rB}	Ouput Rise Time	A	B	Push-Pull	-40°C to 85°C	3.2		8.3	2.9		7.2	2.4		6.1	ns
t_{rB}	Ouput Rise Time	A	B	Open-Drain	-40°C to 85°C	35		151	24		112	12		64	ns
t_{fA}	Output Fall Time	B	A	Push-Pull	-40°C to 85°C	1.9		5.7	1.9		5.5	1.8		5.3	ns
t_{fA}	Output Fall Time	B	A	Open-Drain	-40°C to 85°C	4.4		6.9	4.3		6.2	4.2		5.8	ns
t_{fB}	Output Fall Time	A	B	Push-Pull	-40°C to 85°C	2.2		7.8	2.4		6.7	2.6		6.6	ns
t_{fB}	Output Fall Time	A	B	Open-Drain	-40°C to 85°C	5.1		8.8	5.4		9.4	5.4		10.4	ns

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5.8 Switching Characteristics, V_{CCA} = 3.3 ± 0.3V

PARAMETER		FROM	TO	TEST CONDITIONS		B-Port Supply Voltage (V_{CCB})						UNIT
						3.3 ± 0.3V			5.0 ± 0.5V			
						MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 85°C			2.4			3.1	ns
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Open-Drain	-40°C to 85°C	1.3		4.2	1.4		4.6	ns
t_{PLH}	Propagation Delay (Low-to-High)	A	B	Push-Pull	-40°C to 85°C			4.2			4.4	ns
t_{PLH}	Propagation Delay (Low-to-High)	A	B	Open-Drain	-40°C to 85°C	36		204	28		165	ns
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull	-40°C to 85°C			2.5			3.3	ns
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Open-Drain	-40°C to 85°C	1		124	1		97	ns
t_{PLH}	Propagation Delay (Low-to-High)	B	A	Push-Pull	-40°C to 85°C			2.5			2.6	ns
t_{PLH}	Propagation Delay (Low-to-High)	B	A	Open-Drain	-40°C to 85°C	3		139	3		105	ns
t_{en}	Enable Time	OE	A or B		-40°C to 85°C			200			200	ns
t_{dis}	Disable Time	OE	A or B		-40°C to 85°C			200			200	ns
t_{rA}	Ouput Rise Time	B	A	Push-Pull	-40°C to 85°C	2.3		5.6	1.9		4.8	ns
t_{rA}	Ouput Rise Time	B	A	Open-Drain	-40°C to 85°C	25		116	19		85	ns
t_{rB}	Ouput Rise Time	A	B	Push-Pull	-40°C to 85°C	2.5		6.4	2.1		7.4	ns
t_{rB}	Ouput Rise Time	A	B	Open-Drain	-40°C to 85°C	26		116	14		72	ns
t_{fA}	Output Fall Time	B	A	Push-Pull	-40°C to 85°C	2		5.4	1.9		5	ns
t_{fA}	Output Fall Time	B	A	Open-Drain	-40°C to 85°C	4.3		6.1	4.2		5.7	ns
t_{fB}	Output Fall Time	A	B	Push-Pull	-40°C to 85°C	2.3		7.4	2.4		7.6	ns
t_{fB}	Output Fall Time	A	B	Open-Drain	-40°C to 85°C	5		7.6	4.8		8.3	ns

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5.9 Switching Characteristics: T_{sk}, T_{MAX}

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A) -40°C to 125°C MIN	TYP	MAX	UNIT
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching	Push-Pull Driving	1.8 ± 0.15V	2.5V ± 0.2V			21	Mbps
			1.8 ± 0.15V	3.3V ± 0.3V			22	
			1.8 ± 0.15V	5V ± 0.5V			24	
			2.5V ± 0.2V	2.5V ± 0.2V			20	
			2.5V ± 0.2V	3.3V ± 0.3V			22	
			2.5V ± 0.2V	5V ± 0.5V			24	
			3.3V ± 0.3V	3.3V ± 0.3V			23	
			3.3V ± 0.3V	5V ± 0.5V			24	
		Open-Drain Driving	1.8 ± 0.15V	1.8 ± 0.15V			2	
			1.8 ± 0.15V	2.5V ± 0.2V			2	
			1.8 ± 0.15V	3.3V ± 0.3V			2	
			1.8 ± 0.15V	5V ± 0.5V			2	
			2.5V ± 0.2V	2.5V ± 0.2V			2	
			2.5V ± 0.2V	3.3V ± 0.3V			2	
			2.5V ± 0.2V	5V ± 0.5V			2	
			3.3V ± 0.3V	3.3V ± 0.3V			2	
			3.3V ± 0.3V	5V ± 0.5V			2	
t_w	Pulse Duration, Data Inputs	Push-Pull Driving	1.65V to 3.6V	2.3V to 5.5V	20			ns
		Open-Drain Driving	1.65V to 3.6V	2.3V to 5.5V	500			
t_{sk} - Output skew	Skew between any two outputs of the same package switching in the same direction		1.65V to 3.6V	2.3V to 5.5V			0.7	ns

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5.10 Operating Characteristics: V_{CCA} = 1.5V to 3.3V, V_{CCB} = 1.5V to 3.3V

T_A = 25°C (1)

PARAMETER		TEST CONDITIONS	Supply Voltage (V_{CCA} = V_{CCB} ,unless otherwise noted)			UNIT
			1.8 ± 0.15V	2.5 ± 0.2V	3.3 ± 0.3V	
			TYP	TYP	TYP	
C_{pdA} (2)	A-port input, B-port output to B: outputs enabled	A Port CL = 0, RL = Open f = 10MHz t_{rise} = t_{fall} = 1ns	4.1	4.2	4.7	pF
	B-port input, A-port output to B: outputs enabled		9.0	7.3	7.8	
C_{pdB} (3)	A-port input, B-port output to B: outputs enabled		11.0	9.9	9.2	
	B-port input, A-port output to B: outputs enabled		5.6	7.1	7.4	
C_{pdA} (2)	A-port input, B-port output to B: outputs disabled	B Port CL = 0, RL = Open f = 10MHz t_{rise} = t_{fall} = 1ns	0.1	0.1	0.1	pF
	B-port input, A-port output to B: outputs disabled		0.1	0.1	0.1	
C_{pdB} (3)	A-port input, B-port output to B: outputs disabled		0.2	0.2	0.2	
	B-port input, A-port output to B: outputs disabled		0.2	0.2	0.18	

(1) For additional information about how power dissipation capacitance affects power consumption, see the *CMOS Power Consumption and C_{pd} Calculation* application note.
(2) A-Port power dissipation capacitance per transceiver
(3) B-Port power dissipation capacitance per transceiver

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5.11 Typical Characteristics

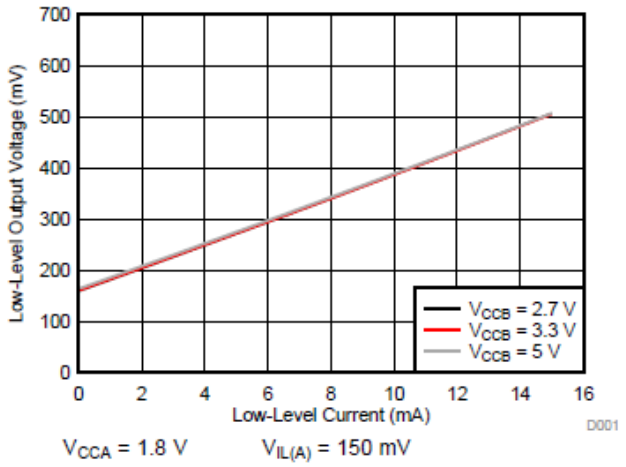


Figure 5-1. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

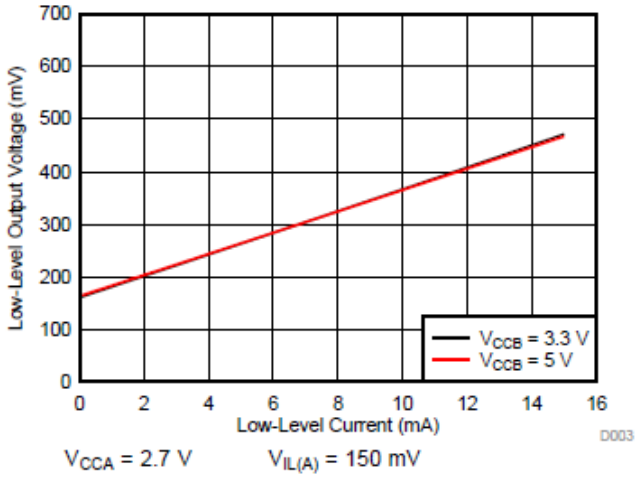


Figure 5-2. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

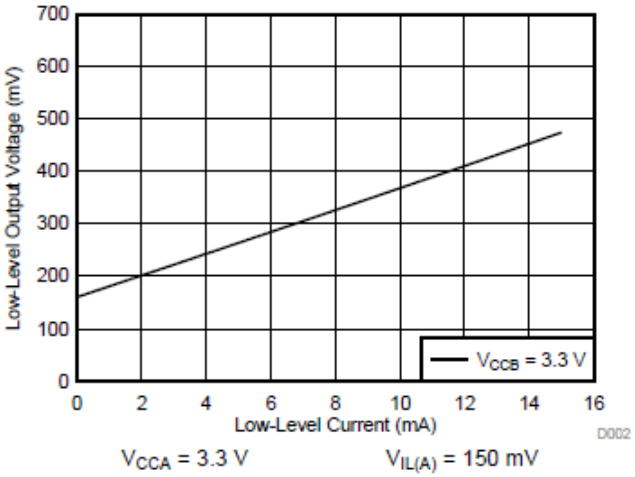


Figure 5-3. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

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6 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- PRR 10MHz
- Z_O = 50Ω
- dv/dt ≥ 1V/ns

Note

All parameters and waveforms are not applicable to all devices.

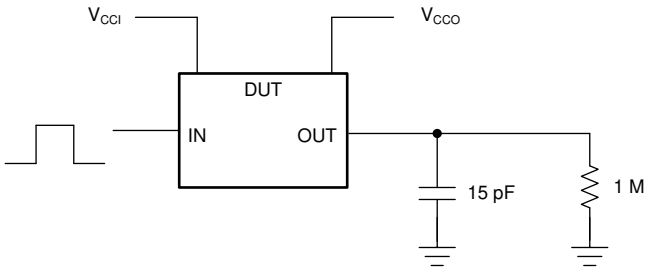


Figure 6-1. Data Rate, Pulse Duration, Propagation Delay, Output Rise And Fall Time Measurement Using A Push-Pull Driver

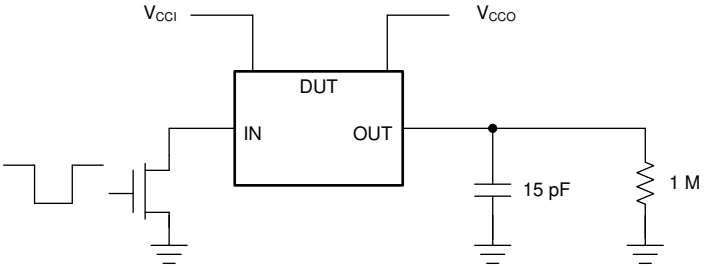


Figure 6-2. Data Rate, Pulse Duration, Propagation Delay, Output Rise And Fall Time Measurement Using An Open-Drain Driver

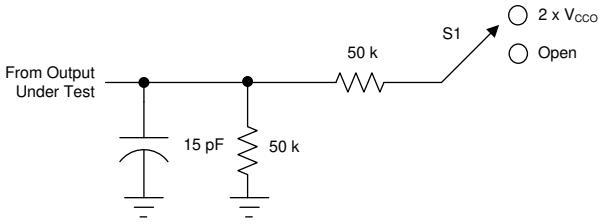


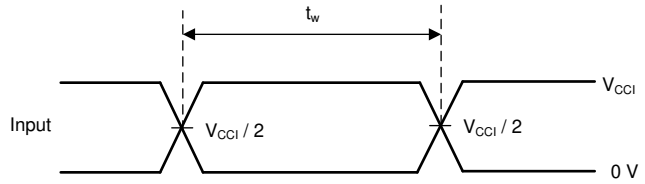
Figure 6-3. Load Circuit For Enable / Disable Time Measurement

Table 6-1. Switch Configuration For Enable / Disable Timing

TEST	S1
t_{PZL} (2), t_{PLZ} (1)	2 × V_{CCO}
t_{PHZ} (1), t_{PZH} (2)	Open

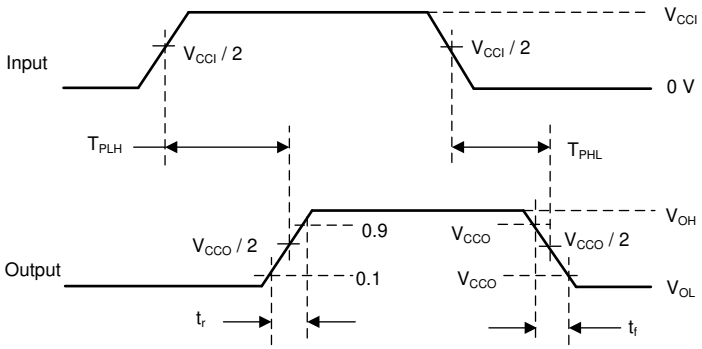
(1) t_{PLZ} and t_{PHZ} are the same as t_{dis}.
(2) t_{PZL} and t_{PZH} are the same as t_{en}.

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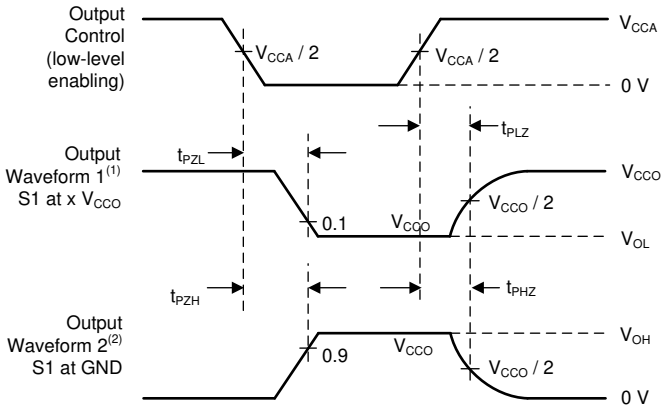
(1) All input pulses are measured one at a time, with one transition per measurement.

Figure 6-4. Voltage Waveforms Pulse Duration



(1) All input pulses are measured one at a time, with one transition per measurement.

Figure 6-5. Voltage Waveforms Propagation Delay Times



(1) Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
(2) Waveform 2 is for an output with internal conditions such that the ouput is high, except when disabled by the output control.

Figure 6-6. Voltage Waveforms Enable And Disable Times

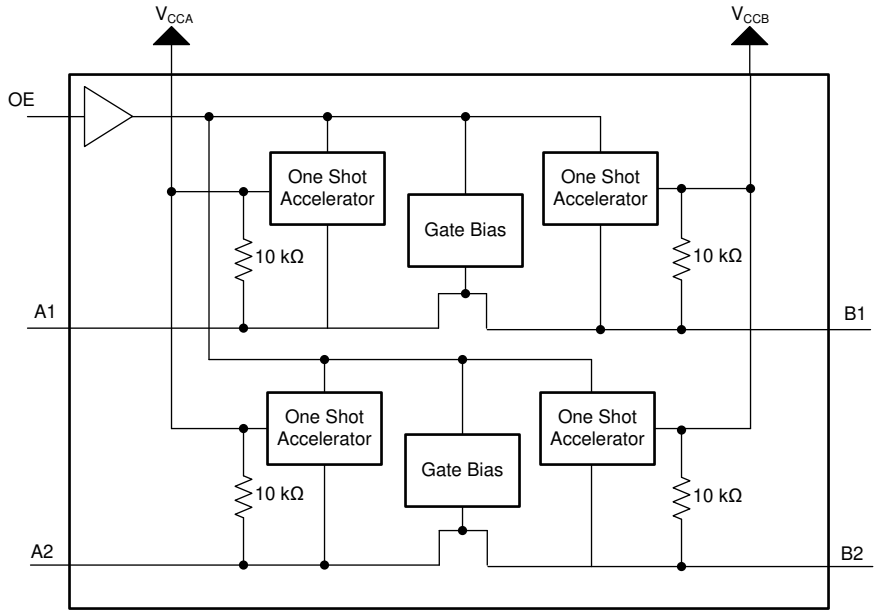
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7 Detailed Description

7.1 Overview

The TXS0102 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.65V to 3.6V, while the B port can accept I/O voltages from 2.3V to 5.5V. The device is a pass-gate architecture with edge-rate accelerators (one-shots) to improve the overall data rate. 10kΩ pullup resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open-drain applications, the device can also translate push-pull CMOS logic outputs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Architecture

The TXS0102 architecture (see Figure 7-1) is an auto-direction-sensing based translator that does not require a direction-control signal to control the direction of data flow from A to B or from B to A.

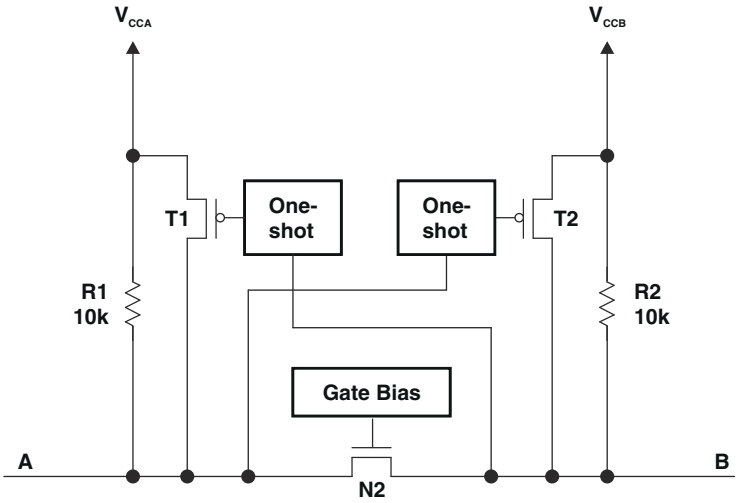


Figure 7-1. Architecture of a TXS0102 Cell

These two bidirectional channels independently determine the direction of data flow without a direction-control signal. Each I/O pin can be automatically reconfigured as either an input or an output, which is how this auto-direction feature is realized.

The TXS0102 device is part of TI's *Switch* type voltage translator family and employs two key circuits to enable this voltage translation:

1. An N-channel pass-gate transistor topology that ties the A-port to the B-port
2. Output one-shot (O.S.) edge-rate accelerator circuitry to detect and accelerate rising edges on the A or B ports

For bidirectional voltage translation, pull-up resistors are included on the device for dc current sourcing capability. The V_{GATE} gate bias of the N-channel pass transistor is set at approximately one threshold voltage (V_T) above the V_{CC} level of the low-voltage side. Data can flow in either direction without guidance from a control signal.

The O.S. rising-edge rate accelerator circuitry speeds up the output slew rate by monitoring the input edge for transitions, helping maintain the data rate through the device. During a low-to-high signal rising edge, the O.S. circuits turn on the PMOS transistors (T1, T2) to increase the current drive capability of the driver for approximately 30ns or 95% of the input edge, whichever occurs first.

This edge-rate acceleration provides high ac drive by bypassing the internal 10kΩ pull-up resistors during the low-to-high transition to speed up the signal. The output resistance of the driver is decreased to approximately 50Ω to 70Ω during this acceleration phase. To minimize dynamic I_{CC} and the possibility of signal contention, the user should wait for the O.S. circuit to turn off before applying a signal in the opposite direction. The worst-case duration is equal to the minimum pulse-width number provided in the *Table 6-1* section of this data sheet.

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7.3.2 Input Driver Requirements

The continuous dc-current *sinking* capability is determined by the external system-level open-drain (or push-pull) drivers that are interfaced to the TXS0102 I/O pins. Since the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest dc-current *sourcing* capability of hundreds of micro-Amps, as determined by the internal 10kΩ pullup resistors.

The fall time (t_{fA}, t_{fB}) of a signal depends on the edge-rate and output impedance of the external device driving TXS0102 data I/Os, as well as the capacitive loading on the data lines.

Similarly, the t_{PHL} and max data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50Ω.

7.3.3 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, causing any reflection to encounter low impedance at the source driver. The O.S. circuits are designed to stay on for approximately 30ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration.

With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic ICC, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TXS0102 device output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

7.3.4 Enable and Disable

The TXS0102 device has an OE input that is used to disable the device by setting OE low, which places all I/Os in the Hi-Z state. The disable time (t_{dis}) indicates the delay between the time when OE goes low and when the outputs are disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

7.3.5 Pullup or Pulldown Resistors on I/O Lines

Each A-port I/O has an internal 10kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10kΩ pullup resistor to V_{CCB}. If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10kΩ resistors). Adding lower value pull-up resistors will effect V_{OL} levels, however. The internal pull-ups of the TXS0102 are disabled when the OE pin is low.

7.4 Device Functional Modes

The device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TXS0102 device can be used to bridge the digital-switching compatibility gap between two voltage nodes to successfully interface logic threshold levels found in electronic systems. It should be used in a point-to-point topology for interfacing devices or systems operating at different interface voltages with one another. Its primary target application use is for interfacing with open-drain drivers on the data I/Os such as I^2C or 1-wire, where the data is bidirectional and no control signal is available. The device can also be used in applications where a push-pull driver is connected to the data I/Os, but the TXB0102 might be a better option for such push-pull applications.

8.2 Typical Application

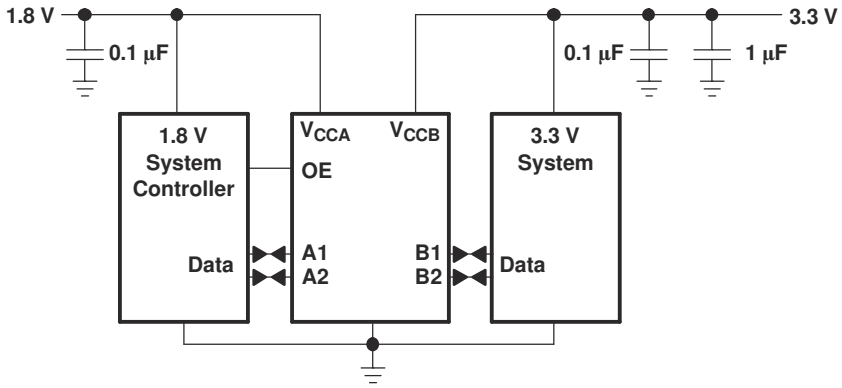


Figure 8-1. Typical Application Circuit

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1. And make sure the $V_{CCA} \leq V_{CCB}$.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.65 to 3.6V
Output voltage range	2.3 to 5.5V

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8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range:
  - Use the supply voltage of the device that is driving the TXS0102 device to determine the input voltage range. For a valid logic high the value must exceed the VIH of the input port. For a valid logic low the value must be less than the VIL of the input port.
- Output voltage range:
  - Use the supply voltage of the device that the TXS0102 device is driving to determine the output voltage range.
  - The TXS0102 device has 10kΩ internal pullup resistors. External pullup resistors can be added to reduce the total RC of a signal trace if necessary.
  - An external pull down resistor decreases the output VOH and VOL. Use Equation 1 to calculate the VOH as a result of an external pull down resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 10kq) \quad (1)$$

where:

- V_{CCx} is the supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pull down resistor

8.2.3 Application Curves

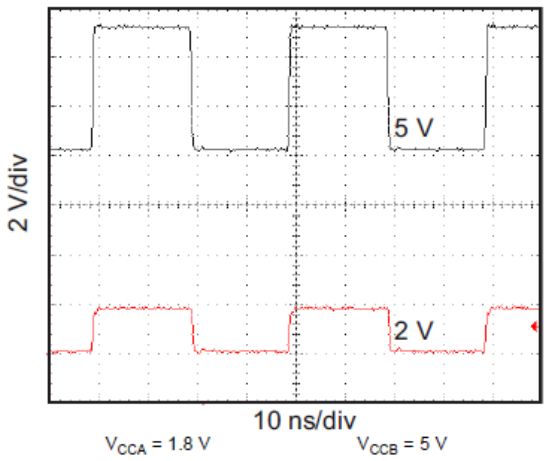


Figure 8-2. Level-Translation of a 2.5MHz Signal

8.3 Power Supply Recommendations

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first. The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To put the outputs in the high-impedance state during power up or power down, tie the OE input pin to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The current-sourcing capability of the driver determines the minimum value of the pulldown resistor to ground.

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8.4 Layout

8.4.1 Layout Guidelines

For device reliability, it is recommended to follow common printed-circuit board layout guidelines such as follows:

- Bypass capacitors should be used on power supplies and should be placed as close as possible to the V_{CCA}, V_{CCB} pin, and G_{ND} pin.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration (approximately 30ns) causing any reflection to encounter low impedance at the source driver.

8.4.2 Layout Example

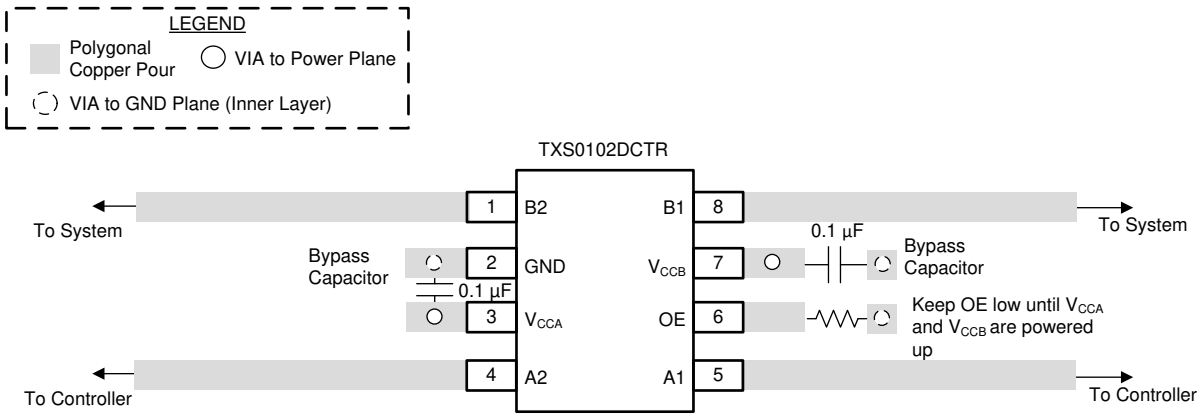


Figure 8-3. TXS0102 Layout Example

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *A Guide to Voltage Translation With TXS-Type Translators* application note
- Texas Instruments, *Factors Affecting VOL for TXS and LSF Auto-bidirectional Translation Devices* application note
- Texas Instruments, *Biasing Requirements for TXS, TXB, and LSF Auto-Bidirectional Translators* application note
- Texas Instruments, *Effects of pullup and pulldown resistors on TXS and TXB devices* application note
- Texas Instruments, *Introduction to logic* application note
- Texas Instruments, *TI Logic and Linear Products Guide* selection and solution guides
- Texas Instruments, *Washing Machine Solutions Guide* selection and solution guides
- Texas Instruments, *TI Smartphone Solutions Guide* selection and solution guides

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (August 2025) to Revision L (January 2026)	Page
• Added YZP package thermal information	5

Changes from Revision J (July 2023) to Revision K (August 2025)	Page
• Updated thermals for all packages, removed YZP package thermal information, and added DTT thermal information	5
• Updated degradation of ICCA/ ICCB	6
• Values updated	7
• Values updated	8
• Values updated	9

Changes from Revision I (August 2018) to Revision J (July 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXS0102DCTR	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(35UT, NFE) (R, Z)
TXS0102DCTR.A	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(35UT, NFE) (R, Z)
TXS0102DCTR.B	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(35UT, NFE) (R, Z)
TXS0102DCTRE4	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFE (R, Z)
TXS0102DCTRE4.A	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFE (R, Z)
TXS0102DCTRE4.B	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFE (R, Z)
TXS0102DCTT	Active	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(35UT, NFE) (R, Z)
TXS0102DCTT.B	Active	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(35UT, NFE) (R, Z)
TXS0102DCTTE4	Active	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFE (R, Z)
TXS0102DCTTE4.B	Active	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFE (R, Z)
TXS0102DCTTG4	Active	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFE (R, Z)
TXS0102DCTTG4.B	Active	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFE (R, Z)
TXS0102DCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(35ST, FE, NFEQ, NFER) NZ
TXS0102DCUR.A	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(35ST, FE, NFEQ, NFER) NZ
TXS0102DCUR.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(35ST, FE, NFEQ, NFER) NZ
TXS0102DCURG4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFER

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXS0102DCURG4.A	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFER
TXS0102DCURG4.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFER
TXS0102DCUT	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(FE, NFEQ, NFER) NZ
TXS0102DCUT.A	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(FE, NFEQ, NFER) NZ
TXS0102DCUT.B	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(FE, NFEQ, NFER) NZ
TXS0102DCUTG4	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFER
TXS0102DCUTG4.A	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFER
TXS0102DCUTG4.B	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFER
TXS0102DQER	Active	Production	X2SON (DQE) | 8	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H
TXS0102DQER.A	Active	Production	X2SON (DQE) | 8	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H
TXS0102DQER.B	Active	Production	X2SON (DQE) | 8	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H
TXS0102DQMR	Active	Production	X2SON (DQM) | 8	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H (2H7, 2HR) (2HG, 2HH)
TXS0102DQMR.A	Active	Production	X2SON (DQM) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H (2H7, 2HR) (2HG, 2HH)
TXS0102DQMR.B	Active	Production	X2SON (DQM) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H (2H7, 2HR) (2HG, 2HH)
TXS0102DQMRG4	Active	Production	X2SON (DQM) | 8	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H (2H7, 2HR) (2HG, 2HH)
TXS0102DQMRG4.A	Active	Production	X2SON (DQM) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H (2H7, 2HR) (2HG, 2HH)
TXS0102DQMRG4.B	Active	Production	X2SON (DQM) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H (2H7, 2HR) (2HG, 2HH)
TXS0102DTTR	Active	Production	X1SON (DTT) | 8	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3HOH
TXS0102YZPR	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	2H
TXS0102YZPR.B	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	2H

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TXS0102 :

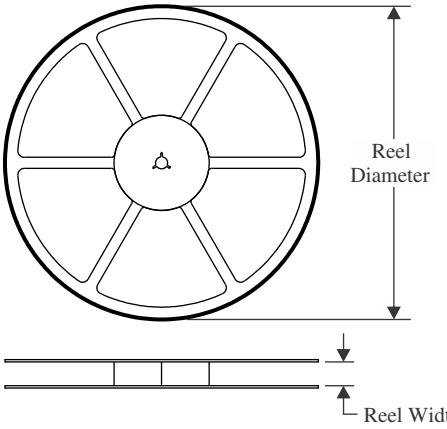
- Automotive : TXS0102-Q1

NOTE: Qualified Version Definitions:

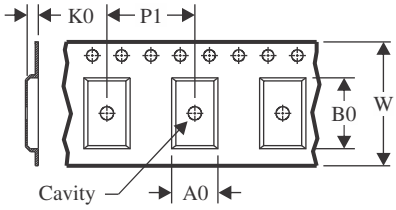
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

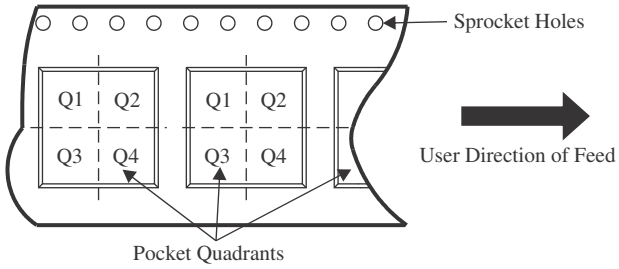


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

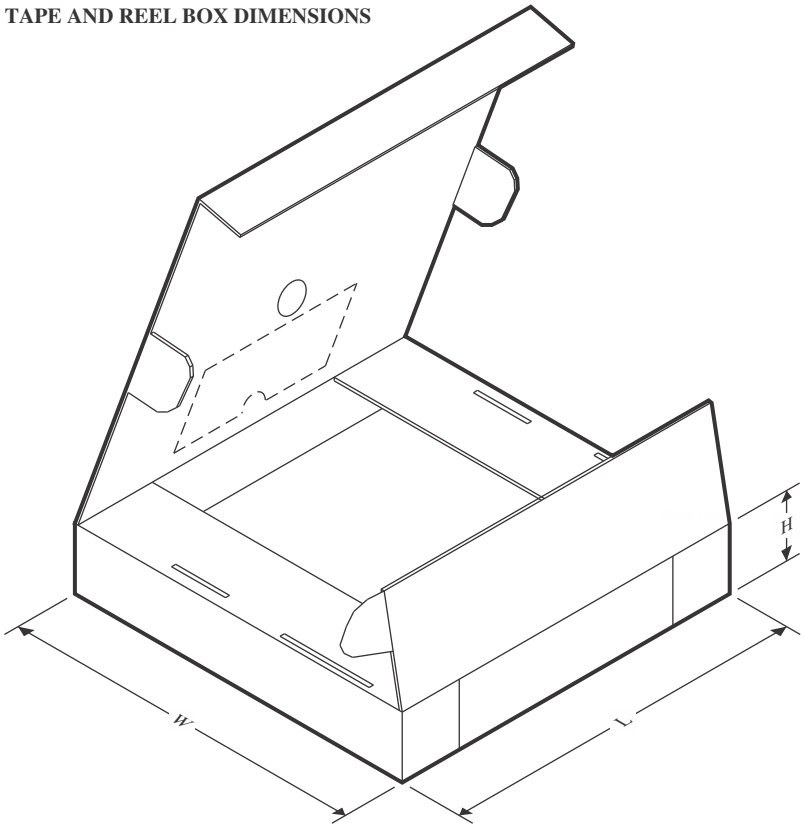
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0102DCTR	SSOP	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
TXS0102DCTRE4	SSOP	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
TXS0102DCTT	SSOP	DCT	8	250	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
TXS0102DCTTE4	SSOP	DCT	8	250	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
TXS0102DCTTG4	SSOP	DCT	8	250	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
TXS0102DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TXS0102DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3
TXS0102DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TXS0102DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TXS0102DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
TXS0102DQMR	X2SON	DQM	8	3000	180.0	9.5	1.4	2.0	0.5	4.0	8.0	Q1
TXS0102DQMR	X2SON	DQM	8	3000	180.0	8.4	1.57	2.21	0.59	4.0	8.0	Q1
TXS0102DQMRG4	X2SON	DQM	8	3000	180.0	9.5	1.4	2.0	0.5	4.0	8.0	Q1
TXS0102DQMRG4	X2SON	DQM	8	3000	180.0	8.4	1.57	2.21	0.59	4.0	8.0	Q1
TXS0102DTTR	X1SON	DTT	8	5000	180.0	8.4	1.15	2.1	0.48	4.0	8.0	Q1
TXS0102YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

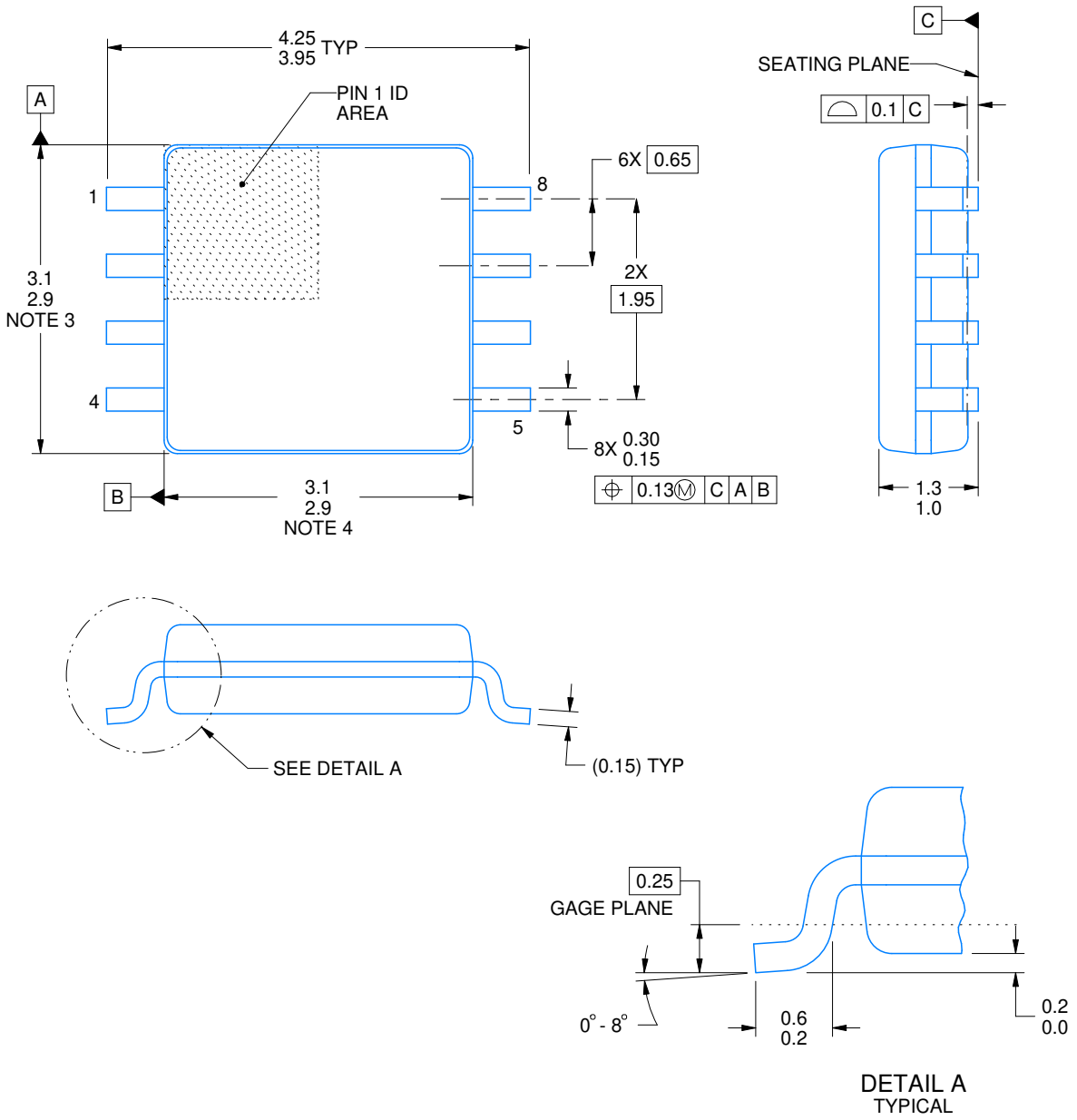
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0102DCTR	SSOP	DCT	8	3000	183.0	183.0	20.0
TXS0102DCTRE4	SSOP	DCT	8	3000	183.0	183.0	20.0
TXS0102DCTT	SSOP	DCT	8	250	190.0	190.0	30.0
TXS0102DCTTE4	SSOP	DCT	8	250	183.0	183.0	20.0
TXS0102DCTTG4	SSOP	DCT	8	250	183.0	183.0	20.0
TXS0102DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TXS0102DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
TXS0102DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
TXS0102DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
TXS0102DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
TXS0102DQMR	X2SON	DQM	8	3000	184.0	184.0	19.0
TXS0102DQMR	X2SON	DQM	8	3000	202.0	201.0	28.0
TXS0102DQMRG4	X2SON	DQM	8	3000	184.0	184.0	19.0
TXS0102DQMRG4	X2SON	DQM	8	3000	202.0	201.0	28.0
TXS0102DTTR	X1SON	DTT	8	5000	210.0	185.0	35.0
TXS0102YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0

PACKAGE OUTLINE

DCT0008A

SSOP - 1.3 mm max height

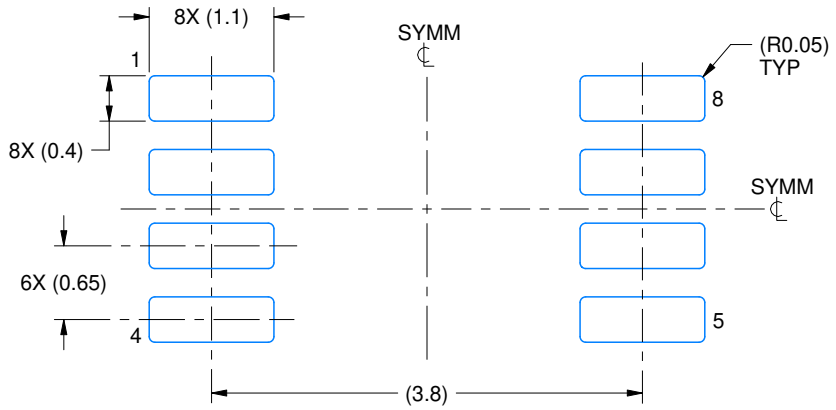
SMALL OUTLINE PACKAGE



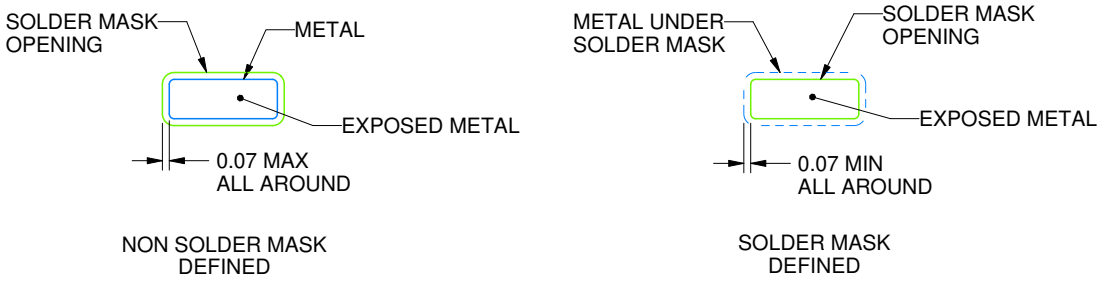
4220784/D 10/2025

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

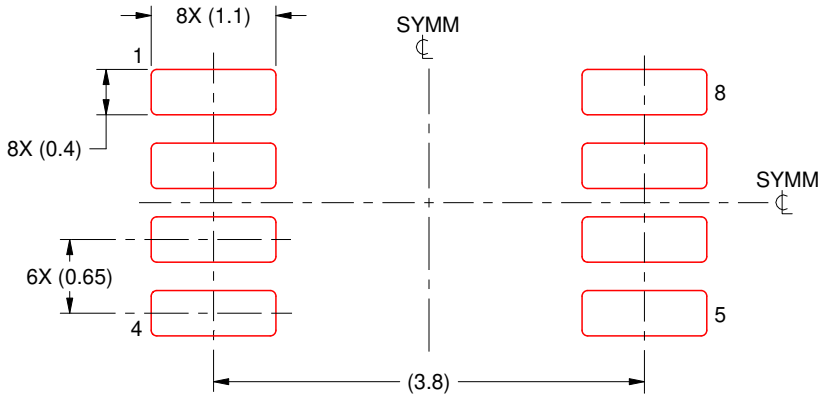


SOLDER MASK DETAILS

4220784/D 10/2025

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/D 10/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

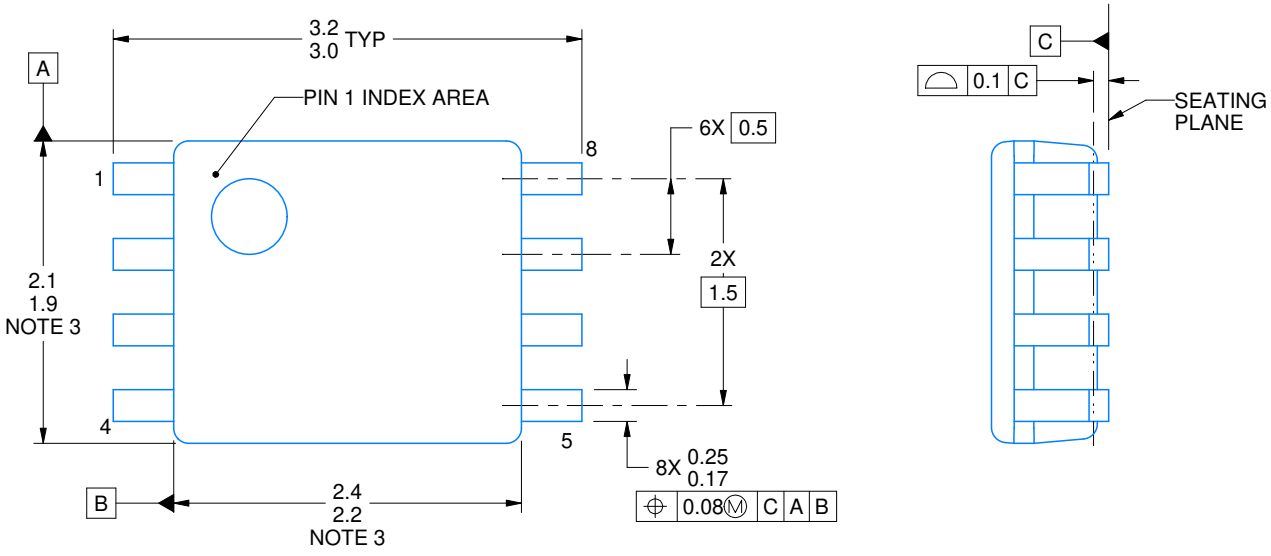
DCU0008A

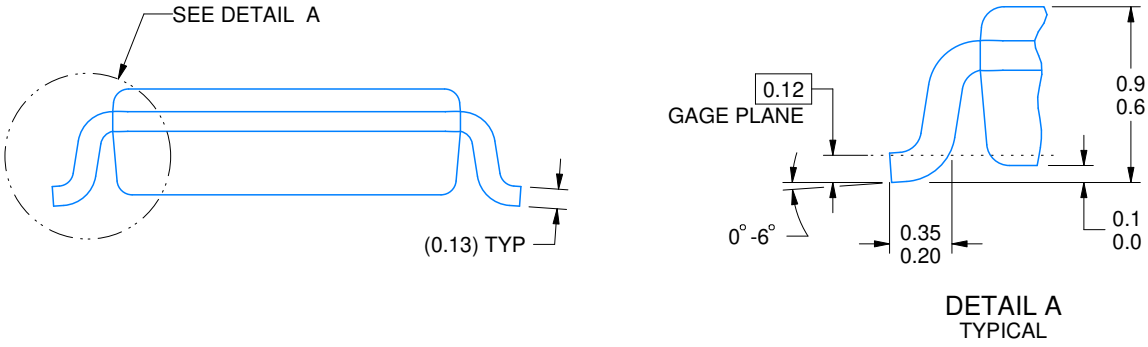


PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

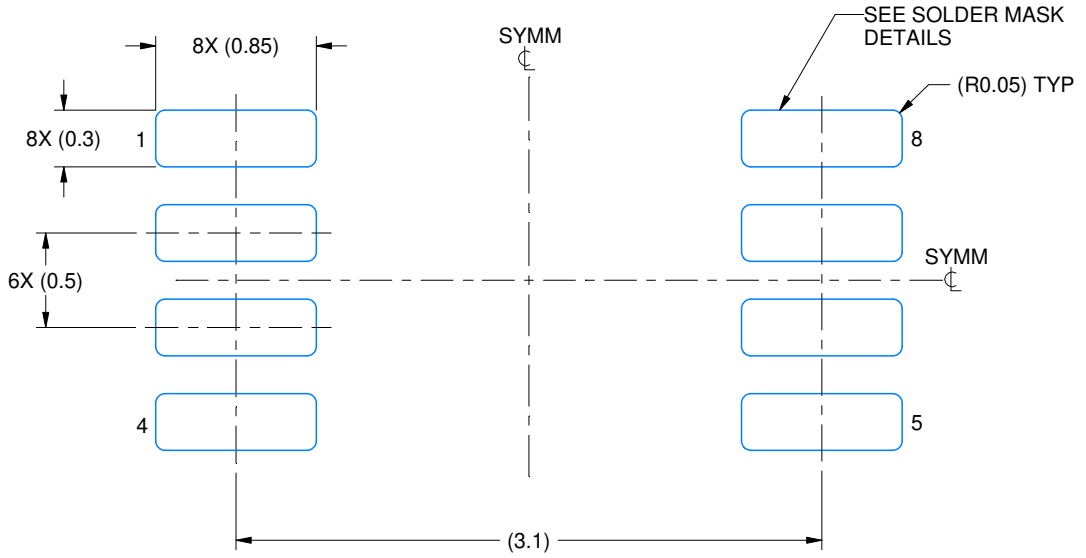




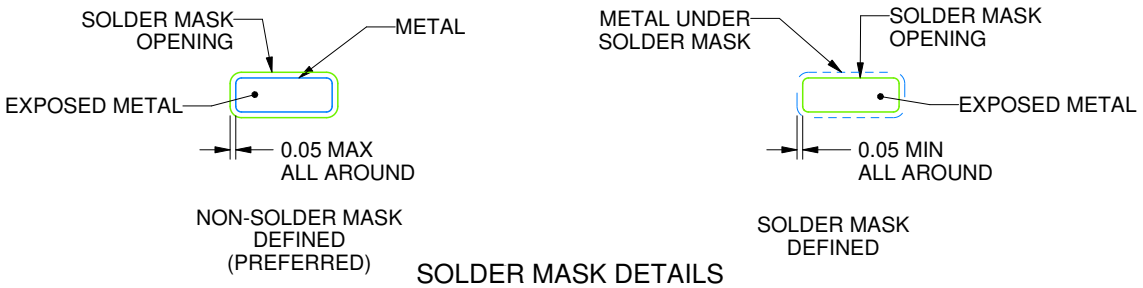
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

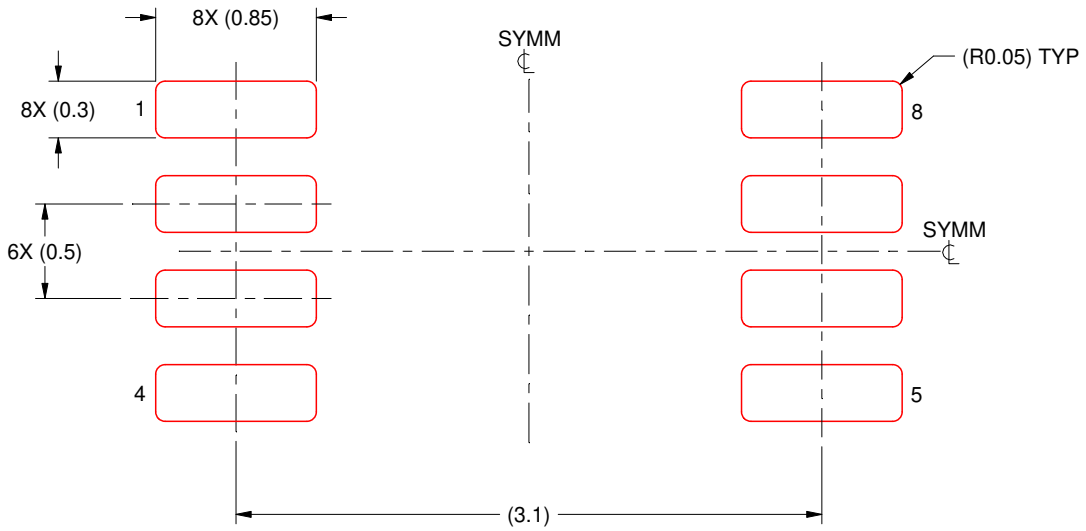


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



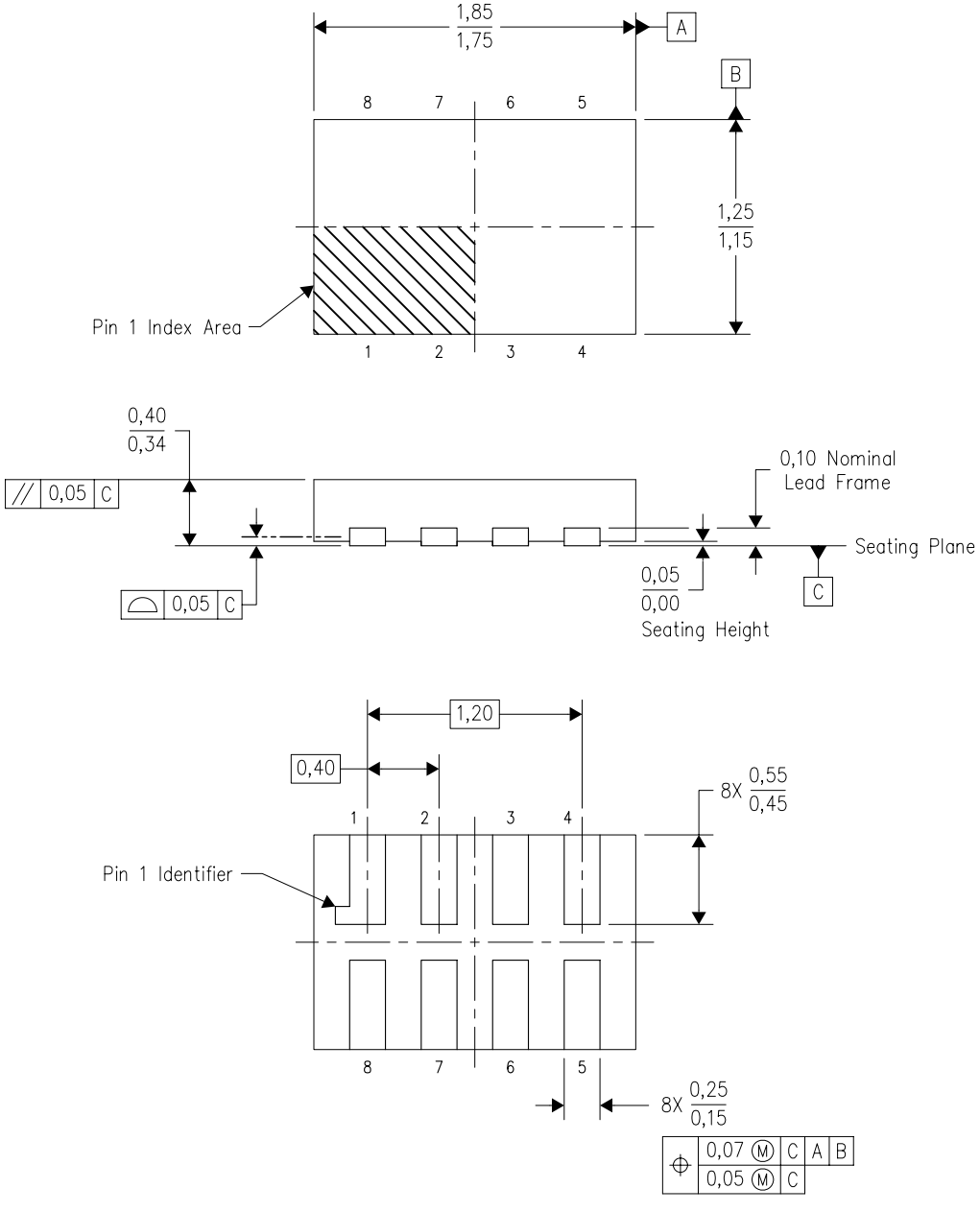
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DQM (R–PX2SON–N8) PLASTIC SMALL OUTLINE NO–LEAD

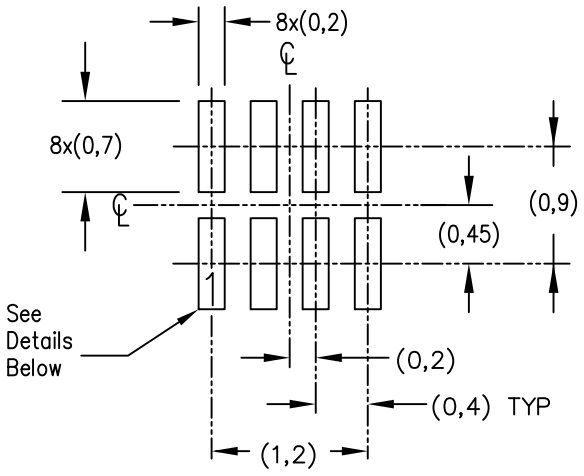


4210302/A 06/2009

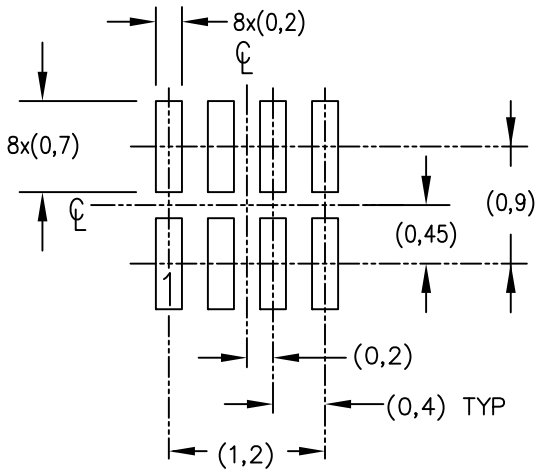
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

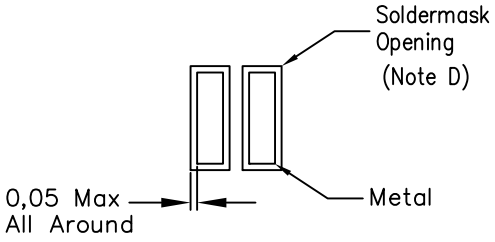
DQM (R–PX2SON–N8) PLASTIC SMALL OUTLINE NO–LEAD

Example Board Layout

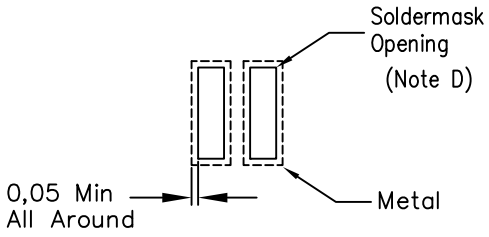


Example Stencil Design
0.1mm Thick Stencil
(Note C)





Non Solder Mask Defined Pad



Solder Mask Defined Pad

Solder Mask Details

4218746/A 07/13

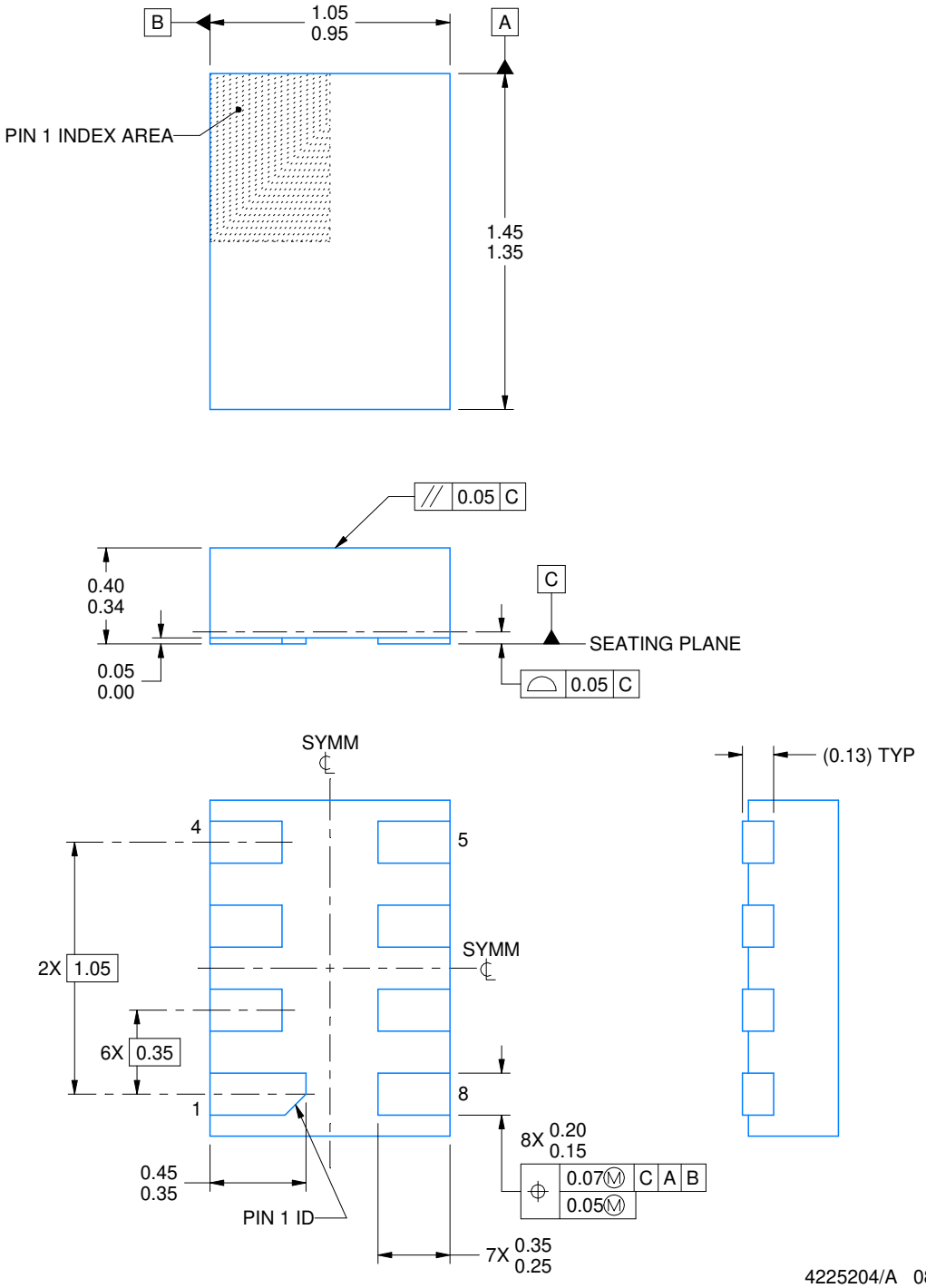
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
D. Customers should contact their board fabrication site for recommended solder mask tolerances.

PACKAGE OUTLINE

DQE0008A

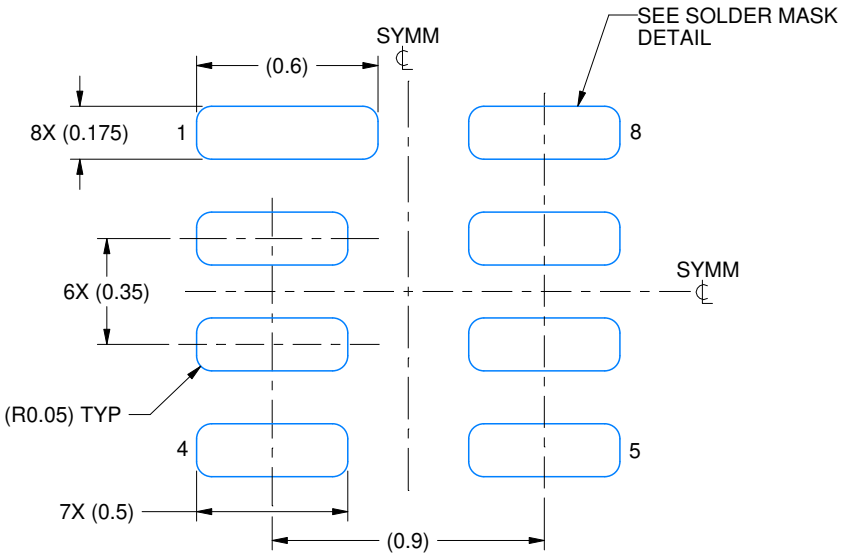
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

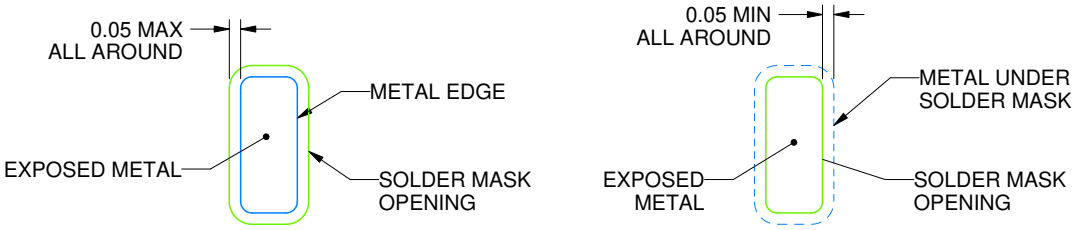


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-287 variation X2EAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS

4225204/A 08/2019

NOTES: (continued)

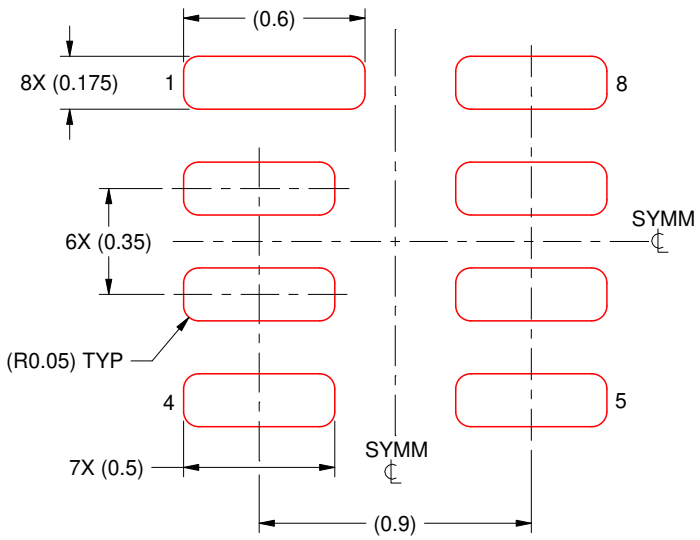
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQE0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



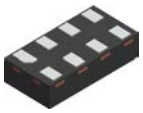
SOLDER PASTE EXAMPLE
BASED ON 0.075 MM THICK STENCIL
SCALE: 40X

4225204/A 08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

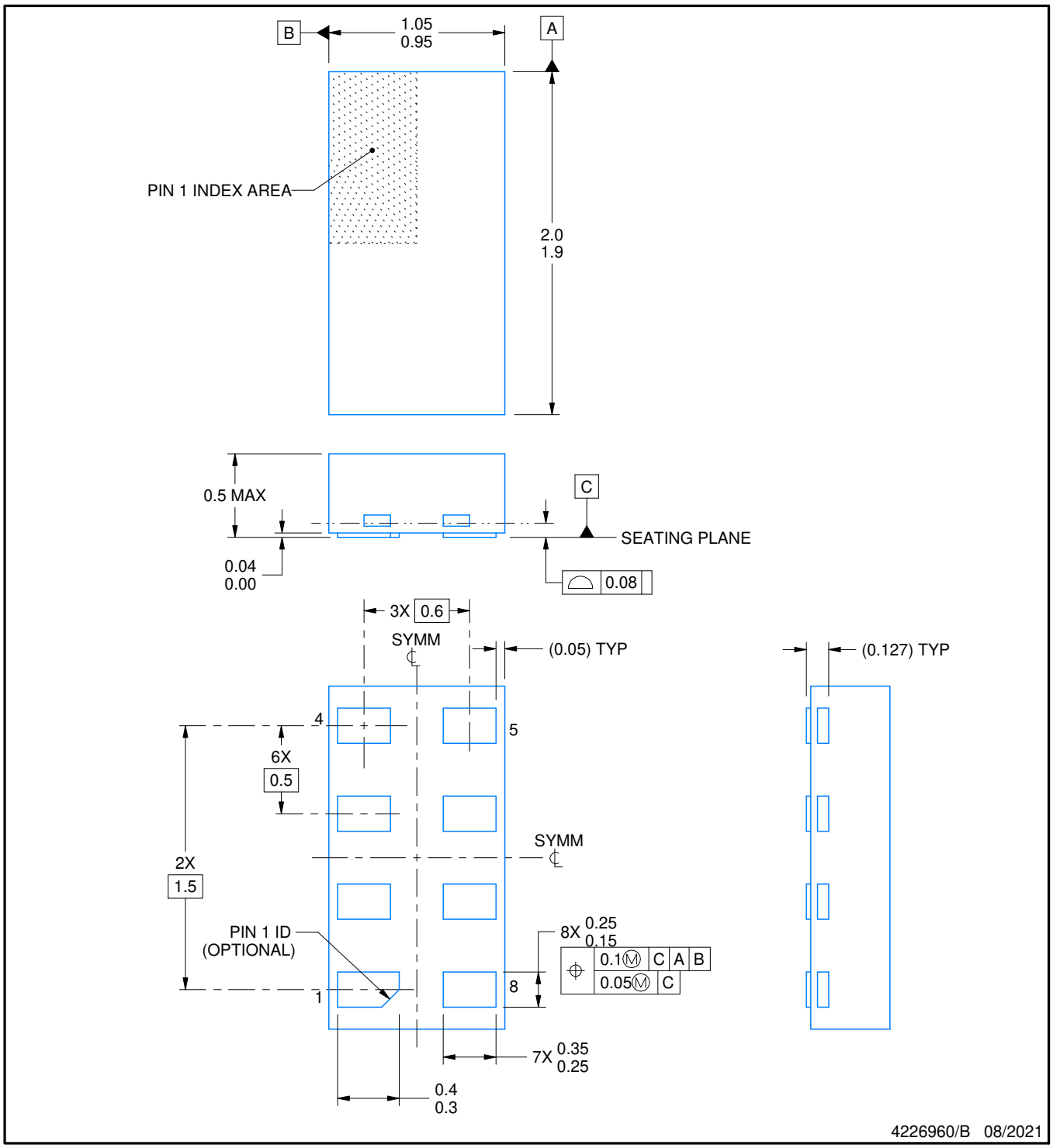
DTT0008A



PACKAGE OUTLINE

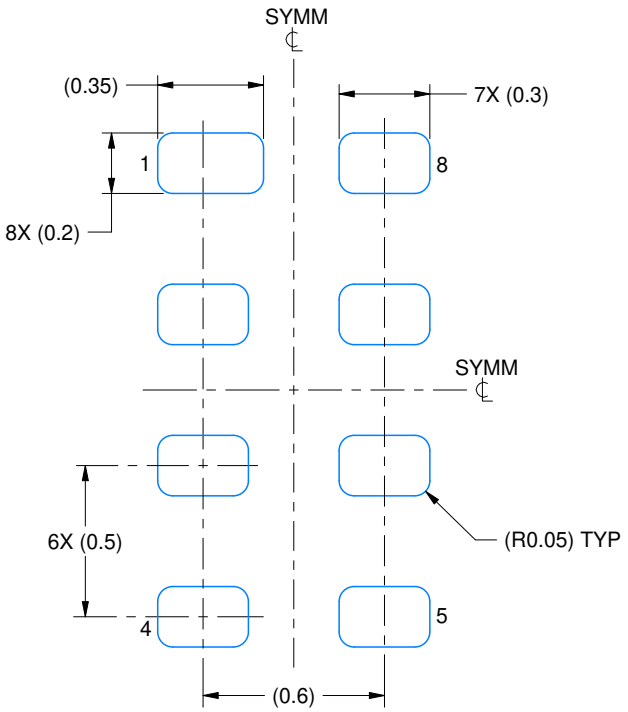
X1SON - 0.5 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

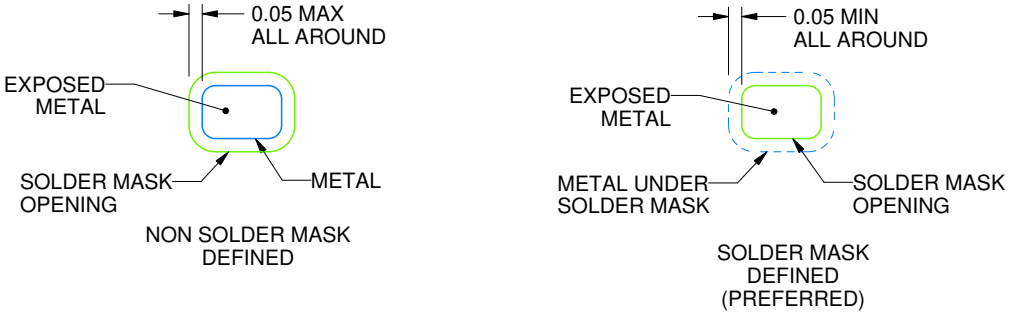


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X

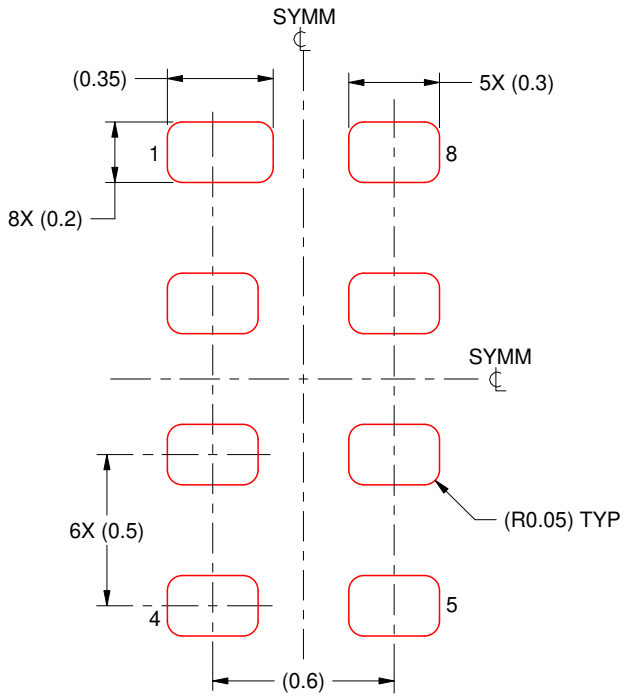


SOLDER MASK DETAILS

4226960/B 08/2021

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4226960/B 08/2021

NOTES: (continued)

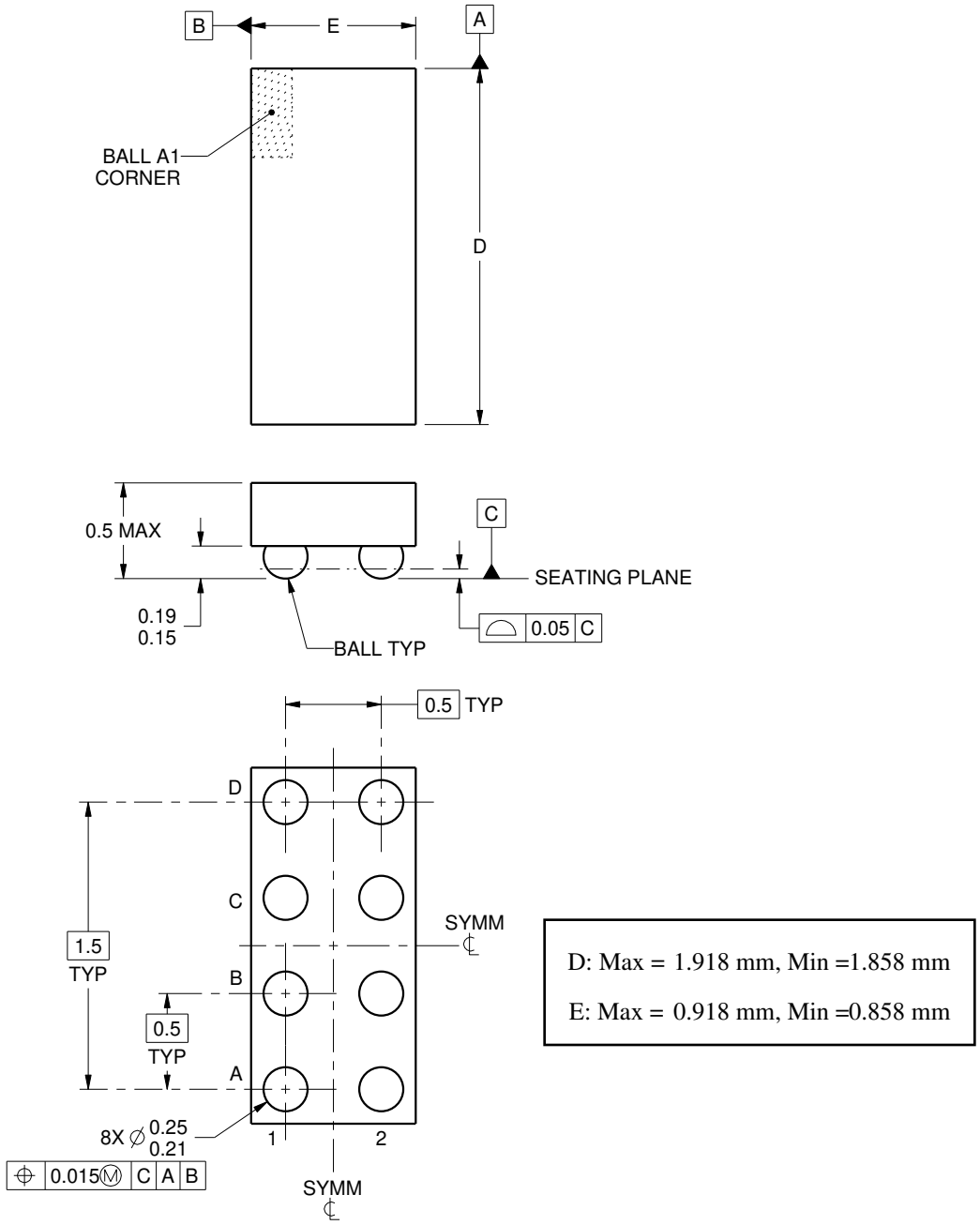
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YZP0008

DSBGA - 0.5 mm max height

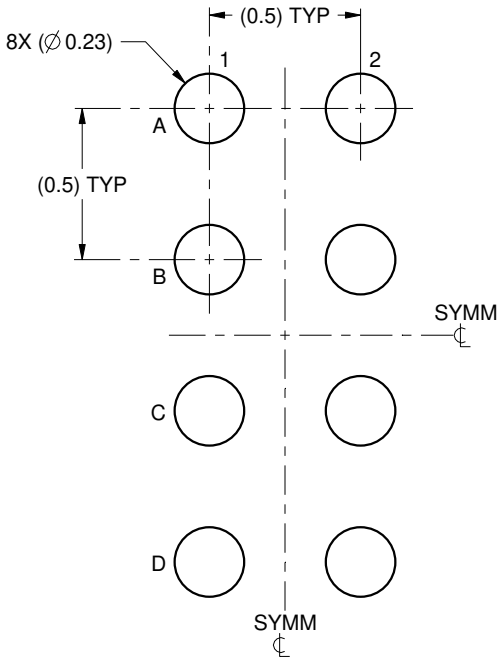
DIE SIZE BALL GRID ARRAY



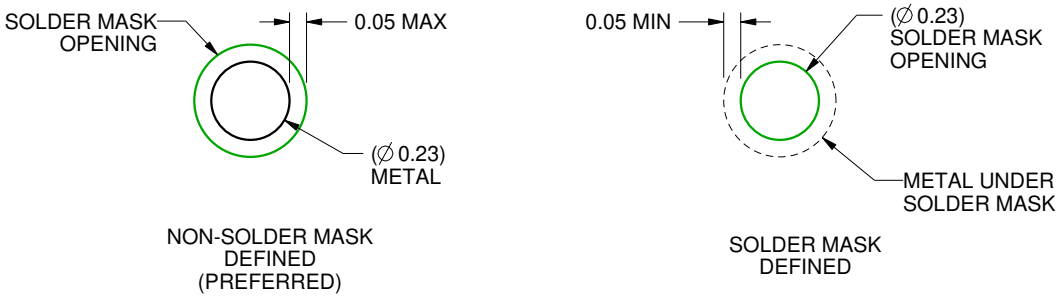
4223082/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

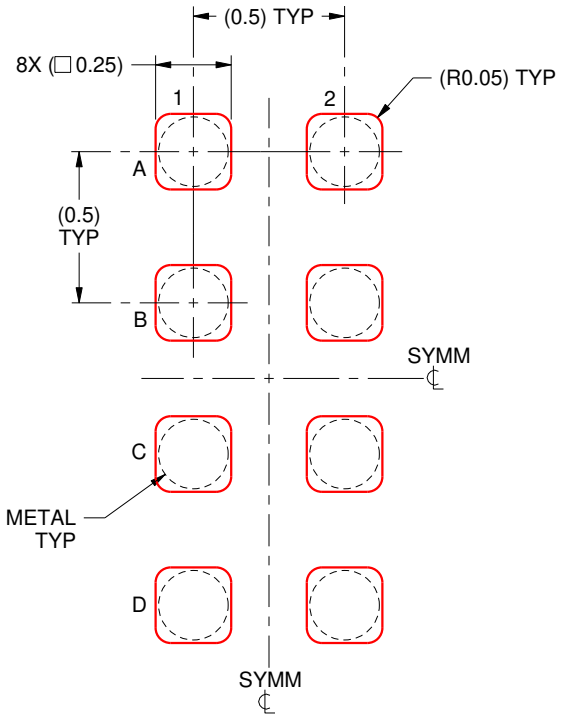


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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