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LIS3MDL

Datasheet

Digital output magnetic sensor: ultralow-power, high-performance 3-axis magnetometer

LGA-12L
(2.0 x 2.0 x 1.0 mm)

Product status link
LIS3MDL

Product summary	
Order code	LIS3MDLTR
Temperature range [°C]	-40 to +85
Package	LGA-12L
Packing	Tape and reel

Product resources
AN4602 (device application note)
TN0018 (design and soldering)

Features

- Wide supply voltage, 1.9 V to 3.6 V
- Independent IO supply (1.8 V)
- ±4/±8/±12/±16 gauss selectable magnetic full scales
- Continuous and single-conversion modes
- 16-bit data output
- Interrupt generator
- Self-test
- I²C/SPI digital output interface
- Power-down mode / low-power mode
- ECOPACK and RoHS compliant

Applications

- Magnetometers
- Compasses

Description

The LIS3MDL is an ultralow-power high-performance 3-axis magnetic sensor with user-selectable full scales of ±4/±8/±12/±16 gauss.

The self-test capability allows the user to check the functioning of the sensor in the final application.

The device may be configured to generate interrupt signals for magnetic field detection.

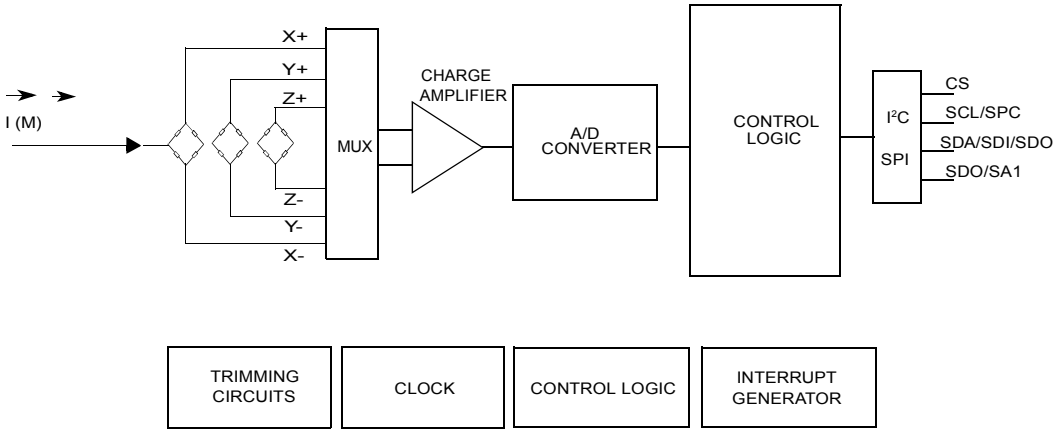
The LIS3MDL includes an I²C serial bus interface that supports standard and fast mode (100 kHz and 400 kHz) and SPI serial standard interfaces.

The device is available in a small thin plastic, land grid array (LGA) package and is guaranteed to operate over an extended temperature range of -40°C to +85°C.

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. **Pin description**

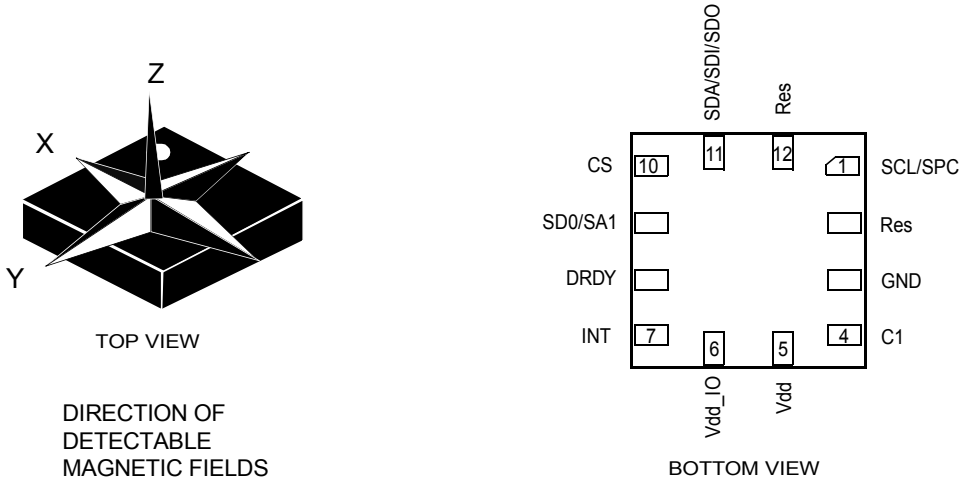


Table 1. **Pin description**

Pin#	Name	Function
1	SCL SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
2	Reserved	Connect to GND
3	GND	Connect to GND
4	C1	Capacitor connection (C1 = 100 nF)
5	Vdd	Power supply
6	Vdd_IO	Power supply for I/O pins
7	INT	Interrupt
8	DRDY	Data ready
9	SDO SA1	SPI serial data output (SDO) I²C less significant bit of the device address (SA1)
10	CS	Enable SPI I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)
11	SDA SDI SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
12	Reserved	Connect to GND

2 Magnetic and electrical specifications

2.1 Magnetic characteristics

@Vdd = 2.5 V, T = 25°C unless otherwise noted. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.9 V to 3.6 V.

Table 2. Magnetic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
FS	Measurement range			±4		gauss
				±8		
				±12		
				±16		
GN	Sensitivity	FS = ±4 gauss		6842		LSB/ gauss
		FS = ±8 gauss		3421		
		FS = ±12 gauss		2281		
		FS = ±16 gauss		1711		
Zgauss	Zero-gauss level	FS = ±4 gauss		±1		gauss
RMS	RMS noise	X-axis; FS = ±12 gauss; Ultrahigh-performance mode		3.2		mgauss
		Y-axis; FS = ±12 gauss Ultrahigh-performance mode		3.2		mgauss
		Z-axis; FS = ±12 gauss Ultrahigh-performance mode		4.1		mgauss
NL	Nonlinearity	Best-fit straight line FS = ±12 gauss Happlied = ±6 gauss		±0.12		%FS
ST	Self test[2]	X-axis FS = ±12 gauss	1		3	gauss
		Y-axis FS = ±12 gauss	1		3	
		Z-axis FS = ±12 gauss	0.1		1	
DF	Magnetic disturbance field	Zero-gauss offset starts to degrade			50	gauss
Top	Operating temperature range		-40		+85	°C

1. *Typical specifications are not guaranteed.*
2. *Absolute value*

2.2 Temperature sensor characteristics

@Vdd = 2.5 V, T = 25°C unless otherwise noted. The product is factory calibrated at 2.5 V.

Table 3. Temperature sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		8		LSB/°C
TODR	Temperature refresh rate(2)			ODR		Hz
Top	Operating temperature range		-40		+85	°C

1. *Typical specifications are not guaranteed.*
2. *If the TEMP_EN bit in CTRL_REG1 (20h) is set to1, temperature data is acquired at each conversion cycle. Refer to Table 21.*

2.3 Electrical characteristics

@Vdd = 2.5 V, T = 25°C unless otherwise noted. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.9 V to 3.6 V.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		1.9		3.6	V
Vdd_IO	Power supply for I/O		1.71	1.8	Vdd+0.1	
Idd_HR	Current consumption in ultrahigh-resolution mode	ODR = 20 Hz		270		µA
Idd_LP	Current consumption in low-power mode	ODR = 20 Hz		40		µA
Idd_PD	Current consumption in power down			1		µA
Top	Operating temperature range		-40		+85	°C

1. *Typical specifications are not guaranteed.*

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

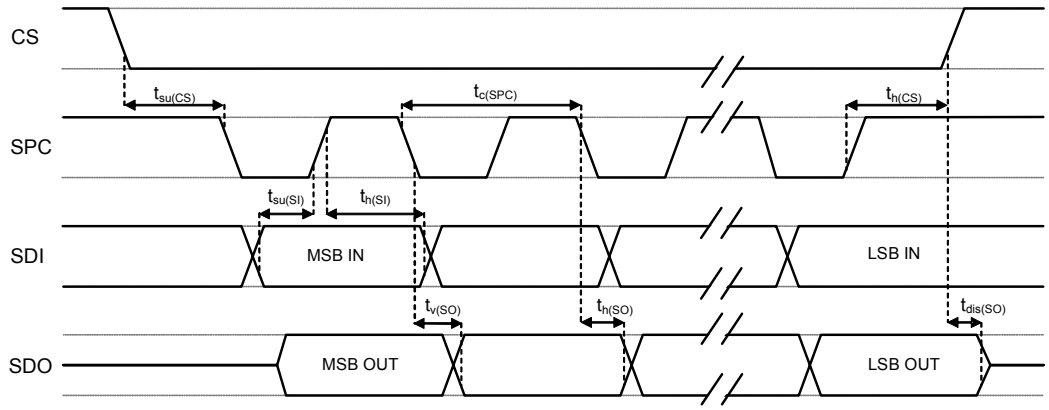
Subject to general operating conditions for Vdd and Top.

Table 5. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min.	Max.	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

1. *Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.*

Figure 3. SPI slave timing diagram



*Note: Measurement points are done at 0.3*Vdd_IO and 0.7*Vdd_IO for both input and output ports.*

2.4.2 I²C - inter IC control interface

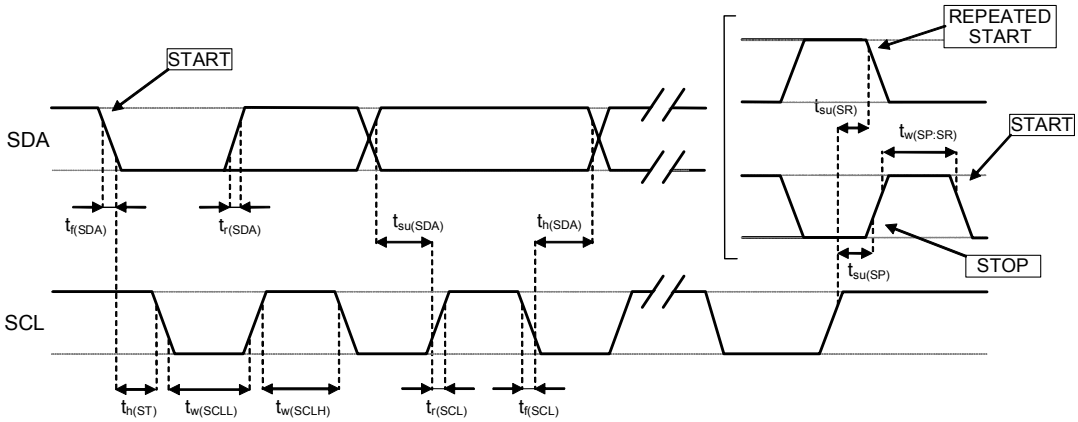
Subject to general operating conditions for Vdd and Top.

Table 6. I²C slave timing values

Symbol	Parameter	I²C standard mode(1)		I²C fast mode(1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$(2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$(2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. *Data based on standard I²C protocol requirement, not tested in production.*
2. *C_b = total capacitance of one bus line, in pF.*

Figure 4. I²C slave timing diagram



*Note: Measurement points are done at 0.3*Vdd_IO and 0.7*Vdd_IO for both ports.*

2.5 Absolute maximum ratings

Stresses above those listed as absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to +4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to +4.8	V
Vin	Input voltage on any control pin (SCL/SPC, SDA/SDI/SDO, SDO/SA1, CS)	-0.3 to Vdd_IO +0.3	V
A_{UNP}	Acceleration (any axis)	3,000 for 0.5 ms	*g*
		10,000 for 0.1 ms	*g*
M_{EF}	Maximum exposed field	1000	gauss
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Terminology and functionality

3.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined, for example, by applying a magnetic field of 1 gauss to it.

3.2 Zero-gauss level

Zero-gauss level offset describes the deviation of an actual output signal from the ideal output if no magnetic field is present.

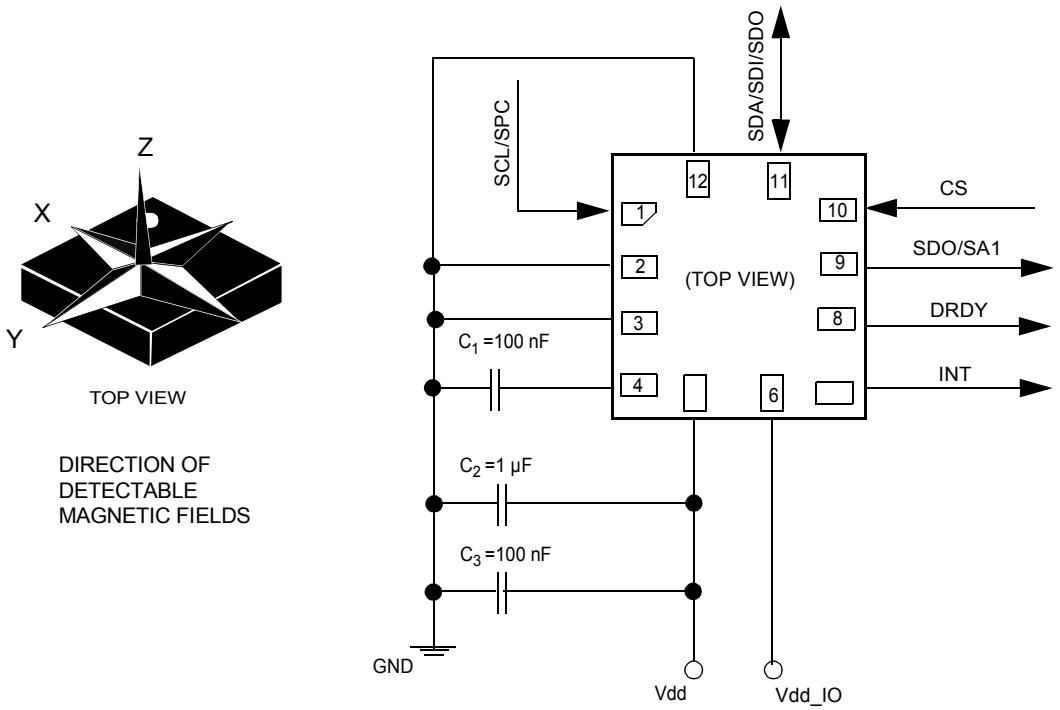
3.3 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and zero-gauss level (TyOff).

The trimming values are stored in the device in nonvolatile memory. Each time the device is turned on, the trimming parameters are downloaded to the registers to be employed during active operation, which allows using the device without further calibration.

4 Application hints

Figure 5. LIS3MDL electrical connections



4.1 External capacitors

The LIS3MDL requires one external capacitor (C1 = 100 nF) connected between pin 4 and GND.

The device core power supply line (Vdd) needs one high-frequency decoupling capacitor (C3 = 100 nF, ceramic) as near as possible to the supply pin, and a low-frequency electrolytic capacitor (C2 = 1 µF). All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to Figure 5).

The functionality of the device and the measured magnetic field data are selectable and accessible through the I²C / SPI interfaces.

The functions, the threshold, and the timing of the interrupt pin (INT) can be completely programmed by the user through the I²C / SPI interfaces.

When the I²C or 3-wire SPI is used, the SDO/SA1 pin must be connected to Vdd_IO or GND.

4.2 Soldering information

The LGA package is compliant with the ECOPACK and RoHS standard.

It is qualified for soldering heat resistance according to JEDEC J-STD-020.

For land pattern and soldering recommendations, consult technical note TN0018 available on www.st.com.

4.3 High-current wiring effects

High current in wiring and printed circuit traces can cause errors in magnetic field measurements for compassing.

Conductor-generated magnetic fields add to the Earth's magnetic field, causing errors in compass heading computation.

Keep currents higher than 10 mA a few millimeters away from the sensor IC.

5 Digital interfaces

The registers embedded in the LIS3MDL may be accessed through both the I²C and SPI serial interfaces. The latter may be software configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped to the same pads. To select/exploit the I²C interface, the CS line must be tied high (that is, connected to Vdd_IO).

Table 8. Serial interface pin description

Pin name	Pin description
CS	Enable SPI I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)
SCL SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SA1 SDO	I²C less significant bit of the device address (SA1) SPI serial data output (SDO)

5.1 I²C serial interface

The LIS3MDL I²C is a bus slave. The I²C is employed to write data to registers whose content can also be read back.

The relevant I²C terminology is given in the table below.

Table 9. I²C terminology

Term	Description
Transmitter	The device that sends data to the bus
Receiver	The device that receives data from the bus
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I²C interface is compliant with fast mode (400 kHz) I²C standards, as well as with normal mode.

When the I²C interface is used, the SDO/SA1 pin has to be connected to Vdd_IO or GND.

5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high to low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first seven bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LIS3MDL is 00111x0b, whereas the x bit is modified by the SDO/SA1 pin in order to modify the device address. If the SDO/SA1 pin is connected to the voltage supply, the address is 0011110b, otherwise, if the SDO/SA1 pin is connected to ground, the address is 0011100b.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver that has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LIS3MDL behaves like a slave device and the following protocol must be adhered to. After the START condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit subaddress (SUB) is transmitted: the 7 LSb represent the actual register address while the MSb enables address autoincrement. If the MSb of the SUB field is 1, the SUB (register address) is automatically increased to allow multiple data read/write.

The slave address is completed with a read/write bit. If the bit is 1 (read), a repeated START (SR) condition must be issued after the two subaddress bytes; if the bit is 0 (write) the master transmits to the slave with direction unchanged. Table 10 explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 10. SAD+read/write patterns

Command	SAD[6:2]	SAD[1] = SDO/SA1	SAD[0]	R/W	SAD+R/W
Read	00111	0	0	1	00111001 (39h)
Write	00111	0	0	0	00111000 (38h)
Read	00111	1	0	1	00111101 (3Dh)
Write	00111	1	0	0	00111100 (3Ch)

Table 11. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 12. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 13. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 14. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+ W		SUB		SR	SAD+ R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (that is, it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low to high transition on the SDA line while the SCL line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the subaddress field. In other words, SUB(7) must be equal to 1, while SUB(6-0) represents the address of the first register to be read.

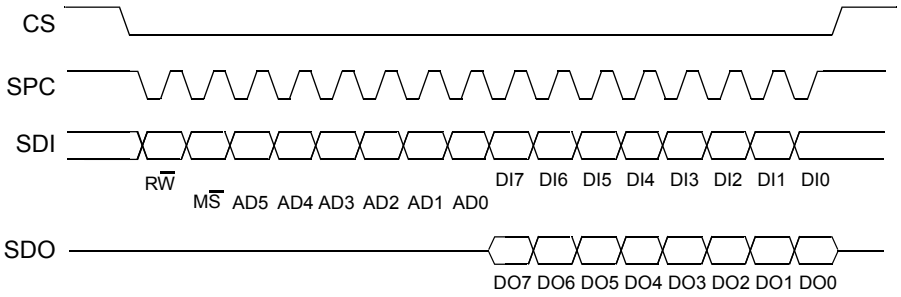
In the presented communication format, MAK is master acknowledge and NMAK is no master acknowledge.

5.2 SPI bus interface

The LIS3MDL SPI is a bus slave. The SPI allows writing to and reading from the registers of the device.

The serial interface interacts with the application using four wires: **CS**, **SPC**, **SDI**, and **SDO**.

Figure 6. Read and write protocol



CS enables the serial port and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in the case of multiple byte read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is autoincremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

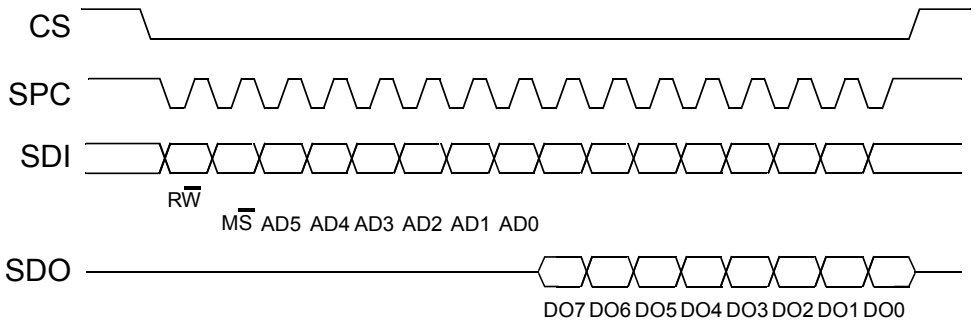
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When the M$\overline{S}$ bit is 0, the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is 1, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.2.1 SPI read

Figure 7. **SPI read**



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: READ bit. The value is 1.

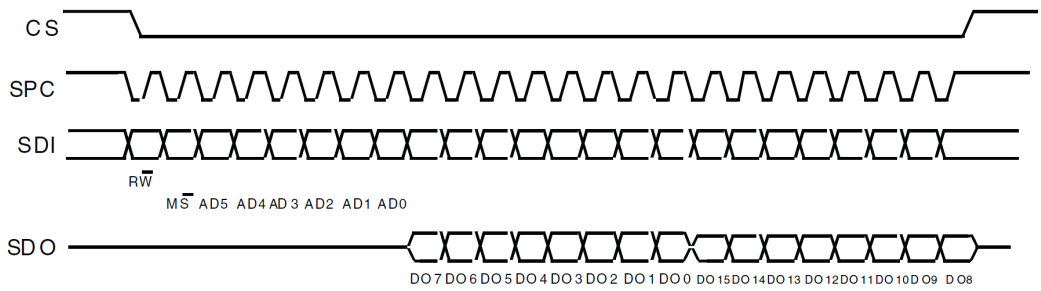
bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

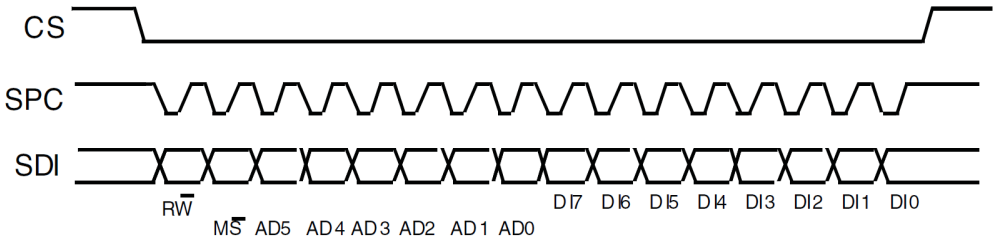
bit 16-... : data DO(...-8). Further data in multiple byte reads.

Figure 8. **Multiple byte SPI read protocol (2-byte example)**



5.2.2 SPI write

Figure 9. **SPI write protocol**



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

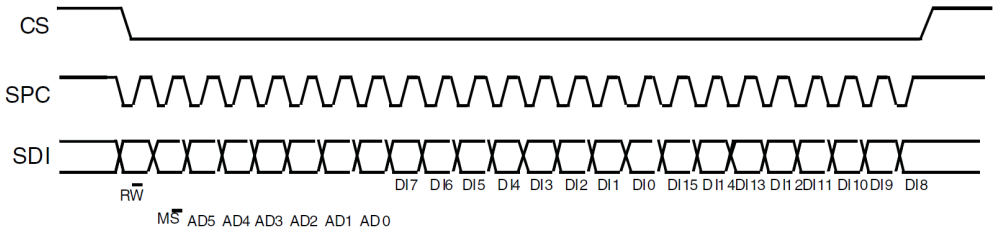
bit 1: $M\overline{S}$ bit. When 0, does not increment the address; when 1, increments the address in multiple writes.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

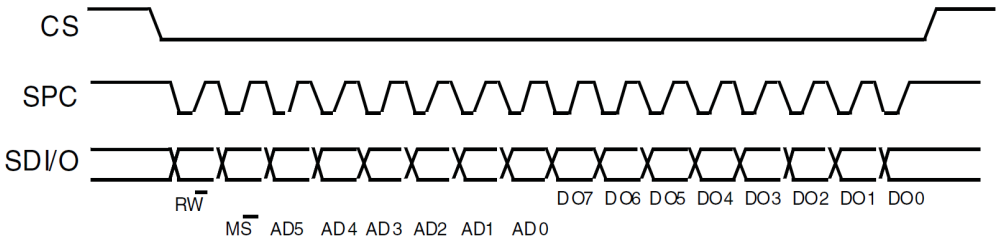
Figure 10. **Multiple byte SPI write protocol (2-byte example)**



5.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting bit SIM to 1 (SPI serial interface mode selection) in CTRL_REG3 (22h).
When 3-wire mode is used, the SDO/SA1 pin has to be connected to GND or Vdd_IO.

Figure 11. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:
bit 0: READ bit. The value is 1.
bit 1: $M\overline{S}$ bit. When 0, does not increment the address; when 1, increments the address in multiple reads.
bit 2-7: address AD(5:0). This is the address field of the indexed register.
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).
A multiple read command is also available in 3-wire mode.

6 Register mapping

The table below provides a list of the 8-bit registers embedded in the device and their respective addresses.

Table 15. Register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved		00 - 04	--	--	Reserved
OFFSET_X_REG_L_M	R/W	05	00000101	00000000	Hard-iron registers
OFFSET_X_REG_H_M	R/W	06	00000110	00000000	
OFFSET_Y_REG_L_M	R/W	07	00000111	00000000	
OFFSET_Y_REG_H_M	R/W	08	00001000	00000000	
OFFSET_Z_REG_L_M	R/W	09	00001001	00000000	
OFFSET_Z_REG_H_M	R/W	0A	00001010	00000000	
Reserved		0B - 0E	--	--	Reserved
WHO_AM_I	R	0F	0000 1111	00111101	Dummy register
Reserved		10 - 1F	--	--	Reserved
CTRL_REG1	R/W	20	0010 0000	00010000	
CTRL_REG2	R/W	21	0010 0001	00000000	
CTRL_REG3	R/W	22	0010 0010	00000011	
CTRL_REG4	R/W	23	0010 0011	00000000	
CTRL_REG5	R/W	24	0010 0100	00000000	
Reserved		25 - 26	--	--	Reserved
STATUS_REG	R	27	0010 0111	Output	
OUT_X_L	R	28	0010 1000	Output	
OUT_X_H	R	29	0010 1001	Output	
OUT_Y_L	R	2A	0010 1010	Output	
OUT_Y_H	R	2B	0010 1011	Output	
OUT_Z_L	R	2C	0010 1100	Output	
OUT_Z_H	R	2D	0010 1101	Output	
TEMP_OUT_L	R	2E	0010 1110	Output	
TEMP_OUT_H	R	2F	0010 1111	Output	
INT_CFG	R/W	30	00110000	11101000	
INT_SRC	R	31	00110001	00000000	
INT_THS_L	R/W	32	00110010	00000000	
INT_THS_H	R/W	33	00110011	00000000	

Reserved registers or those not listed in the table above must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

7 Registers description

7.1 OFFSET_X_REG_L_M (05h) and OFFSET_X_REG_H_M (06h)

These registers comprise a 16-bit register and represent X hard-iron offset in order to compensate environmental effects (data in two's complement). These values act on the magnetic output data value in order to delete the environmental offset.

7.2 OFFSET_Y_REG_L_M (07h) and OFFSET_Y_REG_H_M (08h)

These registers comprise a 16-bit register and represent Y hard-iron offset in order to compensate environmental effects (data in two's complement). These values act on the magnetic output data value in order to delete the environmental offset.

7.3 OFFSET_Z_REG_L_M (09h) and OFFSET_Z_REG_H_M (0Ah)

These registers comprise a 16-bit register and represent Z hard-iron offset in order to compensate environmental effects (data in two's complement). These values act on the magnetic output data value in order to delete the environmental offset.

7.4 WHO_AM_I (0Fh)

Device identification register

Table 16. WHO_AM_I register

0	0	1	1	1	1	0	1

7.5 CTRL_REG1 (20h)

Table 17. CTRL_REG1 register

TEMP_EN	OM1	OM0	DO2	DO1	DO0	FAST_ODR	ST

Table 18. CTRL_REG1 description

TEMP_EN	Enables temperature sensor. Default value: 0 (0: temperature sensor disabled; 1: temperature sensor enabled)
OM[1:0]	X and Y axes operative mode selection (refer to Table 20). Default value: 00
DO[2:0]	Output data rate selection (refer to Table 21). Default value: 100
FAST_ODR	FAST_ODR enables data rates higher than 80 Hz (refer to Table 19). Default value: 0 (0: FAST_ODR disabled; 1: FAST_ODR enabled)
ST	Enables self-test. Default value: 0 (0: self-test disabled; 1: self-test enabled)

Table 19. Data rate configuration

DO2	DO1	DO0	FAST_ODR	ODR [Hz]	OM
X	X	X	1	1000	LP
X	X	X	1	560	MP
X	X	X	1	300	HP
X	X	X	1	155	UHP

Table 20. X and Y axes operating mode selection

OM1	OM0	Operating mode for X and Y axes
0	0	Low-power mode
0	1	Medium-performance mode
1	0	High-performance mode
1	1	Ultrahigh-performance mode

Table 21. Output data rate configuration

DO2	DO1	DO0	ODR [Hz]
0	0	0	0.625
0	0	1	1.25
0	1	0	2.5
0	1	1	5
1	0	0	10
1	0	1	20
1	1	0	40
1	1	1	80

7.6 CTRL_REG2 (21h)

Table 22. CTRL_REG2 register

0[1]	FS1	FS0	0[1]	REBOOT	SOFT_RST	0[1]	0[1]

1. *This bit must be set to 0 for the correct operation of the device.*

Table 23. CTRL_REG2 description

FS[1:0]	Full-scale configuration (refer to Table 24). Default value: 00
REBOOT	Reboots memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
SOFT_RST	Configuration registers and user register reset function. (0: default value; 1: reset operation)

Table 24. Full-scale selection

FS1	FS0	Full-scale
0	0	±4 gauss
0	1	±8 gauss
1	0	±12 gauss
1	1	±16 gauss

7.7 CTRL_REG3 (22h)

Table 25. CTRL_REG3 register

0[1]	0[1]	LP	0[1]	0[1]	SIM	MD1	MD0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 26. CTRL_REG3 description

LP	Low-power mode configuration. Default value: 0 If this bit is 1, DO[2:0] is set to 0.625 Hz and the system performs, for each channel, the minimum number of averages. Once the bit is set to 0, the magnetic data rate is configured by the DO bits in the CTRL_REG1 (20h) register.
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)
MD[1:0]	Operating mode selection (refer to Table 27). Default value: 11

Table 27. System operating mode selection

MD1	MD0	Mode
0	0	Continuous-conversion mode
0	1	Single-conversion mode Single-conversion mode has to be used with sampling frequency from 0.625 Hz to 80 Hz.
1	0	Power-down mode
1	1	Power-down mode

7.8 CTRL_REG4 (23h)

Table 28. CTRL_REG4 register

0[1]	0[1]	0[1]	0[1]	OMZ1	OMZ0	BLE	0[1]

1. *This bit must be set to 0 for the correct operation of the device.*

Table 29. CTRL_REG4 description

OMZ[1:0]	Z-axis operative mode selection (refer to Table 30). Default value: 00
BLE	Big/little endian data selection. Default value: 0 (0: data LSb at lower address; 1: data MSb at lower address)

Table 30. Z-axis operating mode selection

OMZ1	OMZ0	Operating mode for Z-axis
0	0	Low-power mode
0	1	Medium-performance mode
1	0	High-performance mode
1	1	Ultrahigh-performance mode

7.9 CTRL_REG5 (24h)

Table 31. CTRL_REG5 register

FAST_READ	BDU	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

1. *This bit must be set to 0 for the correct operation of the device.*

Table 32. CTRL_REG5 description

FAST_READ	FAST READ allows reading the high part of DATA OUT only in order to increase reading efficiency. Default value: 0 (0: FAST_READ disabled; 1: FAST_READ enabled)
BDU	Block data update for magnetic data. Default value: 0 (0: continuous update; 1: output registers not updated until MSb and LSb have been read)

7.10 STATUS_REG (27h)

Table 33. STATUS_REG register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 34. STATUS_REG description

ZYXOR	X-, Y- and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous set)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X-, Y- and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XDA	X-axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

7.11 OUT_X_L (28h), OUT_X_H (29h)

X-axis data output. The value of the magnetic field is expressed as two's complement.

7.12 OUT_Y_L (2Ah), OUT_Y_H (2Bh)

Y-axis data output. The value of the magnetic field is expressed as two's complement.

7.13 OUT_Z_L (2Ch), OUT_Z_H (2Dh)

Z-axis data output. The value of the magnetic field is expressed as two's complement.

7.14 TEMP_OUT_L (2Eh), TEMP_OUT_H (2Fh)

Temperature sensor data. The value of the temperature is expressed as two's complement.

7.15 INT_CFG (30h)

Table 35. INT_CFG register

XIEN	YIEN	ZIEN	0[1]	1	IEA	LIR	IEN

1. *This bit must be set to 0 for the correct operation of the device.*

Table 36. INT_CFG description

XIEN	Enables interrupt generation on the X-axis. Default value: 1 (0: disable interrupt request; 1: enable interrupt request)
YIEN	Enables interrupt generation on the Y-axis. Default value: 1 (0: disable interrupt request; 1: enable interrupt request)
ZIEN	Enables interrupt generation on the Z-axis. Default value: 1 (0: disable interrupt request; 1: enable interrupt request)
IEA	Interrupt active configuration on INT. Default value: 0 (0: low; 1: high)
LIR	Latch interrupt request. Default value: 0 (0: interrupt request latched; 1: interrupt request not latched) Once latched, the INT pin remains in the same state until INT_SRC (31h) is read.
IEN	Enables the interrupt on the INT pin. Default value: 0 (0: disabled; 1: enabled)

7.16 INT_SRC (31h)

Table 37. INT_SRC register

PTH_X	PTH_Y	PTH_Z	NTH_X	NTH_Y	NTH_Z	MROI	INT

Table 38. INT_SRC description

PTH_X	Value on the X-axis exceeds the threshold on the positive side. Default value: 0
PTH_Y	Value on the Y-axis exceeds the threshold on the positive side. Default value: 0
PTH_Z	Value on the Z-axis exceeds the threshold on the positive side. Default value: 0
NTH_X	Value on the X-axis exceeds the threshold on the negative side. Default value: 0
NTH_Y	Value on the Y-axis exceeds the threshold on the negative side. Default value: 0
NTH_Z	Value on the Z-axis exceeds the threshold on the negative side. Default value: 0
MROI	Internal measurement range overflow on the magnetic value. Default value: 0
INT	This bit signals when an interrupt event occurs.

7.17 INT_THS_L(32h), INT_THS_H(33h)

Interrupt threshold. Default value: 0.

The value is expressed in 16-bit unsigned.

Even if the threshold is expressed in absolute value, the device detects both positive and negative thresholds.

Table 39. INT_THS_L_M

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 40. INT_THS_H_M

0[1]	THS14	THS13	THS12	THS11	THS10	THS9	THS8

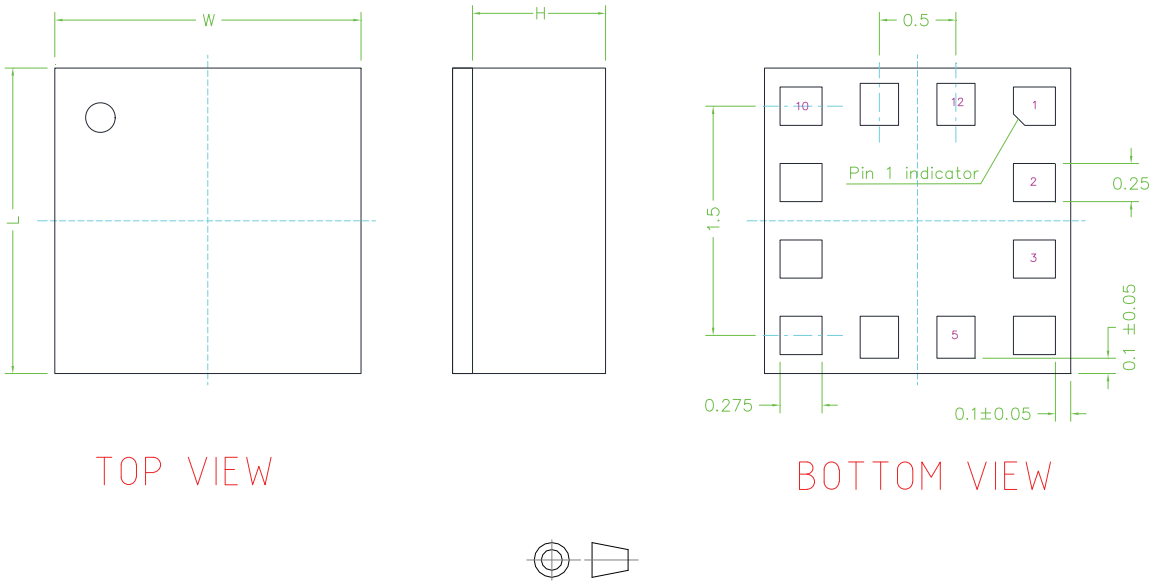
1. *This bit must be set to 0 for the correct operation of the device.*

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 LGA-12L package information

Figure 12. LGA-12 2.0 x 2.0 x 1.0 mm package outline and mechanical data



Dimensions are in millimeter unless otherwise specified
General Tolerance is +/-0.1mm unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2.00	±0.15
Width [W]	2.00	±0.15
Height [H]	1.027	MAX

8365767_5

Revision history

Table 41. Document revision history

Date	Version	Changes
01-Feb-2013	1	Initial release
22-Apr-2013	2	Updated note on page 12 Product status changed from preliminary data to production data
12-Dec-2014	3	Added FAST_ODR bit to Table 18: CTRL_REG1 register and Table 19: CTRL_REG1 description Added FAST_READ bit to Table 32: CTRL_REG5 register and Table 33: CTRL_REG5 description Updated Table 16: Register address map Minor textual updates throughout document
15-May-2015	4	Added Table 20: Data rate configuration
28-Oct-2015	5	Updated registers 32h and 33h in Table 16: Register address map
02-May-2017	6	Updated Table 1: Device summary Updated default values of INT_CFG (30h)
05-Dec-2023	7	Updated Notes below Figure 3. SPI slave timing diagram and Figure 4. I²C slave timing diagram Added hard-iron offset registers OFFSET_X_REG_L_M (05h) and OFFSET_X_REG_H_M (06h) through OFFSET_Z_REG_L_M (09h) and OFFSET_Z_REG_H_M (0Ah) Updated Section 8.1 LGA-12L package information

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