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74HC174; 74HCT174

Hex D-type flip-flop with reset; positive-edge trigger

Rev. 7 — 14 March 2024

Product data sheet

1. General description

The 74HC174; 74HCT174 are hex positive edge-triggered D-type flip-flops with individual data inputs (Dn) and outputs (Qn). The common clock (CP) and master reset (\overline{MR}) inputs load and reset all flip-flops simultaneously. The D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition is stored in the flip-flop and appears at the Q output. A LOW on \overline{MR} causes the flip-flops and outputs to be reset LOW. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Input levels:
 - For 74HC174: CMOS level
 - For 74HCT174: TTL level
- Six edge-triggered D-type flip-flops
- Asynchronous master reset
- Complies with JEDEC standards
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC174D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT174D				
74HC174PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT174PW				

4. Functional diagram

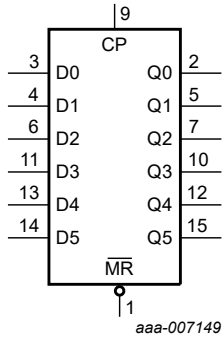


Fig. 1. Logic symbol

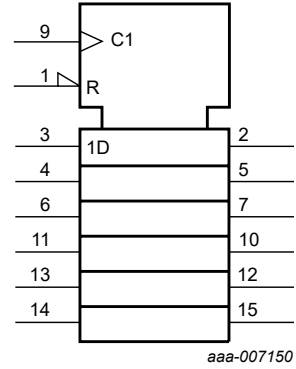


Fig. 2. IEC logic symbol

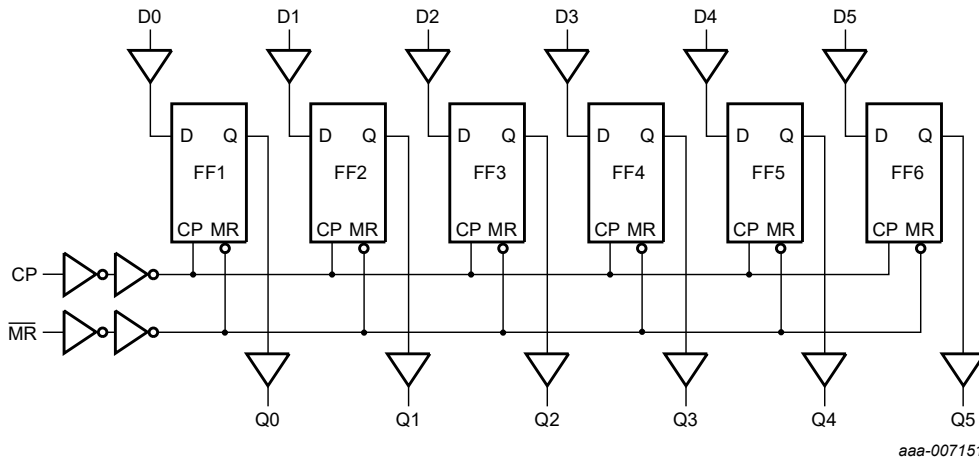


Fig. 3. Logic diagram

5. Pinning information

5.1. Pinning

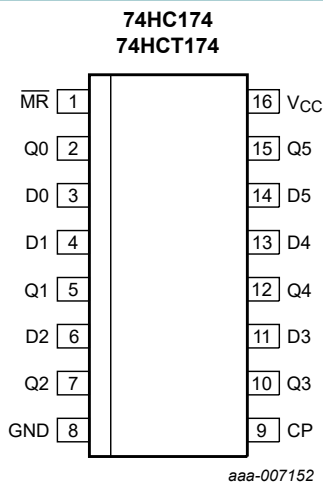


Fig. 4. Pin configuration SOT109-1 (SO16)

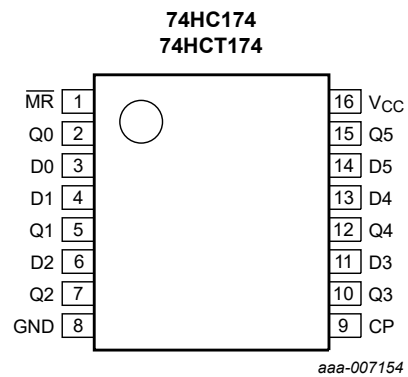


Fig. 5. Pin configuration and SOT403-1 (TSSOP16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
MR	1	asynchronous master reset input (active LOW)
Q0, Q1, Q2, Q3, Q4, Q5	2, 5, 7, 10, 12, 15	flip-flop output
D0, D1, D2, D3, D4, D5	3, 4, 6, 11, 13, 14	data input
GND	8	ground (0 V)
CP	9	clock input (LOW-to-HIGH edge-triggered)
V _{CC}	16	positive supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

X = don't care; ↑ = LOW-to-HIGH clock transition.

Operating modes	Inputs			Outputs
	MR	CP	Dn	Qn
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V [1]	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V [1]	-	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.

For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC174			74HCT174			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC174										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
		V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C _I	input capacitance		-	3.5	-	-	-	-	pF	

Hex D-type flip-flop with reset; positive-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT174										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 5.2 mA; V _{CC} = 5.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		Dn input	-	25	90	-	112.5	-	122.5	µA
		CP input	-	130	468	-	585	-	637	µA
		MR input	-	125	450	-	562.5	-	612.5	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see Fig. 8

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC174										
t_{pd}	propagation delay	CP to Qn; see Fig. 6 [1]								
		$V_{CC} = 2.0$ V	-	55	165	-	205	-	250	ns
		$V_{CC} = 4.5$ V	-	20	33	-	41	-	50	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	16	28	-	35	-	43	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 7								
		$V_{CC} = 2.0$ V	-	44	150	-	190	-	225	ns
		$V_{CC} = 4.5$ V	-	16	30	-	38	-	45	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	13	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	13	26	-	33	-	38	ns
t_t	transition time	Qn output; see Fig. 6 [2]								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns
t_w	pulse width	CP input HIGH or LOW; see Fig. 6								
		$V_{CC} = 2.0$ V	80	17	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	6	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	5	-	17	-	20	-	ns
		MR input LOW; see Fig. 7								
		$V_{CC} = 2.0$ V	80	12	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	4	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	3	-	17	-	20	-	ns
t_{rec}	recovery time	MR to CP; see Fig. 7								
		$V_{CC} = 2.0$ V	5	-11	-	5	-	5	-	ns
		$V_{CC} = 4.5$ V	5	-4	-	5	-	5	-	ns
		$V_{CC} = 6.0$ V	5	-3	-	5	-	5	-	ns
t_{su}	set-up time	Dn to CP; see Fig. 6								
		$V_{CC} = 2.0$ V	60	6	-	75	-	90	-	ns
		$V_{CC} = 4.5$ V	12	2	-	15	-	18	-	ns
		$V_{CC} = 6.0$ V	10	2	-	13	-	15	-	ns
t_h	hold time	Dn to CP; see Fig. 6								
		$V_{CC} = 2.0$ V	3	-6	-	3	-	3	-	ns
		$V_{CC} = 4.5$ V	3	-2	-	3	-	3	-	ns
		$V_{CC} = 6.0$ V	3	-2	-	3	-	3	-	ns

Hex D-type flip-flop with reset; positive-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
f _{max}	maximum frequency	CP input; see Fig. 6								
		V _{CC} = 2.0 V	6	30	-	5	-	4	-	MHz
		V _{CC} = 4.5 V	30	90	-	24	-	20	-	MHz
		V _{CC} = 6.0 V	35	107	-	28	-	24	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	99	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} [3]	-	17	-	-	-	-	-	pF
74HCT174										
t _{pd}	propagation delay	CP to Qn; see Fig. 6 [1]								
		V _{CC} = 4.5 V	-	21	35	-	44	-	53	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	18	-	-	-	-	-	ns
t _{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 7								
		V _{CC} = 4.5 V	-	20	35	-	44	-	53	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	17	-	-	-	-	-	ns
t _t	transition time	Qn output; see Fig. 6 [2]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t _W	pulse width	CP input; see Fig. 6								
		V _{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		MR input LOW; see Fig. 7								
t _{rec}	recovery time	V _{CC} = 4.5 V	20	7	-	25	-	30	-	ns
		MR to CP; see Fig. 7								
t _{su}	set-up time	V _{CC} = 4.5 V	12	-3	-	15	-	18	-	ns
		Dn to CP; see Fig. 6								
t _h	hold time	V _{CC} = 4.5 V	16	4	-	20	-	24	-	ns
		Dn to CP; see Fig. 6								
f _{max}	maximum frequency	V _{CC} = 4.5 V	5	-3	-	5	-	5	-	ns
		CP input; see Fig. 6								
		V _{CC} = 4.5 V	30	63	-	24	-	20	-	MHz
C _{PD}	power dissipation capacitance	V _{CC} = 5.0 V; C _L = 15 pF	-	69	-	-	-	-	-	MHz
		per package; V _I = GND to V _{CC} - 1.5 V [3]	-	17	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

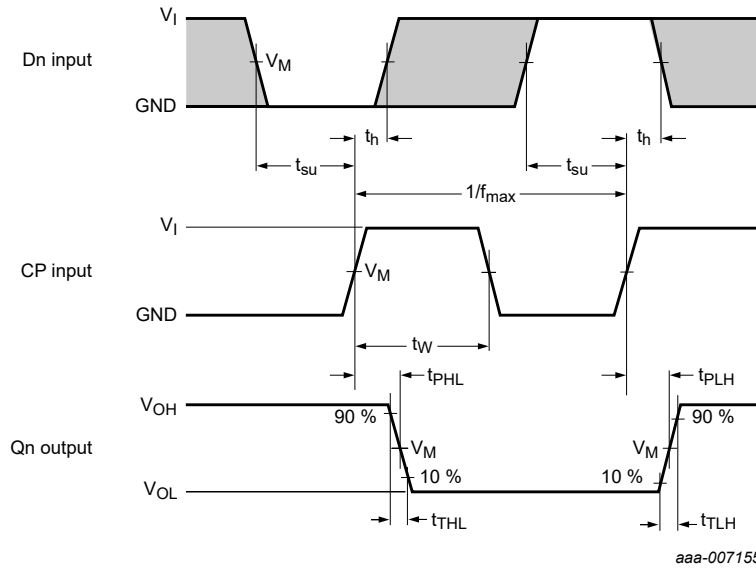
f_o = output frequency in MHz;

∑ (C_L × V_{CC}² × f_o) = sum of outputs;

C_L = output load capacitance in pF;

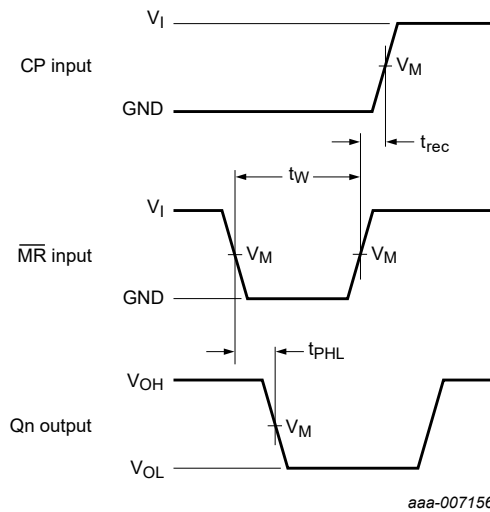
V_{CC} = supply voltage in V.

10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).
 The shaded areas indicate when the input is permitted to change for predictable output performance.
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Input to output propagation delay, output transition time, clock input pulse width, set-up and hold times for data input and maximum frequency



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Master reset to output propagation delays, master reset pulse width and master reset to clock recovery time

Table 8. Measurement points

Type	Input		Output
	V_I	V_M	V_M
74HC174	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
74HCT174	3 V	1.3 V	1.3 V

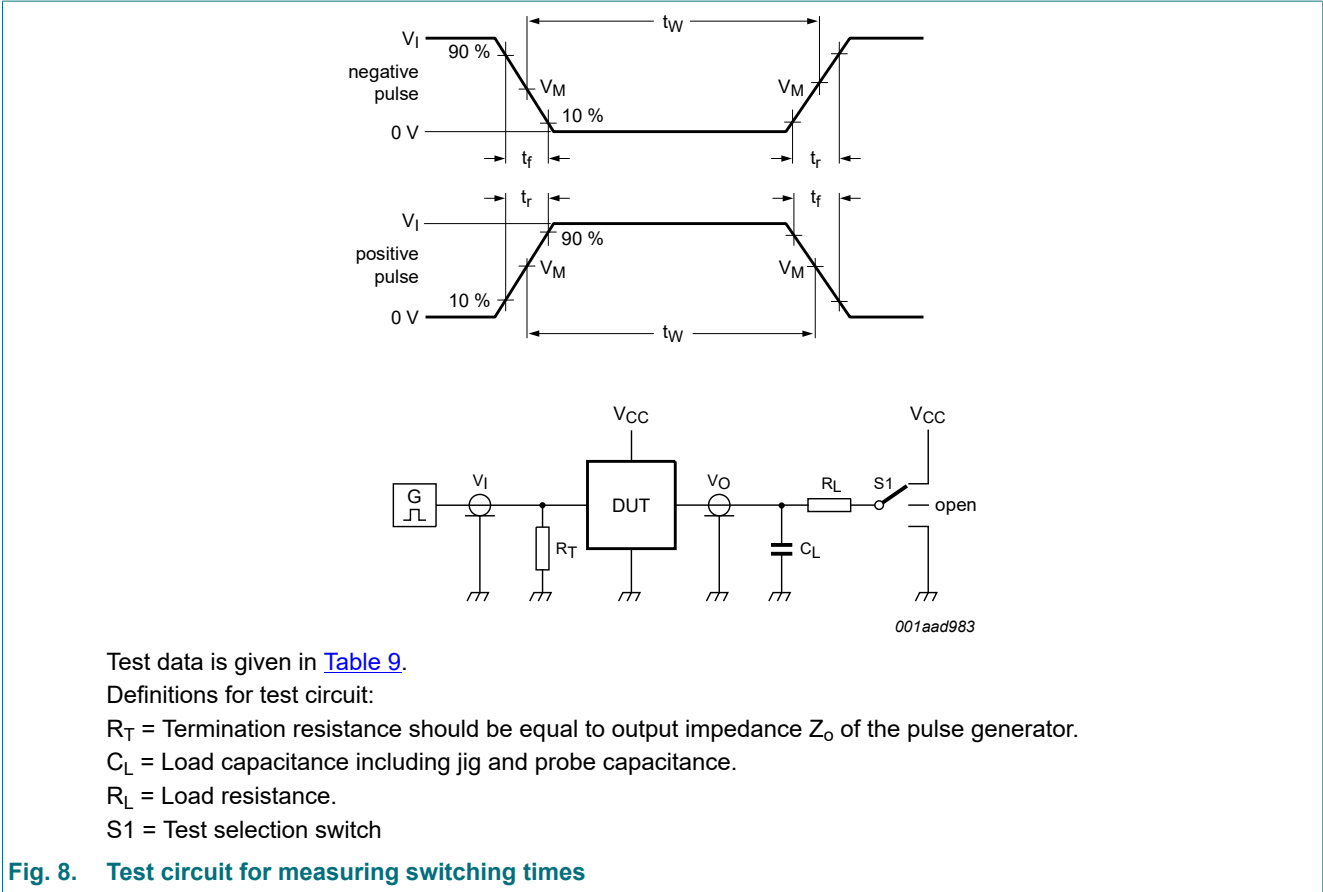


Table 9. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC174	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open
74HCT174	3 V	6 ns	15 pF, 50 pF	1 k Ω	open

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

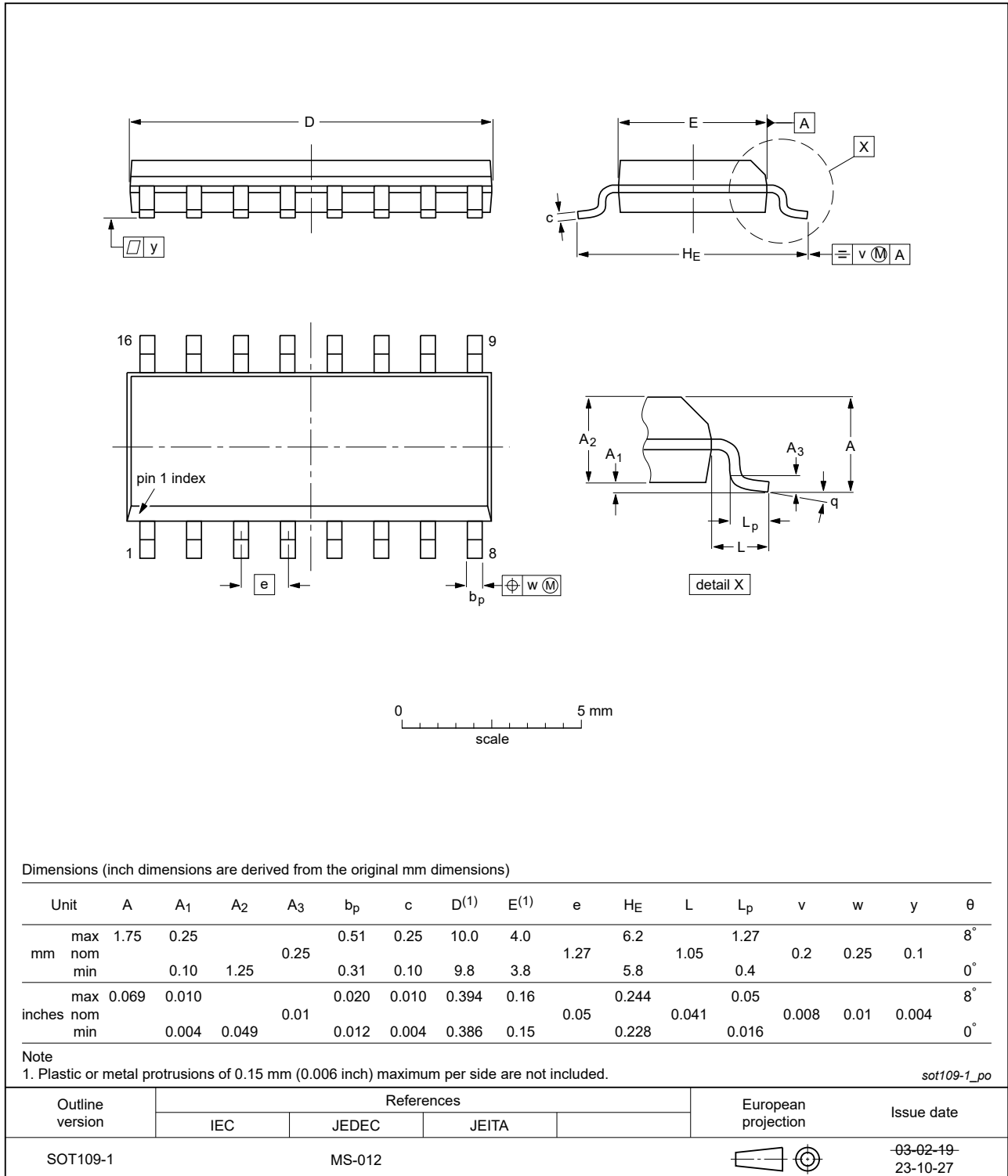


Fig. 9. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

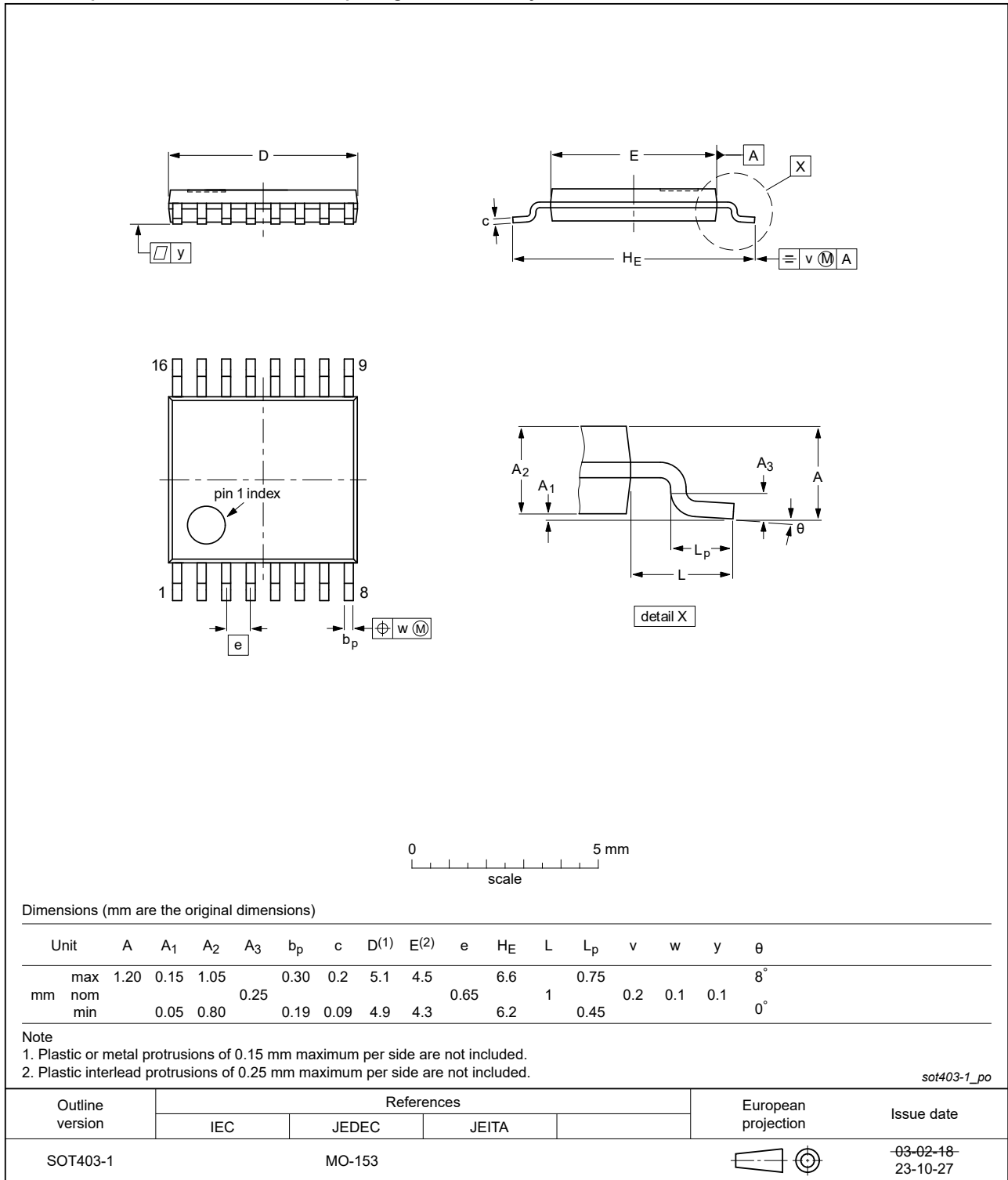


Fig. 10. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT174 v.7	20240314	Product data sheet	-	74HC_HCT174 v.6
Modifications:	<ul style="list-style-type: none"> Fig. 9, Fig. 10: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. Section 2: ESD specification updated according to the latest JEDEC standard. 			
74HC_HCT174 v.6	20210901	Product data sheet	-	74HC_HCT174 v.5
Modifications:	<ul style="list-style-type: none"> Type number 74HCT174DB (SOT338-1/SSOP16) removed. 			
74HC_HCT174 v.5	20210226	Product data sheet	-	74HC_HCT174 v.4
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74HC174DB (SOT338-1/SSOP16) removed. Section 2 updated. Section 7: Derating values for P_{tot} total power dissipation updated. 			
74HC_HCT174 v.4	20160512	Product data sheet	-	74HC_HCT174 v.3
Modifications:	<ul style="list-style-type: none"> Type numbers 74HC174N and 74HCT174N (SOT38-4) removed. 			
74HC_HCT174 v.3	20130416	Product data sheet	-	74HC_HCT174_CNV_2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 			
74HC_HCT174_CNV_2	19980708	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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For more information, please visit: <http://www.nexperia.com>
For sales office addresses, please send an email to: salesaddresses@nexperia.com
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