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Please visit our website for pricing and availability at www.hestore.hu.

Low Voltage I²C/SMBus Accelerator

FEATURES

- **Improves I²C Bus Rise Time Transition**
- **Ensures Data Integrity with Multiple Devices on the I²C Bus.**
- **Wide Supply Voltage Range: 1.6V to 5.5V**
- Improves Low State Noise Margin
- Up to 400kHz Operation
- Auto Detect Low Power Standby Mode
- Low (<5µA) Supply Current Shutdown
- Does Not Load Bus When Disabled or Powered Down
- Strong Slew Limited Pull-up Current
- ±8kV Human Body Model ESD Ruggedness
- 2mm × 2mm DFN and SC70 Packages

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Battery Chargers
- Industrial Controls
- TV/Video Products
- ACPI SMBus Interface

DESCRIPTION

The LTC®4311 is a dual I²C active pull-up designed to enhance data transmission speed and reliability for bus loading conditions well beyond the 400pF I²C specification limit. The LTC4311 operates at supply voltages from 1.6V to 5.5V and is also compatible with SMBus.

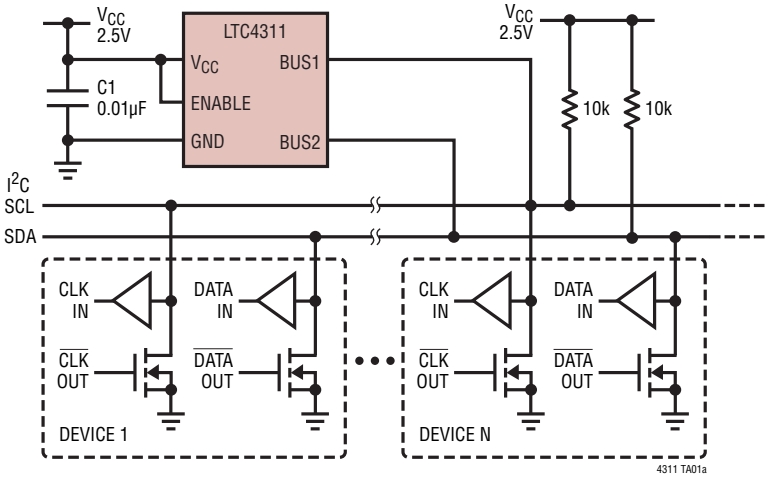
The LTC4311 allows multiple device connections or a longer, more capacitive interconnect, without compromising slew rates or bus performance, by using two slew limited pull-up currents.

During positive bus transitions, the LTC4311 provides slew limited pull-up currents to quickly slew the I²C or SMBus lines to the bus pull-up voltage. During negative transitions or steady DC levels, the currents are disabled to improve negative slew rate, and improve low state noise margins. An auto detect standby mode reduces supply current if both SCL and SDA are high. When disabled, the LTC4311 goes into low (<5µA) current shutdown.

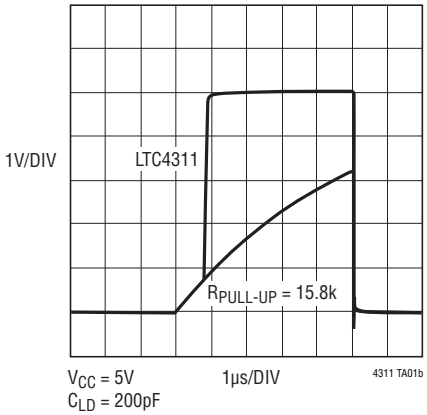
The LTC4311 is available in the 2mm × 2mm × 0.75mm DFN, and SC70 packages.

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TYPICAL APPLICATION



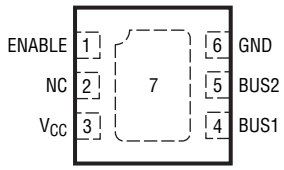
Comparison of I²C Waveforms for the LTC4311 vs Resistor Pull-Up



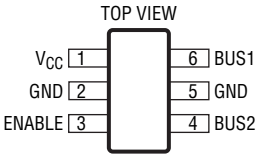
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

V_{CC} to GND ..... –0.3 to 6V
BUS1, BUS2, ENABLE Inputs ..... –0.3 to 6V
Operating Temperature
LTC4311C ..... 0°C to 70°C
LTC4311I ..... –40°C to 85°C
Storage Temperature Range (DFN) ..... –65°C to 125°C
Storage Temperature Range (SC70) ..... –65°C to 125°C
Lead Temperature (Soldering 10, sec)
SC70 ..... 300°C

PIN CONFIGURATION



DFN PACKAGE
6-LEAD (2mm × 2mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 102°C/W
EXPOSED PAD (PIN 7) PCB CONNECTION TO GND IS OPTIONAL (Note 3)



SC70 PACKAGE
6-LEAD PLASTIC SC70
T_{JMAX} = 125°C, θ_{JA} = 150° C/W

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4311CDC#TRMPBF	LTC4311CDC#TRPBF	LCNG	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LTC4311IDC#TRMPBF	LTC4311IDC#TRPBF	LCNG	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LTC4311CSC6#TRMPBF	LTC4311CSC6#TRPBF	LCNF	6-Lead (2mm × 2mm) Plastic SC70	0°C to 70°C
LTC4311ISC6#TRMPBF	LTC4311ISC6#TRPBF	LCNF	6-Lead (2mm × 2mm) Plastic SC70	–40°C to 85°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage		●	1.6		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.5V, ENABLE = 5.5V, V_{BUS1} = V_{BUS2} = 0V	●		200	300	µA
$I_{CC_STANDBY}$	Supply Current, Standby Mode	V_{CC} = 5.5V, ENABLE = 5.5V, V_{BUS1} = V_{BUS2} = 5.5V	●		26	45	µA
$I_{CC_DISABLED}$	Supply Current, Disabled	V_{CC} = 5.5V, ENABLE = 0V, V_{BUS1} = V_{BUS2} = 5.5V	●			±5	µA
$I_{PULLUPAC}$	Transient Boosted Pull-up Current	Positive Transition on Bus, Slew Rate = 0.5V/µs V_{CC} = 1.8V, BUS > V_{THR}	●	2.5	5		mA
$I_{BUS(IN)}$	BUS1,BUS2, Input Leakage Current	V_{CC} = 0V, V_{BUS1} = V_{BUS2} = 5.5V	●			±5	µA
$I_{ENABLE(IN)}$	ENABLE Input Leakage Current	V_{CC} = 0V, V_{ENABLE} = 5.5V	●			±10	µA
V_{THR}	Bus Input Threshold Voltage	V_{CC} = 1.8V	●	0.45	0.55	0.65	V
		V_{CC} = 2.5V	●	0.65	0.75	0.85	V
		V_{CC} = 2.7V to 5.5V	●	0.68	0.78	0.88	V
V_{THR_ENABLE}	ENABLE Threshold Voltage	V_{CC} = 1.6V, 5.5V	●	0.4	1	1.5	V
SR_{THRESH}	Slew Rate Detector Threshold	BUS > V_{THR}, V_{CC} = 1.8V, 5.5V	●		0.2	0.5	V/µs
t_r	Fast Mode I^2C Bus Rise Time	Bus Capacitance = 400pF, V_{CC} = 3V (Note 4)	●			300	ns
f_{MAX}	Bus Maximum Operating Frequency	(Note 5)	●	400			kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive. All voltages are referenced to GND unless otherwise specified.

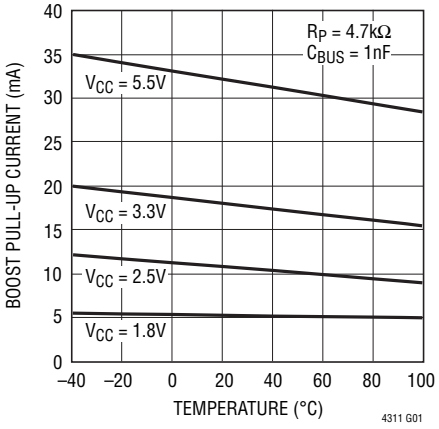
Note 3: Thermal characteristics are determined with exposed pad soldered to GND plane. If the exposed pad is left open, thermal characteristics can be drastically different.

Note 4: The rise time of an I^2C bus line is calculated from $V_{IL(MAX)}$ to $V_{IH(MIN)}$ or 0.9V to 2.1V (with V_{CC} = 3V). This parameter is guaranteed by design and not tested. With a minimum boosted pull-up current of 2.5mA: Rise Time = (2.1V – 0.9V) • 400pF/2.5mA = 0.19µs.

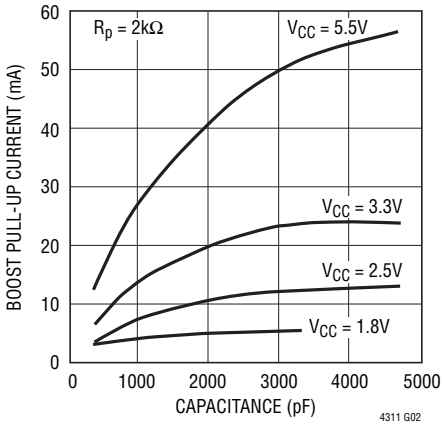
Note 5: Determined by design, not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, unless otherwise indicated)

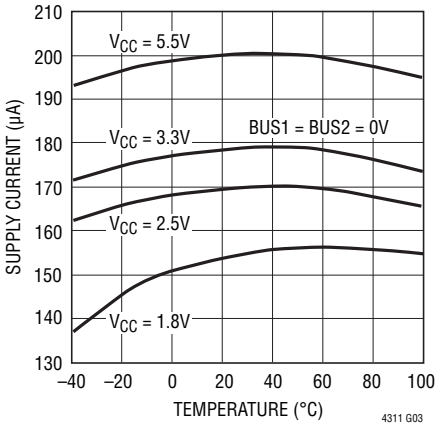
Boost Pull-Up Current vs Temperature



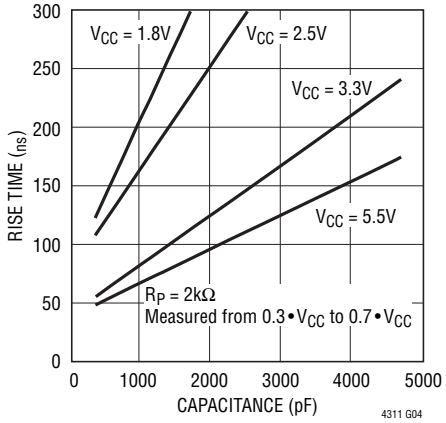
Boost Pull-Up Current vs Bus Capacitance



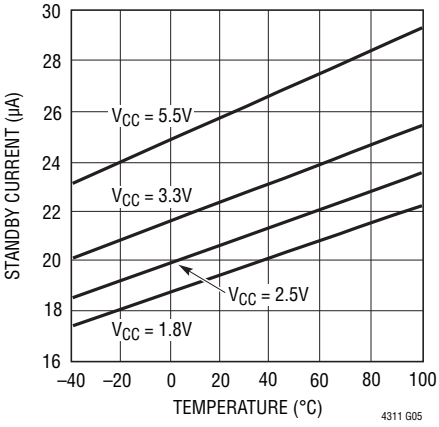
Supply Current vs Temperature



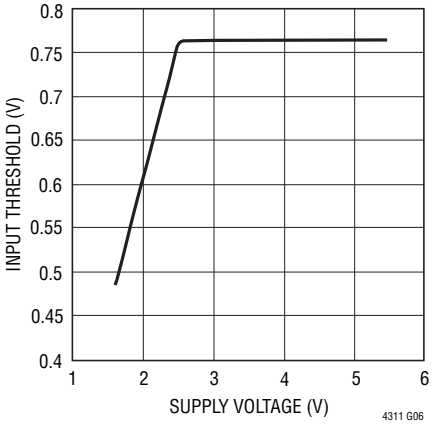
Rise Time vs Capacitance



Standby Current vs Temperature



Bus Input Threshold Voltage vs Supply Voltage



PIN FUNCTIONS

BUS1: Active Pull-up for Bus. Connect to either clock line or data line for 2-wire bus.

BUS2: Active Pull-up for Bus. Connect to either clock line or data line for 2-wire bus.

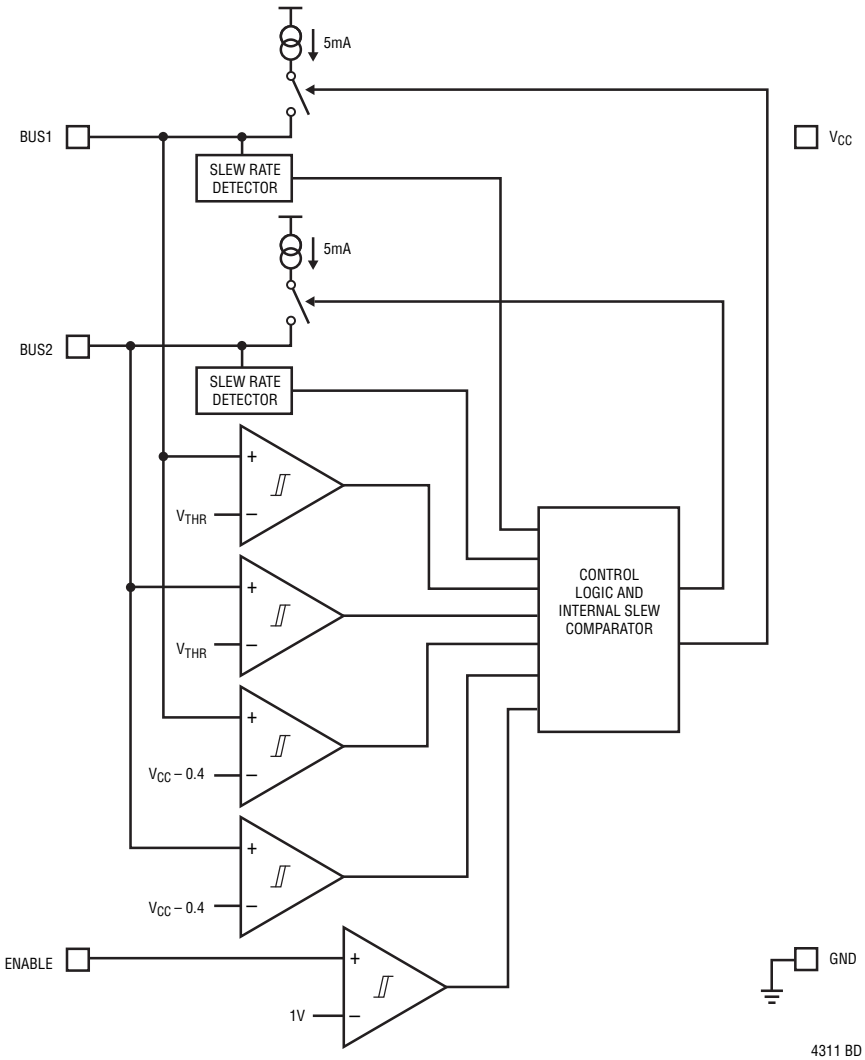
ENABLE: Device Enable Input. This is a 1V nominal digital threshold input pin. For normal operation drive ENABLE to a voltage greater than 1.5V. Driving ENABLE below the 0.4V threshold puts the device in a low (<5µA) current shutdown mode and puts the BUS pins in a high impedance state. If unused, connect to V_{CC}.

EXPOSED PAD (DFN Package Only): Exposed Pad may be left open or connected to device ground.

GND: Device Ground. Connect this pin to a ground plane for best results.

V_{CC}: Supply Voltage Input. Connect this pin to bus supply and place a bypass capacitor of at least 0.01µF close to V_{CC} for best results.

BLOCK DIAGRAM



OPERATION

I²C and SMBus Overview

The I²C communication protocol employs open-drain pull-down drivers with resistive or current source pull-ups. This protocol allows multiple devices to drive and monitor the bus without bus contention. The simplicity of resistive or fixed current source pull-ups is offset by the slow rise times resulting when bus capacitance is high. Rise times can be improved by using lower pull-up resistor values or higher fixed current source values, but the additional current increases the low state bus voltage, decreasing noise margins. Slow rise times can seriously impact data reliability, enforcing a maximum practical bus speed well below the established I²C or SMBus maximum transmission rate.

The LTC4311 overcomes these limitations by providing a boosted pull-up current only during positive bus transitions to quickly slew large bus capacitances. Therefore, rise time is dramatically improved, especially with maximum or out of specification I²C or SMBus loading conditions.

The LTC4311 has separate but identical circuitry for each BUS output pin. The circuitry consists of a positive edge slew rate detector and a voltage comparator. The voltage comparator has a supply dependent threshold. At supply voltages below 2.7V the comparator threshold is $0.3V_{CC}$, and at higher voltages the comparator threshold is a constant 0.8V. This allows the rise time accelerator to be used in non-compliant systems where the bus thresholds are optimized for low voltage operation, while still meeting standard thresholds for compliant I²C and SMBus systems.

The slew limited pull-up current is only turned on if the bus line voltage is greater than the supply dependent comparator threshold voltage and the positive slew rate of the bus line is greater than the typical 0.2V/µs threshold of the slew rate detector. The pull-up current remains on until the voltage on the bus line is within 0.4V of V_{CC} or the slew rate drops below 0.2V/µs.

The pull-up current is slew limited to maintain signal integrity for busses that have very little capacitive load. In a lightly loaded system a strong pull-up could result in fast edge rates that cause reflections on the bus. These reflections can be detected by devices on the bus as extra clock edges, could result in erroneous data, or cause a stuck bus. An internal slew limit comparator limits the rate the pull-up current can slew the bus lines to 100V/µs.

Auto Detect Standby Mode and Shutdown Mode

When BUS1 and BUS2 are both high the LTC4311 reduces the standby supply current. Internal comparators detect when the bus pins are within 400mV of V_{CC}, and reduce the supply current to 26µA. When the ENABLE pin is grounded, the LTC4311 enters a low (<5µA) supply current shutdown mode. Both bus pins are high impedance in shutdown, regardless of the bus pin voltage.

APPLICATIONS INFORMATION

Selecting the values of R_S and R_P

The typical configuration for the data bus for a 2-wire bus is shown in Figure 1. The parameters R_P and R_S should be chosen carefully. A description of the process for choosing the values of R_P and R_S follows.

An external pull-up resistor R_P is required in each bus line to supply a steady state pull-up current if the bus is at logic zero. This pull-up current is used for slewing the bus line during the initial portion of the positive transition in order to activate the LTC4311 pull-up current.

Using an external pull-up resistor R_P to supply steady state pull-up current provides the freedom to adjust rise time versus fall time as well as defining the low state logic-level (V_{OL}).

For I/O stage protection from ESD and high voltage spikes on the bus, a series resistor R_S (Figure 1) is sometimes added to the open drain driver of the bus agents.

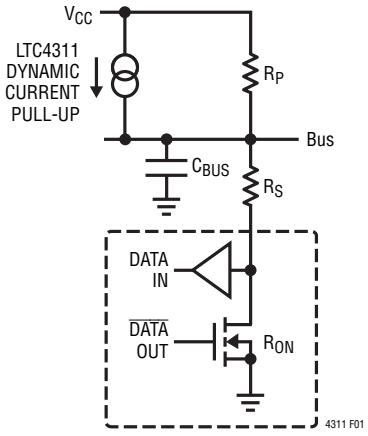


Figure 1. Typical 2-Wire Bus Configuration

Both the values of R_P and R_S must be chosen carefully to meet the low state noise margin and all bus timing requirements.

A discussion of the electrical parameters affected by the values of R_S and R_P, as well as the general procedure for selecting the values of R_S and R_P follows.

Low State Noise Margin

A low value of V_{OL}, the low state logic level, is desired for good noise margin. V_{OL} is calculated as follows:

$$V_{OL} = \frac{R_L \bullet V_{CC}}{R_L + R_P} \quad (1)$$

R_L is the series sum of R_S and R_{ON}, the on resistance of the open-drain driver.

Increasing the value of R_P decreases the value of V_{OL}. Increasing R_L increases the value of V_{OL}.

Initial Slew Rate

The initial slew rate, SR, of the bus is determined by:

$$SR = \frac{V_{CC} - V_{OL}}{R_P \bullet C_{BUS}} \quad (2)$$

SR must be greater than SR_{THRESH}, the LTC4311 slew rate detector threshold (0.5V/µs max), in order to activate the pull-up current.

I^2C Rise and Fall Time

Rise time of an I^2C line is derived using equation 3.

$$t_r = -R_p \bullet C_{BUS} \bullet \ln\left\{\frac{V_{IHMIN} - V_{CC} - R_p \bullet I_{PULLUPAC}}{V_{ILMAX} - V_{CC} - R_p \bullet I_{PULLUPAC}}\right\} \quad (3)$$

Fall time of an I^2C line is derived using equation 4.

$$t_f = R_T \bullet C_{BUS} \bullet \ln\left\{\frac{\frac{V_{IHMIN}}{V_{CC}} \bullet (R_P + R_L) - R_L}{\frac{V_{ILMAX}}{V_{CC}} \bullet (R_P + R_L) - R_L}\right\} \quad (4)$$

where R_T is the parallel equivalent of R_P and R_L.

APPLICATIONS INFORMATION

For an I²C system with fixed input levels, V_{ILMAX} = 1.5V and V_{IHMIN} = 3V. For I²C systems with V_{CC} related input levels, $V_{ILMAX} = 0.3V_{CC}$ and $V_{IHMIN} = 0.7V_{CC}$.

C_{BUS} is the total capacitance of the I²C line.

SMBus Rise and Fall Time

Rise time of a SMBus line is derived using equations 5, 6 and 7.

$$t_r = t_1 + t_2 \quad (5)$$

t_1 is the time from when the bus crosses the lower slew rate measurement point, until the bus reaches V_{THR} and the accelerators fire. The time from when the accelerators fire until the bus reaches the upper slew rate measure point is given by t_2. Equations for t_1 and t_2 are given here:

$$t_1 = -R_P \bullet C_{BUS} \bullet \ln\left\{\frac{V_{THR} - V_{CC}}{V_{ILMAX} - 0.15V - V_{CC}}\right\} \quad (6)$$

If $(V_{ILMAX} - 0.15V) > V_{THR}$, then $t_1 = 0$

$$t_2 = -R_P \bullet C_{BUS} \bullet \ln\left\{\frac{V_{IHMIN} + 0.15V - V_{CC} - R_P \bullet I_{PULLUPAC}}{V_{THR} - V_{CC} - R_P \bullet I_{PULLUPAC}}\right\} \quad (7)$$

Fall time of an SMBus line is derived using equation 8:

$$t_f = R_T \bullet C_{BUS} \bullet \ln\left\{\frac{\frac{V_{IHMIN} + 0.15V}{V_{CC}} \bullet (R_P + R_L) - R_L}{\frac{V_{ILMAX} - 0.15V}{V_{CC}} \bullet (R_P + R_L) - R_L}\right\} \quad (8)$$

For an SMBus system, V_{ILMAX} = 0.8V and V_{IHMIN} = 2.1V.

C_{BUS} is the total bus capacitance of the SMBus line.

A general procedure for selecting R_P and R_L is as follows:

1. R_L is first selected based on the I/O protection requirement. Generally, an R_S of 100Ω is sufficient for high voltage spikes and ESD protection. R_{ON} is determined by the size of the open-drain driver, a large driver will have a lower R_{ON}.
2. The value of R_P is determined based on the V_{OL} and minimum slew rate requirements. The V_{OL} will determine the smallest resistance value that can be used in a system, and the minimum slew requirement will bound the resistance on the upper end. Generally the largest value of resistance that meets the minimum slew rate with some margin will be selected.
3. For I²C systems incorporating the LTC4311, the rise times are met under most loading conditions, due to the strong accelerator current. The pull-down drivers are typically low impedance, and therefore fall times are not generally an issue. Rise and fall time requirements must be verified using equations 3 and 4 (for an I²C system) or equations 5 to 8 (for an SMBus system). The value chosen for R_P must ensure that both the rise and fall time specifications are met simultaneously.

I²C Design Example

Given the following conditions and requirements:

$$V_{CC} = 3.3V \text{ NOMINAL}$$
$$V_{OL} = 0.4V \text{ MAXIMUM}$$
$$C_{BUS} = 600pF$$
$$V_{ILMAX} = 0.99V, V_{IHMIN} = 2.31V$$
$$t_r = 0.3\mu s \text{ MAXIMUM}, t_f = 0.3\mu s \text{ MAXIMUM} \quad (9)$$

If an R_S of 100Ω is used and the max R_{ON} of the driver is 200Ω, then R_L = 200Ω + 100Ω = 300Ω. Use equation 1 to find the required R_P to meet V_{OL}.

$$R_P = \frac{300\Omega \bullet (3.3V - 0.4V)}{0.4V}$$
$$R_P = 2.175k \quad (10)$$

APPLICATIONS INFORMATION

This is the lowest resistor value that may be chosen and still meet V_{OL}. Next calculate the largest value of R_P that will satisfy SR, the minimum slew rate requirement. Using V_{OL} = 0.4V and SR = 0.5V/µs calculate the value of R_P with equation 2.

$$R_P = \frac{3.3V - 0.4V}{600pF \bullet 0.5V/\mu s}$$
$$R_P = 9.667k \quad (11)$$

This is approximately the largest value of R_P that will satisfy the minimum slew rate requirement. Since R_P is larger than 2.175k the V_{OL} will be below 0.4V, and the slew rate will actually be faster than calculated. Choosing R_P = 10k, V_{OL} and SR are recalculated.

$$V_{OL} = \frac{300\Omega \bullet 3.3V}{300\Omega + 10k\Omega} = 96mV$$
$$SR = \frac{3.3V - 96mV}{10k\Omega \bullet 600pF} = 0.534V/\mu s \quad (12)$$

The rise and fall times need to be verified using equations 3 and 4.

$$t_r = -10k\Omega \bullet 600pF \bullet \ln\left\{\frac{2.31V - 3.3V - 10k\Omega \bullet 2.5mA}{0.99V - 3.3V - 10k\Omega \bullet 2.5mA}\right\} = 0.297\mu s \quad (13)$$

$$t_f = 291\Omega \bullet 600pF \bullet \ln\left\{\frac{\frac{2.31}{3.3V} \bullet (10k\Omega + 300\Omega) - 300\Omega}{\frac{0.99V}{3.3V} \bullet (10k\Omega + 300\Omega) - 300\Omega}\right\} = 0.158\mu s \quad (14)$$

Both the rise and fall times meet the 0.3µs I^2C requirement and the V_{OL} is satisfied, while meeting the minimum slew rate requirement, so R_P is chosen to be 10k.

If t_r is not met, R_P should be decreased and if t_f is not met then R_P should be increased.

SMBus Design Example

Given the following conditions and requirements for a low power SMBus system:

$$V_{CC} = 3.3V \text{ NOMINAL}$$
$$V_{OL} = 0.4V \text{ MAXIMUM}$$
$$C_{BUS} = 400pF$$
$$V_{ILMAX} = 0.8V, V_{IHMIN} = 2.1V$$
$$t_r = 1\mu s \text{ MAXIMUM}, t_f = 0.3\mu s \text{ MAXIMUM} \quad (15)$$

If an R_S of 100Ω is used and the max R_{ON} of the driver is 200Ω, then R_L = 200Ω + 100Ω = 300Ω. Use equation 1 to find the required R_P to meet V_{OL}.

$$R_P = \frac{300\Omega \bullet (3.3V - 0.4V)}{0.4V}$$
$$R_P = 2.175k \quad (16)$$

Calculate Maximum R_P from equation 2.

$$R_P = \frac{3.3V - 0.4V}{400pF \bullet 0.5V/\mu s}$$
$$R_P = 14.5k \quad (17)$$

Choose R_P = 13k and recalculate V_{OL} and SR.

$$V_{OL} = \frac{300\Omega \bullet 3.3V}{300\Omega + 13k\Omega} = 74mV$$
$$SR = \frac{3.3V - 74mV}{13k\Omega \bullet 400pF} = 0.62V/\mu s \quad (18)$$

The rise and fall times need to be verified using equations 5 to 8.

$$t_1 = -13k\Omega \bullet 400pF \bullet \ln\left\{\frac{0.9V - 3.3V}{0.8V - 0.15V - 3.3V}\right\} = 0.515\mu s \quad (19)$$

APPLICATIONS INFORMATION

$$t_2 = -13k\Omega \bullet 400pF \bullet \ln\left\{\frac{2.1V + 0.15V - 3.3V - 13k\Omega \bullet 2.5mA}{0.9V - 3.3V - 13k\Omega \bullet 2.5mA}\right\} = 0.205\mu s \quad (20)$$

$$t_r = t_1 + t_2 = 0.515\mu s + 0.205\mu s = 0.72\mu s \quad (21)$$

$$t_f = 293\Omega \bullet 400pF \bullet \ln\left\{\frac{\frac{2.1V + 0.15V}{3.3V} \bullet (13k\Omega + 300\Omega) - 300\Omega}{\frac{0.8V - 0.15V}{3.3V} \bullet (13k\Omega + 300\Omega) - 300\Omega}\right\} = 0.156\mu s \quad (22)$$

The rise time meets the 1µs SMBus requirement and the fall time meets the 0.3µs requirement. The V_{OL} is satisfied while meeting the minimum slew rate requirements, so R_P is chosen to be 13kΩ. If the rise time was not met due to a large t_1, equation 6 can be used to calculate a maximum value of R_P that will meet the rise time requirements.

ACK Data Setup Time

Care must be taken in selecting the value of R_S (in series with the pull-down driver) to ensure that the data setup time requirement for ACK (acknowledge) is fulfilled. An acknowledge is the host releasing the SDA line (pulling high) at the end of the last bit sent and the slave device pulling the SDA line low before the rising edge of the ACK clock pulse.

The LTC4311 5mA pull-up current is activated when the host releases the SDA line, allowing the voltage to rise above the LTC4311's comparator threshold (V_{THR}). If a slave device has a high value of R_S, a longer time is required for the slave device to pull SDA low before the rising edge of the ACK clock pulse. To ensure sufficient data setup time for ACK, slave devices with high values of R_S should pull the SDA low earlier.

An alternative is the slave device can hold the SCL line low until the SDA line reaches a stable state. Then, SCL can be released to generate the ACK clock pulse.

Multiple LTC4311s in Parallel

In very heavily loaded systems, stronger pull up current may be desired. Two LTC4311's may be used in parallel to increase the total pull up current to meet rise time requirements.

Notes on Using the LTC4311 in LTC1694 Applications

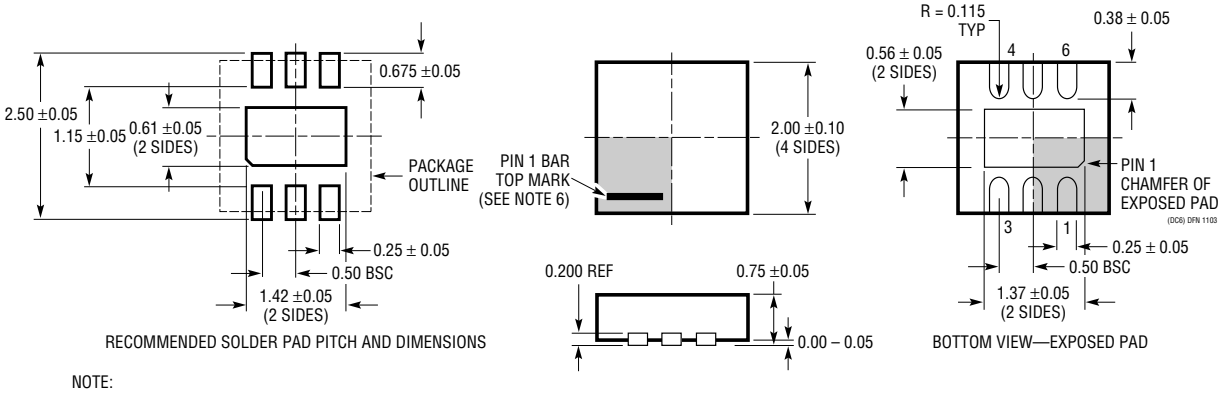
Although the LTC1694 and LTC4311 are functionally similar accelerators for I²C, SMBus, and other comparable open drain/collector bus applications, the LTC4311 offers a lower power, higher performance solution in a smaller package as compared to the LTC1694. These and other differences are listed in Table 1 and must be accounted for if using the LTC4311 in LTC1694 applications.

Table 1. Differences Between LTC1694 and LTC4311

SPECIFICATION	LTC1694	LTC4311	COMMENTS
Enable Pin (typ)	N/A	1V	Allows the LTC4311 to be Disabled, Consuming Less than 5µA
V_{CC}	2.7V – 6V	1.6V – 5.5V	Lower Operating Supply Voltage for Low Voltage Systems
I_{CC} (typ), BUS1, BUS2 High	60µA	26µA	Lower Standby Current to Conserve Power
V_{THRES} (typ)	0.65V	Dependent on V_{CC}	Tighter, Higher Noise Margins and Improved Rise Times
$I_{PULL-UP}$ (typ)	2.2mA	5mA	Stronger Slew-Limited Source Current for Slewing Higher Bus Capacitances
f_{MAX}	100kHz	400kHz	Higher Operating Frequency for I²C's Fast Mode Bus Specification

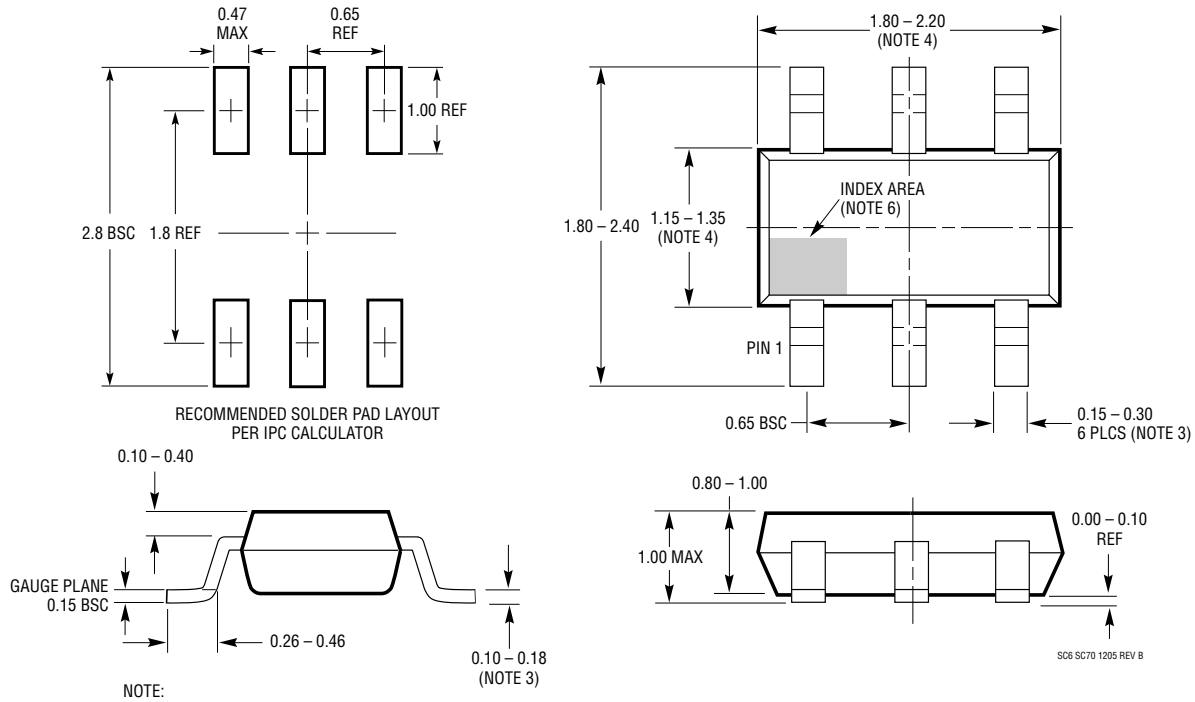
PACKAGE DESCRIPTION

DC Package
6-Lead Plastic DFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1703)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WCCD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

SC6 Package
6-Lead Plastic SC70
(Reference LTC DWG # 05-08-1638 Rev B)

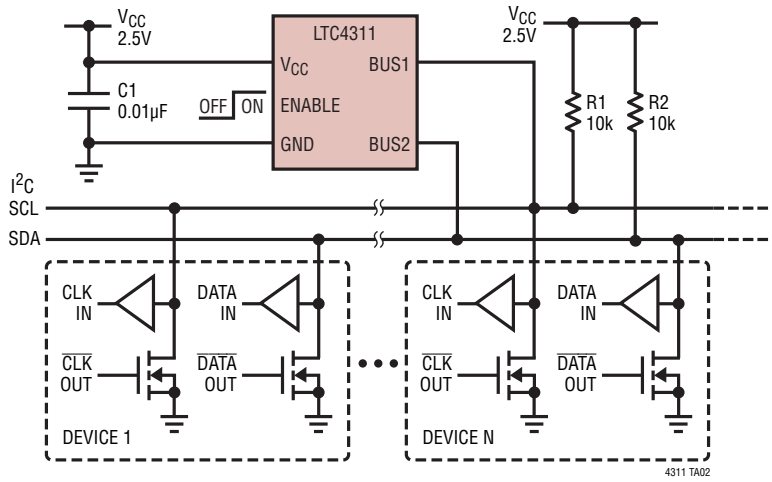


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. DETAILS OF THE PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE INDEX AREA
7. EIAJ PACKAGE REFERENCE IS EIAJ SC-70
8. JEDEC PACKAGE REFERENCE IS MO-203 VARIATION AB

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Application Utilizing Low Current Shutdown



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1380/LTC1393	Single-Ended 8-Channel/Differential 4-Channel Analog MUX with SMBus Interface	Low R_{ON}: 35Ω Single-Ended/70Ω Differential, Expandable to 32 Single or 16 Differential Channels
LTC1427-50	Micropower, 10-Bit Current Output DAC with SMBus Interface	Precision 50µA +/– 2.5% Tolerance Over Temperature, 4 Selectable SMBus Addresses, DAC Powers Up at Zero or Midscale
LTC1623	Dual High Side Switch Controller with SMBus Interface	8 Selectable Addresses/16 Channel Capability
LTC1663	SMBus Interface 10-Bit Rail-to-Rail Micropower DAC	DNL < 0.75 LSB Max, 5-Lead SOT-23 Package
LTC1694/LTC1694-1	SMBus Accelerator	Improved SMBus/I2C Rise-Time, Ensures Data Integrity with Multiple SMBus/I2C Devices
LT1786F	SMBus Controlled CCFL Switching Regulator	1.25A, 200kHz, Floating or Grounded Lamp Configurations
LTC1695	SMBus/ I2C Fan Speed Controller in ThinSOT™	0.75Ω PMOS 180mA Regulator, 6-Bit DAC
LTC1840	Dual I2C Fan Speed Controller	Two 100µA 8-Bit DACs, two Tach Inputs, Four GPIO
LTC4300A-1/ LTC4300A-2/ LTC4300A-3	Hot Swappable 2-Wire Bus Buffers	-1: Bus Buffer with READY, ACC and ENABLE -2: Dual Supply Bus Buffer with READY and ACC -3: Dual Supply Bus Buffer with READY and ENABLE
LTC4301	Supply Independent Hot Swappable 2-Wire Bus Buffer	Supply Independent
LTC4301L	Hot Swappable 2-Wire Bus Buffer with Low Voltage Level Translation	Allows Bus Pull-Up Voltages as Low as 1V on SDAIN and SCLIN
LTC4302-1/ LTC4302-2	Addressable 2-Wire Bus Buffer	Address Expansion, GPIO, Software Controlled
LTC4303/4	Hot Swappable 2-Wire Bus Buffers with Stuck Bus Recovery	Provides Automatic Clocking to Free Stuck I2C Busses
LTC4305/6	2 or 4-Channel, 2 Wire Bus Multiplexers with Capacitance Buffering	2 or 4 Selectable Downstream Buses, Stuck Bus Disconnect, Rise Time Accelerators, Fault Reporting, +/– 10kV HBM ESD Tolerance
LTC4307	Low Offset Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery	60mV Buffer Offset with 30ms Stuck Bus Timeout

ThinSOT is a trademark of Linear Technology Corporation

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