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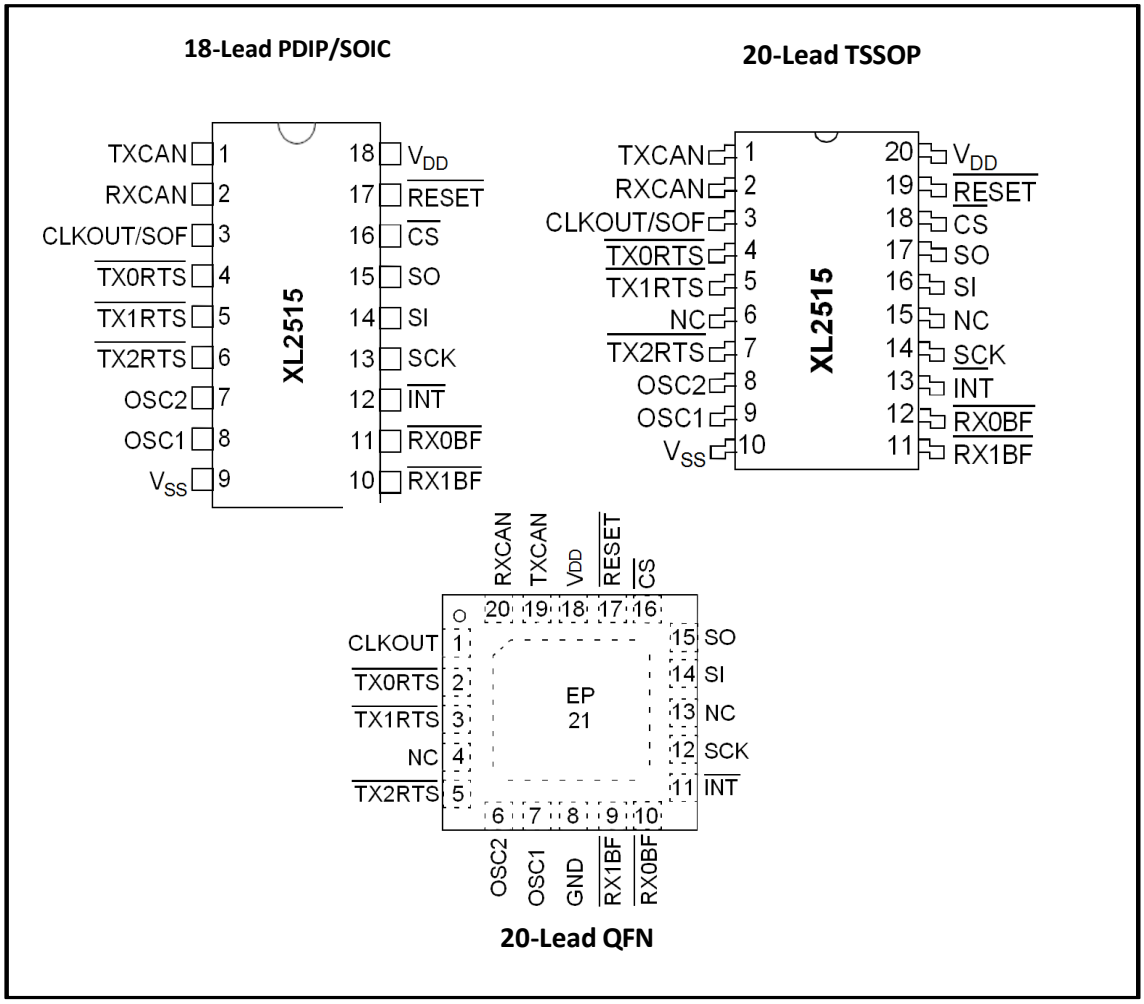
1. DESCRIPTION

The XL2515 is a Controller Area Network (CAN) controller that is stand-alone and implements the CAN version 2.0B specification . The controller can simultaneously transmit and receive standard and extended data as well as remote frames.The XL2515 has two receive masks and six receive filters to filter out unwanted information, minimising the workload on the host MCU.The XL2515 is interfaced to the microcontroller (MCU) via a standard serial peripheral interface (SPI).

2. FEATURES

- Low-Power CMOS Technology:
  - -Operates from 2.7V-5.5V
  - -5 mA active current (typical)
  - -1 µA standby current (typical) (Sleep mode)
- Implements CAN V2.0B at 1 Mb/s:
  - -0 to 8-byte length in the data field
  - -Standard and extended data and remote frames
- Receive Buffers, Masks and Filters:
  - -Two receive buffers with prioritized message storage
  - -Six 29-bit filters
  - -Two 29-bit masks
- Start-of-Frame (SOF) Signal is Available for Monitoring the SOF Signal:
  - -Can be used for time slot-based protocols and/or bus diagnostics to detect early bus degradation
- High-Speed SPI Interface (10 MHz):
  - -SPI Modes 0,0 and 1,1
- One-Shot mode Ensures Message Transmission is Attempted Only One Time
- Clock Out Pin with Programmable Prescaler:
  - -Can be used as a clock source for other device(s)
- Request-to-Send (RTS) Input Pins Individually Configurable as:
  - -Control pins to request transmission for each transmit buffer
  - -General purpose inputs
- Interrupt Output Pin with Selectable Enables
- Three Transmit Buffers with Prioritization and Abort Features
- Data Byte Filtering on the First Two Data Bytes (applies to standard data frames)
- Buffer Full Output Pins Configurable as:
  - -Interrupt output for each receive buffer
  - -General purpose output
- Temperature Ranges :
  - -Industrial (I): -40° C to +85° C

3. PACKAGE AND PINOUT

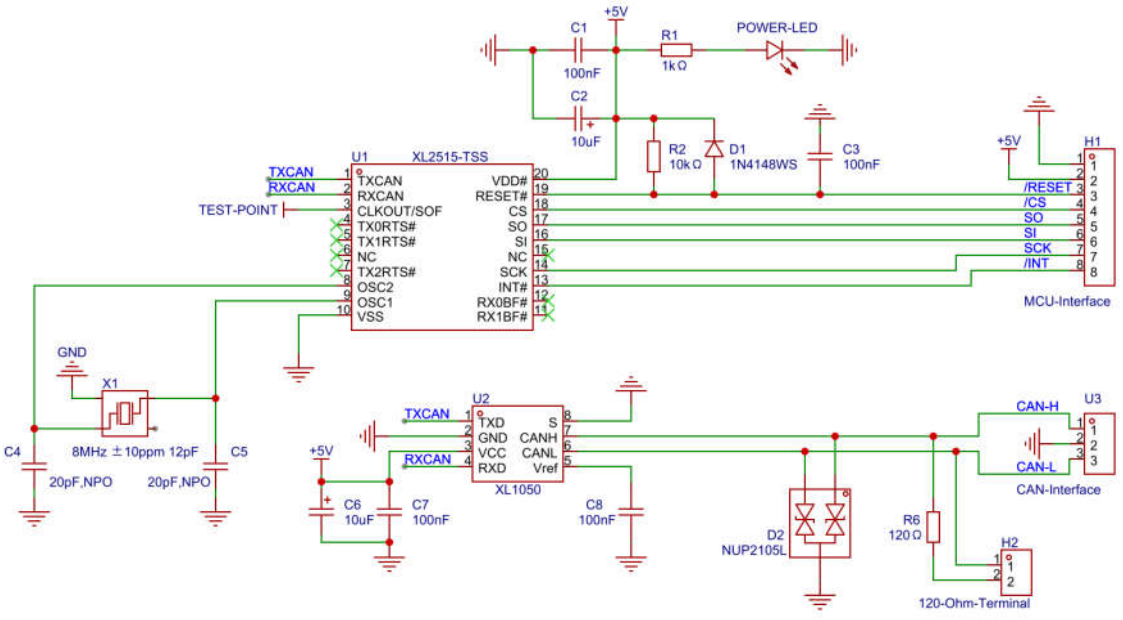


4. PIN CONFIGURATIONS AND FUNCTIONS

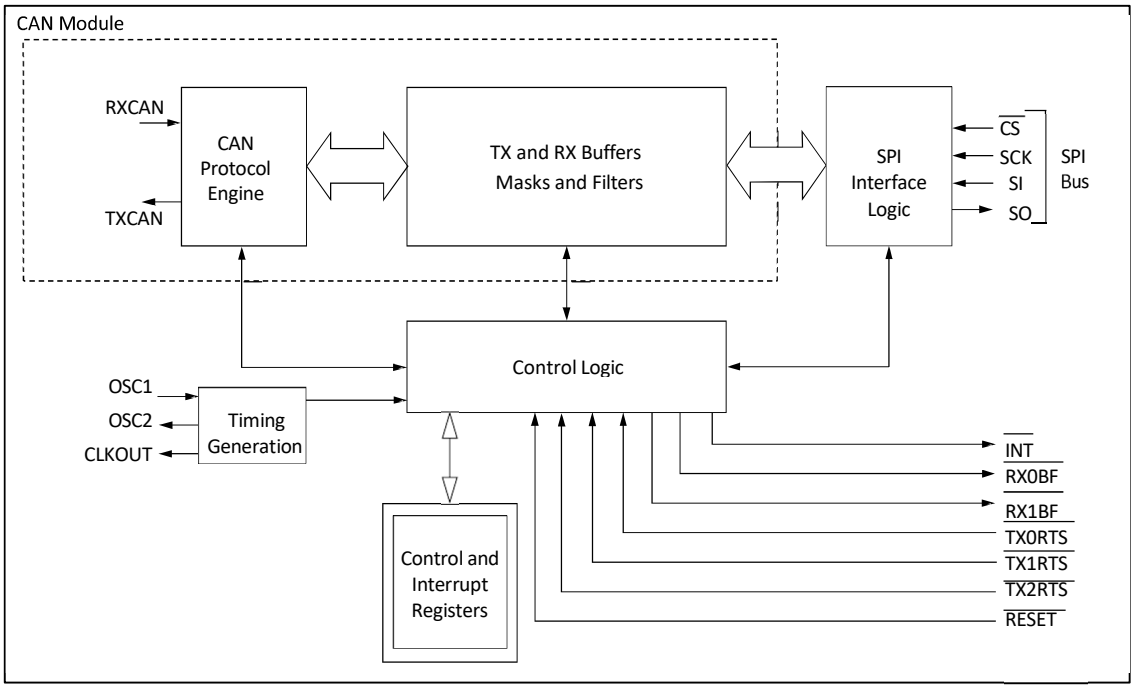
Name	PDIP/ SOIC Pin #	TSSOP Pin #	QFN Pin #	I/O/P Type	Description	Alternate Pin Function
TXCAN	1	1	19	O	Transmit output pin to CAN bus	—
RXCAN	2	2	20	I	Receive input pin from CAN bus	—
CLKOUT	3	3	1	O	Clock output pin with programmable prescaler	Start-of-Frame signal
$\overline{\text{TX0RTS}}$	4	4	2	I	Transmit buffer TXB0 Request-to-Send; 100 k internal pull-up to V_{DD}	General purpose digital input, 100 k internal pull-up to V_{DD}
$\overline{\text{TX1RTS}}$	5	5	3	I	Transmit buffer TXB1 Request-to-Send; 100 k internal pull-up to V_{DD}	General purpose digital input, 100 k internal pull-up to V_{DD}
$\overline{\text{TX2RTS}}$	6	7	5	I	Transmit buffer TXB2 Request-to-Send; 100 k internal pull-up to V_{DD}	General purpose digital input, 100 k internal pull-up to V_{DD}
OSC2	7	8	6	O	Oscillator output	—
OSC1	8	9	7	I	Oscillator input	External clock input
V_{SS}	9	10	8	P	Ground reference for logic and I/O pins	—
$\overline{\text{RX1BF}}$	10	11	9	O	Receive buffer RXB1 interrupt pin or general purpose digital output	General purpose digital output
$\overline{\text{RX0BF}}$	11	12	10	O	Receive buffer RXB0 interrupt pin or general purpose digital output	General purpose digital output
$\overline{\text{INT}}$	12	13	11	O	Interrupt output pin	—
SCK	13	14	12	I	Clock input pin for SPI interface	—
SI	14	16	14	I	Data input pin for SPI interface	—
SO	15	17	15	O	Data output pin for SPI interface	—
$\overline{\text{CS}}$	16	18	16	I	Chip select input pin for SPI interface	—
$\overline{\text{RESET}}$	17	19	17	I	Active-low device Reset input	—
V_{DD}	18	20	18	P	Positive supply for logic and I/O pins	—
NC	—	6,15	4,13	—	No internal connection	—
EP	—	—	21	—	Exposed Thermal Pad, connect to V_{SS}	—

Legend: I = Input; O = Output; P = Power

5. APPLICATION CIRCUIT EXAMPLE



6. BLOCK DIAGRAM



7. DEVICE OVERVIEW

The XL2515 is a stand-alone CAN controller designed to simplify applications requiring connectivity to a CAN bus. A simple block diagram of the XL2515 is shown in Figure 1. The device consists of three main blocks:

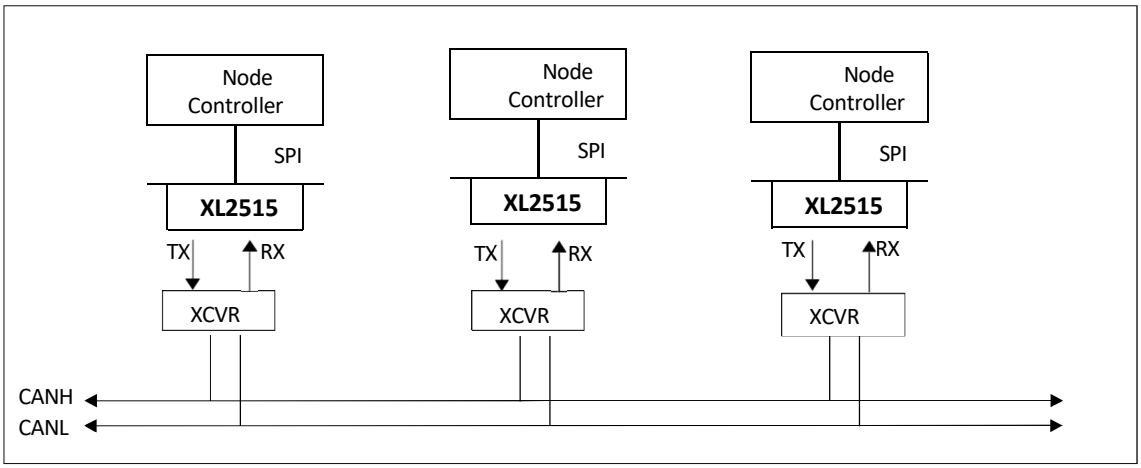
[1] The CAN module, which contains the CAN protocol, transmits and receives buffers, motor, masks and filters.

[2] The control logic and registers used to configure the device and its operation.

[3] The SPI protocol block.

An example of a system implementation with the device is shown in Figure 2.

FIGURE 1 : EXAMPLE SYSTEM IMPLEMENTATION



7.1. CAN Module

The CAN module manages all the functions for transmitting and receiving messages on the CAN bus. Messages are transmitted by first loading the appropriate message buffer and control protocols. Transmission is initiated by the bits in the control register or by using the transmit enable pin via the SPI interface. Status and errors can be checked by reading the corresponding registers. All messages detected on the CAN bus are checked for errors and then compared with user-defined filters to determine whether they should be transmitted to one of the two receive buffers.

7.2. Control Logic

The control logic blocks control the configuration and operation of the XL2515 by interfacing with other blocks to transfer information and commands.

Interrupt pins are provided to increase system flexibility. Each receive register has a general purpose interrupt pin (and a specific interrupt pin) that can be used to indicate that a valid message has been received and loaded into one of the receive buffers. The application of the specific interrupt pins is optional. Use of the general interrupt pins and the status register (accessible via SPI) can also be used to determine whether a valid message has been received.

In addition, three pins can be used to initiate immediate transmission of a message loaded into one of the three transport registers. Use of these pins is optional and can also be accomplished by utilising the control registers accessible via the SPI interface to initiate message transmission.

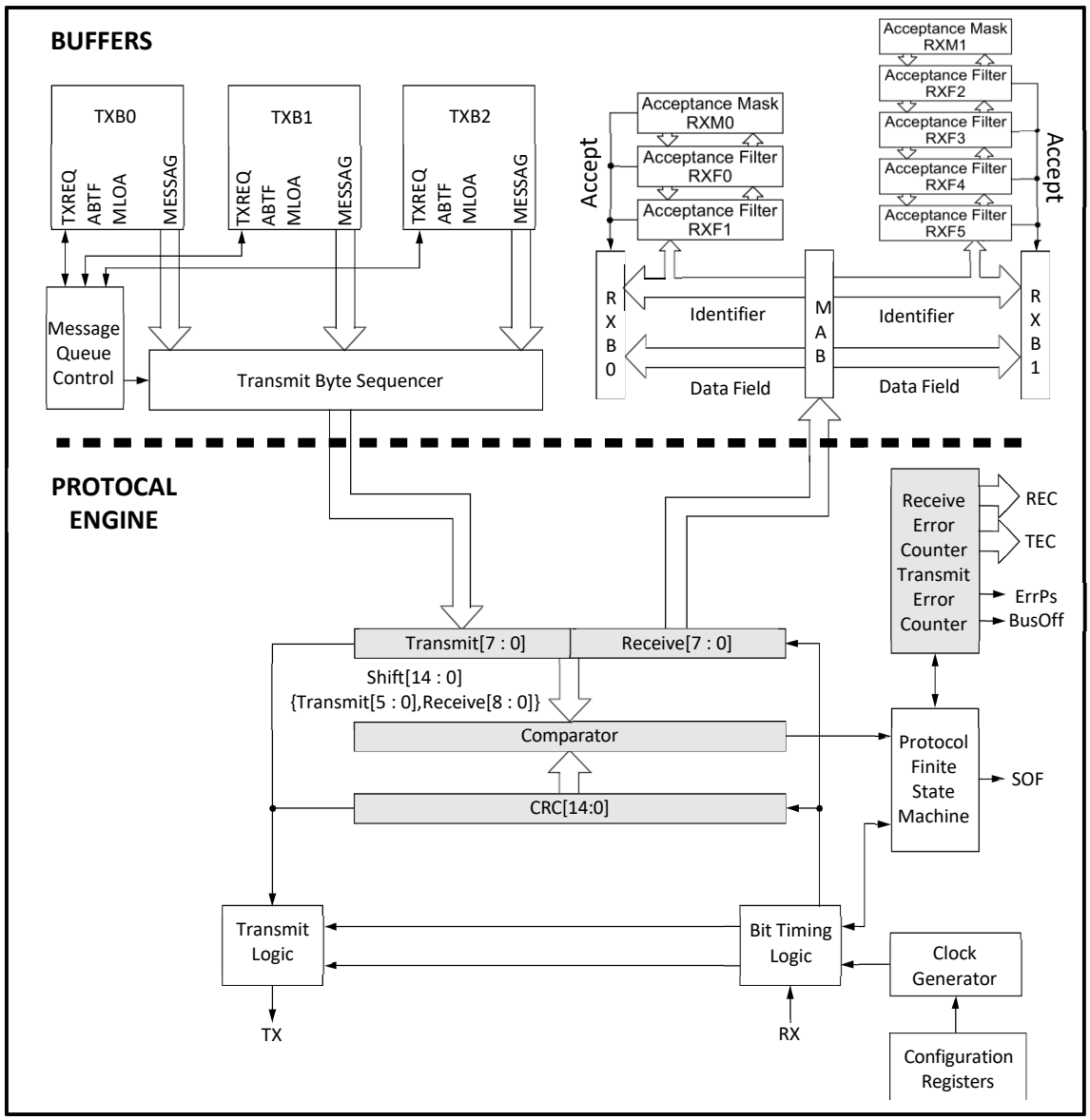
7.3. SPI Protocol Block

The MCU will interface to the device via the SPI interface. All registers are written and retrieved using standard SPI read and write commands in addition to special SPI commands.

7.4. Transmit/Receive Buffers/Masks/ Filters

The XL2515 has three transmit and two receive buffers, two reception masks (of each receive buffer) and a total of six receive filters. Figure 2 shows a block diagram of these buffers and their connections to the protocol engine.

FIGURE 2 : CAN BUFFERS AND PROTOCOL ENGINE BLOCK DIAGRAM



8. REGISTER MAP

The XL2515's register map is shown in Table 1 .The values in the column (four highest bits) and row (four lowest bits) are used to determine the address of each register.The registers are positioned with sequential reads and writes of optimised data.In certain control and status registers, individual bits can be modified using the SPI BIT MODIFY command.Registers that accept this command are indicated by the shadow positions in Table 1.Table 2 summarises the XL2515's control registers.A summary of the MCP2515 control registers is shown in Table 2.

TABLE 1 : CAN CONTROLLER REGISTER MAP

Lower Address Bits	Higher Order Address Bits							
	0000 xxxx	0001 xxxx	0010 xxxx	0011 xxxx	0100 xxxx	0101 xxxx	0110 xxxx	0111 xxxx
0000	RXF0SIDH	RXF3SIDH	RXM0SIDH	TXB0CTRL	TXB1CTRL	TXB2CTRL	RXB0CTRL	RXB1CTRL
0001	RXF0SIDL	RXF3SIDL	RXM0SIDL	TXB0SIDH	TXB1SIDH	TXB2SIDH	RXB0SIDH	RXB1SIDH
0010	RXF0EID8	RXF3EID8	RXM0EID8	TXB0SIDL	TXB1SIDL	TXB2SIDL	RXB0SIDL	RXB1SIDL
0011	RXF0EID0	RXF3EID0	RXM0EID0	TXB0EID8	TXB1EID8	TXB2EID8	RXB0EID8	RXB1EID8
0100	RXF1SIDH	RXF4SIDH	RXM1SIDH	TXB0EID0	TXB1EID0	TXB2EID0	RXB0EID0	RXB1EID0
0101	RXF1SIDL	RXF4SIDL	RXM1SIDL	TXB0DLC	TXB1DLC	TXB2DLC	RXB0DLC	RXB1DLC
0110	RXF1EID8	RXF4EID8	RXM1EID8	TXB0D0	TXB1D0	TXB2D0	RXB0D0	RXB1D0
0111	RXF1EID0	RXF4EID0	RXM1EID0	TXB0D1	TXB1D1	TXB2D1	RXB0D1	RXB1D1
1000	RXF2SIDH	RXF5SIDH	CNF3	TXB0D2	TXB1D2	TXB2D2	RXB0D2	RXB1D2
1001	RXF2SIDL	RXF5SIDL	CNF2	TXB0D3	TXB1D3	TXB2D3	RXB0D3	RXB1D3
1010	RXF2EID8	RXF5EID8	CNF1	TXB0D4	TXB1D4	TXB2D4	RXB0D4	RXB1D4
1011	RXF2EID0	RXF5EID0	CANINTE	TXB0D5	TXB1D5	TXB2D5	RXB0D5	RXB1D5
1100	BFPCTRL	TEC	CANINTF	TXB0D6	TXB1D6	TXB2D6	RXB0D6	RXB1D6
1101	TXRTSCTRL	REC	EFLG	TXB0D7	TXB1D7	TXB2D7	RXB0D7	RXB1D7
1110	CANSTAT	CANSTAT	CANSTAT	CANSTAT	CANSTAT	CANSTAT	CANSTAT	CANSTAT
1111	CANCTRL	CANCTRL	CANCTRL	CANCTRL	CANCTRL	CANCTRL	CANCTRL	CANCTRL

TABLE 2 : CONTROL REGISTER SUMMARY

Register Name	Address (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR/Reset Value
BFPCTRL	0C	—	—	B1BFS	B0BFS	B1BFE	B0BFE	B1BFM	B0BFM	--00 0000
TXRTSCTRL	0D	—	—	B2RTS	B1RTS	B0RTS	B2RTSM	B1RTSM	B0RTSM	--xx x000
CANSTAT	XE	OPMOD2	OPMOD1	OPMOD0	—	ICOD2	ICOD1	ICOD0	—	100- 000-
CANCTRL	XF	REQOP2	REQOP1	REQOP0	ABAT	OSM	CLKEN	CLKPRE1	CLKPRE0	1000 0111
TEC	1C	Transmit Error Counter (TEC)								0000 0000
REC	1D	Receive Error Counter (REC)								0000 0000
CNF3	28	SOF	WAKFIL	—	—	—	PHSEG22	PHSEG21	PHSEG20	00-- -000
CNF2	29	BTLMODE	SAM	PHSEG12	PHSEG11	PHSEG10	PRSEG2	PRSEG1	PRSEG0	0000 0000
CNF1	2A	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	0000 0000
CANINTE	2B	MERRE	WAKIE	ERRIE	TX2IE	TX1IE	TX0IE	RX1IE	RX0IE	0000 0000
CANINTF	2C	MERRF	WAKIF	ERRIF	TX2IF	TX1IF	TX0IF	RX1IF	RX0IF	0000 0000
EFLG	2D	RX1OVR	RX0OVR	TXBO	TXEP	RXEP	TXWAR	RXWAR	EWARN	0000 0000
TXB0CTRL	30	—	ABTF	MLOA	TXERR	TXREQ	—	TXP1	TXP0	-000 0-00
TXB1CTRL	40	—	ABTF	MLOA	TXERR	TXREQ	—	TXP1	TXP0	-000 0-00
TXB2CTRL	50	—	ABTF	MLOA	TXERR	TXREQ	—	TXP1	TXP0	-000 0-00
RXB0CTRL	60	—	RXM1	RXM0	—	RXRTR	BUKT	BUKT1	FILHIT0	-00- 0000
RXB1CTRL	70	—	RXM1	RXM0	—	RXRTR	FILHIT2	FILHIT1	FILHIT0	-00- 0000

9. SPI INTERFACE

9.1. Overview

The XL2515 is designed to communicate directly with the serial peripheral interface (SPI) port commonly associated with many microcontrollers and supports both 0.0 and 1.1 modes. Commands and data are sent to the device via the SI pin, with data coming from the rising edge of the SCK signal. Data is generated by the XL2515 (along the SO line) along the falling edge of the SCK. During any operation, the CS output must be kept low. Table 1 shows the instruction bytes for all operations. Figures 3 and 4 show detailed time diagrams of input and output data for modes 0.0 and 1.1.

Note: The XL2515 expects the first byte after lowering the CS to be an instruction/command byte. This means that it is necessary to raise the CS and lower it again to invoke another instruction.

TABLE 3 : SPI INSTRUCTION SET

Instruction Name	Instruction Format	Description
RESET	1100 0000	Resets internal registers to the default state, sets Configuration mode.
READ	0000 0011	Reads data from the register beginning at selected address.
READ RX BUFFER	1001 0nm0	When reading a receive buffer, reduces the overhead of a normal READcommand by placing the Address Pointer at one of four locations, as indicated by 'n,m'. **Note :** The associated RX flag bit, RXnIF (CANINTF), will be cleared after bringing CS high.
WRITE	0000 0010	Writes data to the register beginning at the selected address.
LOAD TX BUFFER	0100 0abc	When loading a transmit buffer, reduces the overhead of a normal WRITEcommand by placing the Address Pointer at one of six locations, as indicated by 'a,b,c'.
RTS (Message Request-to-Send)	1000 0nnn	Instructs controller to begin message transmission sequence for any of the transmit buffers. 1000 0nnn Request-to-Send for TXB2 / Request-to-Send for TXB1 / Request-to-Send for TXBO
READ STATUS	1010 0000	Quick polling command that reads several status bits for transmit and receive functions.
RX STATUS	1011 0000	Quick polling command that indicates filter match and message type (standard, extended and/or remote) of received message.
BIT MODIFY	0000 0101	Allows the user to set or clear individual bits in a particular register. **Note:** Not all registers can be bit modified with this command. Executing this command on registers that are not bit modifiable will force the mask to FFh. See the register map in **Section 11.0 "Register Map"** for a list of the registers that apply.

FIGURE 3 : SPI INPUT TIMING

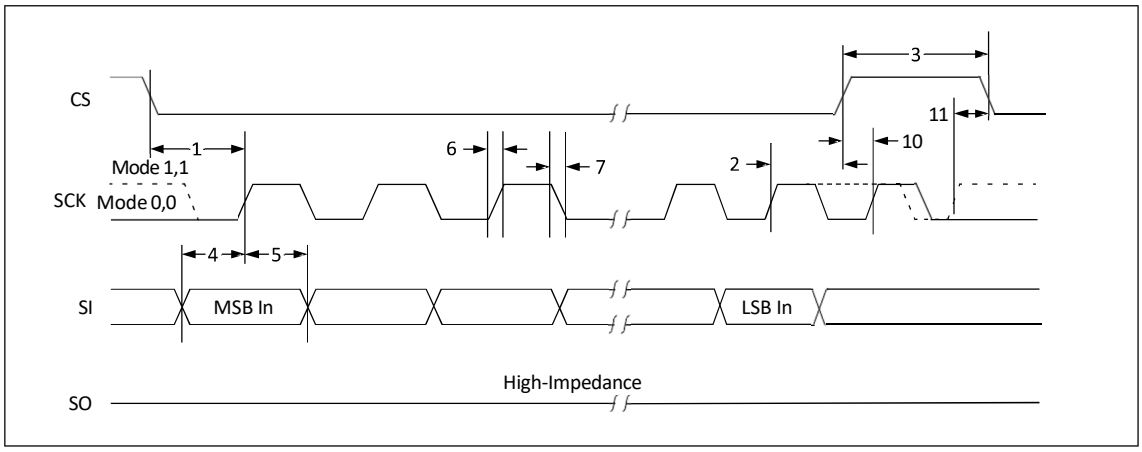
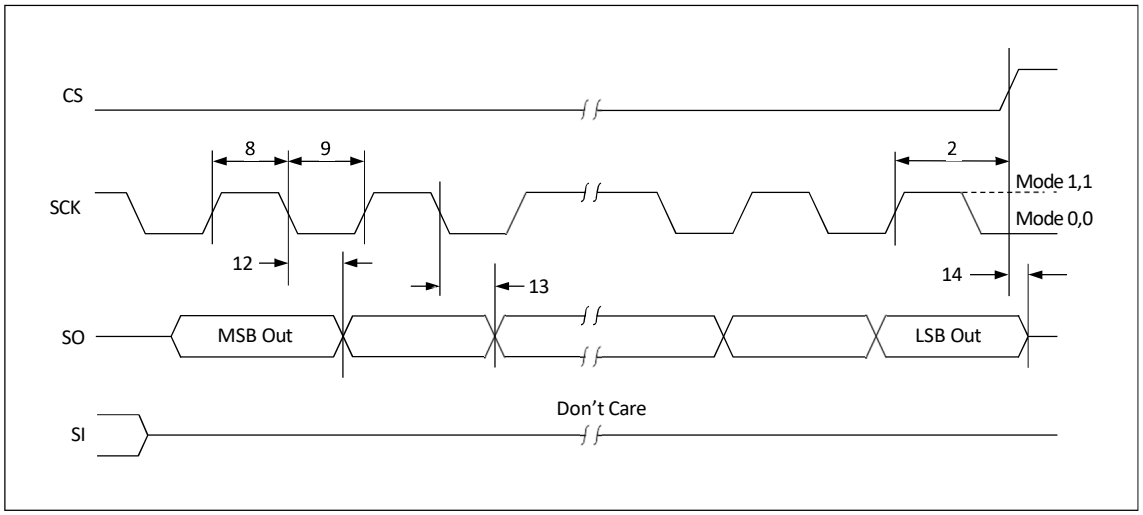


FIGURE 4 : SPI OUTPUT TIMING



9.2. RESET Instruction

The RESET instruction can be used to reinitialise the XL2515's internal registers and set the configuration mode. This command provides the same functionality as the RESET pin through the SPI interface.

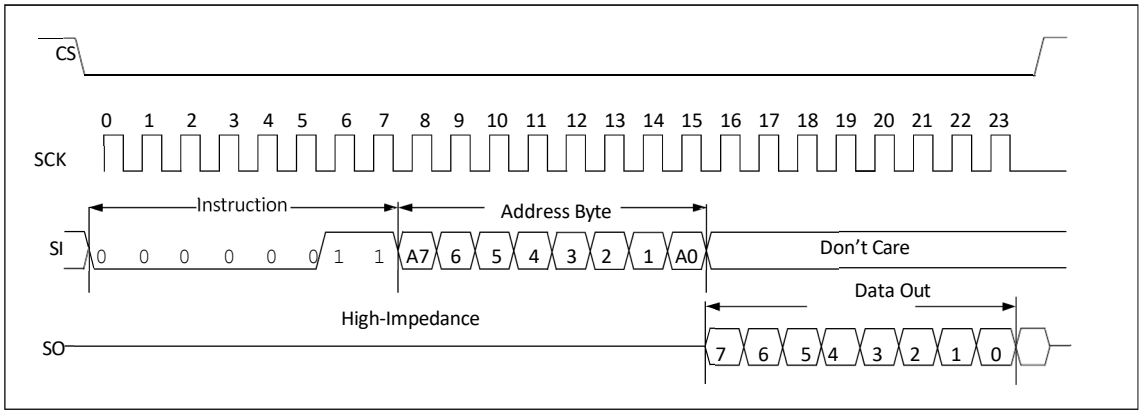
The RESET instruction is a single-byte operation that requires selecting the device by pulling the CS pin low, sending the operation byte, and then pulling the CS pin high. It is recommended to send the RESET command (or to lower the RESET pin)as part of the power-on initialisation sequence .

9.3. READ Instruction

The READ instruction is initiated by pulling the CS pin low. Next, a READ instruction is sent to the XL2515 and an 8-bit address (A7 to A0) is transmitted. The data stored in the register at the selected address is shifted on the SO pin.

The internal address pointer is automatically incremented to the next address as each byte of data is moved. Therefore, the next consecutive register address can be read by continuously supplying clock pulses. In this way, an arbitrary number of consecutive register locations can be read sequentially. Read operation is terminated by pulling the CS pin up (Figure 5).

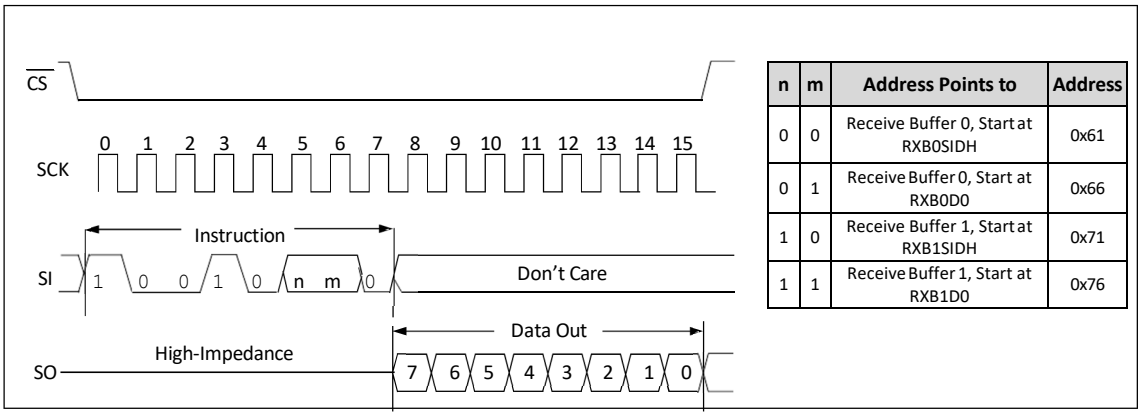
FIGURE 5 : READ INSTRUCTION



9.4. READ RX BUFFER Instruction

The READ RX BUFFER instruction (Figure 6) provides a rapid technique to process the address of the receive buffer for reading. This command can reduce the SPI overhead by one byte of the address byte. The command byte has four possible values that determine the position of the address pointer. When the command byte is sent, the controller clocks out the data at the same address location as the READ command (i.e., sequential reads are possible). The command further reduces SPI overhead by automatically clearing the associated receive flag RXnIF (CANINTF) when a CS occurs at the end of the command.

FIGURE 6 : READ RX BUFFER INSTRUCTION



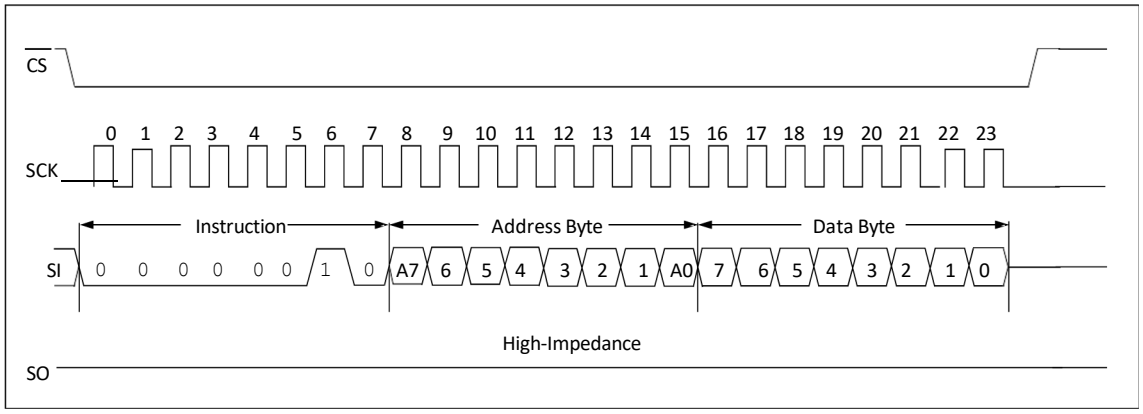
n	m	Address Points to	Address
0	0	Receive Buffer 0, Start at RXB0SIDH	0x61
0	1	Receive Buffer 0, Start at RXB0D0	0x66
1	0	Receive Buffer 1, Start at RXB1SIDH	0x71
1	1	Receive Buffer 1, Start at RXB1D0	0x76

9.5. WRITE Instruction

A WRITE instruction is initiated by pulling the CS pin low. A WRITE command is then sent to the XL2515, followed by the address and at least one byte of data.

Data bytes can be clocked in to write to contiguous registers while CS is held low. The data is actually written to the registers on the rising edge of the D0-bit SCK line. If the CS line goes high before the 8 bits are loaded, the write of that data byte is aborted and the previous byte of the instruction is written. For more information about the byte write sequence, see the timing diagram in Figure 7.

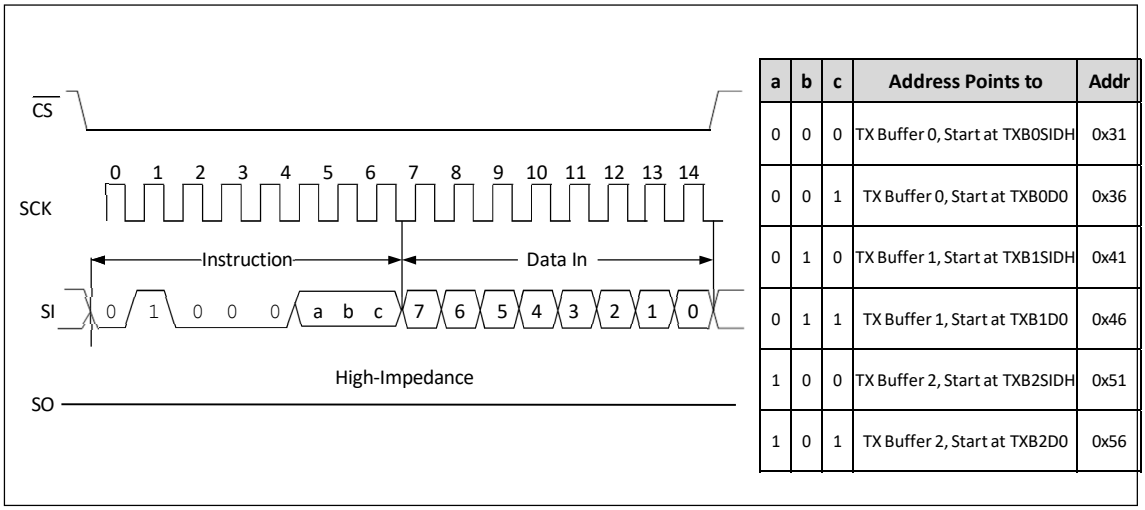
FIGURE 7 : BYTE WRITE INSTRUCTION



9.6. LOAD TX BUFFER Instruction

The LOAD TX BUFFER instruction (Figure 8) obliterates the 8-bit addresses required by the standard WRITE instruction. This 8-bit command sets the address pointer to one of six addresses and quickly writes to the transfer buffer pointing to the "ID" or "Data" address in one of the three transfer buffers.

FIGURE 8: LOAD TX BUFFER INSTRUCTION



a	b	c	Address Points to	Addr
0	0	0	TX Buffer 0, Start at TXB0SIDH	0x31
0	0	1	TX Buffer 0, Start at TXB0D0	0x36
0	1	0	TX Buffer 1, Start at TXB1SIDH	0x41
0	1	1	TX Buffer 1, Start at TXB1D0	0x46
1	0	0	TX Buffer 2, Start at TXB2SIDH	0x51
1	0	1	TX Buffer 2, Start at TXB2D0	0x56

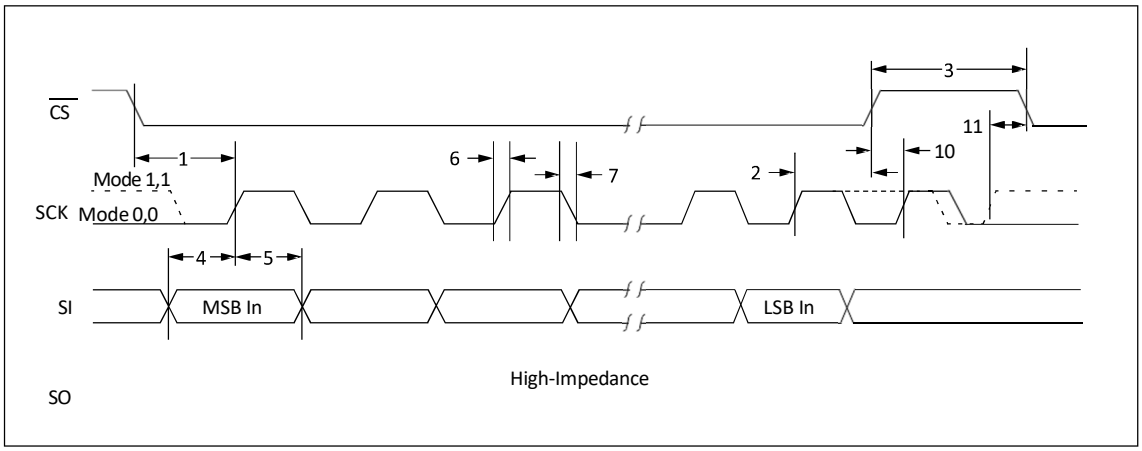
9.7. Request-to-Send (RTS) Instruction

The RTS command can be used to initiate message transmission for one or more sending buffers.

The XL2515 is selected by lowering the CS pin. The bytes of the RTS command are then sent. As shown in Figure 9, the last three bits of this command indicate which transmit buffer is available for transmission.

This command sets the TXREQ bit (TXBnCTRL[3]) for each buffer. All or part of the last three bits can be defined with a single command. If send an RTS command with nnn = 000, the command is ignored.

FIGURE 9 : SPI INPUT TIMING



9.8. READ STATUS Instruction

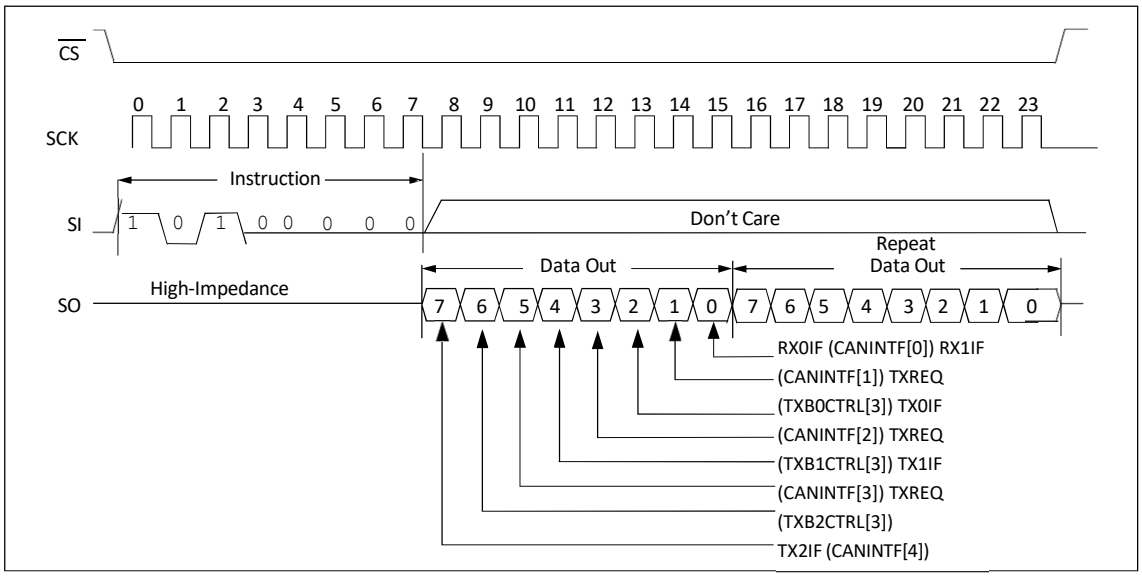
The READ STATUS instruction provides a single instruction access to several of the status bits that are frequently used to receive and transmit messages.

Pulling the CS pin low selects the XL2515 and sends the READ STATUS command byte shown in Figure 10 to the XL2515.After the command byte is sent, the XL2515 will return eight bits of data, including the status.

If additional clocks are sent after the first 8 bits are transmitted, the XL2515 will continue to output status bits as long as the CS pin is held low and a clock is supplied from SCK.

Each status bit returned by this command can also be read using the standard READ command by specifying the appropriate register address.

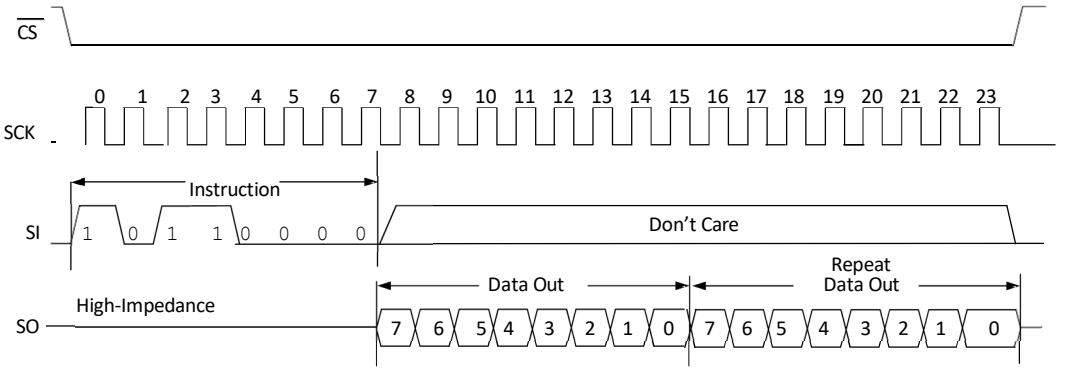
FIGURE 10 : READ STATUS INSTRUCTION



9.9. RX STATUS Instruction

The RX STATUS instruction (Figure 11) is used to quickly determine the filters for the corresponding messages and the message types (standard, extended, remote). After sending the command bytes, the controller will return 8 bits of data, including status data. If more clocks are sent after 8 bits have been sent, the controller continues to display the same status bit, provided that the clock is supplied if the CS pin remains low.

FIGURE 11 : RX STATUS INSTRUCTION



7	6	Received Message
0	0	No RX message
0	1	Message in RXB0
1	0	Message in RXB1
1	1	Messages in both buffers*

RXnIF (CANINTF) bits are mapped. to bits 7 and 6.

4	3	Msg Type Received
0	0	Standard data frame
0	1	Standard remote frame
1	0	Extended data frame
1	1	Extended remote frame

The extended ID bit is mapped to bit 4. The RTR bit is mapped to bit 3.

2	1	0	Filter Match
0	0	0	RXF0
0	0	1	RXF1
0	1	0	RXF2
0	1	1	RXF3
1	0	0	RXF4
1	0	1	RXF5
1	1	0	RXF0 (rollover to RXB1)
1	1	1	RXF1 (rollover to RXB1)

*Buffer 0 has higher priority; therefore, RXB0 status is reflected in

9.10. BIT MODIFY Instruction

The BIT MODIFY instruction is used to set or clear the individual bits of a particular state and control register. This command is not available for all registers . See section *8 'REGISTER MAP'* for information on which registers allow the use of this command.

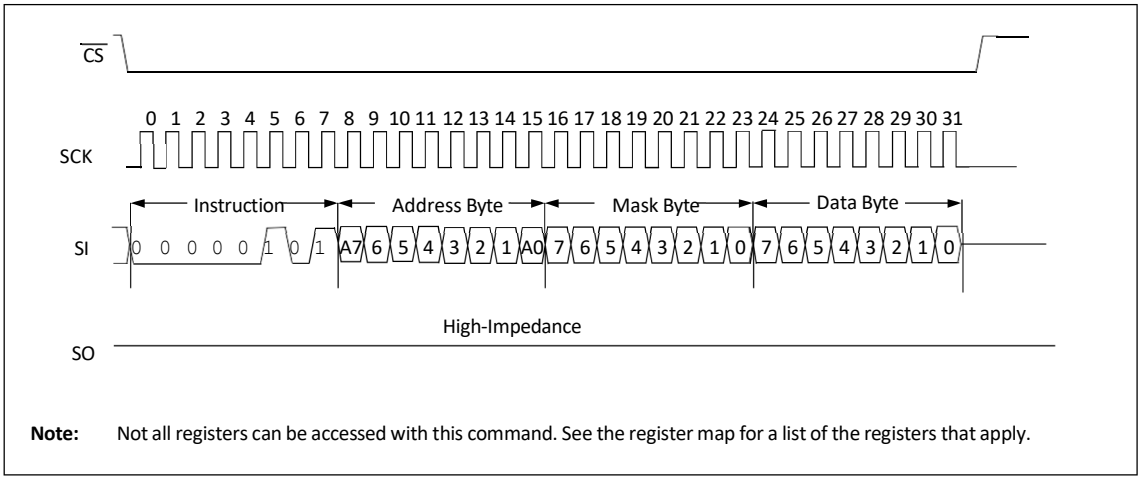
Note: If the BIT MODIFY command is executed on a register with unmodifiable bits, the mask will force FFh. This allows bytes to be written to the register instead of MODIFY BIT.

Lower the CS pin, select the part, then send BIT MODIFY command byte to XL2515. The command is successively the register address, the mask byte, and finally the data byte.

The mask byte determines which register bit is to be changed. If the mask byte is specified as '1', the register bit is changed, while '0' is the constant bit.

The data bytes determine to which value the bits changed in the register will be modified. Sets the bits "1", "0" in the data bytes. However, the condition is that the mask for this bit is set to '1' (see figure 12).

FIGURE 12 : BIT MODIFY INSTRUCTION



Note: Not all registers can be accessed with this command. See the register map for a list of the registers that apply.

10. ELECTRICAL CHARACTERISTICS

10.1. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply	6.5	V
VSS	All Inputs and Outputs w.r.t.	V to V_{DD} + 1.0V	V
T_{ST}	Storage Temperature	-50 to +100	℃
T_{ATPA}	Ambient Temperature with Power Applied	-40 to +85	℃
T_{STL}	Soldering Temperature of Leads (10 seconds)	+300	℃

Notice: Stresses above the maximum rating "may cause permanent damage to the equipment. This is a pressure assessment only and does not imply operation of the appliance under conditions in excess of those indicated in the operating list in this manual or under other conditions. Equipment reliability may be compromised by prolonged exposure to maximum rated conditions.

TABLE 3: DC CHARACTERISTICS

DC Characteristics			V_{DD} = 2.7V to 5.5V		Industrial (I): T_{AMB} = -40°C to +85°C	
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
	V_{DD}	Supply Voltage	2.7	5.5	V	
	V_{RET}	Register Retention Voltage	2.4	—	V	
		High-Level Input Voltage				
	V_{IH}	RXCAN Pin	2	V_{DD} + 1	V	
		SCK, $\overline{CS}$, SI, $\overline{TXnRTS}$ Pins	0.7 V_{DD}	V_{DD} + 1	V	
		OSC1 Pin	0.85 V_{DD}	V_{DD}	V	
		$\overline{RESET}$ Pin	0.85 V_{DD}	V_{DD}	V	
		Low-Level Input Voltage				
	V_{IL}	RXCAN, $\overline{TXnRTS}$ Pins	-0.3	0.15 * V_{DD}	V	
		SCK, $\overline{CS}$, SI Pins	-0.3	0.4 * V_{DD}	V	
		OSC1 Pin	V_{SS}	0.3 * V_{DD}	V	
		$\overline{RESET}$ Pin	V_{SS}	0.15 * V_{DD}	V	
		Low-Level Output Voltage				
	V_{OL}	TXCAN Pin	—	0.6	V	I_{OL} = +6.0 mA, V_{DD} = 4.5V
		$\overline{RXnBF}$ Pin	—	0.6	V	I_{OL} = +8.5 mA, V_{DD} = 4.5V
		SO, CLKOUT Pins	—	0.6	V	I_{OL} = +2.1 mA, V_{DD} = 4.5V
		$\overline{INT}$ Pin	—	0.6	V	I_{OL} = +1.6 mA, V_{DD} = 4.5V
		High-Level Output Voltage			V	
	V_{OH}	TXCAN, $\overline{RXnBF}$ Pins	V_{DD} – 0.7	—	V	I_{OH} = -3.0 mA, V_{DD} = 4.5V
		SO, CLKOUT Pins	V_{DD} – 0.5	—	V	I_{OH} = -400 µA, V_{DD} = 4.5V
		$\overline{INT}$ Pin	V_{DD} – 0.7	—	V	I_{OH} = -1.0 mA, V_{DD} = 4.5V
		Input Leakage Current				
	I_{LI}	All I/Os except OSC1 and $\overline{TXnRTS}$ Pins	-1	+1	µA	$\overline{CS}$ = $\overline{RESET}$ = V_{DD}, V_{IN} = V_{SS} to V_{DD}
		OSC1 Pin	-5	+5	µA	
	C_{INT}	Internal Capacitance (all inputs and outputs)	—	7	pF	T_{AMB} = +25°C, f_C = 1.0 MHz, V_{DD} = 0V **(Note 1)**
	I_{DD}	Operating Current	—	10	mA	V_{DD} = 5.5V, F_{OSC} = 25 MHz, F_{CLK} = 1 MHz, SO = Open
	I_{DDS}	Standby Current (Sleep mode)	—	5	µA	$\overline{CS}$, $\overline{TXnRTS}$ = V_{DD}, inputs tied to V_{DD} or V_{SS}, -40°C to +85°C
			—	8	µA	$\overline{CS}$, $\overline{TXnRTS}$ = V_{DD}

Note : This parameter is periodically sampled and not 100% tested.

TABLE 4 : OSCILLATOR TIMING CHARACTERISTICS

Oscillator Timing Characteristics			V_{DD} = 2.7V to 5.5V		Industrial (I): T_{AMB} = -40°C to +85°C	
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
	F_{OSC}	Clock In Frequency	1 1	40 25	MHz MHz	V_{DD} = 4.5V to 5.5V V_{DD} = 2.7V to 5.5V
	T_{OSC}	Clock In Period	25 40	1000 1000	ns	V_{DD} = 4.5V to 5.5V V_{DD} = 2.7V to 5.5V
	T_{DUTY}	Duty Cycle (external clock input)	0.45	0.55	—	$T_{OSH} / (T_{OSH} + T_{OSL})$

Note 1 : This parameter is periodically sampled and not 100% tested.

TABLE 5 : CAN INTERFACE AC CHARACTERISTICS

CAN Interface AC Characteristics			V_{DD} = 2.7V to 5.5V		Industrial (I): T_{AMB} = -40°C to +85°C	
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
	T_{WF}	Wake-up Noise Filter	100	—	ns	

TABLE 6 : RESET AC CHARACTERISTICS

Reset AC Characteristics			V_{DD} = 2.7V to 5.5V		Industrial (I): T_{AMB} = -40°C to +85°C	
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
	t_{RL}	$\overline{\text{RESET}}$ Pin Low Time	2	—	µs	

TABLE 7 : CLKOUT PIN AC CHARACTERISTICS

CLKOUT Pin AC/DC Characteristics			V_{DD} = 2.7V to 5.5V		Industrial (I): T_{AMB} = -40°C to +85°C	
ıram. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
	$t_{hCLKOUT}$	CLKOUT Pin High Time	15	—	ns	T_{OSC} = 40 ns **(Note 1)**
	$t_{lCLKOUT}$	CLKOUT Pin Low Time	15	—	ns	T_{OSC} = 40 ns **(Note 1)**
	$t_{rCLKOUT}$	CLKOUT Pin Rise Time	—	5	ns	Measured from 0.3 V_{DD} to 0.7 V_{DD} **(Note 1)**
	$t_{fCLKOUT}$	CLKOUT Pin Fall Time	—	5	ns	Measured from 0.7 V_{DD} to 0.3 V_{DD} **(Note 1)**
	$t_{dCLKOUT}$	CLKOUT Propagation Delay	—	100	ns	**Note 1**
15	t_{hSOF}	Start-of-Frame High Time	—	2 T_{OSC}	ns	**Note 1**
16	t_{dSOF}	Start-of-Frame Propagation Delay	—	2 T_{OSC} + 0.5 T_Q	ns	Measured from CAN bit sample point; device is a receiver, BRP[5:0] (CNF1[5:0]) = 0 **(Note 2)**

Note 1: All CLKOUT mode functionality and output frequency are tested at device frequency limits; however, the CLKOUT prescaler is set to divide by one. This parameter is periodically sampled and not 100% tested.

2: Design guidance only, not tested.

FIGURE 13 : START-OF-FRAME PIN AC CHARACTERISTICS

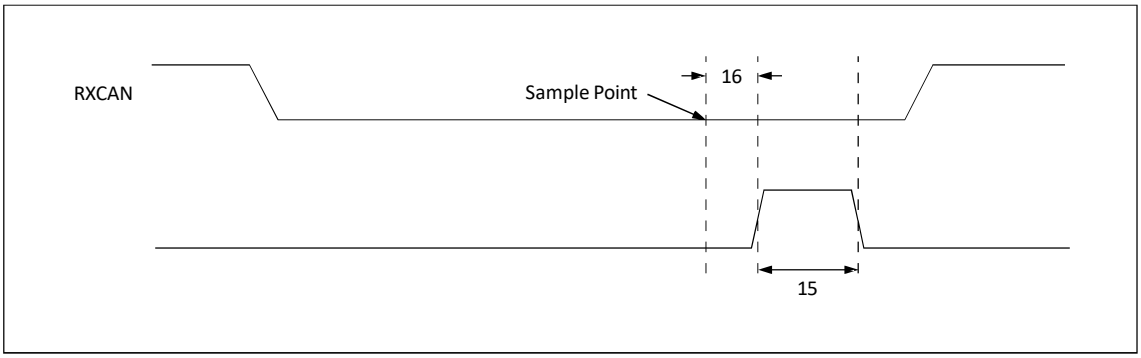


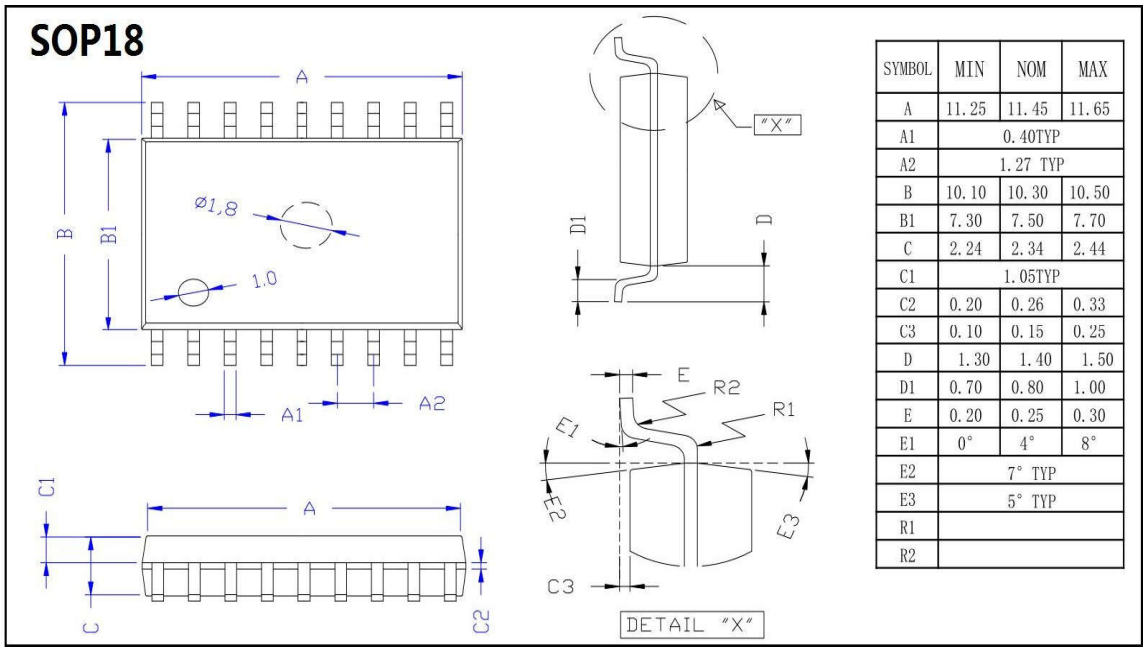
TABLE 8 : SPI INTERFACE AC CHARACTERISTICS

SPI Interface AC Characteristics			**V_{DD} = 2.7V to 5.5V**		**Industrial (I):** T_{AMB} = -40°C to +85°C	
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
	F_{CLK}	Clock Frequency	—	10	MHz	
1	T_{CSS}	$\overline{CS}$ Setup Time	50	—	ns	
2	T_{CSH}	$\overline{CS}$ Hold Time	50	—	ns	
3	T_{CSD}	$\overline{CS}$ Disable Time	50	—	ns	
4	T_{SU}	Data Setup Time	10	—	ns	
5	T_{HD}	Data Hold Time	10	—	ns	
6	T_R	Clock Rise Time	—	2	µs	**Note 1**
7	T_F	Clock Fall Time	—	2	µs	**Note 1**
8	T_{HI}	Clock High Time	45	—	ns	
9	T_{LO}	Clock Low Time	45	—	ns	
10	T_{CLD}	Clock Delay Time	50	—	ns	
11	T_{CLE}	Clock Enable Time	50	—	ns	
12	T_V	Output Valid from Clock Low	—	45	ns	
13	T_{HO}	Output Hold Time	0	—	ns	
14	T_{DIS}	Output Disable Time	—	100	ns	

Note 1 : This parameter is not 100% tested.

11. PACKAGING INFORMATION

FIGURE 14 : SOP18(300mil) Package outline dimensions



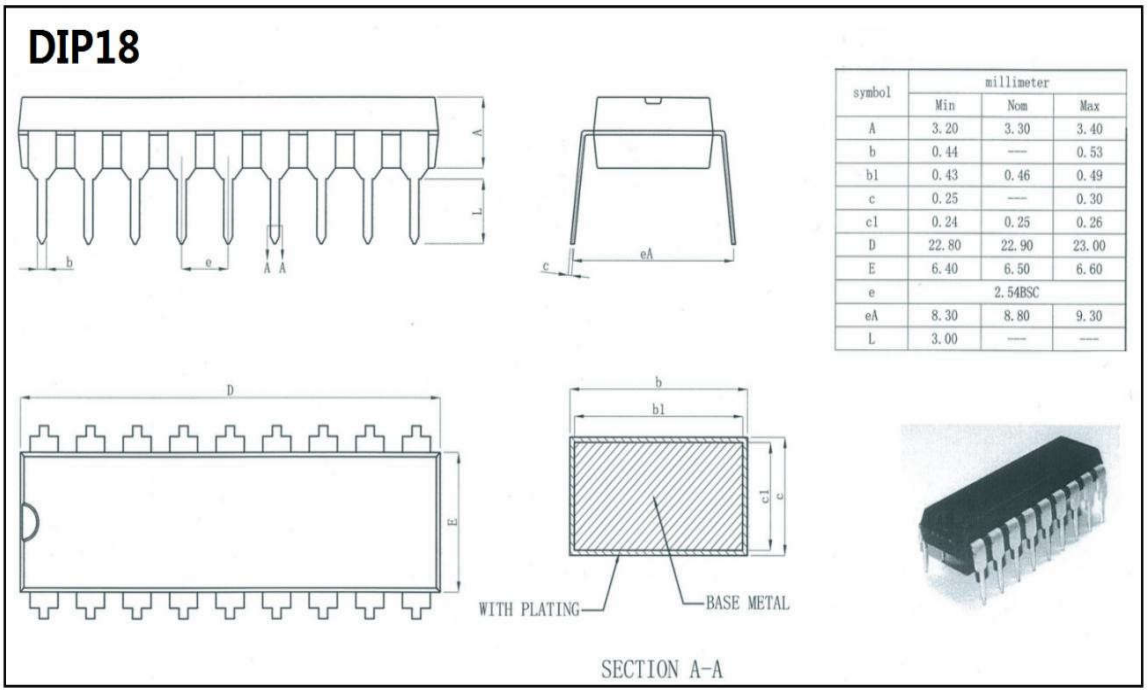
SYMBOL	MIN	NOM	MAX
A	11.25	11.45	11.65
A1		0.40TYP	
A2		1.27 TYP	
B	10.10	10.30	10.50
B1	7.30	7.50	7.70
C	2.24	2.34	2.44
C1		1.05TYP	
C2	0.20	0.26	0.33
C3	0.10	0.15	0.25
D	1.30	1.40	1.50
D1	0.70	0.80	1.00
E	0.20	0.25	0.30
E1	0°	4°	8°
E2		7° TYP	
E3		5° TYP	
R1			
R2			

Unit		Inch			mm		
Size Range		Min	Normal	Max	Min	Normal	Max
Number of Pin	n		18			18	
Pin spacing	p		.050			1.27	
Total height	A	.093	.099	.104	2.36	2.50	2.64
Moulded package thickness	A2	.088	.091	.094	2.24	2.31	2.39
Overhang clearance §	A1	.004	.008	.012	0.10	0.20	0.30
Total width	E	.394	.407	.420	10.01	10.34	10.67
Plastic moulded package width	E1	.291	.295	.299	7.39	7.49	7.59
Total length	D	.446	.454	.462	11.33	11.53	11.73
Inverted projection distance	h	.010	.020	.029	0.25	0.50	0.74
Foot length	L	.016	.033	.050	0.41	0.84	1.27
Angle of inclination of the foot	φ	0	4	8	0	4	8
Pin thickness	c	.009	.011	.012	0.23	0.27	0.30
Pin width	B	.014	.017	.020	0.36	0.42	0.51
Module tip taper	α	0	12	15	0	12	15
Taper at the bottom of the module	β	0	12	15	0	12	15

NOTES:

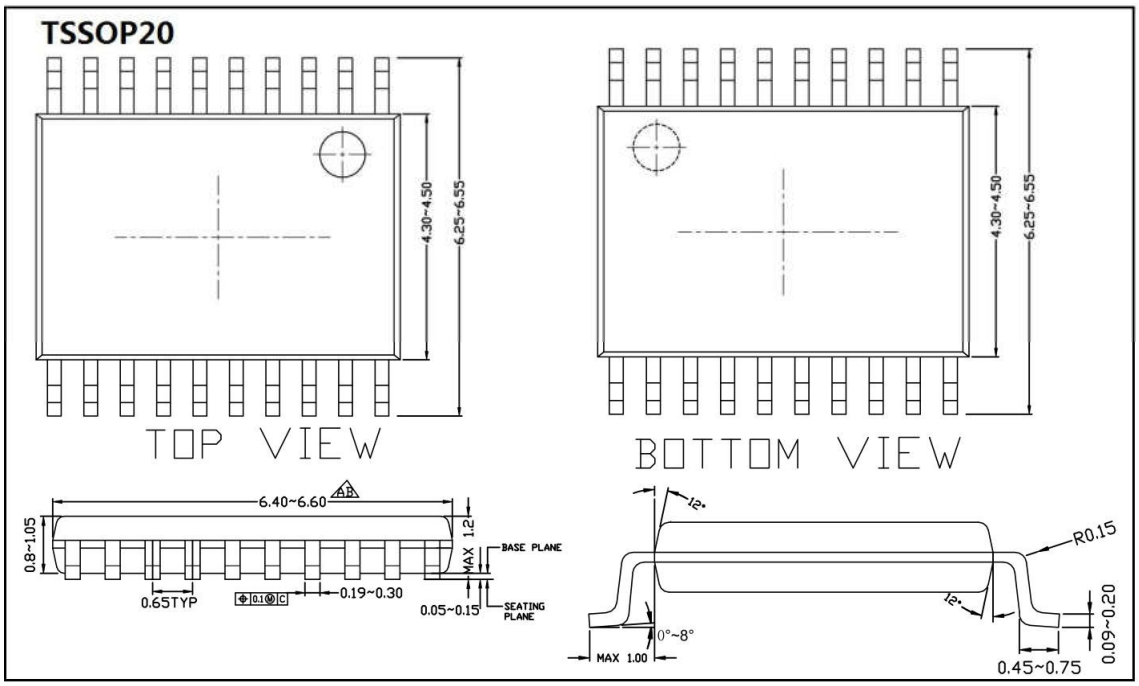
DIMENSIONS D AND E1 DO NOT INCLUDE RAW EDGES AND PROTRUSIONS OF THE MOULD. BURRS OR PROTRUSIONS ON EACH SIDE OF THE MOULD MUST NOT EXCEED 0.010" (0.254MM).

FIGURE 15 : DIP8 Package dimensions



symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	---	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	22.80	22.90	23.00
E	6.40	6.50	6.60
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	---	---

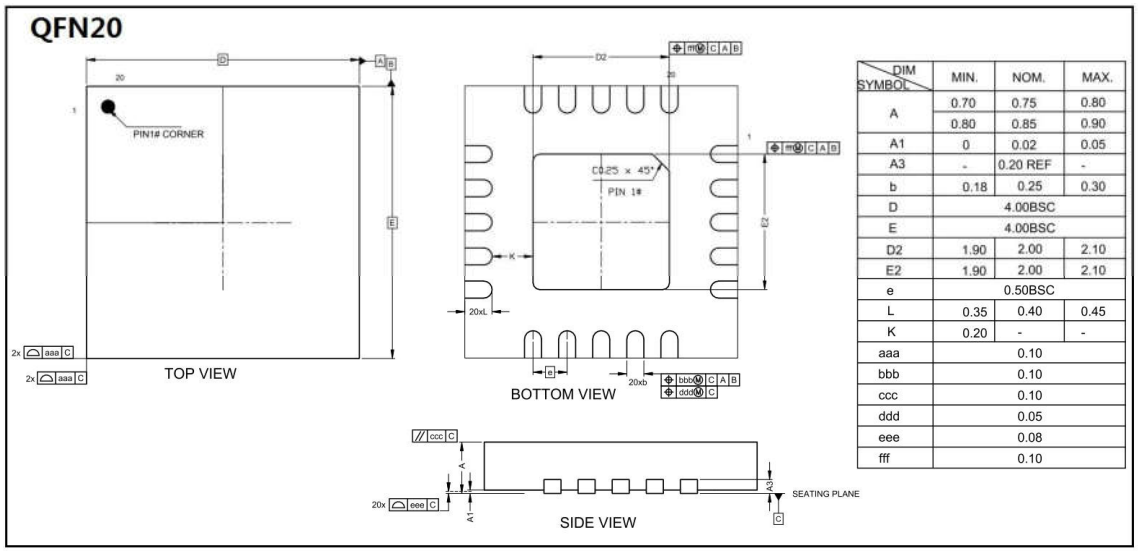
FIGURE 16 : TSSOP20 Package dimensions



NOTES:

1) LEAD FRAME : C7025 (THICKNESS : 0.127MM)
2) LEAD FINISH : SOLDER PLATED
3) BOTH PACKAGE LENGTH AND WDTHDO NOTINCLUDE FLASH.
4) FORMED LEAD SHALL BE PLANAR WITH RESPECTTRO ONE ANOTHER WITHIN 0.10(0.004)
5) CONTROLLING DIMENSION : MM
6) UNREMOVED FLASH BETWEEN LEADS&PACKAGE END FLASH SHALLNOT EXCEED 0.15MM FROM BOTTOM BODY PERSIDE.
7) EDP PACKAGE: EXPOSED PAD SIZE P1&P2 ARE VARIATIONSDEPENDING ON DEVCE FUNCTION (DIE PADDLE SIZE).

FIGURE 17 : QFN20 Package dimensions



DIM / SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
	0.80	0.85	0.90
A1	0	0.02	0.05
A3	-	0.20 REF	-
b	0.18	0.25	0.30
D		4.00BSC	
E		4.00BSC	
D2	1.90	2.00	2.10
E2	1.90	2.00	2.10
e		0.50BSC	
L	0.35	0.40	0.45
K	0.20	-	-
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

NOTES:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220
5) DRAWING IS NOT TO SCALE.

12. ORDERING INFORMATION

Ordering Information							
Part Number	**Device Marking**	**Package type**	**Body size(mm)**	**Temperature (℃)**	**MSL**	**Transport Media**	**Package Quantity**
XD2515	XD2515	DIP18	22.90*6.50	-40 to + 85	MSL3	Tube 20	800
XL2515	XL2515	SOP18	11.53*7.49	-40 to + 85	MSL3	T&R	1000
XL2515-TSS	XL2515-TSS	TSSOP20	6.5*4.4	-40 to + 85	MSL3	T&R	2500
XL2515QF20	XL2515QF20	QFN20	4.0*4.0	-40 to + 85	MSL3	T&R	3300

13. REVISION HISTORY

Revision	Date	Description of Change
V1.0	2019/10/1	Initial Release
V1.1	2024/8/27	Update package dimensions（FIGURE 14 ~ 17）

[if you need help contact us. XINLUDA reserves the right to change the above information without prior notice.]