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Stable 6MHz, Low Cost Dual Op Amp

Features

- **Stable 6 MHz GBWP in V_{CM} from 0-V to V_{DD}**
- **Excellent EMI Suppress Performance**
- **Offset Voltage: ±400 μV Maximum**
- **Offset Voltage Temperature Drift: 1 μV/°C**
- **Input Bias Current: 1 pA Typical**
- **THD+Noise: -115 dB at 1kHz, -99 dB at 10kHz**
- **High CMRR/PSRR: 110/95 dB**
- **Beyond the Rails Input Common-Mode Range**
- **Outputs Swing to within 3 mV of Each Rail**
- **No Phase Reversal for Overdriven Inputs**
- **High Output Capability: 100mA**
- **Supply Voltage Range:**
  - **Single +2.1 V to +6.0 V Supply**
  - **Or Dual ±1.05 V to ±3.0 V Supplies**
- **–40°C to 125°C Operation Temperature Range**
- **ESD Rating: 8KV – HBM, 2KV–CDM and 500V–MM**
- **Green, Popular Type Package**

Applications

- Multimedia Audio
- Headphone Drivers
- LCD Drivers
- Photo Diode Pre-amp
- Medical Equipments
- Portable Devices
- ASIC Input or Output
- Sensor Interfaces

Description

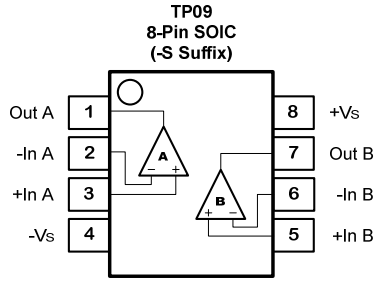
The TP09 is CMOS dual RRIO op-amp with low offset, low power and stable high frequency response. They incorporate 3PEAK's proprietary and patented design techniques to achieve very good AC performance with 6MHz bandwidth, 4.5V/μs slew rate and low distortion while drawing only 500μA of quiescent current per amplifier. The input common-mode voltage range extends 300mV beyond V– and V+, and the outputs swing rail-to-rail. The TP09 can be used as plug-in replacements for many commercially available op-amps to reduce power and improve input/output range and performance.

The TP09 Op-amp is unity gain stable with any capacitive load. They operate from either single +2.1V to +6.0V supply or dual ±1.05V to ±3.0V supplies. Analog trim and calibration routine reduce input offset voltage to below 400μV, and proprietary precision temperature compensation technique makes offset voltage temperature drift at 1μV/°C. Adaptive biasing and dynamic compensation enables the TP09 to achieve 'THD +Noise' for 1kHz/10kHz $2V_{PP}$ signal at -115dB/ -99dB. Beyond the rails input and rail-to-rail output characteristics allow the full power-supply voltage to be used for signal range.

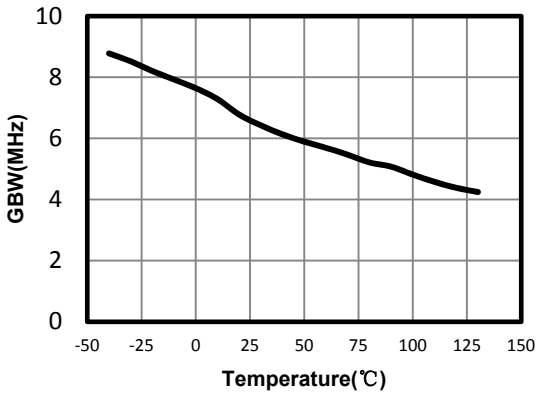
The combination of features makes the TP09 ideal choices for audio amplification of computers, sound ports, and other consumer Audio. The TP09 Op-amp is very stable, and it is capable of driving heavy capacitive loads such as those found in LCDs. The ability to swing rail-to-rail at the inputs and outputs enables designers to buffer CMOS DACs, ASICs, or other wide output swing devices in single-supply systems.

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Pin Configuration (Top View)



Unity Gain Bandwidth vs. Temperature



Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ – V^–$.....7.0V
Input Voltage..... $V^–$ – 0.3 to V^+ + 0.3
Input Current: +IN, –IN, SHDN Note 2..... ±20mA
SHDN Pin Voltage……$V^–$ to V^+
Output Current: OUT.....±100mA

Output Short-Circuit Duration Note 3…..... Infinite
Operating Temperature Range.....–40°C to 125°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	8	kV
MM	Machine Model ESD	JEDEC-EIA/JESD22-A115	500	V
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TP09	TP09-SR	8-Pin SOIC	Tape and Reel, 4000	TP09

Electrical Characteristics

The specifications are at T_A = 27°C. V_S = +2.1 V to +6.0 V, or ±1.05 V to ±3.0 V, R_L = 2kΩ, C_L =100pF.Unless otherwise noted.

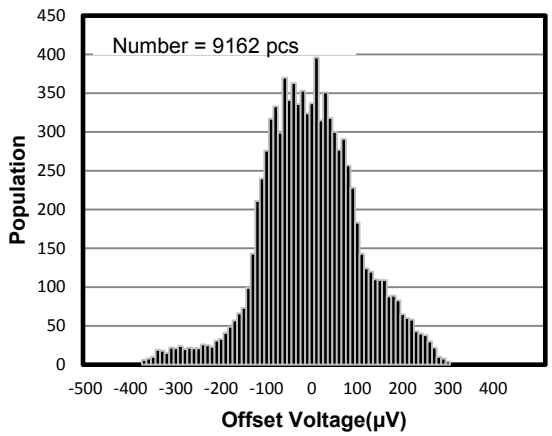
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V_{ss}+0.1V	-400	±50	+400	μV
V_{OS} TC	Input Offset Voltage Drift	-40°C to 125°C		1	2	μV/°C
I_B	Input Bias Current	T_A = 27 °C		1	10	pA
		T_A = 85 °C		25		pA
I_{OS}	Input Offset Current			0.001		pA
V_n	Input Voltage Noise	f = 0.1Hz to 10Hz		8		μV_{PP}
e_n	Input Voltage Noise Density	f = 1kHz		19		nV/√Hz
i_n	Input Current Noise	f = 1kHz		2		fA/√Hz
C_{IN}	Input Capacitance	Differential Common Mode		7.76 6.87		pF
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 2.5V	90	110		dB
V_{CM}	Common-mode Input Voltage Range		V^- -0.1		V^+-0.1	V
PSRR	Power Supply Rejection Ratio	V_{CM} = 0V, V_S = 3V to 5V	80	95		dB
A_{VOL}	Open-Loop Large Signal Gain	R_{LOAD} = 10kΩ	95	105		dB
V_{OL}, V_{OH}	Output Swing from Supply Rail	R_{LOAD} = 10kΩ		3	6	mV
R_{OUT}	Closed-Loop Output Impedance	G = 1, f =1kHz, I_{OUT} = 0		0.024		Ω
I_{SC}	Output Short-Circuit Current	Sink or source current	90	100		mA
I_O	Output Current	Sink or source current, Output 1V Drop		50		mA
V_{DD}	Supply Voltage		2.1		6.0	V
I_Q	Quiescent Current per Amplifier	V_S = 5V		500	800	μA
PM	Phase Margin	R_{LOAD} = 1kΩ, C_{LOAD} = 60pF		60		°
GM	Gain Margin	R_{LOAD} = 1kΩ, C_{LOAD} = 60pF		15		dB
GBWP	Gain-Bandwidth Product	f = 1kHz		6		MHz
SR	Slew Rate	AV = 1, V_{OUT} = 1.5V to 3.5V, C_{LOAD} = 60pF, R_{LOAD} = 1kΩ	3.6	4.5		V/μs
FPBW	Full Power Bandwidth Note 1			280		kHz
t_S	Settling Time, 0.1% Settling Time, 0.01%	A_V = –1, 1V Step		8.5 9.5		μs
THD+N	Total Harmonic Distortion and Noise	f = 1kHz, AV =1, RL = 2kΩ, VOUT = 1Vp-p		0.0003		%
X_{talk}	Channel Separation	f = 1kHz, R_L = 2kΩ		110		dB

Note 1: Full power bandwidth is calculated from the slew rate FPBW = SR/π • V_{P-P}

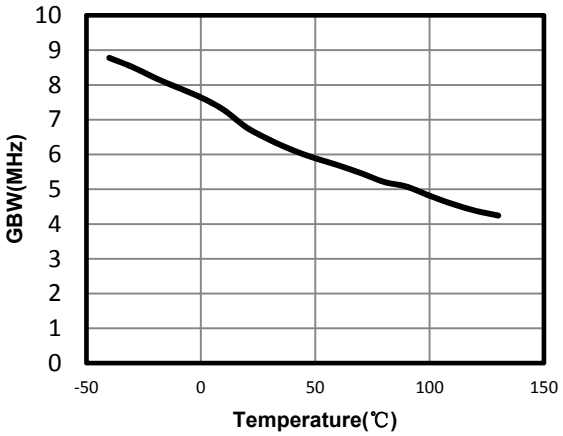
Typical Performance Characteristics

V_S = ±2.75V, V_{CM} = 0V, R_L = Open, unless otherwise specified.

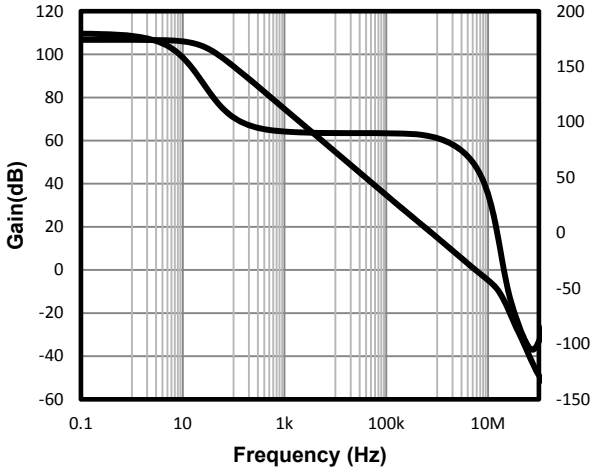
Offset Voltage Production Distribution



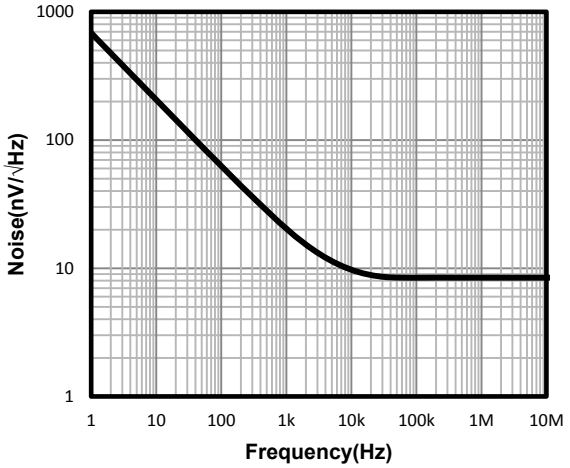
Unity Gain Bandwidth vs. Temperature



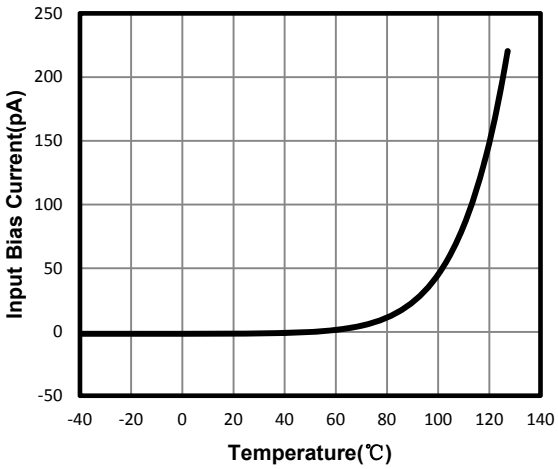
Open-Loop Gain and Phase



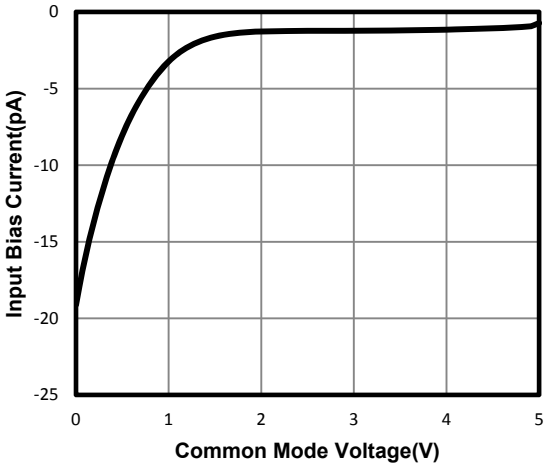
Input Voltage Noise Spectral Density



Input Bias Current vs. Temperature



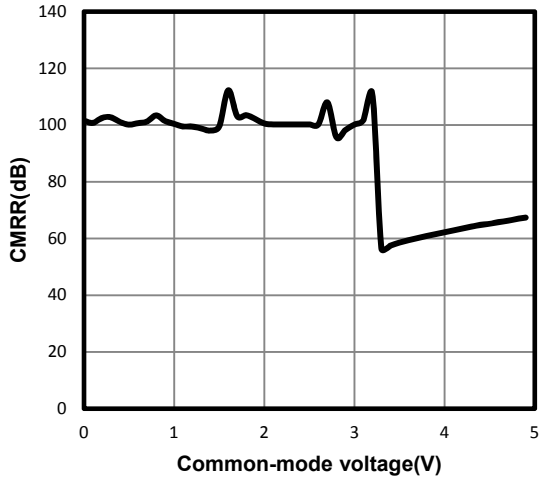
Input Bias Current vs. Input Common Mode Voltage



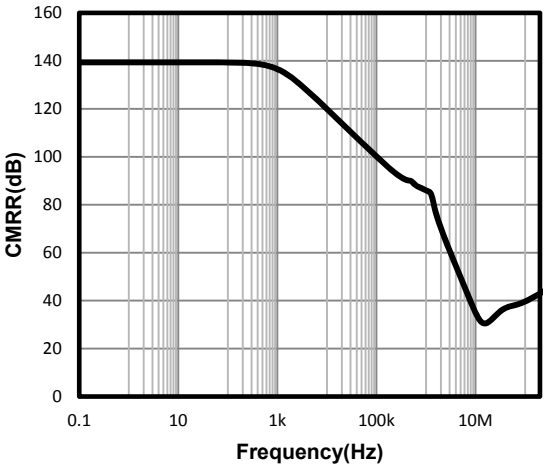
Typical Performance Characteristics

V_S = ±2.75V, V_{CM} = 0V, R_L = Open, unless otherwise specified. (Continued)

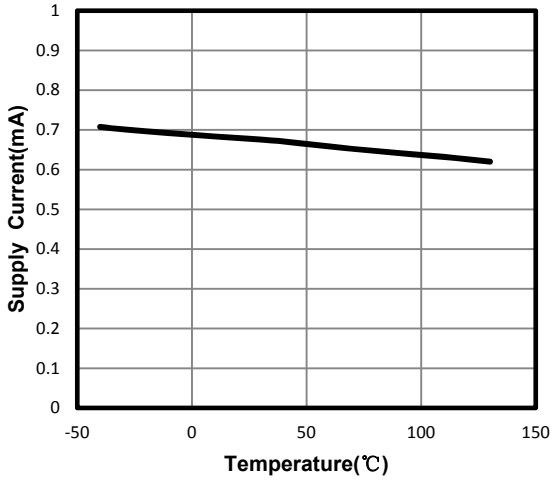
Common Mode Rejection Ratio



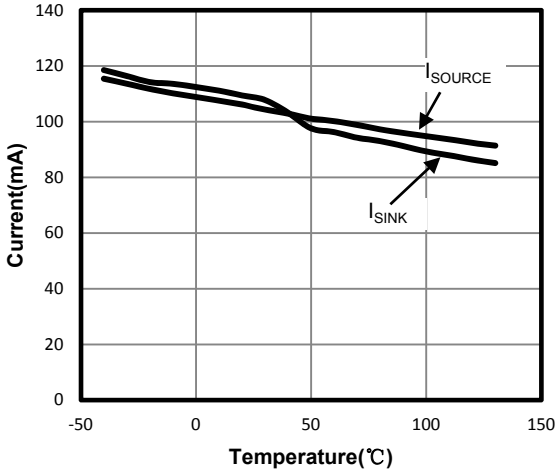
CMRR vs. Frequency



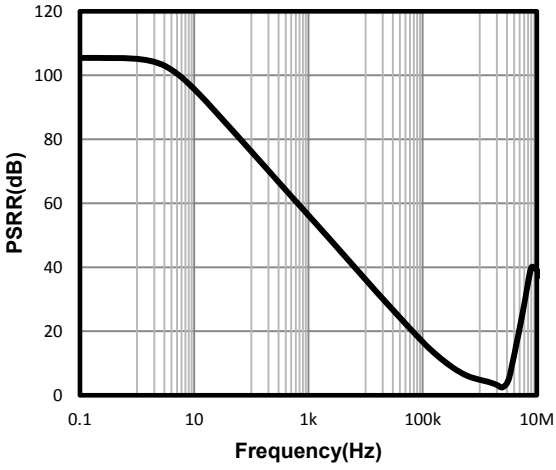
Quiescent Current vs. Temperature



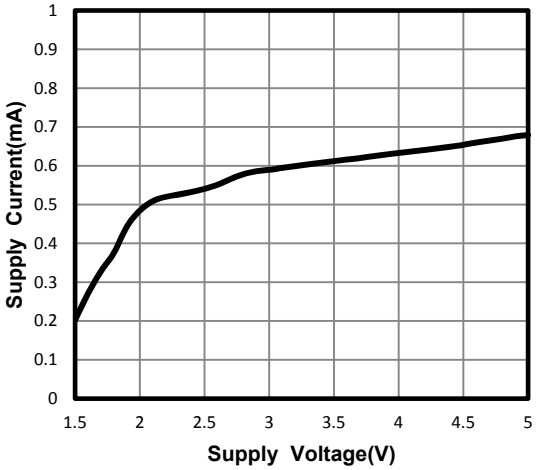
Short Circuit Current vs. Temperature



Power-Supply Rejection Ratio



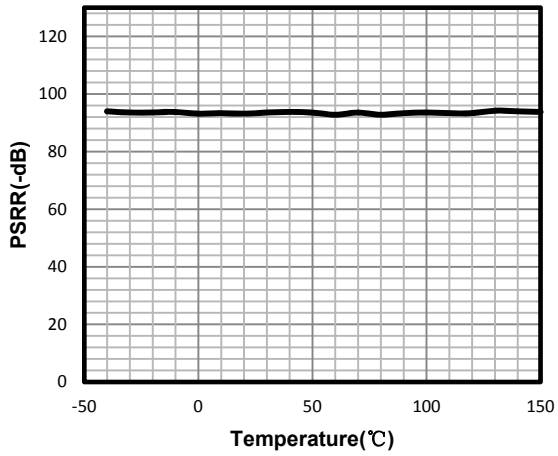
Quiescent Current vs. Supply Voltage



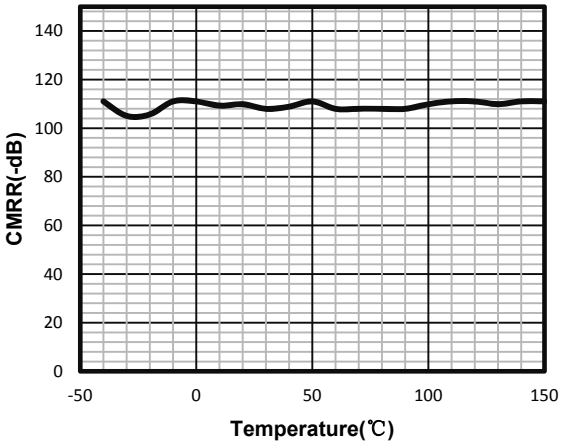
Typical Performance Characteristics

V_S = ±2.75V, V_{CM} = 0V, R_L = Open, unless otherwise specified. (Continued)

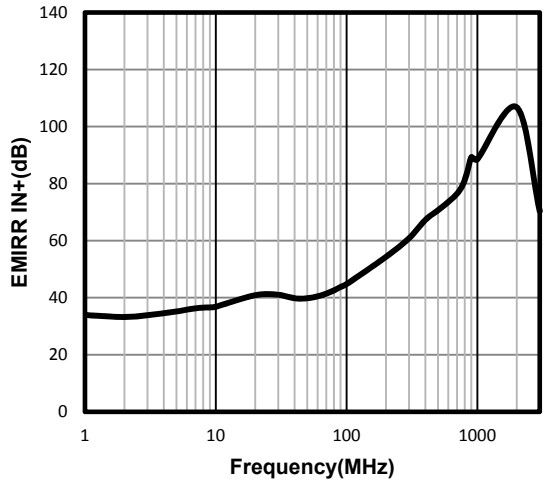
PSRR vs. Temperature



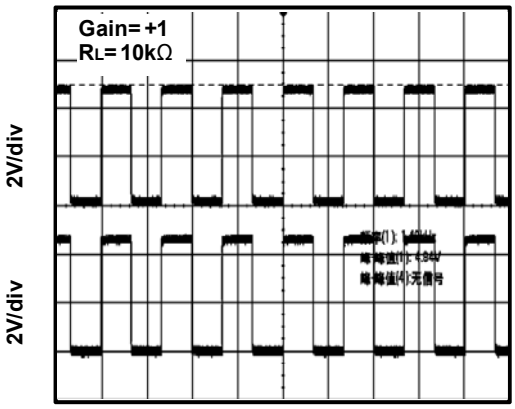
CMRR vs. Temperature



EMIRR IN+ vs. Frequency

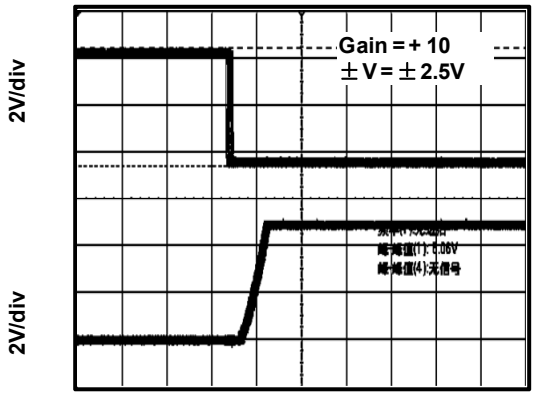


Large-Scale Step Response



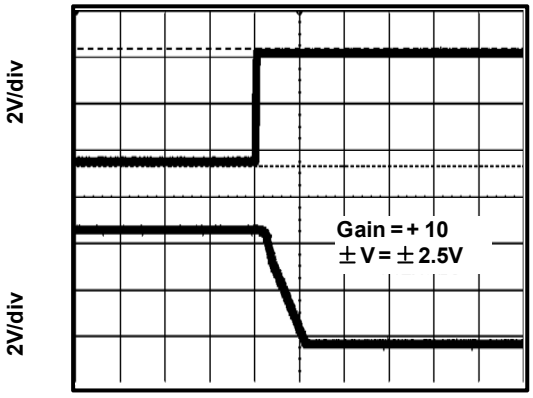
Time (500μs/div)

Negative Over-Voltage Recovery



Time (2μs/div)

Positive Over-Voltage Recovery

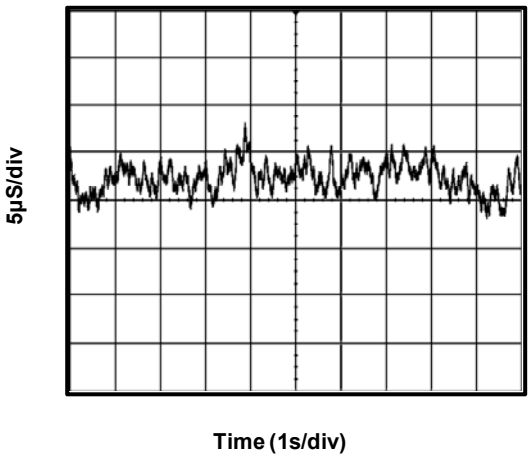


Time (1μs/div)

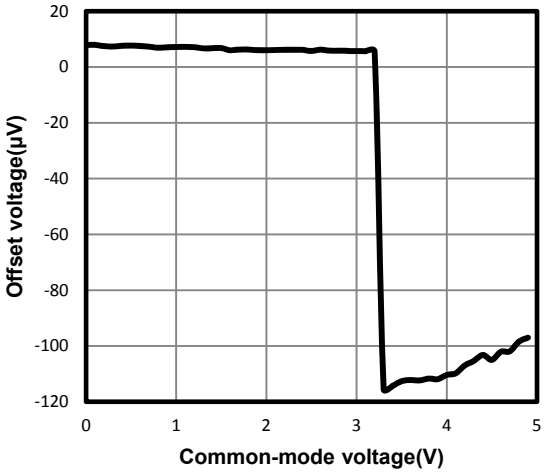
Typical Performance Characteristics

V_S = ±2.75V, V_{CM} = 0V, R_L = Open, unless otherwise specified. (Continued)

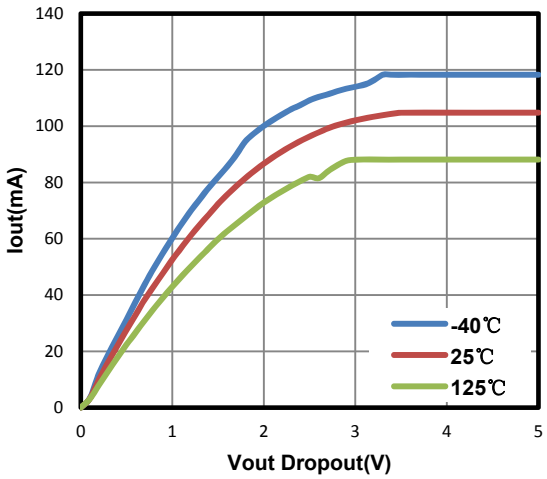
0.1 Hz TO 10 Hz Input Voltage Noise



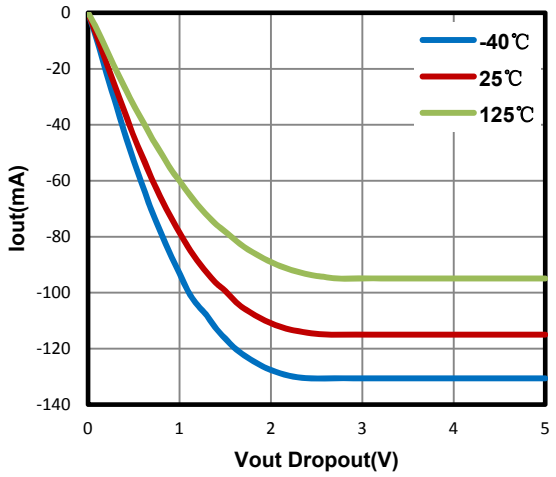
Offset Voltage vs Common-Mode Voltage



Positive Output Swing vs. Load Current



Negative Output Swing vs. Load Current



Pin Functions

–IN: Inverting Input of the Amplifier. Voltage range of this pin can go from V^- – 0.3V to V^+ + 0.3V.

+IN: Non-Inverting Input of Amplifier. This pin has the same voltage range as –IN.

+V_S: Positive Power Supply. Typically the voltage is from 2.1V to 6V. Split supplies are possible as long as the voltage between V+ and V– is between 2.1V and 6V. A bypass capacitor of 0.1μF as close to the part as possible should be used between power supply pins or between supply pins and ground.

N/C: No Connection.

-V_S: Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V^+ and V^- is from 2.1V to 6V. If it is not connected to ground, bypass it with a capacitor of 0.1μF as close to the part as possible.

OUT: Amplifier Output. The voltage range extends to within millivolts of each supply rail.

Operation

The TP09 input signal range extends beyond the negative and positive power supplies. The output can even extend all the way to the negative supply. The input stage is comprised of two CMOS differential amplifiers, a PMOS stage and NMOS stage that are active over different ranges of common mode input voltage. The Class-AB control buffer and output bias stage uses a proprietary compensation technique to take full advantage of the process technology to drive very high capacitive loads. This is evident from the transient over shoot measurement plots in the Typical Performance Characteristics.

Applications Information

Low Supply Voltage and Low Power Consumption

The TP09 of operational amplifier can operate with power supply voltages from 2.1 V to 6.0 V. Each amplifier draws only 500 μA quiescent current. The low supply voltage capability and low supply current are ideal for portable applications demanding high capacitive load driving capability and stable wide bandwidth. The TP09 is optimized for wide bandwidth low power applications. They have an industry leading high GBWP to power ratio and are unity gain stable for any capacitive load. When the load capacitance increases, the increased capacitance at the output pushed the non-dominant pole to lower frequency in the open loop frequency response, lowering the phase and gain margin. Higher gain configurations tend to have better capacitive drive capability than lower gain configurations due to lower closed loop bandwidth and hence higher phase margin.

Low Input Referred Noise

The TP09 provides a low input referred noise density of 19 nV/ √ Hz at 1 kHz. The voltage noise will grow slowly with the frequency in wideband range, and the input voltage noise is typically 8 μV_{P-P} at the frequency of 0.1 Hz to 10 Hz.

Low Input Offset Voltage

The TP09 has a low offset voltage of 400 μV maximum which is essential for precision applications. The offset voltage is trimmed with a proprietary trim algorithm to ensure low offset voltage for precision signal processing requirement.

Low Input Bias Current

The TP09 is a CMOS OPA family and features very low input bias current in pA range. The low input bias current allows the amplifiers to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on “PCB Surface Leakage” for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is 10^{12} Ω. A 5 V difference would cause 5 pA of current to flow, which is greater than the TP09 OPA's input bias current at +27°C (±1pA, typical). It is recommended to use multi-layer PCB layout and route the OPA's -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 1 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the Common Mode input voltage.
2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op-amp (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

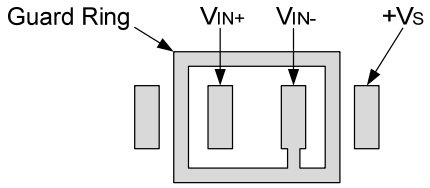


Figure 1

Ground Sensing and Rail to Rail Output

The TP09 has excellent output drive capability, delivering over 100 mA of output drive current. The output stage is a rail-to-rail topology that is capable of swinging to within 10mV of either rail. Since the inputs can go 300 mV beyond either rail, the op-amp can easily perform 'true ground' sensing.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

ESD

The TP09 has reverse-biased ESD protection diodes on all inputs and output. Input and out pins can not be biased more than 300 mV beyond either supply rail.

Feedback Components and Suppression of Ringing

Care should be taken to ensure that the pole formed by the feedback resistors and the parasitic capacitance at the inverting input does not degrade stability. For example, in a gain of +2 configuration with gain and feedback resistors of 10k, a poorly designed circuit board layout with parasitic capacitance of 5 pF (part +PC board) at the amplifier's inverting input will cause the amplifier to ring due to a pole formed at 8.1 MHz. An additional capacitor of 5 pF across the feedback resistor as shown in Figure 2 will eliminate any ringing.

Careful layout is extremely important because low power signal conditioning applications demand high-impedance circuits. The layout should also minimize stray capacitance at the OPA's inputs. However some stray capacitance may be unavoidable and it may be necessary to add a 2 pF to 10 pF capacitor across the feedback resistor. Select the smallest capacitor value that ensures stability.

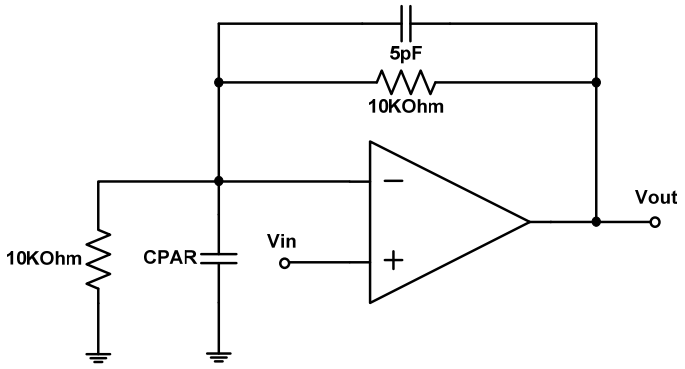


Figure 2

Shut-down

The single channel OPA versions have SHDN pins that can shut down the amplifier to less than 0.2 μA supply current. The SHDN pin voltage needs to be within 0.5 V of V– for the amplifier to shut down. During shutdown, the output will be in high output resistance state, which is suitable for multiplexer applications. When left floating, the SHDN pin is internally pulled up to the positive supply and the amplifier remains enabled.

Driving Large Capacitive Load

The TP09 of OPA is designed to drive large capacitive loads. Refer to Typical Performance Characteristics for "Phase Margin vs. Load Capacitance". As always, larger load capacitance decreases overall phase margin in a feedback system where internal frequency compensation is utilized. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in output step response. The unity-gain buffer (G = +1V/V) is the most sensitive to large capacitive loads.

When driving large capacitive loads with the TP09 OPA family (e.g., > 200 pF when G = +1V/V), a small series resistor at the output (R_{ISO} in Figure 3) improves the feedback loop's phase margin and stability by making the output load resistive at higher frequencies.

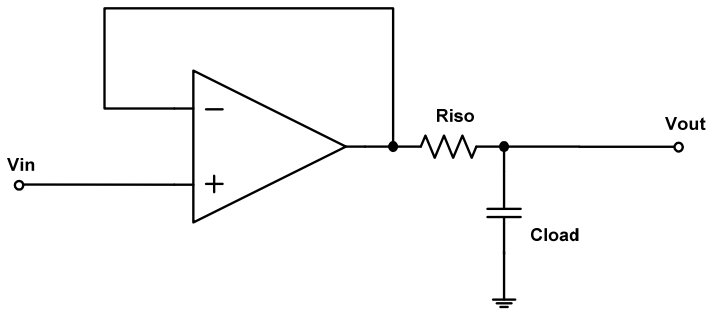


Figure 3

Power Supply Layout and Bypass

The TP09 OPA's power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 μF to 0.1 μF) within 2 mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA's inputs and outputs. To decrease stray capacitance, minimize PC board lengths and resistor leads, and place external components as close to the op amps' pins as possible.

Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be

connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

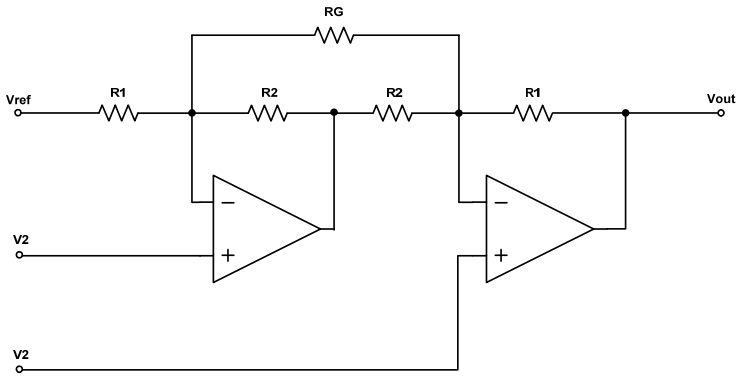
A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

Instrumentation Amplifier

The TP09 op-amp series is well suited for conditioning sensor signals in battery-powered applications. Figure 4 shows a two op-amp instrumentation amplifier, using the TP09 op-amp.

The circuit works well for applications requiring rejection of Common Mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single voltage supply applications, V_{REF} is typically $V_{DD}/2$.



$$V_{OUT}=(V_1-V_2)(1+\frac{R_1}{R_2}+\frac{2R_1}{R_G})+V_{REF}$$

Figure 4

Gain-of-100 Amplifier Circuit

Figure 5 shows a Gain-of-100 amplifier circuit using two TP09 op-amp. It draws 500 uA total current from supply rail, and has a -3dB frequency at 100kHz.

Figure 6 shows the small signal frequency response of the circuit.

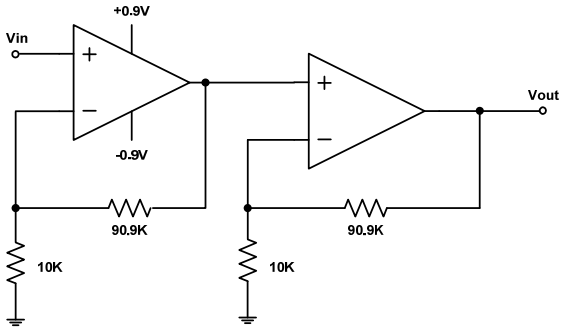


Figure 5: 100kHz, 500μA Gain-of-100 Amplifier

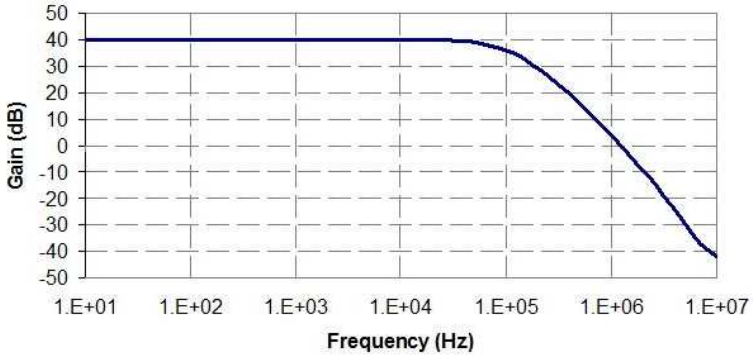
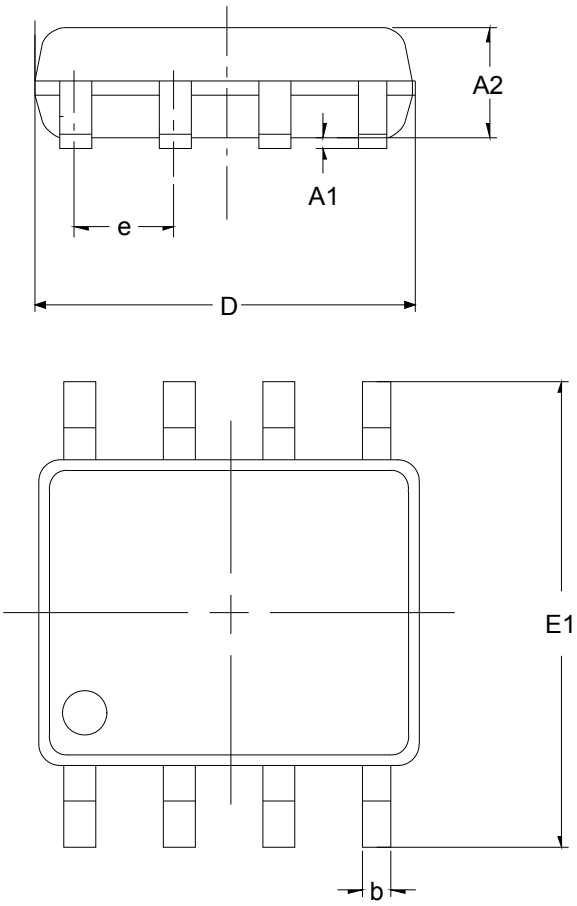


Figure 6: Frequency response of 100kHz, 500uA Gain-of-100 Amplifier

Package Outline Dimensions

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270 TYP		0.050 TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°