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AS608 Processor Datasheet

Version 1.00, September 2015

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Previous Versions

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		Chapter	Revised by	Description
1.00	2015-09-29	All	Coins	Initial version, font marked as red to be tested

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Abbreviations and Terms

SCM : System Control Module

GPIO : General Purpose Input/Output

SPI : Serial Peripheral Interface

I2C : Inter-integrated Circuit

UART : Universal Asynchronous Receiver/Transmitter

USB : Universal Serial Bus

BVD : Battery Voltage Detector

SQI : Serial Quad Interface

SEA : Symmetric encryption algorithm

AEA : Asymmetric encryption algorithm

EFC : Embedded Flash Controller

TRNG : True Random Number Generator

ACMP : Analog Comparator

SCI : Smart Card Interface

VPWM : Voice Pulse Width Modulation Interface

T0 : Timer 0

T1 : Timer 1

BOD : Brown Out Detection

SSI : Slave-synchronous Serial Interface

1 Introduction

AS608 series is a high-performance 32-bit micro-processor based on ARM Cortex-M developed by Synochip. The chip integrates 4KB Cache, with working frequency of 144MHz, 512KB embedded Flash, 128KB SRAM and extendible external SQI Flash up to 16MB. With MPU protection, the embedded Flash can effectively secure user code.

AS608 series has abundant on-chip peripherals, 1 USB2.0 full-speed Device, 2 SPI (master), 1 SPI (slave), 2 UART, 1 I2C, 1 LOCSC, 1 SCI, 1 VPWM, up to 48 GPIO, and each one of the GPIO is interrupt available.

AS608 series has embedded with multiple encryption and decryption algorithms, it supports DES, AES, RSA, ECC and many different HASH algorithms.

AS608 series adopts a design of analog-digital technology and internally integrates multiple functional analog modules to reduce peripheral circuit and board level cost.

It internally integrates 3 LDO for power switchover: 1 LDO5033 for 5V to 3.3V, 1 LDO3318 for 3.3V to 1.8V, 1 LDO1812 for 1.8V to 1.2V. The LDOs power supply not only functional modules in the chip but also the peripheral circuits.

The chip internally integrates 2 ring oscillators: one is to output HFROSC up to 144MHz, the precision could be ±1.5% after factory calibration; another is to output LFROSC at 32KHz, available for CLK under SLEEP.

2 Overview of Configuration

AS608 series provides components of different packages, memory capacity and features, these components are described with different suffix as shown in Figure 2-1.

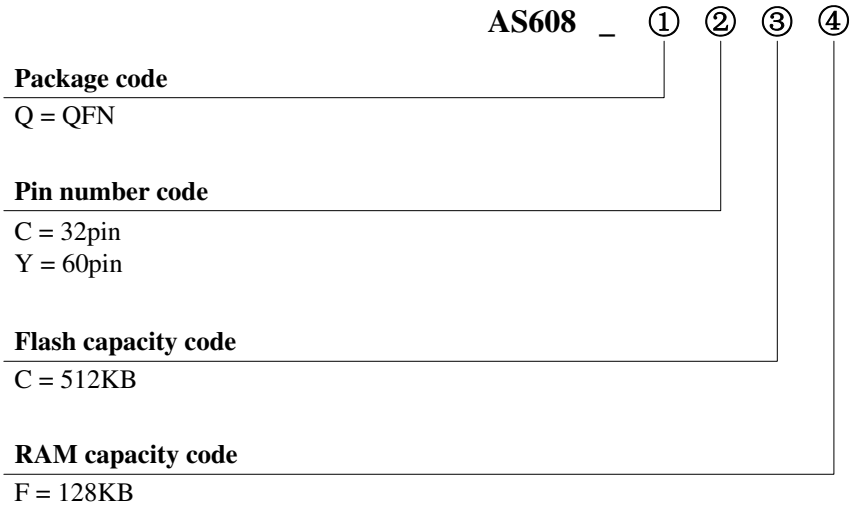


Figure 2-1 AS608 component type suffix

It lists different components' functions and configurations in Table 2-1.

Table 2-1 AS608 component configuration

Function	Component type	
	AS608_QYCF	AS608_QCCF
Flash (Kbytes)	512	512
SRAM (Kbytes)	128	128
Package	QFN60	QFN32
BOOT mode	USB SSI UART	USB SSI UART
GPIO no.	48	22
I2C	1	1
SPI	2	1(SPI0)
SSI	1	1
UART	2	1(UART0)
DMA	1	1
SCI	1	1
VPWM	1	0
CRC	1	1
TMR	3	3
LOCSC	1	1

Function	Component type	
	AS608_QYCF	AS608_QCCF
BVD	1	0
USB	1	1
SQI	1	0
TRNG	1	1
SEA	DES AES	DES AES
AEA	RSA ECC	RSA ECC
HASH	MD5 SHA-1 SHA-256	MD5 SHA-1 SHA-256

3 Application Fields

AS608_QYCF, a low-cost, low-consumption and high-performance 32-bit micro-controller designed for fingerprint security field by Synochip.

AS608_QYCF internally integrates 3 LDO with a design of interior ring oscillator, the LDOs power supply its peripheral circuits with suitable current, which dramatically simplifies the peripheral circuits. The chip integrates abundant peripherals, embeds with fingerprint unit and security element to meet demands of single-chip solutions in fingerprint security field. The in-chip 48KB execute-only memory can effectively secure user application programs or 3rd party algorithms.

AS608_QYCF main targeted markets:

- Fingerprint security applications
- Fingerprint single chip solutions

AS608_QCCF a low-cost, low-consumption and high-performance 32-bit micro-controller designed for fingerprint recognition field by Synochip. AS608_QCCF internally integrates 3 LDO with a design of interior ring oscillator, the LDOs power supply its peripheral circuits with suitable current, which dramatically simplifies the peripheral circuits. With the advantages of simple peripheral circuits, small size, low consumption and working with different kinds of sensor, the chip applies to fingerprint module applications.

AS608_QCCF main targeted market:

- Fingerprint module field

4 Main Features

- ARM Cortex M
  - 3-stage pipelines, branch prediction
  - Thumb-2 instruction set, excellent code density and memory footprint
  - 32-bit single cycle Multiplication
  - Low-latency interrupt response system
  - Low- consumption Sleep mode
  - 2-wire debugging interface
  - 24-bit SysTick integrated
- Interior memory
  - ROM: 16KB (non-programmable for users, BOOT and ISP download available only)
  - SRAM: 128KB
  - FLASH: 512KB
  - OTP: 1KB
- External memory interface/extension peripheral interface
  - SQI: Support single/dual/quad channel serial Flash, capacity up to 16MB
- Peripheral interface
  - USB 2.0 FS interface: support full-speed and low-speed mode
  - SPI x 2, I2C x 1, UART x 2
  - SSI x 1: Support Motorola SPI slave mode
  - LOCSC x 1: Support optical CMOS general interface
  - VPWM: Voice data PWM signal output available, support 8/16-bit audio source data
  - GPIO: up to 48, each GPIO is interrupt available
  - SCI x 1: ISO7816 (smart card) master interface
  - BVD x 1: 8-seg Battery Voltage Detection Controller
  - 32-bit Timer (except SysTick) x 3: WDT available
  - CRC16 verification: Support CRC-16 and CRC-CCITT
  - DMA x 1: Support peripherals incl. SSI, SPI, LOCSC and VPWM
  - True Random Number Generator, compatible with FIPS140-2
- Security Feature

- 32B unique serial number
- JTAG LOCK
- Test LOCK, test mode disabled permanently
- Self-destruction
- Symmetric Encryption Algorithm engine, support DES, 3DES, AES128\192\256
- Asymmetric Encryption Algorithm engine, support RSA1024/2048, ECC

✧ Power Feature

- Integrated 3.3V LDO, 5V power can be input from pin LDO5033_IN, 3.3V power output from LDO5033_OUT, support input voltage 4.0V~5.5V, output drive current up to 150mA, available to enable pin LDO5033_EN, active High
- Integrated 1.8V LDO, 3.3V power input from pin LDO3318_IN, 1.8V power output from LDO3318_OUT/LDO1812_IN for embedded Flash power supply, max. output current up to 150mA, support input voltage 3.0V~3.6V
- Integrated 1.2V LDO, 1.8V power input from pin LDO3318_OUT/LDO1812_IN, 1.2V power output from LDO1812_OUT/CORE_VDD for kernel power supply, max. output current up to 100mA
- Sleep consumption<200uA (DeepSleep, GPIO or other interrupt wake up available)
- Dynamic consumption < 25mA when master frequency is 144MHz

✧ Other Features

- On-chip POR/BOD, high-low voltage detection
- High-precision interior ring oscillator, factory calibration ±1.5%, USB dynamic calibration could be ±0.25%
- Dynamic frequency switchover available
- Sleep mode and interrupt wake up available
- Independent maskable interrupt
- Disable various peripheral CLK independently available
- Peripheral reset available

5 Block Diagram

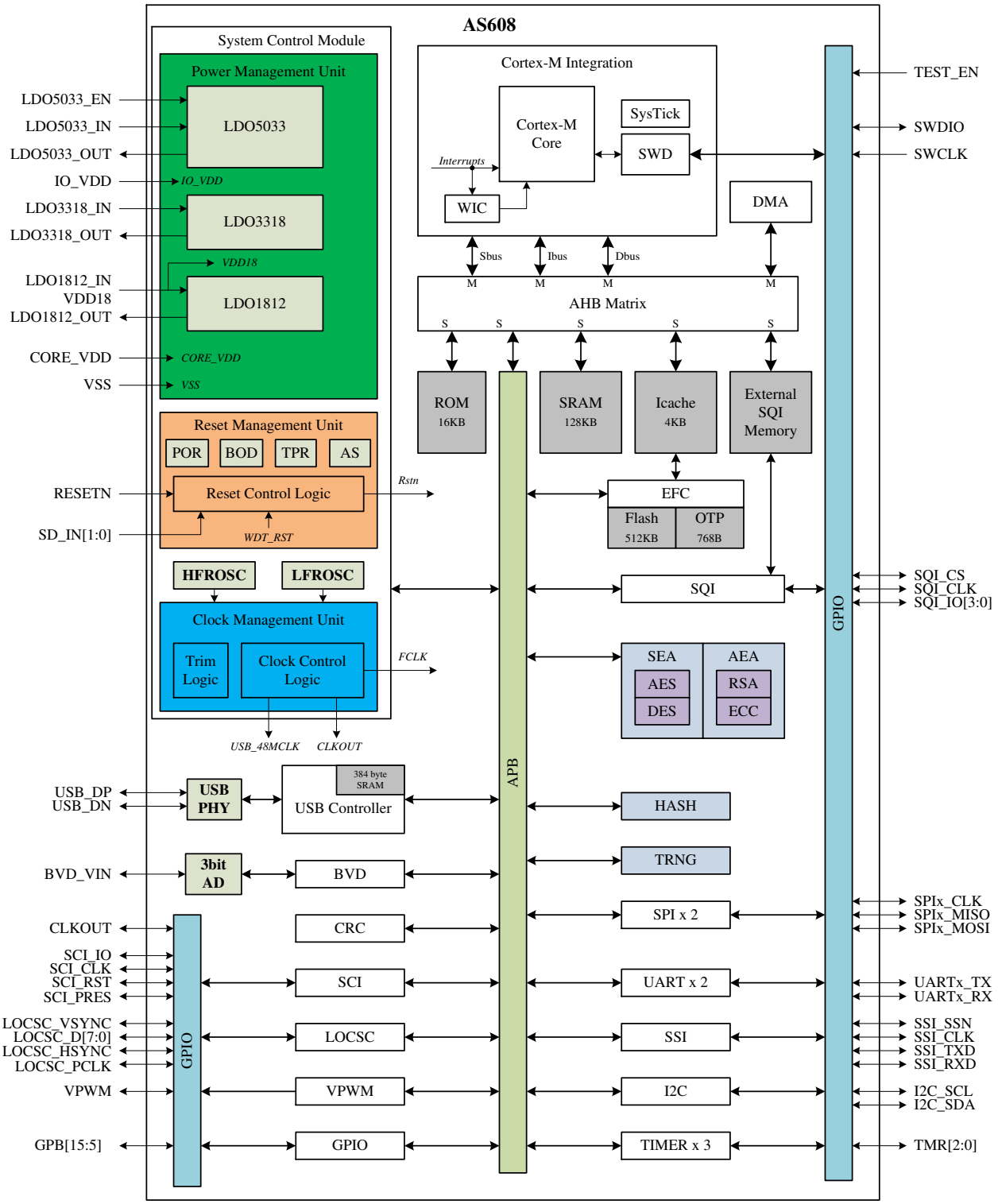


Figure 5-1 AS608 Block diagram

6 Package and Pin

6.1 Package

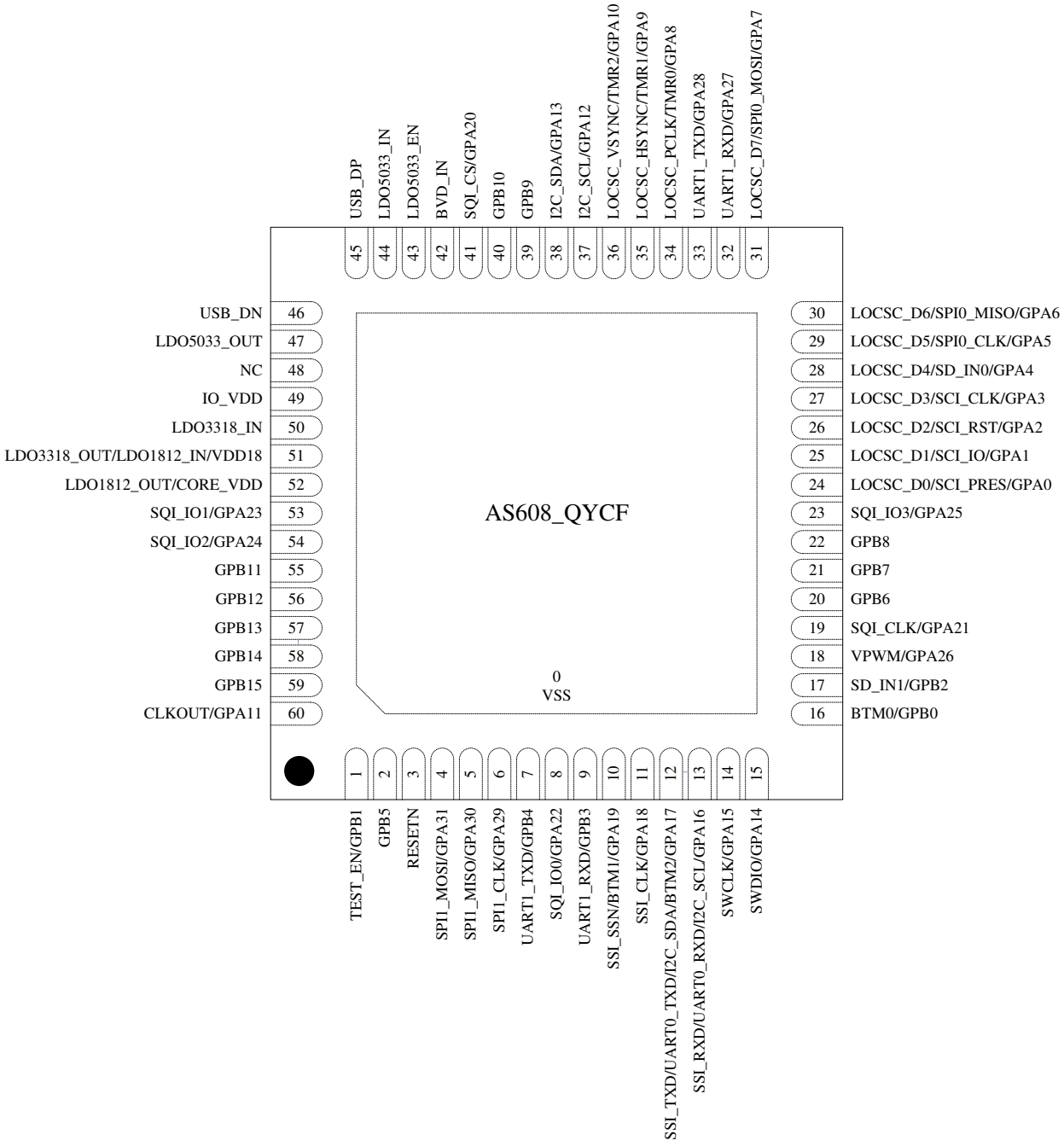


Figure 6-1 AS608_QYCF package

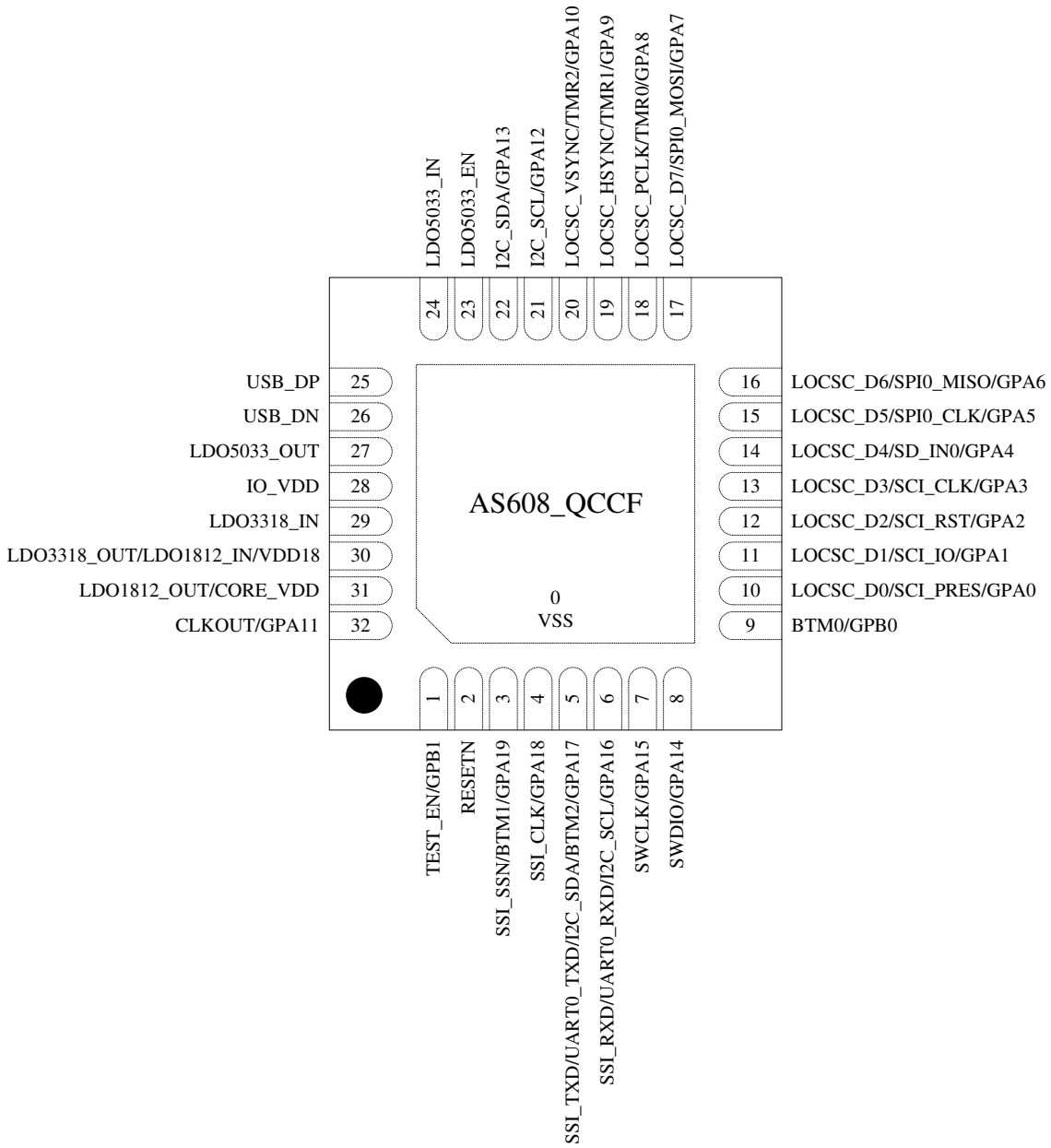


Figure 6-2 AS608_QCCF package

6.2 List of Pins

Table 6-1 List of AS608 pins

Pin No.		Pins	I/O	Description
AS608_QYCF	AS608_QCCF			
0	0	VSS	P	Ground

Pin No.		Pins	I/O	Description
AS608_QYCF	AS608_QCCF			
1	1	TEST_EN/GPB1	I	Enable test mode, while under normal operation, connect to pull-down (interior pull-down)
			I/O	GPIO port B1
2	--	GPB5	I/O	GPIO port B5
3	2	RESETN	I	External reset input, active Low (interior pull-up)
4	--	SPI1_MOSI/GPA31	I/O	SPI1 master output slave input signal
			I/O	GPIO port A31
5	--	SPI1_MISO/GPA30	I/O	SPI1 master input slave output signal
			I/O	GPIO port A30
6	--	SPI1_CLK/GPA29	I/O	SPI1 CLK
			I/O	GPIO port A29
7	--	UART1_TXD/GPB4	O	UART1 transfer data signal
			I/O	GPIO port B4
8	--	SQI_IO0/GPA22	I/O	SQI serial data0 (single channel SI)
			I/O	GPIO port A22
9	--	UART1_RXD/GPB3	O	UART1 receive data signal
			I/O	GPIO port B3
10	3	SSI_SSN/BTM1/GPA19	I	SSI chip select signal
			I	ROM Boot mode select 1
			I/O	GPIO port A19
11	4	SSI_CLK/GPA18	I	SSI CLK
			I/O	GPIO port A18
12	5	SSI_TXD/UART0_TXD/I2C_SDA/BTM2/ GPA17	O	SSI transfer data signal
			O	UART0 transfer data signal
			I/O	I2C serial data
			I	ROM Boot mode select 2
			I/O	GPIO port A17
13	6	SSI_RXD/UART0_RXD/I2C_SCL/GPA16	I	SSI receive data signal
			I	UART0 receive data signal
			I/O	I2C serial CLK
			I/O	GPIO port A16
14	7	SWCLK/GPA15	I	SW debugging port CLK input
			I/O	GPIO port A15
15	8	SWDIO/GPA14	I/O	SW debugging port data input/output
			I/O	GPIO port A14
16	9	BTM0/GPB0	I	ROM Boot mode select0
			I/O	GPIO port B0

Pin No.		Pins	I/O	Description
AS608_QYCF	AS608_QCCF			
17	--	SD_IN1/GPB2	I	Self-destruction input detection port 1
			I/O	GPIO port B2
18	--	VPWM/GPA26	O	Voice PWM output
			I/O	GPIO port A26
19	--	SQI_CLK/GPA21	O	SQI CLK output
			I/O	GPIO port A21
20	--	GPB6	I/O	GPIO port B6
21	--	GPB7	I/O	GPIO port B7
22	--	GPB8	I/O	GPIO port B8
23	--	SQI_IO3/GPA25	I/O	SQI data3 (single channel HOLD)
			I/O	GPIO port A25
24	10	LOCSC_D0/SCI_PRES/GPA0	I	LOCSC input data signal0
			I	SCI insert detection signal
			I/O	GPIO port A0
25	11	LOCSC_D1/SCI_IO/GPA1	I	LOCSC input data signal1
			I/O	SCI data signal
			I/O	GPIO port A1
26	12	LOCSC_D2/SCI_RST/GPA2	I	LOCSC input data signal2
			O	SCI reset signal
			I/O	GPIO port A2
27	13	LOCSC_D3/SCI_CLK/GPA3	I	LOCSC input data signal3
			O	SCI CLK
			I/O	GPIO port A3
28	14	LOCSC_D4/SD_IN0/GPA4	I	LOCSC input data signal4
			I	Self-destruction input detection port0
			I/O	GPIO port A4
29	15	LOCSC_D5/SPI0_CLK/GPA5	I	LOCSC input data signal5
			I/O	SPI0 CLK
			I/O	GPIO port A5
30	16	LOCSC_D6/SPI0_MISO/GPA6	I	LOCSC input data signal6
			I/O	SPI0 master input slave output signal
			I/O	GPIO port A6
31	17	LOCSC_D7/SPI0_MOSI/GPA7	I	LOCSC input data signal7
			I/O	SPI0 master output slave input signal
			I/O	GPIO port A7
32	--	UART1_RXD/GPA27	O	UART1 receive data signal
			I/O	GPIO port A27

Pin No.		Pins	I/O	Description
AS608_QYCF	AS608_QCCF			
33	--	UART1_TXD/GPA28	O	UART1 transfer data signal
			I/O	GPIO port A28
34	18	LOCSC_PCLK/TMR0/GPA8	I	LOCSC pixel CLK input
			I	Timer0 external CLK source input
			I/O	GPIO port A8
35	19	LOCSC_HSYNC/TMR1/GPA9	I	LOCSC row sync signal input
			I	Timer1 external CLK source input
			I/O	GPIO port A9
36	20	LOCSC_VSYNC/TMR2/GPA10	I	LOCSC frame sync signal input
			I	Timer2 external CLK source input
			I/O	GPIO port A10
37	21	I2C_SCL/GPA12	I/O	I2C serial CLK
			I/O	GPIO port A12
38	22	I2C_SDA/GPA13	I/O	I2C serial data
			I/O	GPIO port A13
39	--	GPB9	I/O	GPIO port B9
40	--	GPB10	I/O	GPIO port B10
41	--	SQI_CS/GPA20	O	SQI chip select signal output
			I/O	GPIO port A20
42	--	BVD_IN	I	BVD input port
43	23	LDO5033_EN	I	Enable interior LDO5033 regulator, active High
44	24	LDO5033_IN	P	Interior LDO5033 regulator power input
45	25	USB_DP	I/O	USB D+
46	26	USB_DN	I/O	USB D-
47	27	LDO5033_OUT	P	Interior LDO5033 regulator power output
48	--	NC	--	Not connected
49	28	IO_VDD	P	IO power input
50	29	LDO3318_IN	P	Interior LDO3318 regulator power input
51	30	LDO3318_OUT/LDO1812_IN/VDD18	P	Interior LDO3318 regulator power output /LDO1812 regulator power input /1.8V power
52	31	LDO1812_OUT/CORE_VDD	P	Interior LDO1812 regulator power output/kernel power input
53	--	SQI_IO1/GPA23	I/O	SQI data 1 (single channel SO)
			I/O	GPIO port A23
54	--	SQI_IO2/GPA24	I/O	SQI data 2 (single channel WP)
			I/O	GPIO port A24
55	--	GPB11	I/O	GPIO port B11

Pin No.		Pins	I/O	Description
AS608_QYCF	AS608_QCCF			
56	--	GPB12	I/O	GPIO port B12
57	--	GPB13	I/O	GPIO port B13
58	--	GPB14	I/O	GPIO port B14
59	--	GPB15	I/O	GPIO port B15
60	32	CLKOUT/GPA11	O	Programmable system CLK output
			I/O	GPIO port A11

7 Description of Functions

7.1 Core

7.1.1 Overview

AS608 series adopts 32-bit ARM Cortex™-M core.

Features:

- 3-stage pipelines, branch prediction
- Thumb-2 instruction set, excellent code density and memory footprint
- 32-bit single cycle Multiplication
- Low-latency interrupt response system
- Low-consumption Sleep mode
- 2-wire debugging interface
- Integrated 24-bit SysTick

7.1.2 System Timer (SysTick)

Cortex-M integrates a system Timer – SysTick. SysTick provides a simple, flexible-controlled 24-bit loop count-down counter.

Features:

- 24-bit loop count-down counting
- Auto-load initial count value
- Count clock could be configured to system clock or LFROSC/4
- Configurable interrupt

7.1.3 SW Debugging Interface

Cortex-M core integrates a full hardware debugging interface, it contains optional hardware breakpoint and observation point; accesses processor, memory and peripherals through a 2-wire serial debugging interface SWD; supports program debugging in embedded Flash. 2-wire debugging interface signals are SWCLK and SWDIO.

Features:

- On-chip debug

- In-system program
- Unlimited software breakpoints

7.2 Memory

7.2.1 Overview

AS608 supports up to 4GB addressing memory space, which includes:

- 512KB embedded Flash and 768B user OTP area
- 128KB in-chip SRAM
- 16KB in-chip ROM
- 16MB external SQI storage space
- AHB/APB on-chip peripheral register space

7.2.2 Memory Map

Memory itself has no system address information. Memory map means a process to distribute core memory space while chip is being designed. AS608 memory maps as shown in Figure 7-1.

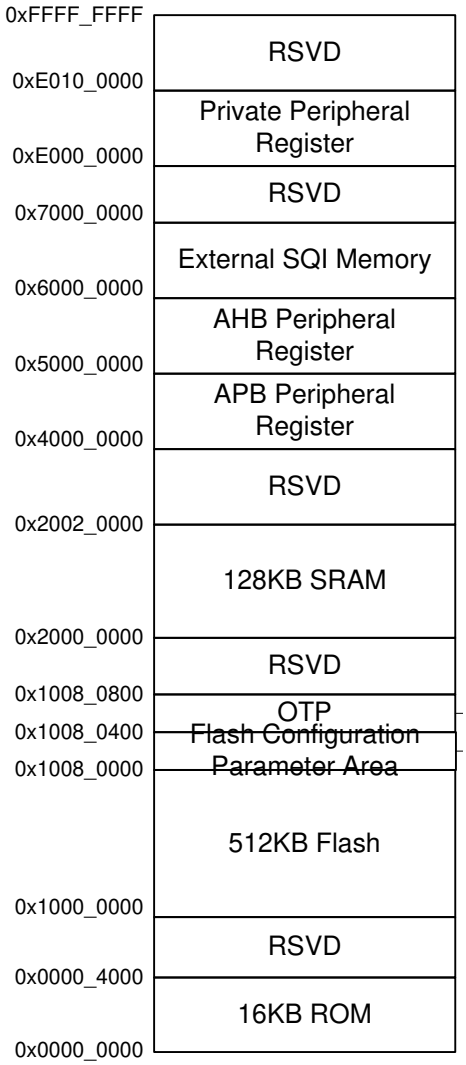


Figure 7-1 AS608 memory map

7.2.3 AHB/APB Peripheral Register

AHB/APB peripheral register space area is 256MB separately, each APB peripheral space is 16KB, each AHB peripheral space is 64KB; core private space area is 1MB for core and its components' register space, mainly for system control, SysTick, NVIC and Debug components.

Table 7-1 AHB/APB peripheral register base address

Ab.	Base address	Description
SCM	0x4000_0000	System Control Module
GPIO	0x4000_4000	General Purposed Input/Output
T0	0x4000_8000	Timer0
SPI0	0x4001_4000	Serial Peripheral Interface0
TRNG	0x4001_8000	True Random Number Generator
USB	0x5001_0000	USB2.0 full speed controller
T1	0x4002_0000	Timer1
T2	0x4002_4000	Timer2

Ab.	Base address	Description
SSI	0x4002_8000	Slave-synchronous Serial Interface
UART0	0x4002_C000	Universal Asynchronous Receiver/Transmitter0
I2C	0x4003_0000	I2C
SCI	0x4004_0000	Smart Card Master Interface
VPWM	0x4004_8000	Voice PWM output controller
UART1	0x4004_C000	Universal Asynchronous Receiver/Transmitter 1
EFC	0x4005_4000	Embedded Flash controller
SQI	0x4005_8000	SQI controller
CRC	0x4005_C000	Cyclic Redundancy Code Generator
BVD	0x4006_0000	Battery Voltage Detector
LOCSC	0x4006_8000	LOCSC controller
SPI1	0x4006_C000	Serial Peripheral Interface1
DMA	0x4007_0000	DMA controller

7.2.4 In-chip SRAM

Internally integrate 128KB single-cycle access SRAM.

7.2.5 Embedded FLASH

Embedded Flash memory maps on 512KB of system address start from 0x1000_0000 by unified addressing, it could be code storage operation space, or data storage space, it is protected by being divided into special areas with different authorities through MPU.

- Page size: 512B, formed by 128x32-bit
- Access time: 50ns
- Programming (32-bit) time: 4μs
- Page erase (512B) time: 1ms
- Entire chip erase time: 20ms
- Programming/erase: >100,000 times (entire chip erase: >1000 times)
- Data storage: >100 years at room temperature

7.2.6 OTP

OTP storage area is for data storage only, write and read through Embedded Flash Controller (EFC), so its read/write is synchronous with embedded Flash's. The write can only write "1" to "0" on certain bit, but not "0" to "1", write "1" on certain bit will not change the value of the bit. Programming is based on word (32-bit) only.

- Divided into 8 areas by the unit of 128B, among them, area 0 is read only, area 7 is for function

configuration

- Six 128B user OTP areas
- Program inhibit in each user area

7.3 Interrupt

Cortex-M core integrates interrupt controller as main part of exception handling mode, it supports 32 (IRQ[31:0]) four-level configurable priority interrupt.

Features:

- Support nesting and vector interrupt
- Automatic save and recover processor status
- Dynamically change priority
- Reduce and confirm interrupt time
- Interrupt wake up

Table 7-2 AS608 interrupt vector table

Exception No.	IRQ No.	Exception type	Priority	Vector add.	Description
0	-	-	-	0x00000000	Initial SP value
1	-	Reset	-3	0x00000004	Reset vector
2	-14	NMI	-2	0x00000008	Non-maskable interrupt
3	-13	HardFault	-1	0x0000000C	Non-maskable interrupt
4	-12	MemManageFault	Configurable	0x00000010	Maskable interrupt
5	-11	BusFault	Configurable	0x00000014	Maskable interrupt
6	-10	UsageFault	Configurable	0x00000015	Maskable interrupt
7 - 10	-	Rsvd	-	0x0000001C – 0x00000028	Rsvd
11	-5	SVCall	Configurable	0x0000002C	Non-maskable interrupt
12	-4	DebugMon	Configurable	0x00000030	Maskable interrupt
13	-	Rsvd	-	0x00000034	Rsvd
14	-2	PendSV	Configurable	0x00000038	Maskable interrupt
15	-1	SysTick	Configurable	0x0000003C	SysTick interrupt
16	0	IRQ0（N/A）	Configurable	0x00000040	Rsvd
17	1	IRQ1（GPIO）	Configurable	0x00000044	GPIO interrupt
18	2	IRQ2（T0）	Configurable	0x00000048	T0 interrupt
19	3	IRQ3（N/A）	-	0x0000004C	Rsvd
20	4	IRQ4（N/A）	-	0x00000050	Rsvd
21	5	IRQ5（SPI0）	Configurable	0x00000054	SPI0 interrupt
22	6	IRQ6（TRNG）	Configurable	0x00000058	TRNG interrupt

Exception No.	IRQ No.	Exception type	Priority	Vector add.	Description
23	7	IRQ7（USB）	Configurable	0x0000005C	USB interrupt
24	8	IRQ8（T1）	Configurable	0x00000060	T1 interrupt
25	9	IRQ9（T2）	Configurable	0x00000064	T2 interrupt
26	10	IRQ10（SSI）	Configurable	0x00000068	SSI interrupt
27	11	IRQ11（UART0）	Configurable	0x0000006C	UART0 interrupt
28	12	IRQ12（I2C）	Configurable	0x00000070	I2C interrupt
29	13	IRQ13（N/A）	-	0x00000074	Rsvd
30	14	IRQ14（N/A）	-	0x00000078	Rsvd
31	15	IRQ15（N/A）	-	0x0000007C	Rsvd
32	16	IRQ16（SCI）	Configurable	0x00000080	SCI interrupt
33	17	IRQ17（N/A）	-	0x00000084	Rsvd
34	18	IRQ18（VPWM）	Configurable	0x00000088	VPWM interrupt
35	19	IRQ19（UART1）	Configurable	0x0000008C	UART1 interrupt
36	20	IRQ20（N/A）	-	0x00000090	Rsvd
37	21	IRQ21（EFC）	Configurable	0x00000094	EFC interrupt
38	22	IRQ22（N/A）	-	0x00000098	Rsvd
39	23	IRQ23（N/A）	-	0x0000009C	Rsvd
40	24	IRQ24（N/A）	-	0x000000A0	Rsvd
41	25	IRQ25（N/A）	-	0x000000A4	Rsvd
42	26	IRQ26（LOCSC）	Configurable	0x000000A8	LOCSC interrupt
43	27	IRQ27（SPI1）	Configurable	0x000000AC	SPI1 interrupt
44	28	IRQ28（DMA）	Configurable	0x000000B0	DMA interrupt
45	29	IRQ29（N/A）	-	0x000000B4	Rsvd
46	30	IRQ30（N/A）	-	0x000000B8	Rsvd
47	31	IRQ31（N/A）	-	0x000000BC	Rsvd

7.4 BOOT ROM

AS608 series integrates 16KB ROM for Boot after system is powered on, the Boot mode includes idle operation status, ISP and embedded Flash operation, it is decided by external boot pin BTM and programming flags in configuration parameter area in embedded Flash space. ISP mode supports USB, SSI and UART0 boot mode.

Table 7-3 AS608 boot mode

Boot mode		BTM0	Programming flag	BTM1	BTM2	Description
Idle		0	--	--	--	Idle loop
RUN		1	Not 0xFFFFFFFF	--	--	Directly jump to application entrance and run
ISP	USB	1	0xFFFFFFFF	--	--	Run USB ISP, download user program
	SSI	1	0xFFFFFFFF	1	1	Run SSI ISP, download user program

Boot mode		BTM0	Programming flag	BTM1	BTM2	Description
	UART0	1	0xFFFFFFFF	0	1	Run UART0 ISP, download user program

After chip is powered on and reset, always run from ROM, and run corresponding programs according to pin status and programming flag as shown in Table 7-3.

7.5 SCM

The System Control Module is the control core of entire chip to manage system memory, system and peripheral module working clock, reset Logic and system working power. The interior contains 1 interior clock generation unit, 1 clock management unit, 1 reset management unit and 1 power management unit.

Interior clock generation unit integrates 2 interior ring oscillators, one is high-frequency high-precision ring oscillator, the other is low-frequency low-consumption ring oscillator, for system and its peripheral working clock generation.

Clock management unit is to manage system clock input selection, control working clocks of various peripherals and memory, it dynamically switches over system frequency, enables and disables peripheral clock, output system clock frequency division.

Reset management unit manages multiple system reset sources, controls system and peripheral module reset.

Power management unit controls system and analog module power.

Features:

- High-precision ring oscillator integrated for system cost reduction and system stability
- Low-frequency and low-consumption ring oscillator integrated for system Sleep consumption reduction
- Available to configure system clock to 1, 2, 4, 8 frequency division of interior high-precision ring oscillator, support dynamic switchover
- Programmable system clock output for 1-256 frequency division of the system clock
- Controllable peripheral clock and software reset to lower system power consumption
- On-chip POR/BOD for stabilizing system power-on/down process
- Available to detect chip temperature and voltage to resist temperature and power attack
- ActiveShield available to resist physical detection and modification
- In-chip regulator provides core and IO voltage for chip and peripherals
- SRAM address and data bus encryption for better data security
- Controllable analog module power

7.6 GPIO

AS608 series has up to 48 GPIO, each GPIO pin input/output direction can be separately controlled, each GPIO

can be configured as interrupt input to support interrupt trigger mode of rising edge and falling edge, all GPIO interrupt shares one interrupt entrance. Each GPIO pin can be separately controlled without affecting other GPIO.

GPIO module is divided into 2 groups: GPIOA (32 pin), GPIOB (16 pin).

GPIOA[14] and GPIOA[15] is as debugging interface SWDIO and SWCLK separately by default.

Features:

- All GPIO pins can be configured as interrupt input
- Some IO drive current could be configured to be 4/8mA, some could be fixed to 12mA
- Configurable IO with 4/8mA drive are also available for pull up/down enable control

7.7 I2C

Inter-Integrated Circuit--I2C is a 2-wire synchronous series interface, it enables controller to communicate with various peripheral devices in 2-wire serial mode. The I2C module is embedded with 4-byte send FIFO for transmitter data buffer and 4-byte receive FIFO for receiver buffer to improve data transmission efficiency. The I2C mode supports to be configured as master mode to connect with multiple salve devices, or as slave mode and used as slave device.

Features:

- Compatible with Philips I2C specifications V2.1
- Half duplex synchronous operation
- 16-bit programmable Baud rate generator
- MSB-first data transmission
- Support I2C master mode and slave mode
- Support transmission and receiving operation
- Support 7-bit and 10-bit address mode
- Do not support broadcast addressing mode
- Do not support START byte mode
- Do not support CBUS mode
- Support standard mode up to 100KHz, fast-speed mode up to 400KHz
- START/STOP/repeat START/ACK generation/detection
- Support one master device operation only under master mode
- Embedded with 4-byte send FIFO and 4-byte receive FIFO
- Support device address automatic detection and ACK or NACK automatic transmission under slave mode
- Interrupt drive operation

- Send FIFO empty interrupt, non-response interrupt, request to send data interrupt, receive data valid interrupt and receive overflow interrupt

7.8 SPI

Serial Peripheral Interface bus system is a synchronous serial peripherals interface, it enables controller to communicate with various peripheral devices in serial mode. SPI module is a 3-wire serial peripheral interface with no slave selection signal, it supports master mode and slave mode communication and various data frame formats. SPI module is embedded with 4-byte send FIFO for transmitter data buffer and 4-byte receive FIFO for receiver buffer to improve data transmission efficiency, if it interacts with master device (master mode) as slave mode, it needs other 2 GPIO ports as handshaking and acknowledge signal between master and slave.

Features:

- Compatible with Motorola SPI specifications
- Support master/slave SPI mode
- 16-bit programmable Baud rate generator
- Support up to two divided-frequency of the system clock under Baud rate master mode, support up to four divided-frequency of the system clock under slave mode
- Programmable serial clock polarity and phase
- Support MSB and LSB data frame format
- Support 7-bit or 8-bit data transmitting or receiving
- Embedded with 4-byte send FIFO and 4-byte receive FIFO
- Support receive/send interrupt and overflow, underrun interrupt

7.9 SSI

Slave-synchronous Serial Interface is a 4-wire full duplex synchronous serial interface, it supports Motorola SPI, TI SSP and NS Microwire protocol.

Features:

- Compatible with Motorola SPI, TI SSP and NS Microwire
- Each frame supports length of 4~16-bit
- 8-frame depth transceiver FIFO
- Support MSB only
- Input clock supports 8 frequency division of system clock frequency to the maximum

7.10 UART

Universal Asynchronous Receiver Transmitter - UART is a 2-wire asynchronous communication interface, it supports full duplex asynchronous communication. The UART transceiver is embedded with 16-byte send FIFO for transmitter data buffer and 16-byte receive FIFO for receiver buffer to effectively reduce service overhead; supports various data frame formats, and handles all kinds of exceptions to ensure completion of data transmission, such as transmission line disconnection detection, odd-even parity error and frame error; supports programmable Baud rate.

Features:

- Support asynchronous mode (UART) RS-232 protocol
- Support full duplex asynchronous operation
- 16-bit programmable Baud rate generator
- Mutually independent transmit and receive shift register
- Mutually independent transmit and receive buffer register
- LSB-first data transmit and receive
- Support the serial frame formats of 1 start bit, 5-bit, 6-bit, 7-bit or 8-bit data bit, even/odd/non-even-odd parity bit , 1-bit, 1.5-bit or 2-bit stop bit
- Odd or even parity generation, support hardware odd/-even parity checking
- Embedded with 16-byte send FIFO and 16-byte receive FIFO
- Transmission line disconnection, generation and detection
- Interrupt drive operation
- Support send FIFO empty interrupt, receive data valid interrupt, receive FIFO overflow interrupt, frame error interrupt, odd-even parity error interrupt and transmission line disconnection error interrupt

7.11 DMA

DMA controller is Direct Memory Asset access control interface based on AHB bus interface, it provides high-speed data transmission channels between peripherals and memory or between memory and memory, each channel can be configured independently for transmission between one-way peripherals or memory and memory.

Features:

- 4 one-way transmission channels, configurable source devices and destination devices
- Programmable priority
- Independent FIFO per channel, size: 16-byte
- Support transmission in 8 byte, 16-byte and 32-byte bus width

- Support source/destination address increasing/decreasing and unchanged any combination
- Support burst transmission: 1, 4, 8
- Max. transmission: 4095 times

7.12 SCI

ISO7816 T0/T1 Smart Card Interface—SCI is compatible with ISO7816 protocol, it supports transmission mode of T=0/T=1. SCI automatically controls data transmission with smart card, activates or inactivates smart card, cold BOOT or warm BOOT smart card, processes received ATR response and other basic functions.

Features:

- Support asynchronous transmission protocol T=0 and T=1
- Support clock frequency conversion factor F = 372 or 512, bit rate regulatory factor D = 1, 2, 4, 8, and 16
- 8-byte depth buffer TX and RX
- Direct interrupt for TX and RX FIFO threshold detection
- Discrete interrupt mask
- Interrupt status register
- Hardware start card inactivation timing while smart card is removed
- Software start card inactivation timing while transmission is completed
- Support synchronous smart card

7.13 VPWM

The VPWM contains 1 PWM output, 1 interior Timer and 8 16-bit FIFO for voice PWM output.

Features:

- Support 8-bit, 16-bit audio source
- Support simple volume control (audio source data translation)

7.14 CRC

The CRC module supports CRC-16 and CRC-CCITT algorithms, CRC-16 generates polynomial: G(x)=x16+x15+x2+1, CRC-CCITT generates polynomial: G(x)=x16+x12+x5+1.

Features:

- 8-bit calculation in one cycle
- Support standard CRC-16 and CRC-CCITT algorithms

- Support bit sequence selection of input data and output results

7.15 TMR

The chip integrates multiple independent 32-bit (Timer) TMR. TMR adopts unique protection mechanism designed by Synochip, which can effectively avoid system errors caused by error operation.

TIMR could be configured to Watch Dog Timer (WDT) mode. When timer counts upwards from 0 to upper limit value, interrupt generated (reset if under WDT mode), cleat counter, and re-start counting.

Features:

- 32-bit counter, count upwards 2^{32} cycles to the maximum
- Multiple clock sources, counter mode available
- More stable WDT mode
- Synochip unique hardware protection mechanism

7.16 LOCSC

LOCSC is a flexible and powerful CMOS optical sensor interface and can easily acquire images needed by customers without any CPU intervention during the entire process.

Features:

- Flexible configuration, just need to configure a few simple registers for acquisition of images needed
- Pure hardware acquisition
- FIFO size: 32x32bit
- FIFO transmits 4 bytes one time, fast transmission
- If cooperates with DMA, no CPU intervention needed during the entire image acquisition process
- Size of images acquired must be integral multiples of 4
- Hardware support images acquired toggle
- Support most CMOS chips in the market (such as HV7131R, GC0303, GC0307, GC0309, OV7670 etc.)

7.17 BVD

BVD (Battery Voltage Detector) is a low-consumption 8-seg non-linear analog to digital converter dedicated for battery voltage detection, it is applicable for lithium battery or dry battery applications. BVD module output 3-bit conversion results.

Features:

- 2 voltage input ranges: 3.0 – 4.2V and 2.1 – 3.3V

- 3-bit result output
- Low conversion rate for operation consumption reduction

7.18 USB

The USB module supports USB2.0 full speed and operates under interrupt or polling mode. It communicates by connecting USB and master device. It is available to configure device to HID device, Mass storage device or other devices.

Features:

- Fully comply with “General Serial Bus Specifications, Revision 2.0”
- Support 12Mbps full speed mode
- Support 2 control endpoints, 1 IN and 1 OUT operations, share a 64-byte FIFO
- Support 4 pairs of IN/OUT endpoints, available to operate under Bulk and interrupt mode, endpoint 1 IN and OUT uses independent 64-byte FIFO separately, each pair of endpoint 2, 3, 4 shares a 64-byte FIFO
- Do not support synchronous transmission
- Support 48M high-precision ring oscillator automatic calibration mechanism
- USB interior 1.5K pull-up resistor, enable and disable controlled by software

7.19 SQI

SQI controller supports standard SPI Flash. SQI data transmission rate could be up to 2 or 4 times of SPI through changing SPI data input and output pin into bi-directional, and multiplexing WP pin and HOLD pin to I/O2 and I/O3.

Features:

- Compatible with 1, 2, 4-channel serial Flash
- Configurable Baud rate
- Configurable and send SQI/SPI FLASH commands
- MPU (Memory Protection Unit) available
- Support address space up to 16MB

7.20 EFC

Embedded Flash Controller not only reads, writes, erases interior Flash, but also provides a set of memory security solution. It divides embedded Flash into different areas for protection, different operating authorities in

each areas, which satisfies various application needs, and, it also secures data and code.

Features:

- Memory protection, prevent code or data from unexpected revision
- Code/data encryption, stored by cipher text, and 32-bit configurable key integrated
- Address disruption
- Area protection, different authorities in different areas

7.21 TRNG

TRNG generates true random number seeds through analog oscillator ring, and 128-bit width true random numbers finally. TRNG is authorized by FIPS140-2. TRNG sub-module oscillator ring could be disabled for consumption reduction by setting register. TRNG supports interrupt, it triggers an interrupt after true random number generation.

Features:

- FIPS140-2 authorized
- Oscillator ring disable available to reduce consumption
- Interrupt available
- Fast random number generation, up to 0.69 MBytes/S@96MHz

7.22 SEA

Embedded with encryption/decryption algorithm modules of AES, DES/3DES, users can call designated algorithm base functions accordingly. Under master frequency of 96MHz, and 5-cycle read timing of embedded Flash, encryption/decryption data block size is 512B, SEA performance index as shown in Table 7-4.

Table 7-4 SEA performance index

Algorithm type	ECB(Bytes/s)	CBC(Bytes/s)
DES		
3DES		
DES accelerator		
AES128		
AES192		
AES256		
AES accelerator (128)		
AES accelerator (192)		
AES accelerator (256)		

7.23 AEA

Embedded with AEA module, RSA supports up to 2048-bit key pair generation algorithm, public key encryption algorithm, private key decryption algorithm, private key encryption algorithm and public key decryption algorithm. ECDSA supports up to 384-bit. Users could call designated algorithm base functions accordingly. Under master frequency of 96MHz, and 5-cycle read timing of embedded Flash, AEA performance index as shown in Table 7-5.

Table 7-5 AEA performance index

Algorithm	Key length (bit)	Key pair generation	Signature
RSA	1024		
	2048		
ECDSA	256		

7.24 HASH

Embedded HASH modules: MD5, SHA1 and SHA256. Users could call designated algorithm base functions accordingly. Under master frequency of 96MHz, and 5-cycle read timing of embedded Flash, HASH data block size is 512B, HASH performance index as shown in Table 7-6.

Table 7-6 HASH performance index

Algorithm	Performance (Bytes/s)
MD5	
SHA1	
SHA256	

8 Electric Parameters

8.1 Limit Electric Parameters

Table 8-1 Limit electric parameters

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{CORE_VDD}	Core voltage				V
V_{IO_VDD}	I/O voltage				V
V_{VDD18}	1.8V voltage				V
$V_{I(IO)}$	I/O input voltage				V
$V_{O(IO)}$	I/O output voltage				V
T_{stg}	Storage temperature				℃
T_{amb}	Ambient temperature				℃
V_{esd}	Electrostatic discharge voltage	On all pins			
		Human body model			V
		Machine mode			V
		Charged device model			V
		On corner pins			
		Charged device model			V

8.2 Recommended Operation Parameters

Table 8-2 Recommended operation electric parameters

Symbol	Parameter	Condition	Min.	Typical value	Max.
T_{OP}	Working temperature range				℃
V_{IO_VDD}	I/O voltage	1.62	1.8/3.3	3.6	V
V_{CORE_VDD}	Core voltage	1.08	1.2	1.32	V
V_{VDD18}	1.8V voltage	1.62	1.8	1.98	V

8.3 DC Electric Parameters

Table 8-3 DC electric parameters

Symbol	Parameter	Condition	Min.	Typical value	Max.	Unit
V_{IH}	Input High Voltage	I/O				V
V_{IL}	Input Low Voltage	I/O				V
V_T	Threshold voltage	I/O				V

Symbol	Parameter	Condition		Min.	Typical value	Max.	Unit
V_{T+}	Threshold+ voltage	Reset pin RESETN					V
V_{T-}	Threshold- voltage						V
I_L	IO input leakage current						μA
I_{OZ}	IO Tri-state output leakage current						μA
R_{PU}	IO pull-up resistor						kΩ
R_{PD}	IO pull-down resistor						kΩ
V_{OH}	Output High Voltage						V
V_{OL}	Output Low Voltage						V
I_{OH}	Output High Current@ VOH (min)	4mA I/O					mA
		8mA I/O					mA
		12mA I/O					mA
I_{OL}	Output Low Current@ VOL (max)	4mA I/O					mA
		8mA I/O					mA
		12mA I/O					mA
I_{DD1}	AES operates working current	Enable peripherals: USB, GPIO, EFC, and test designated algorithm accelerator					mA
							mA
							mA
							mA
I_{DD2}	DES operates working current						mA
							mA
							mA
							mA
I_{DD3}	RSA1024 operates working current						mA
							mA
							mA
							mA
I_{DD4}	RSA2048 operates working current						mA
							mA
							mA
							mA
I_{IDLE1}	System idle working current (execute while (1); operation)	Enable peripherals: USB, GPIO, EFC					mA
I_{IDLE2}							mA
I_{IDLE3}							mA
I_{IDLE4}							mA
I_{SLEEP1}	System Sleep mode current (execute WFI operation)						mA
I_{SLEEP2}							mA
I_{SLEEP3}							mA
I_{SLEEP4}							mA

Symbol	Parameter	Condition	Min.	Typical value	Max.	Unit
I_{SLEEP5}	System Deepsleep mode current (set DEEPSLEEP to1, execute WFI operation)	Disable peripherals except for EFC,GPIO; Interior LDO: low consumption mode; Disable ActiveShield; Disable all analog modules; System low frequency clock: interior ring oscillator				μA

8.4 On-chip Ring Oscillator

8.4.1 On-chip High-frequency Ring Oscillator

Table 8-4 On-chip high-frequency ring oscillator electric parameters

Symbol	Parameter	Condition		Min.	Typical value	Max.	Unit
F_{OUT}	Output clock frequency	12MHz level	25℃ IO_VDD=3.3V				MHz
		48MHz level					MHz
		96MHz level					MHz
		144MHz level					MHz
D	Duty cycle						%
Deviation	Frequency deviation of 48MHz level	Factory calibration, -40~85℃					%
I_{NORMAL}	Current consumption in normal power mode						mA
I_{PD}	Current consumption in power down mode						nA

8.4.2 On-chip Low-frequency Ring Oscillator

Table 8-5 On-chip low-frequency ring oscillator electric parameters

Symbol	Parameter	Condition	Min.	Typical value	Max.	Unit
F_{OUT}	Output clock frequency	25℃, IO_VDD=3.3V				KHz
D	Duty cycle					%
I_{DD}	Current consumption in normal power mode					nA

8.5 POR

Table 8-6 POR electric parameters

Symbol	Parameter	Condition	Min.	Typical value	Max.	Unit
V_{td}	Power-on reset trigger voltage					V
I_{CC}	Current consumption					μA
T_{rst}	Reset latency time					ms

8.6 BOD

8.6.1 IO Power BOD

Table 8-7 IO power BOD electric parameters

Symbol	Parameter	Condition	Min.	Typical value	Max.	Unit
V_{T+}	Trigger+ voltage					V
V_{T-}	Trigger- voltage					V
V_{TH}	Trigger hysteresis voltage					mV
I_{DD}	Current consumption in normal power mode					μA

8.6.2 VDD18 Power BOD

Table 8-8 VDD18 power BOD electric parameters

Symbol	Parameter	Condition	Min.	Typical value	Max.	Unit
V_{T+}	Trigger+ voltage					V
V_{T-}	Trigger- voltage					V
V_{TH}	Trigger hysteresis voltage					mV
I_{DD}	Current consumption in normal power mode					μA

8.7 TPR

Table 8-9 TPR electric parameters

Symbol	Parameter	Condition	Min.	Typical value	Max.	Unit

Symbol	Parameter	Condition	Min.	Typical value	Max.	Unit
T_{LOW}	Low temperature detection point					℃
T_{HIGH}	High temperature detection point					℃
V_{CORE_LOW}	Core low voltage detection point					V
V_{CORE_HIGH}	Core high voltage detection point					V
V_{IO_HIGH}	IO high voltage detection point					
I_{DD}	Current consumption in normal power mode					μA

8.8 LDO

8.8.1 LDO5033

Table 8-10 LDO5033 electric parameters

Symbol	Parameter	Condition	Min.	Typical value	Max.	Unit
$V_{LDO5033_IN}$	Input voltage					V
$V_{LDO5033_OUT}$	Output voltage					V
I_{MAX}	Max. load current					mA
V_{drop}	Input/output voltage differential	$V_{LDO5033_IN}$ > $V_{LDO5033_IN}$ min, I_{LOAD}=0 to max				mV
V_{p-p}	Max. output ripple	VDD50 200mV ripple				mV
t_{ON}	Starting time					μs
I_{leak}	Leakage current	VDD33_EN= 0				μA
C_{out}	External capacitor					μF
	Input stability	I_{LOAD} =max, $V_{LDO5033_IN}$ from 3.5V to 5.5V, DC				mV
	Transient input stability	$V_{LDO5033_IN}$ is variable from 4.2V to 5.5V, rising/falling time: 5μs, I_{LOAD} =Max				mV
	Load stability	$V_{LDO5033_IN}$=5V, I_{LOAD} from 0 to max				mV
	Transient load stability	$V_{LDO5033_IN}$ =5V, I_{LOAD} from 0 to max, rising/falling time: 5μs				mV
	Hot plug and peak protection		Peak duration: <30ns, <10V			
	Current limit	Shorted, $V_{LDO5033_IN}$ =5V				mA

Symbol	Parameter	Condition	Min.	Typical value	Max.	Unit
V_{EN_IL}	LDO5033_EN Logic low input voltage					V
V_{EN_IH}	LDO5033_EN Logic high input voltage					V
I_Q	Current consumption	Normal, LDO5033_EN HIGH				
		Standby, LDO5033_EN LOW				

8.8.2 LDO3318

Table 8-11 LDO3318 electric parameters

Symbol	Parameter	Condition	Min.	Typical value	Max.	Unit
$V_{LDO3318_IN}$	Input voltage					V
$V_{LDO3318_OUT}$	Output voltage					V
I_{MAX}	Max. load current					mA
I_Q	Current consumption					

8.8.3 LDO1812

Table 8-12 LDO1812 electric parameters

Symbol	Parameter	Condition	Min.	Typical value	Max.	Unit
$V_{LDO1812_IN}$	Input voltage					V
$V_{LDO1812_OUT}$	Output voltage					V
I_{MAX}	Max. load current					mA
I_Q	Current consumption					

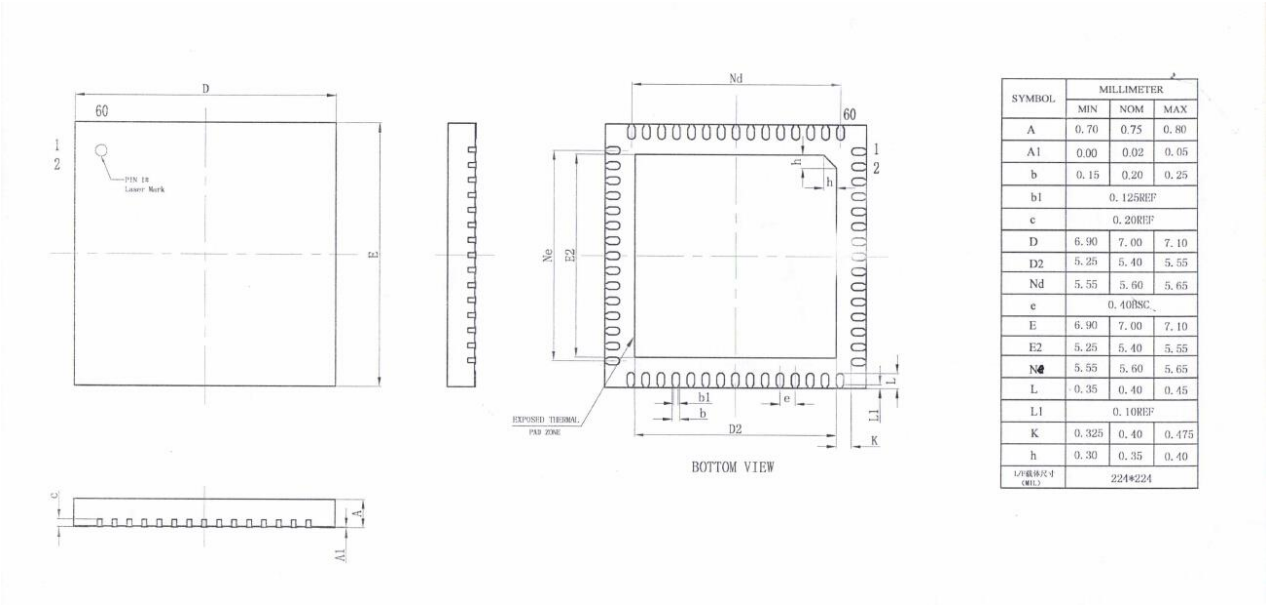
8.9 Embedded Flash

Table 8-13 Embedded Flash electric parameters

Symbol	Parameter	Condition	Min.	Typical value	Max.	Unit
V_{VDD18}	Flash power supply voltage		1.62	1.8	1.98	V
I_{DD_READ}	Read current	CORE_VDD	--	1	2	mA
		VDD18	--	5	8	mA
I_{DD_PROG}	Programming time	CORE_VDD	--	0.1	0.5	mA
		VDD18	--	5	6.5	mA
I_{DD_PE}	Page erase current	CORE_VDD	--	0.1	0.5	mA

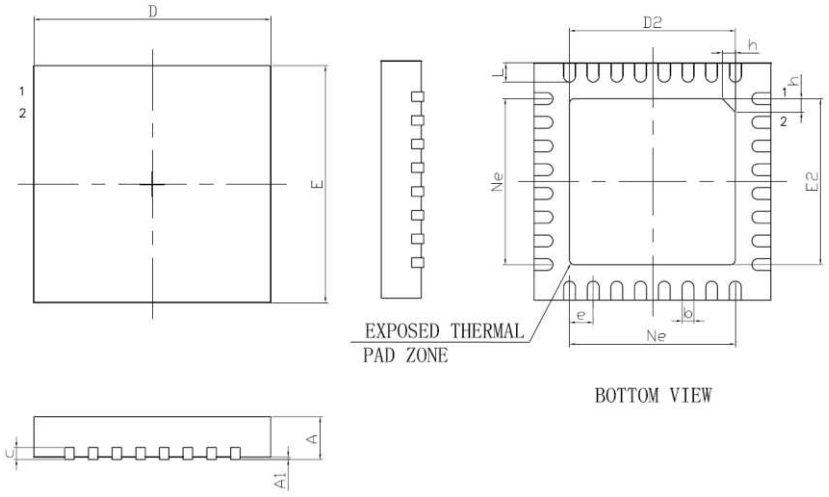
Symbol	Parameter	Condition	Min.	Typical value	Max.	Unit
		VDD18	--	3	3.5	mA
I_{DD_ME}	Entire chip erase current	CORE_VDD	--	0.1	0.5	mA
		VDD18	--	3	3.5	mA
I_{SB}	Idle current	CORE_VDD	--	2	10	μA
		VDD18	--	50	100	μA
I_{SLM}	Sleep mode current	CORE_VDD	--	2	10	μA
		VDD18	--	1	5	μA
t_{ACC}	Read access time				50	ns
t_{PROG}	Programming time			4		μs
t_{PE}	Page erase time			1		ms
t_{ME}	Entire chip erase time			20		ms

9 Mechanical Parameters



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
b1	0.125REF		
c	0.20REF		
D	6.90	7.00	7.10
D2	5.25	5.40	5.55
Nd	5.55	5.60	5.65
e	0.40BSC		
E	6.90	7.00	7.10
E2	5.25	5.40	5.55
Ne	5.55	5.60	5.65
L	0.35	0.40	0.45
L1	0.10REF		
K	0.325	0.40	0.475
h	0.30	0.35	0.40
1/0锡球尺寸(MIL)	224*224		

Figure 9-1 AS608_QYCF package dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Figure 9-2 AS608_QCCF package dimension