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CS5460A

Single Phase, Bi-directional Power/Energy IC

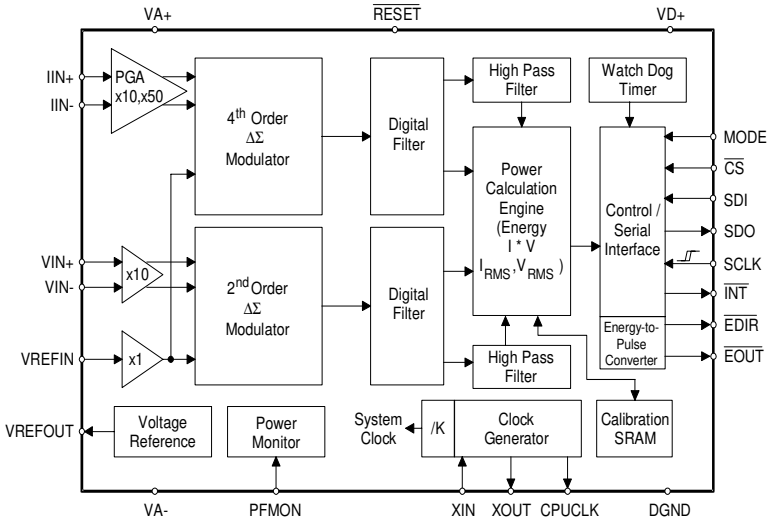
Features

- Energy Data Linearity: ±0.1% of Reading over 1000:1 Dynamic Range.
- On-Chip Functions: (Real) Energy, I ∗ V, I_{RMS} and V_{RMS}, Energy-to-Pulse Conversion
- Smart "Auto-boot" Mode from Serial EEPROM Enables Use without MCU.
- AC or DC System Calibration
- Mechanical Counter/Stepper Motor Driver
- Meets Accuracy Spec for IEC 687/1036, JIS
- Typical Power Consumption <12 mW
- Interface Optimized for Shunt Sensor
- *V* vs. *I* Phase Compensation
- Ground-Referenced Signals with Single Supply
- On-chip 2.5 V Reference (MAX 60 ppm/°C drift)
- Simple Three-wire Digital Serial Interface
- Watch Dog Timer
- Power Supply Monitor
- Power Supply Configurations
  VA+ = +5 V; VA- = 0 V; VD+ = +3.3 V to +5 V

Description

The CS5460A is a highly integrated power measurement solution which combines two ΔΣ Analog-to-digital Converters (ADCs), high-speed power calculation functions, and a serial interface on a single chip. It is designed to accurately measure and calculate: Real (True) Energy, Instantaneous Power, I_{RMS}, and V_{RMS} for single phase 2- or 3-wire power metering applications. The CS5460A interfaces to a low-cost shunt resistor or transformer to measure current, and to a resistive divider or potential transformer to measure voltage. The CS5460A features a bi-directional serial interface for communication with a microcontroller and a pulse output engine for which the average pulse frequency is proportional to the real power. The CS5460A has on-chip functionality to facilitate AC or DC system-level calibration.

The "Auto-boot" feature allows the CS5460A to function 'stand-alone' and to initialize itself on system power-up. In Auto-boot Mode, the CS5460A reads the calibration data and start-up instructions from an external EEPROM. In this mode, the CS5460A can operate without a microcontroller, in order to lower the total bill-of-materials cost.



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ANALOG CHARACTERISTICS

(T_A = -40 °C to +85 °C; VA+ = VD+ = +5 V ±10%; VREFIN = +2.5 V; VA- = AGND = 0 V; MCLK = 4.096 MHz, K = 1; N = 4000 ==> OWR = 4000 Sps.)(See Notes 1, 2, 3, 4, and 5.)

Parameter		Symbol	Min	Typ	Max	Unit
Accuracy (Both Channels)						
Common Mode Rejection	(DC, 50, 60 Hz)	CMRR	80	-	-	dB
Offset Drift (Without the High Pass Filter)			-	5	-	nV/°C
Analog Inputs (Current Channel)						
Maximum Differential Input Voltage Range {(V_{IIN+}) - (V_{IIN-})}	(Gain = 10) (Gain = 50)	I_{IN}	- -	- -	500 100	mV_{P-P} mV_{P-P}
Total Harmonic Distortion		THD_I	80	-	-	dB
Common Mode + Signal on IIN+ or IIN-	(Gain = 10 or 50)		-0.25	-	VA+	V
Crosstalk with Voltage Channel at Full Scale	(50, 60 Hz)		-	-	-115	dB
Input Capacitance	(Gain = 10) (Gain = 50)	C_{in}	- -	25 25	- -	pF pF
Effective Input Impedance	(Note 6) (Gain = 10) (Gain = 50)	 Z_{inI} Z_{inI}	 - -	 30 30	 - -	 kΩ kΩ
Noise (Referred to Input)	(Gain = 10) (Gain = 50)		- -	- -	20 4	μV_{rms} μV_{rms}
Accuracy (Current Channel)						
Bipolar Offset Error	(Note 1)	VOS_I	-	±0.001	-	%F.S.
Full-Scale Error	(Note 1)	FSE_I	-	±0.001	-	%F.S.
Analog Inputs (Voltage Channel)						
Maximum Differential Input Voltage Range	{(V_{VIN+}) - (V_{VIN-})}	V_{IN}	-	-	500	mV_{P-P}
Total Harmonic Distortion		THD_V	62	-	-	dB
Common Mode + Signal on VIN+ or VIN-			VA-	-	VA+	V
Crosstalk with Current Channel at Full Scale	(50, 60 Hz)		-	-	-70	dB
Input Capacitance		C_{inV}	-	0.2	-	pF
Effective Input Impedance	(Note 6)	Z_{inV}	-	5	-	MΩ
Noise (Referred to Input)			-	-	250	μV_{rms}
Accuracy (Voltage Channel)						
Bipolar Offset Error	(Note 1)	VOS_V	-	±0.01	-	%F.S.
Full-Scale Error	(Note 1)	FSE_V	-	±0.01	-	%F.S.

Notes:
1. Bipolar Offset Errors and Full-Scale Gain Errors for the current and voltage channels refer to the respective Irms Register and Vrms Register output, when the device is operating in 'continuous computation cycles' data acquisition mode, *after* offset/gain system calibration sequences have been executed. These specs do *not* apply to the error of the Instantaneous Current/Voltage Register output.
2. Specifications guaranteed by design, characterization, and/or test.
3. Analog signals are relative to VA- and digital signals to DGND unless otherwise noted.
4. In requiring VA+ = VD+ =5 V ±10%, note that it is allowable for VA+, VD+ to differ by as much as ±200 mV, as long as VA+ > VD+.
5. Note that "Sps" is an abbreviation for units of "samples per second".
6. Effective Input Impedance (Zin) is determined by clock frequency (DCLK) and Input Capacitance (IC). Zin = 1/(IC*DCLK/4). Note that DCLK = MCLK / K.

ANALOG CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Typ	Max	Unit
Dynamic Characteristics						
Phase Compensation Range (Voltage Channel, 60 Hz)			-2.4	-	+2.5	°
High Rate Filter Output Word Rate (Both Channels)		OWR	-	DCLK/1024	-	Sps
Input Sample Rate DCLK = MCLK/K			-	DCLK/8	-	Sps
Full Scale DC Calibration Range (Note 7)		FSCR	25	-	100	%F.S.
Channel-to-Channel Time-Shift Error (when PC[6:0] bits are set to "0000000")				1.0		µs
High Pass Filter Pole Frequency -3 dB			-	0.5	-	Hz
Power Supplies						
Power Supply Currents (Active State)	I_{A+}	PSCA	-	1.3	-	mA
	I_{D+} (VD+ = 5 V)	PSCD	-	2.9	-	mA
	I_{D+} (VD+ = 3.3 V)	PSCD	-	1.7	-	mA
Power Consumption (Note 8)	Active State (VD+ = 5 V)	PC	-	21	25	mW
	Active State (VD+ = 3.3 V)		-	11.6	-	mW
	Stand-By State		-	6.75	-	mW
	Sleep State		-	10	-	µW
Power Supply Rejection Ratio for Current Channel (Note 9)	(50, 60 Hz) (Gain = 10)	PSRR	56	-	-	dB
	(50, 60 Hz) (Gain = 50)	PSRR	75	-	-	dB
Power Supply Rejection Ratio for Voltage Channel	(50, 60 Hz) (Note 9)	PSRR	-	65	-	dB
PFMON Power-Fail Detect Threshold (Note 10)		PMLO	2.3	2.45	-	V
PFMON "Power-Restored" Detect Threshold (Note 11)		PMHI	-	2.55	2.7	V

Notes:
7. The minimum FSCR is limited by the maximum allowed gain register value.
8. All outputs unloaded. All inputs CMOS level.
9. Definition for PSRR: VREFIN tied to VREFOUT, VA+ = VD+ = 5 V, a 150 mV zero-to-peak sinewave (frequency = 60 Hz) is imposed onto the +5 V supply voltage at VA+ and VD+ pins. The "+" and "-" input pins of both input channels are shorted to VA-. Then the CS5460A is commanded to 'continuous computation cycles' data acquisition mode, and digital output data is collected for the channel under test. The zero-peak value of the digital sinusoidal output signal is determined, and this value is converted into the zero-peak value of the sinusoidal voltage that would need to be applied at the channel's inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as Veq. PSRR is then (in dB):

$$PSRR = 20 \cdot \log\left\{\frac{0.150V}{V_{eq}}\right\}$$

10. When voltage level on PFMON is sagging, and LSD bit is 0, the voltage at which LSD bit is set to 1.
11. Assuming that the LSD bit has been set to 1 (because PFMON voltage fell below PMLO), then if/when the PFMON voltage starts to rise again, PMHI is the voltage level (on PFMON pin) at which the LSD bit can be permanently reset back to 0 (without instantaneously changing back to 1). Attempts to reset the LSD bit before this condition is true will not be successful. This condition indicates that power has been restored. Typically, for a given sample, the PMHI voltage will be ~100 mV above the PMLO voltage.

VREFOUT REFERENCE OUTPUT VOLTAGE

Parameter	Symbol	Min	Typ	Max	Unit
Reference Output					
Output Voltage	REFOUT	+2.4	-	+2.6	V
VREFOUT Temperature Coefficient (Note 12)	$T_{VREFOUT}$	-	30	60	ppm/°C
Load Regulation (Output Current 1 µA Source or Sink)	ΔV_R	-	6	10	mV
Reference Input					
Input Voltage Range	VREFIN	+2.4	+2.5	+2.6	V
Input Capacitance		-	4	-	pF
Input CVF Current		-	25	-	nA

Notes: 12. The voltage at VREFOUT is measured across the temperature range. From these measurements the following formula is used to calculate the VREFOUT Temperature Coefficient:.

$$T_{VREFOUT} = \left(\frac{(VREFOUT_{MAX} - VREFOUT_{MIN})}{VREFOUT_{AVG}}\right)\cdot\left(\frac{1}{T_{A}MAX - T_{A}MIN}\right)\cdot\left(1.0 \times 10^{6}\right)$$

5V DIGITAL CHARACTERISTICS

(T_A = -40 °C to +85 °C; VA+ = VD+ = 5 V ±10% VA-, DGND = 0 V) (See Notes 3, 4, and 13)

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}				
All Pins Except XIN, SCLK and $\overline{RESET}$		0.6 VD+	-	-	V
XIN		(VD+) - 0.5	-	-	V
SCLK and $\overline{RESET}$		0.8 VD+	-	-	V
Low-Level Input Voltage	V_{IL}				
All Pins Except XIN, SCLK, and $\overline{RESET}$		-	-	0.8	V
XIN		-	-	1.5	V
SCLK and $\overline{RESET}$		-	-	0.2 VD+	V
High-Level Output Voltage (except XOUT) I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage (except XOUT) I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current (Note 14)	I_{in}	-	±1	±10	µA
High Impedance State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

13. Note that the 5 V characteristics are guaranteed by characterization. Only the more rigorous 3.3 V digital characteristics are actually verified during production test.
14. Applies to all INPUT pins except XIN pin (leakage current < 50 µA) and MODE pin (leakage current < 25 µA).

3.3 V DIGITAL CHARACTERISTICS

(T_A = -40 °C to +85 °C; VA+ = 5 V ±10%, VD+ = 3.3 V ±10%; VA-, DGND = 0 V) (See Notes 3, 4, and 13)

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}				
All Pins Except XIN, XOUT, SCLK, and $\overline{\text{RESET}}$		0.6 VD+	-	-	V
XIN		(VD+) - 0.5	-	-	V
SCLK and $\overline{\text{RESET}}$		0.8 VD+	-	-	V
Low-Level Input Voltage	V_{IL}				
All Pins Except XIN, XOUT, SCLK, and $\overline{\text{RESET}}$		-	-	0.48	V
XIN		-	-	0.3	V
SCLK and $\overline{\text{RESET}}$		-	-	0.2 VD+	V
High-Level Output Voltage (except XIN, XOUT) I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage (except XIN, XOUT) I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current (Note 14)	I_{in}	-	±1	±10	µA
3-State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

Notes: 15. All measurements performed under static conditions.

16. If VD+ = 3 V and if XIN input is generated using crystal, then XIN frequency must remain between 2.5 MHz - 5.0 MHz. If using oscillator, full XIN frequency range is available, see *Switching Characteristics*.

ABSOLUTE MAXIMUM RATINGS

(DGND = 0 V; See Note 17) WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Parameter	Symbol	Min	Typ	Max	Unit
DC Power Supplies (Notes 18 and 19)					
Positive Digital	VD+	-0.3	-	+6.0	V
Positive Analog	VA+	-0.3	-	+6.0	V
Negative Analog	VA-	+0.3	-	-6.0	V
Input Current, Any Pin Except Supplies (Note 20, 21, and 22)	I_{IN}	-	-	±10	mA
Output Current	I_{OUT}	-	-	±25	mA
Power Dissipation (Note 23)	P_D	-	-	500	mW
Analog Input Voltage All Analog Pins	V_{INA}	(VA-) - 0.3	-	(VA+) + 0.3	V
Digital Input Voltage All Digital Pins	V_{IND}	DGND - 0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature	T_A	-40	-	85	°C
Storage Temperature	T_{stg}	-65	-	150	°C

Notes: 17. All voltages with respect to ground.

18. VA+ and VA- must satisfy {(VA+) - (VA-)} ≤ +6.0 V.
19. VD+ and VA- must satisfy {(VD+) - (VA-)} ≤ +6.0 V.
20. Applies to all pins including continuous over-voltage conditions at the analog input (AIN) pins.
21. Transient current of up to 100 mA will not cause SCR latch-up.
22. Maximum DC input current for a power supply pin is ±50 mA.
23. Total power dissipation, including all input currents and output currents.

SWITCHING CHARACTERISTICS

(T_A = -40 °C to +85 °C; VA+ = 5.0 V ±10%; VD+ = 3.0 V ±10% or 5.0 V ±10%; VA- = 0.0 V; Logic Levels: Logic 0 = 0.0 V, Logic 1 = VD+; CL = 50 pF))

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	Crystal/Internal Gate Oscillator (Note 24)	MCLK	2.5	4.096	20	MHz
Master Clock Duty Cycle			40	-	60	%
CPUCLK Duty Cycle	(Note 25)		40		60	%
Rise Times	Any Digital Input Except SCLK (Note 26)	t_{rise}	-	-	1.0	µs
	SCLK		-	-	100	µs
	Any Digital Output		-	50	-	ns
Fall Times	Any Digital Input Except SCLK (Note 26)	t_{fall}	-	-	1.0	µs
	SCLK		-	-	100	µs
	Any Digital Output		-	50	-	ns
Start-up						
Oscillator Start-Up Time	XTAL = 4.096 MHz (Note 27)	t_{ost}	-	60	-	ms
Serial Port Timing						
Serial Clock Frequency		SCLK	-	-	2	MHz
Serial Clock	Pulse Width High	t_1	200	-	-	ns
	Pulse Width Low	t_2	200	-	-	ns
SDI Timing						
CS Falling to SCLK Rising		t_3	50	-	-	ns
Data Set-up Time Prior to SCLK Rising		t_4	50	-	-	ns
Data Hold Time After SCLK Rising		t_5	100	-	-	ns
SCLK Falling Prior to CS Disable		t_6	100	-	-	ns
SDO Timing						
CS Falling to SDI Driving		t_7	-	20	50	ns
SCLK Falling to New Data Bit		t_8	-	20	50	ns
CS Rising to SDO Hi-Z		t_9	-	20	50	ns
Auto-boot Timing						
Serial Clock	Pulse Width High	t_{10}		8		MCLK
	Pulse Width Low	t_{11}		8		MCLK
MODE setup time to RESET Rising		t_{12}	50			ns
RESET rising to CS falling		t_{13}	48			MCLK
CS falling to SCLK rising		t_{14}	100	8		MCLK
SCLK falling to CS rising		t_{15}		16		MCLK
CS rising to driving MODE low (to end auto-boot sequence).		t_{16}	50			ns
SDO guaranteed setup time to SCLK rising		t_{17}	100			ns

Notes: 24. Device parameters are specified with a 4.096 MHz clock, yet, clocks between 3 MHz to 20 MHz can be used. However, for input frequencies over 5 MHz, an external oscillator must be used.

25. If external MCLK is used, then duty cycle must be between 45% and 55% to maintain this specification.

26. Specified using 10% and 90% points on wave-form of interest. Output loaded with 50 pF.

27. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

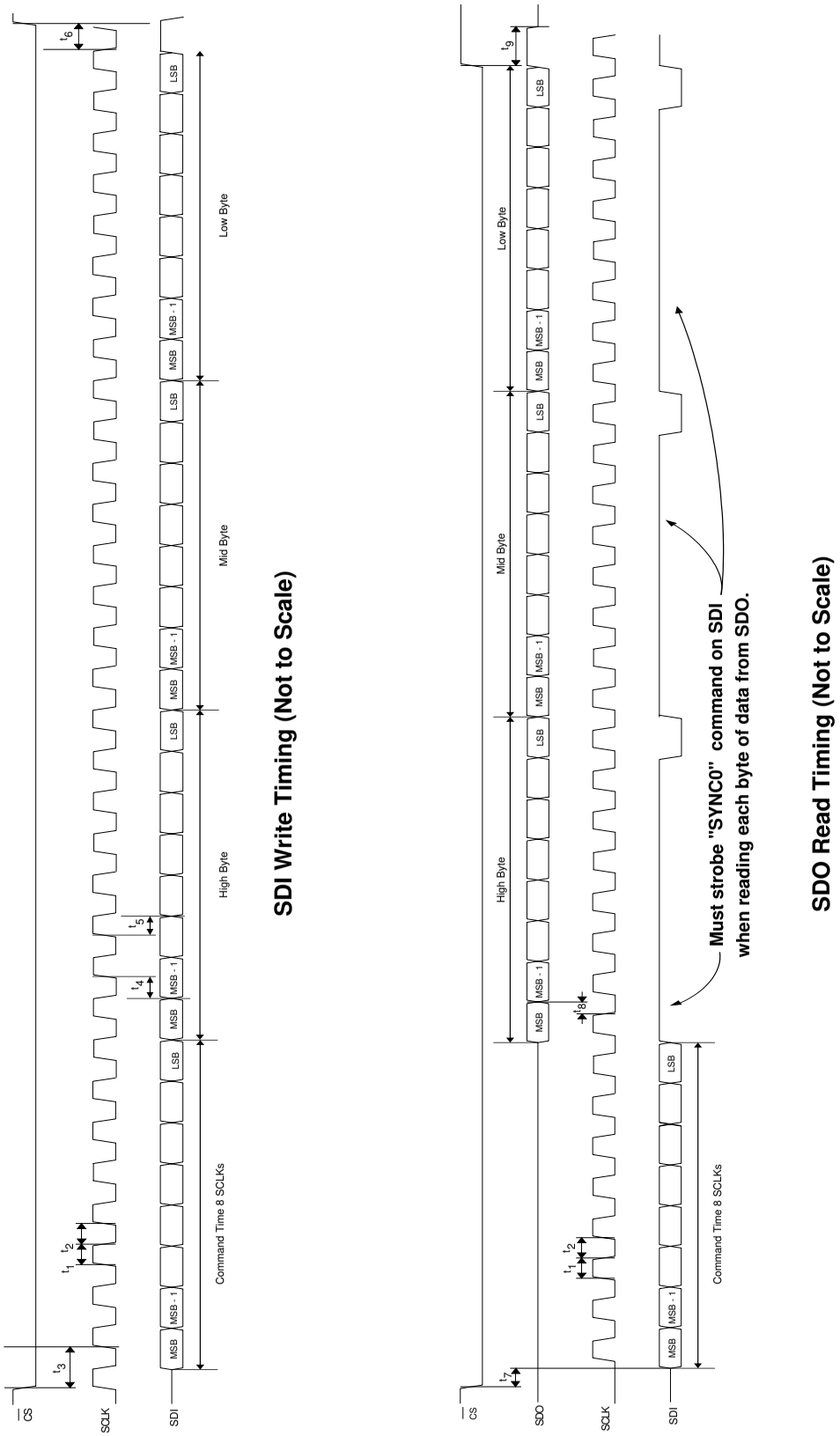

Figure 1. CS5460A Read and Write Timing Diagrams

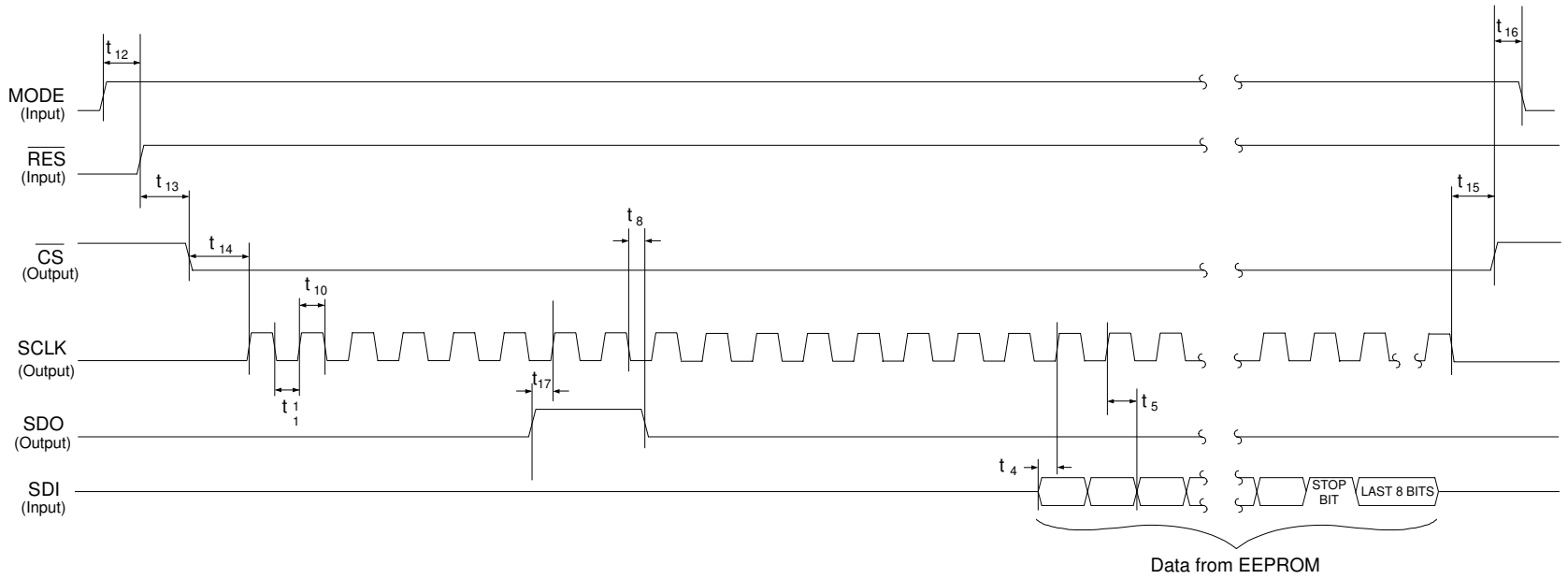

Figure 2. CS5460A Auto-boot Sequence Timing

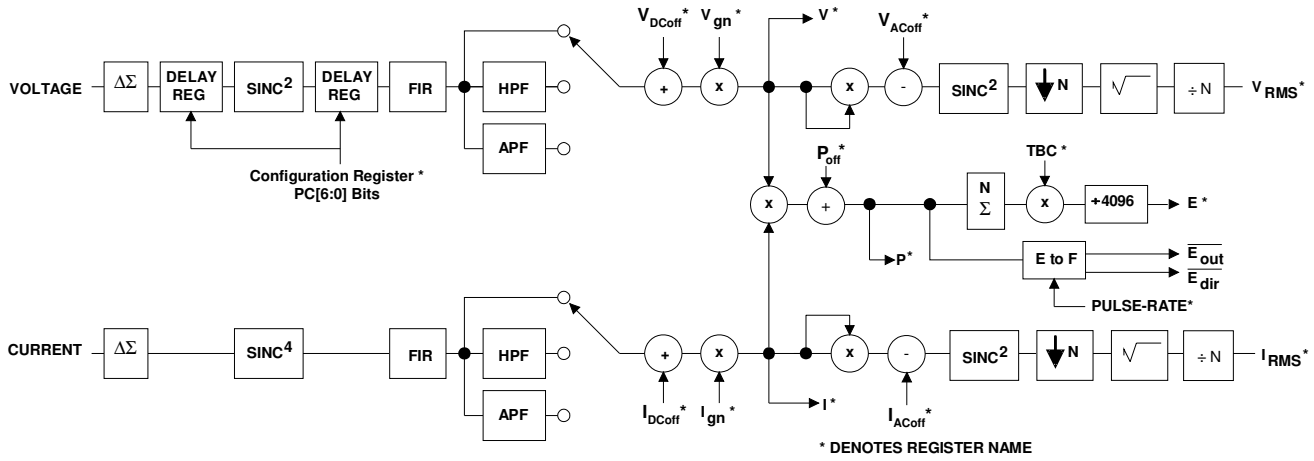

Figure 3. Data Flow.

Figure 3) will be enabled on the other channel; in order to preserve the relative phase relationship between the voltage-sense and current-sense input signals. For example, if the HPF is engaged for the voltage channel, but not the current channel, then the APF will be engaged in the current channel, to nullify the additional phase delay introduced by the high-pass filter in the current channel.

2.1.5 Overall Filter Response

When the CS5460A is driven with a 4.096 MHz clock (K = 1), the composite magnitude response (over frequency) of the voltage channel's input filter network is shown in Figure 4, while the composite magnitude response of the current channel's input filter network is given in Figure 5. Note that the composite filter response of both channels scales with MCLK frequency and K.

2.1.6 Gain and DC Offset Adjustment

After filtering, the instantaneous voltage and current digital codes are subjected to offset/gain adjustments, based on the values in the DC offset registers (additive) and the gain registers (multiplicative). These registers are used for calibration of the device (see *Section 3.8, Calibration*). After offset and gain, the 24-bit instantaneous data sample values are stored in the Instantaneous Voltage and Current Registers.

2.1.7 Real Energy and RMS Computations

The digital instantaneous voltage and current data is then processed further. Referring to Figure 3, the instantaneous voltage/current data samples are multiplied together (one multiplication for each pair of voltage/current samples) to form instantaneous (real) power samples. After each A/D conversion cycle, the new instantaneous power sample is stored in the Instantaneous Power Register.

The instantaneous power samples are then grouped into sets of N samples (where N = value in Cycle Count Register). The cumulative sum of each successive set of N instantaneous power is used to compute the result stored in the Energy Register, which will be proportional to the amount of real energy registered by the device during the most recent N A/D conversion cycles. Note from Figure 3 that the bits in this running energy sum are right-shifted 12 times (divided by 4096) to avoid overflow in the Energy Register. RMS calculations are also performed on the data using the last N instantaneous voltage/current samples, and these results can be read from the RMS Voltage Register and the RMS Current Register.

2.2 Performing Measurements

To summarize Section 2.1, the CS5460A performs measurements of instantaneous current and instantaneous voltage, and from this, performs computations of the corresponding instantaneous power, as well as periodic calculations of real energy, RMS current, and RMS voltage. These measurement/calculation results are available in the form of 24-bit signed and unsigned words. The scaling of all output words is normalized to unity