



**EN:** This Datasheet/Document is presented by the manufacturer.

Please visit our website for pricing and availability at [www.hestore.hu](http://www.hestore.hu).

## Single Phase, Bi-directional Power/Energy IC

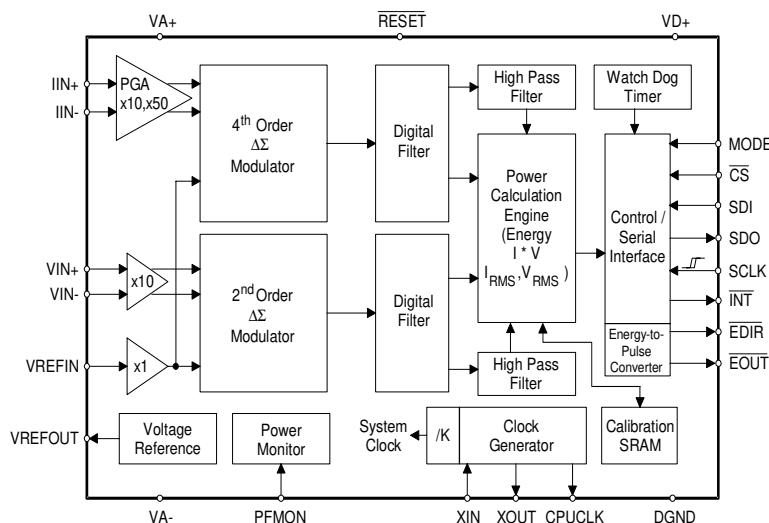
### Features

- Energy Data Linearity:  $\pm 0.1\%$  of Reading over 1000:1 Dynamic Range.
- On-Chip Functions: (Real) Energy,  $I * V$ ,  $I_{RMS}$  and  $V_{RMS}$ , Energy-to-Pulse Conversion
- Smart "Auto-boot" Mode from Serial EEPROM Enables Use without MCU.
- AC or DC System Calibration
- Mechanical Counter/Stepper Motor Driver
- Meets Accuracy Spec for IEC 687/1036, JIS
- Typical Power Consumption <12 mW
- Interface Optimized for Shunt Sensor
- $V$  vs.  $I$  Phase Compensation
- Ground-Referenced Signals with Single Supply
- On-chip 2.5 V Reference (MAX 60 ppm/ $^{\circ}\text{C}$  drift)
- Simple Three-wire Digital Serial Interface
- Watch Dog Timer
- Power Supply Monitor
- Power Supply Configurations  
 $VA+ = +5\text{ V}$ ;  $VA- = 0\text{ V}$ ;  $VD+ = +3.3\text{ V to } +5\text{ V}$

### Description

The CS5460A is a highly integrated power measurement solution which combines two  $\Delta\Sigma$  Analog-to-digital Converters (ADCs), high-speed power calculation functions, and a serial interface on a single chip. It is designed to accurately measure and calculate: Real (True) Energy, Instantaneous Power,  $I_{RMS}$ , and  $V_{RMS}$  for single phase 2- or 3-wire power metering applications. The CS5460A interfaces to a low-cost shunt resistor or transformer to measure current, and to a resistive divider or potential transformer to measure voltage. The CS5460A features a bi-directional serial interface for communication with a microcontroller and a pulse output engine for which the average pulse frequency is proportional to the real power. The CS5460A has on-chip functionality to facilitate AC or DC system-level calibration.

The "Auto-boot" feature allows the CS5460A to function 'stand-alone' and to initialize itself on system power-up. In Auto-boot Mode, the CS5460A reads the calibration data and start-up instructions from an external EEPROM. In this mode, the CS5460A can operate without a microcontroller, in order to lower the total bill-of-materials cost.



## TABLE OF CONTENTS

|                                                                                                 |           |
|-------------------------------------------------------------------------------------------------|-----------|
| <b>1. CHARACTERISTICS AND SPECIFICATIONS .....</b>                                              | <b>5</b>  |
| ANALOG CHARACTERISTICS .....                                                                    | 5         |
| VREFOUT REFERENCE OUTPUT VOLTAGE .....                                                          | 7         |
| 5V DIGITAL CHARACTERISTICS .....                                                                | 7         |
| 3.3 V DIGITAL CHARACTERISTICS .....                                                             | 8         |
| ABSOLUTE MAXIMUM RATINGS .....                                                                  | 8         |
| SWITCHING CHARACTERISTICS .....                                                                 | 9         |
| <b>2. OVERVIEW .....</b>                                                                        | <b>12</b> |
| 2.1 Theory of Operation .....                                                                   | 12        |
| 2.1.1 DS Modulators .....                                                                       | 12        |
| 2.1.2 High-Rate Digital Low-Pass Filters .....                                                  | 12        |
| 2.1.3 Digital Compensation Filters .....                                                        | 12        |
| 2.1.4 Digital High-Pass Filters .....                                                           | 12        |
| 2.1.5 Overall Filter Response .....                                                             | 13        |
| 2.1.6 Gain and DC Offset Adjustment .....                                                       | 13        |
| 2.1.7 Real Energy and RMS Computations .....                                                    | 13        |
| 2.2 Performing Measurements .....                                                               | 13        |
| 2.2.1 CS5460A Linearity Performance .....                                                       | 15        |
| 2.2.2 Single Computation Cycle (C=0) .....                                                      | 15        |
| 2.2.3 Continuous Computation Cycles (C=1) .....                                                 | 16        |
| 2.3 Basic Application Circuit Configurations .....                                              | 16        |
| <b>3. FUNCTIONAL DESCRIPTION .....</b>                                                          | <b>21</b> |
| 3.1 Pulse-Rate Output .....                                                                     | 21        |
| 3.2 Pulse Output for Normal Format,<br>Stepper Motor Format and Mechanical Counter Format ..... | 22        |
| 3.2.1 Normal Format .....                                                                       | 22        |
| 3.2.2 Mechanical Counter Format .....                                                           | 23        |
| 3.2.3 Stepper Motor Format .....                                                                | 23        |
| 3.3 Auto-Boot Mode Using EEPROM .....                                                           | 24        |
| 3.3.1 Auto-Boot Configuration .....                                                             | 24        |
| 3.3.2 Auto-Boot Data for EEPROM .....                                                           | 25        |
| 3.3.3 Application Note AN225 .....                                                              | 26        |
| 3.4 Interrupt and Watchdog Timer .....                                                          | 26        |
| 3.4.1 Interrupt .....                                                                           | 26        |
| 3.4.1.1 Clearing the Status Register .....                                                      | 26        |
| 3.4.1.2 Typical use of the INT pin .....                                                        | 26        |
| 3.4.1.3 INT Active State .....                                                                  | 26        |
| 3.4.1.4 Exceptions .....                                                                        | 26        |
| 3.4.2 Watch Dog Timer .....                                                                     | 26        |
| 3.5 Oscillator Characteristics .....                                                            | 27        |
| 3.6 Analog Inputs .....                                                                         | 27        |
| 3.7 Voltage Reference .....                                                                     | 27        |
| 3.8 Calibration .....                                                                           | 27        |
| 3.8.1 Overview of Calibration Process .....                                                     | 27        |
| 3.8.2 The Calibration Registers .....                                                           | 28        |
| 3.8.3 Calibration Sequence .....                                                                | 28        |
| 3.8.4 Calibration Signal Input Level .....                                                      | 29        |
| 3.8.5 Calibration Signal Frequency .....                                                        | 29        |
| 3.8.6 Input Configurations for Calibrations .....                                               | 29        |
| 3.8.7 Description of Calibration Algorithms .....                                               | 30        |
| 3.8.7.1 AC Offset Calibration Sequence .....                                                    | 30        |
| 3.8.7.2 DC Offset Calibration Sequence .....                                                    | 31        |

|                                                                                     |           |
|-------------------------------------------------------------------------------------|-----------|
| 3.8.7.3 AC Gain Calibration Sequence .....                                          | 31        |
| 3.8.7.4 DC Gain Calibration Sequence .....                                          | 31        |
| 3.8.8 Duration of Calibration Sequence .....                                        | 31        |
| 3.9 Phase Compensation .....                                                        | 31        |
| 3.10 Time-Base Calibration Register .....                                           | 32        |
| 3.11 Power Offset Register .....                                                    | 32        |
| 3.12 Input Protection - Current Limit .....                                         | 32        |
| 3.13 Input Filtering .....                                                          | 34        |
| 3.14 Protection Against High-Voltage and/or High-Current Surges .....               | 37        |
| 3.15 Improving RFI Immunity .....                                                   | 38        |
| 3.16 PCB Layout .....                                                               | 38        |
| <b>4. SERIAL PORT OVERVIEW .....</b>                                                | <b>38</b> |
| 4.1 Commands (Write Only) .....                                                     | 39        |
| 4.2 Serial Port Interface .....                                                     | 42        |
| 4.3 Serial Read and Write .....                                                     | 42        |
| 4.3.1 Register Write .....                                                          | 42        |
| 4.3.2 Register Read .....                                                           | 42        |
| 4.4 System Initialization .....                                                     | 42        |
| 4.5 Serial Port Initialization .....                                                | 43        |
| 4.6 CS5460A Power States .....                                                      | 43        |
| <b>5. REGISTER DESCRIPTION .....</b>                                                | <b>44</b> |
| 5.1 Configuration Register.....                                                     | 44        |
| 5.2 Current Channel DC Offset Register and Voltage Channel DC Offset Register ..... | 46        |
| 5.3 Current Channel Gain Register and Voltage Channel Gain Register.....            | 46        |
| 5.4 Cycle Count Register.....                                                       | 46        |
| 5.5 Pulse-Rate Register .....                                                       | 47        |
| 5.6 I,V,P,E Signed Output Register Results .....                                    | 47        |
| 5.7 IRMS, VRMS Unsigned Output Register Results.....                                | 47        |
| 5.8 Timebase Calibration Register .....                                             | 47        |
| 5.9 Power Offset Register .....                                                     | 48        |
| 5.10 Current Channel AC Offset Register and Voltage Channel AC Offset Register..... | 48        |
| 5.11 Status Register and Mask Register .....                                        | 48        |
| 5.12 Control Register.....                                                          | 50        |
| <b>6. PIN DESCRIPTION .....</b>                                                     | <b>51</b> |
| <b>7. PACKAGE DIMENSIONS .....</b>                                                  | <b>53</b> |
| <b>8. ORDERING INFORMATION .....</b>                                                | <b>54</b> |
| <b>9. CHANGE HISTORY .....</b>                                                      | <b>54</b> |

## LIST OF FIGURES

|                                                                                                        |    |
|--------------------------------------------------------------------------------------------------------|----|
| Figure 1. CS5460A Read and Write Timing Diagrams.....                                                  | 10 |
| Figure 2. CS5460A Auto-Boot Sequence Timing.....                                                       | 11 |
| Figure 3. Data Flow.....                                                                               | 13 |
| Figure 4. Voltage Input Filter Characteristics.....                                                    | 14 |
| Figure 5. Current Input Filter Characteristics.....                                                    | 14 |
| Figure 6. Typical Connection Diagram (One-Phase 2-Wire, Direct Connect to Power Line).....             | 17 |
| Figure 7. Typical Connection Diagram (One-Phase 2-Wire, Isolated from Power Line).....                 | 18 |
| Figure 8. Typical Connection Diagram (One-Phase 3-Wire).....                                           | 19 |
| Figure 9. Typical Connection Diagram (One-Phase 3-Wire - No Neutral Available).....                    | 20 |
| Figure 10. Time-plot representation of pulse output for a typical burst of pulses (Normal Format)..... | 23 |
| Figure 11. Mechanical Counter Format on EOUT and EDIR.....                                             | 23 |
| Figure 12. Stepper Motor Format on EOUT and EDIR.....                                                  | 24 |
| Figure 13. Typical Interface of EEPROM to CS5460A.....                                                 | 24 |
| Figure 14. Timing Diagram for Auto-Boot Sequence.....                                                  | 25 |
| Figure 15. Oscillator Connection.....                                                                  | 27 |
| Figure 16. System Calibration of Gain.....                                                             | 30 |
| Figure 17. System Calibration of Offset.....                                                           | 30 |
| Figure 18. Calibration Data Flow.....                                                                  | 30 |
| Figure 19. Example of AC Gain Calibration.....                                                         | 31 |
| Figure 20. Input Protection for Single-Ended Input Configurations.....                                 | 37 |
| Figure 21. CS5460A Register Diagram.....                                                               | 44 |

## LIST OF TABLES

|                                                                                                                      |    |
|----------------------------------------------------------------------------------------------------------------------|----|
| Table 1. Differential Input Voltage vs. Output Code.....                                                             | 14 |
| Table 2. Available range of $\pm 0.1\%$ output linearity,<br>with default settings in the gain/offset registers..... | 15 |
| Table 3. Default Register Values upon Reset Event.....                                                               | 43 |

## 1. CHARACTERISTICS & SPECIFICATIONS

### ANALOG CHARACTERISTICS

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $V_{A+} = V_{D+} = +5\text{ V} \pm 10\%$ ;  $V_{REFIN} = +2.5\text{ V}$ ;  $V_{A-} = \text{AGND} = 0\text{ V}$ ;  $\text{MCLK} = 4.096\text{ MHz}$ ,  $K = 1$ ;  $N = 4000 \Rightarrow \text{OWR} = 4000\text{ Sps}$ .) (See Notes 1, 2, 3, 4, and 5.)

| Parameter                                                                                             | Symbol           | Min             | Typ         | Max             | Unit                       |
|-------------------------------------------------------------------------------------------------------|------------------|-----------------|-------------|-----------------|----------------------------|
| <b>Accuracy (Both Channels)</b>                                                                       |                  |                 |             |                 |                            |
| Common Mode Rejection (DC, 50, 60 Hz)                                                                 | CMRR             | 80              | -           | -               | dB                         |
| Offset Drift (Without the High Pass Filter)                                                           |                  | -               | 5           | -               | nV/ $^{\circ}\text{C}$     |
| <b>Analog Inputs (Current Channel)</b>                                                                |                  |                 |             |                 |                            |
| Maximum Differential Input Voltage Range (Gain = 10)<br>{(V <sub>IIN+</sub> ) - (V <sub>IIN-</sub> )} | I <sub>IN</sub>  | -               | -           | 500             | mV <sub>P-P</sub>          |
| (Gain = 50)                                                                                           |                  | -               | -           | 100             | mV <sub>P-P</sub>          |
| Total Harmonic Distortion                                                                             | THD <sub>I</sub> | 80              | -           | -               | dB                         |
| Common Mode + Signal on IIN+ or IIN- (Gain = 10 or 50)                                                |                  | -0.25           | -           | V <sub>A+</sub> | V                          |
| Crosstalk with Voltage Channel at Full Scale (50, 60 Hz)                                              |                  | -               | -           | -115            | dB                         |
| Input Capacitance (Gain = 10)                                                                         | C <sub>in</sub>  | -               | 25          | -               | pF                         |
| (Gain = 50)                                                                                           |                  | -               | 25          | -               | pF                         |
| Effective Input Impedance (Note 6)                                                                    |                  |                 |             |                 |                            |
| (Gain = 10)                                                                                           | Z <sub>inI</sub> | -               | 30          | -               | k $\Omega$                 |
| (Gain = 50)                                                                                           | Z <sub>inI</sub> | -               | 30          | -               | k $\Omega$                 |
| Noise (Referred to Input) (Gain = 10)                                                                 |                  | -               | -           | 20              | $\mu\text{V}_{\text{rms}}$ |
| (Gain = 50)                                                                                           |                  | -               | -           | 4               | $\mu\text{V}_{\text{rms}}$ |
| <b>Accuracy (Current Channel)</b>                                                                     |                  |                 |             |                 |                            |
| Bipolar Offset Error (Note 1)                                                                         | VOS <sub>I</sub> | -               | $\pm 0.001$ | -               | %F.S.                      |
| Full-Scale Error (Note 1)                                                                             | FSE <sub>I</sub> | -               | $\pm 0.001$ | -               | %F.S.                      |
| <b>Analog Inputs (Voltage Channel)</b>                                                                |                  |                 |             |                 |                            |
| Maximum Differential Input Voltage Range {(V <sub>VIN+</sub> ) - (V <sub>VIN-</sub> )}                | V <sub>IN</sub>  | -               | -           | 500             | mV <sub>P-P</sub>          |
| Total Harmonic Distortion                                                                             | THD <sub>V</sub> | 62              | -           | -               | dB                         |
| Common Mode + Signal on VIN+ or VIN-                                                                  |                  | V <sub>A-</sub> | -           | V <sub>A+</sub> | V                          |
| Crosstalk with Current Channel at Full Scale (50, 60 Hz)                                              |                  | -               | -           | -70             | dB                         |
| Input Capacitance                                                                                     | C <sub>inV</sub> | -               | 0.2         | -               | pF                         |
| Effective Input Impedance (Note 6)                                                                    | Z <sub>inV</sub> | -               | 5           | -               | M $\Omega$                 |
| Noise (Referred to Input)                                                                             |                  | -               | -           | 250             | $\mu\text{V}_{\text{rms}}$ |
| <b>Accuracy (Voltage Channel)</b>                                                                     |                  |                 |             |                 |                            |
| Bipolar Offset Error (Note 1)                                                                         | VOS <sub>V</sub> | -               | $\pm 0.01$  | -               | %F.S.                      |
| Full-Scale Error (Note 1)                                                                             | FSE <sub>V</sub> | -               | $\pm 0.01$  | -               | %F.S.                      |

- Notes:
1. Bipolar Offset Errors and Full-Scale Gain Errors for the current and voltage channels refer to the respective I<sub>rms</sub> Register and V<sub>rms</sub> Register output, when the device is operating in 'continuous computation cycles' data acquisition mode, *after* offset/gain system calibration sequences have been executed. These specs do *not* apply to the error of the Instantaneous Current/Voltage Register output.
  2. Specifications guaranteed by design, characterization, and/or test.
  3. Analog signals are relative to V<sub>A-</sub> and digital signals to DGND unless otherwise noted.
  4. In requiring V<sub>A+</sub> = V<sub>D+</sub> = 5 V  $\pm 10\%$ , note that it is allowable for V<sub>A+</sub>, V<sub>D+</sub> to differ by as much as  $\pm 200\text{ mV}$ , as long as V<sub>A+</sub> > V<sub>D+</sub>.
  5. Note that "Sps" is an abbreviation for units of "samples per second".
  6. Effective Input Impedance (Z<sub>in</sub>) is determined by clock frequency (DCLK) and Input Capacitance (IC).  
 $Z_{in} = 1/(IC \cdot DCLK/4)$ . Note that  $DCLK = \text{MCLK} / K$ .

**ANALOG CHARACTERISTICS** (Continued)

| Parameter                                                                    | Symbol                     | Min  | Typ       | Max  | Unit  |
|------------------------------------------------------------------------------|----------------------------|------|-----------|------|-------|
| <b>Dynamic Characteristics</b>                                               |                            |      |           |      |       |
| Phase Compensation Range (Voltage Channel, 60 Hz)                            |                            | -2.4 | -         | +2.5 | °     |
| High Rate Filter Output Word Rate (Both Channels)                            | OWR                        | -    | DCLK/1024 | -    | Sps   |
| Input Sample Rate DCLK = MCLK/K                                              |                            | -    | DCLK/8    | -    | Sps   |
| Full Scale DC Calibration Range (Note 7)                                     | FSCR                       | 25   | -         | 100  | %F.S. |
| Channel-to-Channel Time-Shift Error (when PC[6:0] bits are set to "0000000") |                            |      | 1.0       |      | µs    |
| High Pass Filter Pole Frequency -3 dB                                        |                            | -    | 0.5       | -    | Hz    |
| <b>Power Supplies</b>                                                        |                            |      |           |      |       |
| Power Supply Currents (Active State)                                         | I <sub>A+</sub>            | PSCA | -         | 1.3  | mA    |
| I <sub>D+</sub> (VD+ = 5 V)                                                  |                            | PSCD | -         | 2.9  | mA    |
| I <sub>D+</sub> (VD+ = 3.3 V)                                                |                            | PSCD | -         | 1.7  | mA    |
| Power Consumption (Note 8)                                                   | Active State (VD+ = 5 V)   | PC   | -         | 21   | mW    |
|                                                                              | Active State (VD+ = 3.3 V) |      | -         | 11.6 | mW    |
|                                                                              | Stand-By State             |      | -         | 6.75 | mW    |
|                                                                              | Sleep State                |      | -         | 10   | µW    |
| Power Supply Rejection Ratio (50, 60 Hz) for Current Channel (Note 9)        | (Gain = 10)                | PSRR | 56        | -    | dB    |
|                                                                              | (Gain = 50)                | PSRR | 75        | -    | dB    |
| Power Supply Rejection Ratio (50, 60 Hz) for Voltage Channel (Note 9)        |                            | PSRR | -         | 65   | dB    |
| PFMON Power-Fail Detect Threshold (Note 10)                                  | PMLO                       | 2.3  | 2.45      | -    | V     |
| PFMON "Power-Restored" Detect Threshold (Note 11)                            | PMHI                       | -    | 2.55      | 2.7  | V     |

- Notes: 7. The minimum FSCR is limited by the maximum allowed gain register value.
8. All outputs unloaded. All inputs CMOS level.
9. Definition for PSRR: VREFIN tied to VREFOUT, VA+ = VD+ = 5 V, a 150 mV zero-to-peak sinewave (frequency = 60 Hz) is imposed onto the +5 V supply voltage at VA+ and VD+ pins. The "+" and "-" input pins of both input channels are shorted to VA-. Then the CS5460A is commanded to 'continuous computation cycles' data acquisition mode, and digital output data is collected for the channel under test. The zero-peak value of the digital sinusoidal output signal is determined, and this value is converted into the zero-peak value of the sinusoidal voltage that would need to be applied at the channel's inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as V<sub>eq</sub>. PSRR is then (in dB):

$$PSRR = 20 \cdot \log \left\{ \frac{0.150V}{V_{eq}} \right\}$$

10. When voltage level on PFMON is sagging, and LSD bit is 0, the voltage at which LSD bit is set to 1.
11. Assuming that the LSD bit has been set to 1 (because PFMON voltage fell below PMLO), then if/when the PFMON voltage starts to rise again, PMHI is the voltage level (on PFMON pin) at which the LSD bit can be permanently reset back to 0 (without instantaneously changing back to 1). Attempts to reset the LSD bit before this condition is true will not be successful. This condition indicates that power has been restored. Typically, for a given sample, the PMHI voltage will be ~100 mV above the PMLO voltage.

**VREFOUT REFERENCE OUTPUT VOLTAGE**

| Parameter                                            | Symbol               | Min  | Typ  | Max  | Unit   |
|------------------------------------------------------|----------------------|------|------|------|--------|
| <b>Reference Output</b>                              |                      |      |      |      |        |
| Output Voltage                                       | REFOUT               | +2.4 | -    | +2.6 | V      |
| VREFOUT Temperature Coefficient (Note 12)            | T <sub>VREFOUT</sub> | -    | 30   | 60   | ppm/°C |
| Load Regulation (Output Current 1 µA Source or Sink) | ΔV <sub>R</sub>      | -    | 6    | 10   | mV     |
| <b>Reference Input</b>                               |                      |      |      |      |        |
| Input Voltage Range                                  | VREFIN               | +2.4 | +2.5 | +2.6 | V      |
| Input Capacitance                                    |                      | -    | 4    | -    | pF     |
| Input CVF Current                                    |                      | -    | 25   | -    | nA     |

Notes: 12. The voltage at VREFOUT is measured across the temperature range. From these measurements the following formula is used to calculate the VREFOUT Temperature Coefficient:

$$T_{VREFOUT} = \left( \frac{(VREFOUT_{MAX} - VREFOUT_{MIN})}{VREFOUT_{AVG}} \right) \cdot \left( \frac{1}{T_{A_{MAX}} - T_{A_{MIN}}} \right) \cdot (1.0 \times 10^6)$$

**5V DIGITAL CHARACTERISTICS**

(T<sub>A</sub> = -40 °C to +85 °C; V<sub>A+</sub> = V<sub>D+</sub> = 5 V ±10% V<sub>A-</sub>, DGND = 0 V) (See Notes 3, 4, and 13)

| Parameter                                                                                                                        | Symbol           | Min                                                                    | Typ         | Max                               | Unit        |
|----------------------------------------------------------------------------------------------------------------------------------|------------------|------------------------------------------------------------------------|-------------|-----------------------------------|-------------|
| High-Level Input Voltage<br>All Pins Except XIN, SCLK and $\overline{\text{RESET}}$<br>XIN<br>SCLK and $\overline{\text{RESET}}$ | V <sub>IH</sub>  | 0.6 V <sub>D+</sub><br>(V <sub>D+</sub> ) - 0.5<br>0.8 V <sub>D+</sub> | -<br>-<br>- | -<br>-<br>-                       | V<br>V<br>V |
| Low-Level Input Voltage<br>All Pins Except XIN, SCLK, and $\overline{\text{RESET}}$<br>XIN<br>SCLK and $\overline{\text{RESET}}$ | V <sub>IL</sub>  | -<br>-<br>-                                                            | -<br>-<br>- | 0.8<br>1.5<br>0.2 V <sub>D+</sub> | V<br>V<br>V |
| High-Level Output Voltage (except XOUT) I <sub>out</sub> = +5 mA                                                                 | V <sub>OH</sub>  | (V <sub>D+</sub> ) - 1.0                                               | -           | -                                 | V           |
| Low-Level Output Voltage (except XOUT) I <sub>out</sub> = -5 mA                                                                  | V <sub>OL</sub>  | -                                                                      | -           | 0.4                               | V           |
| Input Leakage Current (Note 14)                                                                                                  | I <sub>in</sub>  | -                                                                      | ±1          | ±10                               | µA          |
| High Impedance State Leakage Current                                                                                             | I <sub>OZ</sub>  | -                                                                      | -           | ±10                               | µA          |
| Digital Output Pin Capacitance                                                                                                   | C <sub>out</sub> | -                                                                      | 5           | -                                 | pF          |

13. Note that the 5 V characteristics are guaranteed by characterization. Only the more rigorous 3.3 V digital characteristics are actually verified during production test.
14. Applies to all INPUT pins except XIN pin (leakage current < 50 µA) and MODE pin (leakage current < 25 µA).



### 3.3 V DIGITAL CHARACTERISTICS

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $V_{A+} = 5\text{ V} \pm 10\%$ ,  $V_{D+} = 3.3\text{ V} \pm 10\%$ ;  $V_{A-}$ , DGND = 0 V) (See Notes 3, 4, and 13)

| Parameter                                                                                                                               | Symbol    | Min                                                | Typ         | Max                         | Unit          |
|-----------------------------------------------------------------------------------------------------------------------------------------|-----------|----------------------------------------------------|-------------|-----------------------------|---------------|
| High-Level Input Voltage<br>All Pins Except XIN, XOUT, SCLK, and $\overline{\text{RESET}}$<br>XIN<br>SCLK and $\overline{\text{RESET}}$ | $V_{IH}$  | 0.6 $V_{D+}$<br>( $V_{D+}$ ) - 0.5<br>0.8 $V_{D+}$ | -<br>-<br>- | -<br>-<br>-                 | V<br>V<br>V   |
| Low-Level Input Voltage<br>All Pins Except XIN, XOUT, SCLK, and $\overline{\text{RESET}}$<br>XIN<br>SCLK and $\overline{\text{RESET}}$  | $V_{IL}$  | -<br>-<br>-                                        | -<br>-<br>- | 0.48<br>0.3<br>0.2 $V_{D+}$ | V<br>V<br>V   |
| High-Level Output Voltage (except XIN, XOUT) $I_{out} = +5\text{ mA}$                                                                   | $V_{OH}$  | ( $V_{D+}$ ) - 1.0                                 | -           | -                           | V             |
| Low-Level Output Voltage (except XIN, XOUT) $I_{out} = -5\text{ mA}$                                                                    | $V_{OL}$  | -                                                  | -           | 0.4                         | V             |
| Input Leakage Current (Note 14)                                                                                                         | $I_{in}$  | -                                                  | $\pm 1$     | $\pm 10$                    | $\mu\text{A}$ |
| 3-State Leakage Current                                                                                                                 | $I_{OZ}$  | -                                                  | -           | $\pm 10$                    | $\mu\text{A}$ |
| Digital Output Pin Capacitance                                                                                                          | $C_{out}$ | -                                                  | 5           | -                           | pF            |

Notes: 15. All measurements performed under static conditions.

16. If  $V_{D+} = 3\text{ V}$  and if XIN input is generated using crystal, then XIN frequency must remain between 2.5 MHz - 5.0 MHz. If using oscillator, full XIN frequency range is available, see *Switching Characteristics*.

### ABSOLUTE MAXIMUM RATINGS

(DGND = 0 V; See Note 17) WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

| Parameter                                                                                     | Symbol                           | Min                  | Typ         | Max                  | Unit               |
|-----------------------------------------------------------------------------------------------|----------------------------------|----------------------|-------------|----------------------|--------------------|
| DC Power Supplies (Notes 18 and 19)<br>Positive Digital<br>Positive Analog<br>Negative Analog | $V_{D+}$<br>$V_{A+}$<br>$V_{A-}$ | -0.3<br>-0.3<br>+0.3 | -<br>-<br>- | +6.0<br>+6.0<br>-6.0 | V<br>V<br>V        |
| Input Current, Any Pin Except Supplies (Note 20, 21, and 22)                                  | $I_{IN}$                         | -                    | -           | $\pm 10$             | mA                 |
| Output Current                                                                                | $I_{OUT}$                        | -                    | -           | $\pm 25$             | mA                 |
| Power Dissipation (Note 23)                                                                   | $P_D$                            | -                    | -           | 500                  | mW                 |
| Analog Input Voltage All Analog Pins                                                          | $V_{INA}$                        | ( $V_{A-}$ ) - 0.3   | -           | ( $V_{A+}$ ) + 0.3   | V                  |
| Digital Input Voltage All Digital Pins                                                        | $V_{IND}$                        | DGND - 0.3           | -           | ( $V_{D+}$ ) + 0.3   | V                  |
| Ambient Operating Temperature                                                                 | $T_A$                            | -40                  | -           | 85                   | $^{\circ}\text{C}$ |
| Storage Temperature                                                                           | $T_{stg}$                        | -65                  | -           | 150                  | $^{\circ}\text{C}$ |

Notes: 17. All voltages with respect to ground.

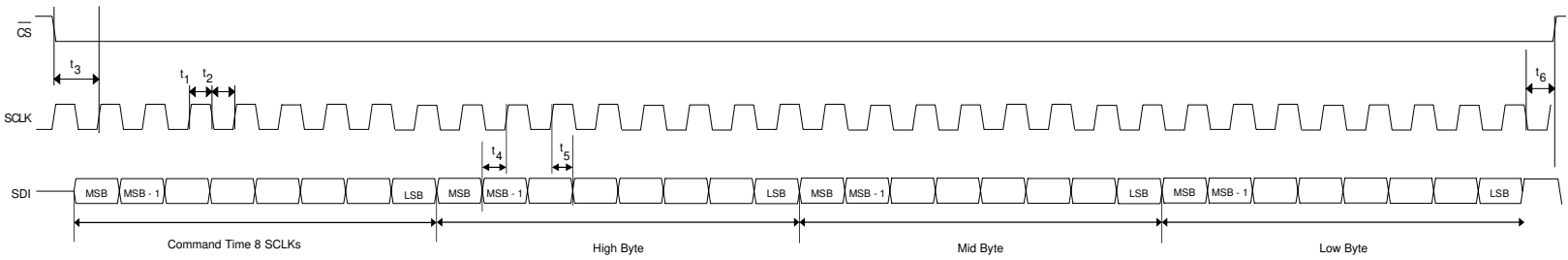
18.  $V_{A+}$  and  $V_{A-}$  must satisfy  $\{(V_{A+}) - (V_{A-})\} \leq +6.0\text{ V}$ .  
19.  $V_{D+}$  and  $V_{A-}$  must satisfy  $\{(V_{D+}) - (V_{A-})\} \leq +6.0\text{ V}$ .  
20. Applies to all pins including continuous over-voltage conditions at the analog input (AIN) pins.  
21. Transient current of up to 100 mA will not cause SCR latch-up.  
22. Maximum DC input current for a power supply pin is  $\pm 50\text{ mA}$ .  
23. Total power dissipation, including all input currents and output currents.

## SWITCHING CHARACTERISTICS

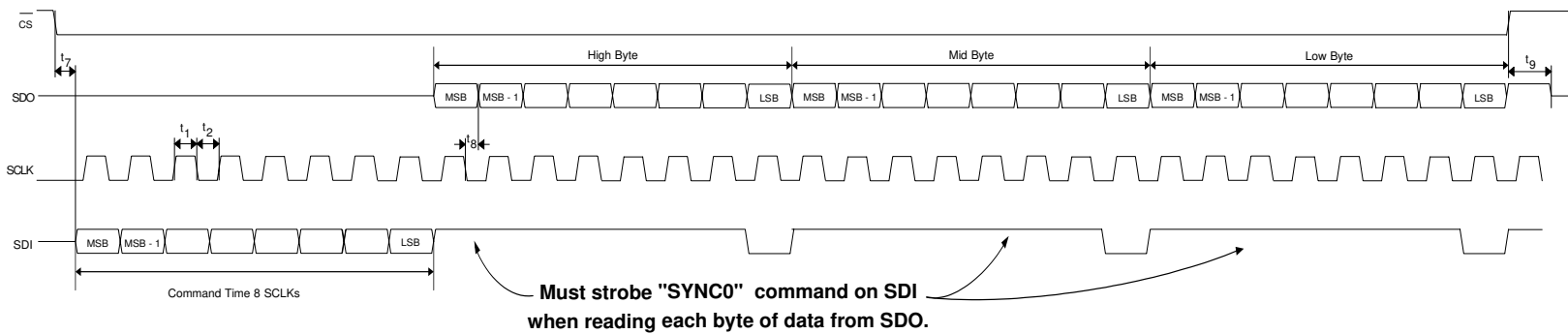
( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $V_{A+} = 5.0\text{ V} \pm 10\%$ ;  $V_{D+} = 3.0\text{ V} \pm 10\%$  or  $5.0\text{ V} \pm 10\%$ ;  $V_{A-} = 0.0\text{ V}$ ; Logic Levels: Logic 0 = 0.0 V, Logic 1 =  $V_{D+}$ ;  $CL = 50\text{ pF}$ )

| Parameter                                                        | Symbol            | Min | Typ   | Max | Unit |
|------------------------------------------------------------------|-------------------|-----|-------|-----|------|
| Master Clock FrequencyCrystal/Internal Gate Oscillator (Note 24) | MCLK              | 2.5 | 4.096 | 20  | MHz  |
| Master Clock Duty Cycle                                          |                   | 40  | -     | 60  | %    |
| CPUCLK Duty Cycle (Note 25)                                      |                   | 40  |       | 60  | %    |
| Rise TimesAny Digital Input Except SCLK (Note 26)                | t <sub>rise</sub> | -   | -     | 1.0 | μs   |
| SCLK                                                             |                   | -   | -     | 100 | μs   |
| Any Digital Output                                               |                   | -   | 50    | -   | ns   |
| Fall TimesAny Digital Input Except SCLK (Note 26)                | t <sub>fall</sub> | -   | -     | 1.0 | μs   |
| SCLK                                                             |                   | -   | -     | 100 | μs   |
| Any Digital Output                                               |                   | -   | 50    | -   | ns   |
| <b>Start-up</b>                                                  |                   |     |       |     |      |
| Oscillator Start-Up TimeXTAL = 4.096 MHz (Note 27)               | t <sub>ost</sub>  | -   | 60    | -   | ms   |
| <b>Serial Port Timing</b>                                        |                   |     |       |     |      |
| Serial Clock Frequency                                           | SCLK              | -   | -     | 2   | MHz  |
| Serial ClockPulse Width High                                     | t <sub>1</sub>    | 200 | -     | -   | ns   |
| Pulse Width Low                                                  | t <sub>2</sub>    | 200 | -     | -   | ns   |
| <b>SDI Timing</b>                                                |                   |     |       |     |      |
| CS Falling to SCLK Rising                                        | t <sub>3</sub>    | 50  | -     | -   | ns   |
| Data Set-up Time Prior to SCLK Rising                            | t <sub>4</sub>    | 50  | -     | -   | ns   |
| Data Hold Time After SCLK Rising                                 | t <sub>5</sub>    | 100 | -     | -   | ns   |
| SCLK Falling Prior to CS Disable                                 | t <sub>6</sub>    | 100 | -     | -   | ns   |
| <b>SDO Timing</b>                                                |                   |     |       |     |      |
| CS Falling to SDI Driving                                        | t <sub>7</sub>    | -   | 20    | 50  | ns   |
| SCLK Falling to New Data Bit                                     | t <sub>8</sub>    | -   | 20    | 50  | ns   |
| CS Rising to SDO Hi-Z                                            | t <sub>9</sub>    | -   | 20    | 50  | ns   |
| <b>Auto-boot Timing</b>                                          |                   |     |       |     |      |
| Serial ClockPulse Width High                                     | t <sub>10</sub>   |     | 8     |     | MCLK |
| Pulse Width Low                                                  | t <sub>11</sub>   |     | 8     |     | MCLK |
| MODE setup time to RESET Rising                                  | t <sub>12</sub>   | 50  |       |     | ns   |
| RESET rising to CS falling                                       | t <sub>13</sub>   | 48  |       |     | MCLK |
| CS falling to SCLK rising                                        | t <sub>14</sub>   | 100 | 8     |     | MCLK |
| SCLK falling to CS rising                                        | t <sub>15</sub>   |     | 16    |     | MCLK |
| CS rising to driving MODE low (to end auto-boot sequence).       | t <sub>16</sub>   | 50  |       |     | ns   |
| SDO guaranteed setup time to SCLK rising                         | t <sub>17</sub>   | 100 |       |     | ns   |

- Notes: 24. Device parameters are specified with a 4.096 MHz clock, yet, clocks between 3 MHz to 20 MHz can be used. However, for input frequencies over 5 MHz, an external oscillator must be used.
25. If external MCLK is used, then duty cycle must be between 45% and 55% to maintain this specification.
26. Specified using 10% and 90% points on wave-form of interest. Output loaded with 50 pF.
27. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.



SDI Write Timing (Not to Scale)



SDO Read Timing (Not to Scale)

Figure 1. CS5460A Read and Write Timing Diagrams

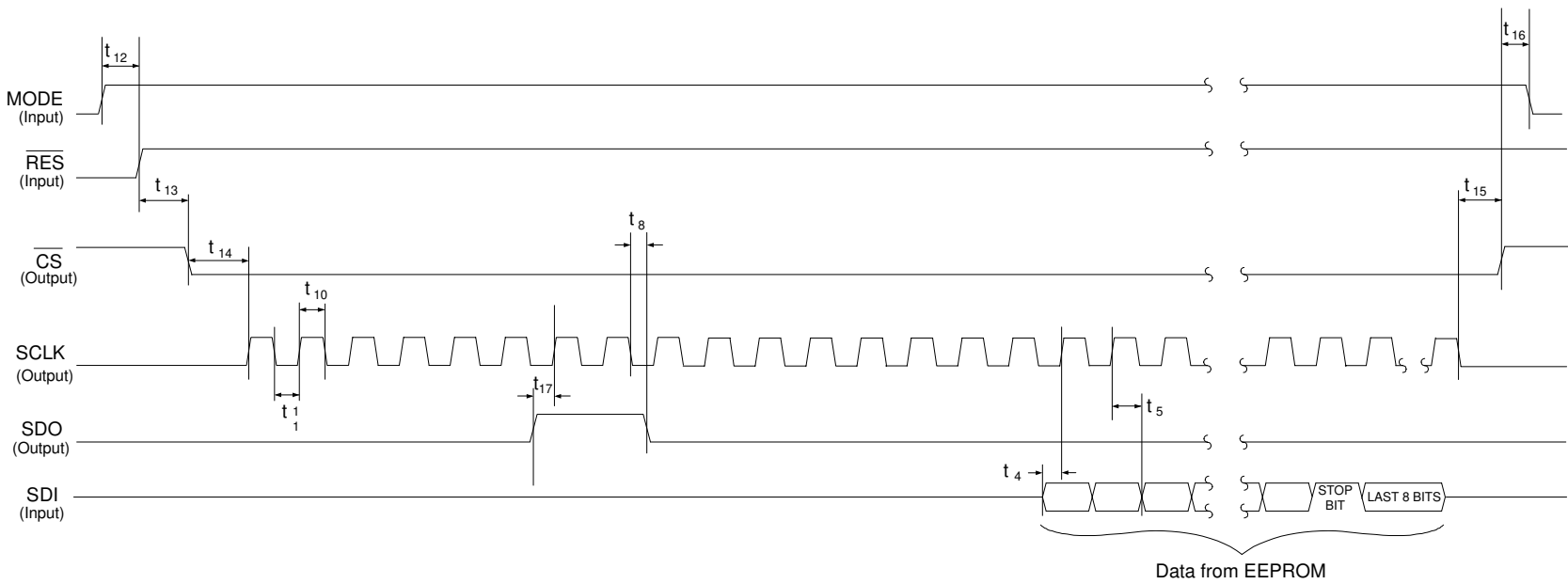
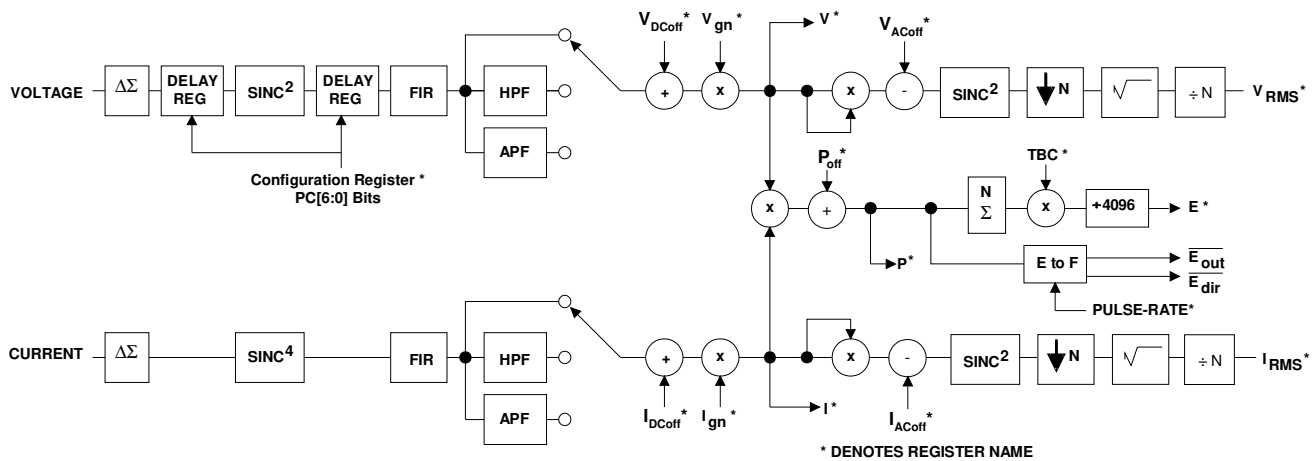


Figure 2. CS5460A Auto-boot Sequence Timing





**Figure 3. Data Flow.**

Figure 3) will be enabled on the other channel; in order to preserve the relative phase relationship between the voltage-sense and current-sense input signals. For example, if the HPF is engaged for the voltage channel, but not the current channel, then the APF will be engaged in the current channel, to nullify the additional phase delay introduced by the high-pass filter in the current channel.

### 2.1.5 Overall Filter Response

When the CS5460A is driven with a 4.096 MHz clock ( $K = 1$ ), the composite magnitude response (over frequency) of the voltage channel's input filter network is shown in Figure 4, while the composite magnitude response of the current channel's input filter network is given in Figure 5. Note that the composite filter response of both channels scales with MCLK frequency and  $K$ .

### 2.1.6 Gain and DC Offset Adjustment

After filtering, the instantaneous voltage and current digital codes are subjected to offset/gain adjustments, based on the values in the DC offset registers (additive) and the gain registers (multiplicative). These registers are used for calibration of the device (see *Section 3.8, Calibration*). After offset and gain, the 24-bit instantaneous data sample values are stored in the Instantaneous Voltage and Current Registers.

### 2.1.7 Real Energy and RMS Computations

The digital instantaneous voltage and current data is then processed further. Referring to Figure 3, the

instantaneous voltage/current data samples are multiplied together (one multiplication for each pair of voltage/current samples) to form instantaneous (real) power samples. After each A/D conversion cycle, the new instantaneous power sample is stored in the Instantaneous Power Register.

The instantaneous power samples are then grouped into sets of  $N$  samples (where  $N$  = value in Cycle Count Register). The cumulative sum of each successive set of  $N$  instantaneous power is used to compute the result stored in the Energy Register, which will be proportional to the amount of real energy registered by the device during the most recent  $N$  A/D conversion cycles. Note from Figure 3 that the bits in this running energy sum are right-shifted 12 times (divided by 4096) to avoid overflow in the Energy Register. RMS calculations are also performed on the data using the last  $N$  instantaneous voltage/current samples, and these results can be read from the RMS Voltage Register and the RMS Current Register.

## 2.2 Performing Measurements

To summarize Section 2.1, the CS5460A performs measurements of instantaneous current and instantaneous voltage, and from this, performs computations of the corresponding instantaneous power, as well as periodic calculations of real energy, RMS current, and RMS voltage. These measurement/calculation results are available in the form of 24-bit signed and unsigned words. The scaling of all output words is normalized to unity