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1. General description

High voltage, high speed NPN planar-passivated power switching transistor in a SOT78 plastic package intended for use in high frequency electronic lighting ballast applications

2. Features and benefits

- Fast switching
- High voltage capability of 700 V
- Low thermal resistance

3. Applications

- Electronic lighting ballasts

4. Quick reference data

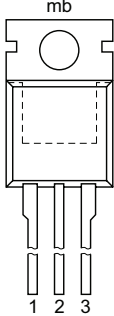
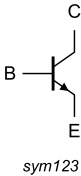
Table 1. Quick reference data

Table 11. Quick reference data

Symbol	Parameter	Conditions	Values				Unit
Absolute maximum rating							
V _{CESM}	peak collector-emitter voltage	V _{BE} = 0 V	700				V
I _C	collector current (DC)	DC; Fig. 1 ; Fig. 2 ; Fig. 4	4				A
P _{tot}	total power dissipation	T _{mb} ≤ 25 °C; Fig. 3	75				W
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
h _{FE}	DC current gain	I _C = 1 A; V _{CE} = 5 V; T _{mb} = 25 °C; Fig. 11		12	20	40	
		I _C = 2 A; V _{CE} = 5 V; T _{mb} = 25 °C; Fig. 11		10	17	28	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base		
2	C	collector		
3	E	emitter		
mb	C	mounting base; connected to collector		

6. Ordering information

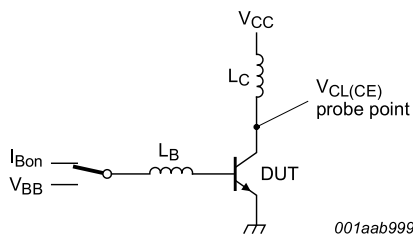
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHE13005	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Values	Unit
V_{CESM}	peak collector-emitter voltage	$V_{BE} = 0\text{ V}$	700	V
V_{CBO}	collector-base voltage	$I_E = 0\text{ A}$	700	V
V_{CEO}	collector-emitter voltage	$I_B = 0\text{ A}$	400	V
I_C	collector current	DC; Fig. 1 ; Fig. 2 ; Fig. 4	4	A
I_{CM}	peak collector current		8	A
I_B	base current	DC	2	A
I_{BM}	peak base current		4	A
P_{tot}	total power dissipation	$T_{mb} \leq 25\text{ °C}$; Fig. 3	75	W
T_{stg}	storage temperature		-65 to 150	°C
T_j	junction temperature		150	°C
V_{EBO}	emitter-base voltage	$I_C = 0\text{ A}$	9	V



$V_{CL(CE)} \leq 1000\text{V}$; $V_{CC} = 150\text{ V}$; $V_{BB} = -5\text{ V}$;
 $L_C = 200\text{ }\mu\text{H}$; $L_B = 1\text{ }\mu\text{H}$

Fig. 1. Test circuit for reverse bias safe operating area

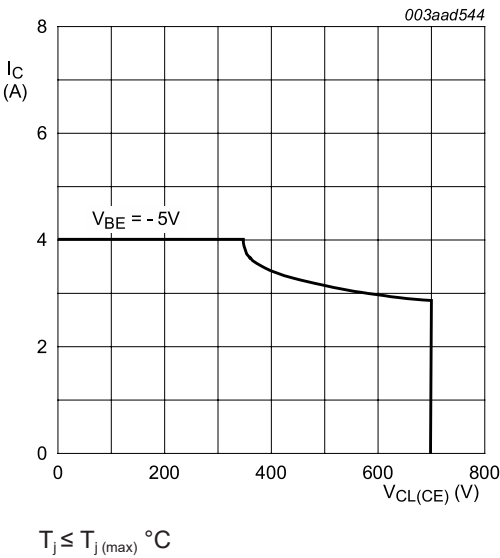
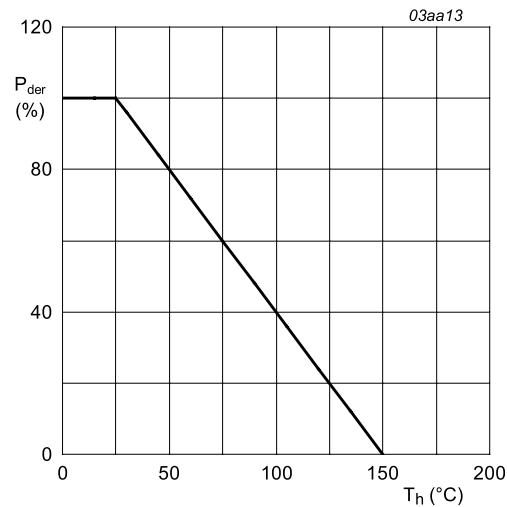
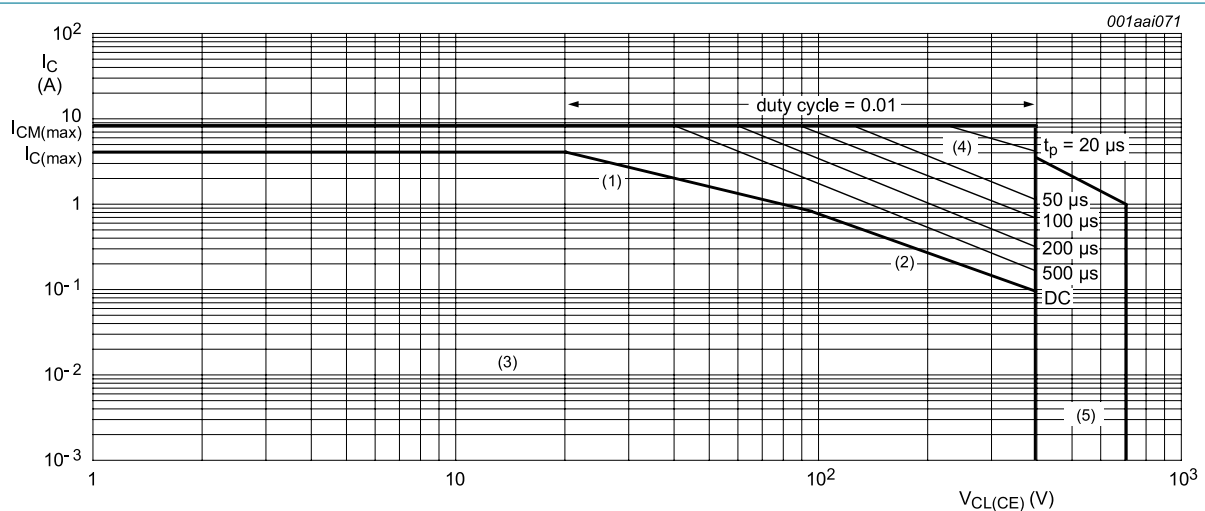


Fig. 2. Reverse bias safe operating area



$$P_{\text{der}}(\%) = \frac{P_{\text{tot}}}{P_{\text{tot}}(25^{\circ}\text{C})} \times 100\%$$

Fig. 3. Normalized total power dissipation as a function of heatsink temperature



$T_h \leq 25^{\circ}\text{C}$

Mounted with heatsink compound and (30 ± 5) N force on the centre of the envelope

(1) P_{tot} maximum and P_{tot} peak maximum lines

(2) Second breakdown limits

(3) Region of permissible DC operation

(4) Extension of operating region for repetitive pulse operation

(5) Extension of operating region during turn-on in single transistor converters provided that $R_{\text{BE}} \leq 100 \Omega$ and

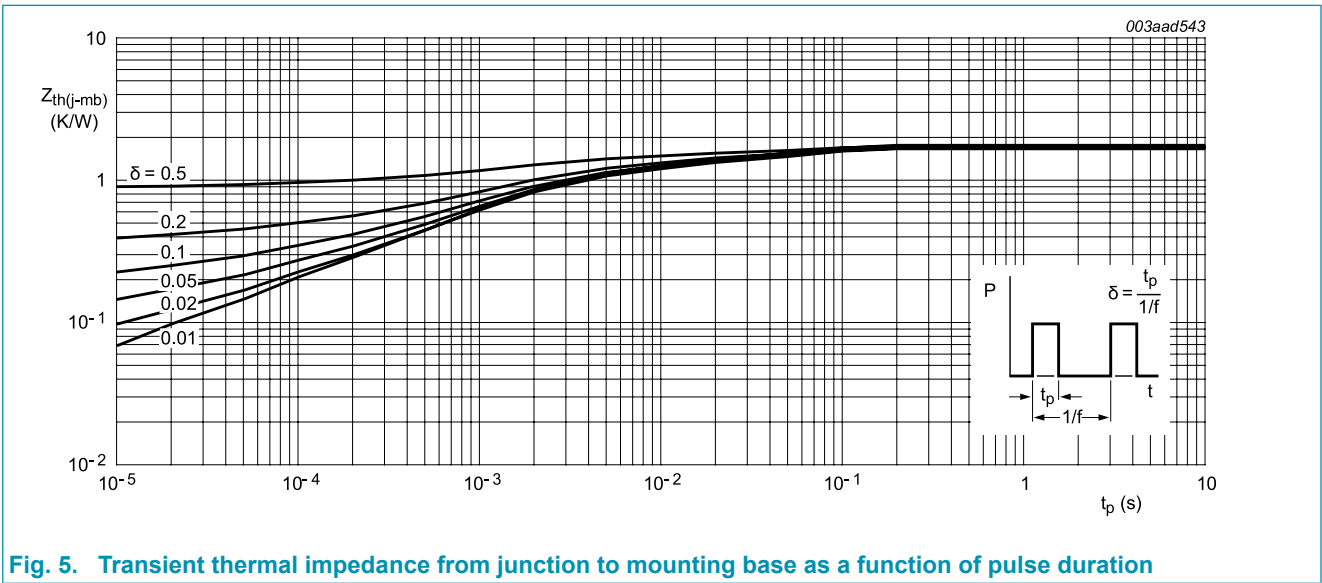
$t_p \leq 0.6 \mu\text{s}$

Fig. 4. Forward bias safe operating area

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	-	1.67	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		-	60	-	K/W



9. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I _{CES}	collector-emitter cut-off current	V _{BE} = -1.5 V; V _{CE} = 700 V; T _{mb} = 25 °C		-	-	1	mA
		V _{BE} = -1.5 V; V _{CE} = 700 V; T _j = 125 °C		-	-	5	mA
I _{CBO}	collector-base cut-off current	V _{CB} = 700 V; I _E = 0 A; T _{mb} = 25 °C		-	-	1	mA
I _{CEO}	collector-emitter cut-off current	V _{CEO} = 400 V; I _B = 0 A; T _{mb} = 25 °C		-	-	0.1	mA
I _{EBO}	emitter-base cut-off current	V _{EB} = 9 V; I _C = 0 A; T _{mb} = 25 °C		-	-	1	mA
V _{CEOsus}	collector-emitter sustaining voltage	I _B = 0 A; I _C = 10 mA; L _C = 25 mH; T _{mb} = 25 °C; Fig. 6 ; Fig. 7		400	-	-	V
V _{CEsat}	collector-emitter saturation voltage	I _C = 1.0 A; I _B = 0.2 A; T _{mb} = 25 °C; Fig. 8 ; Fig. 9		-	0.1	0.5	V
		I _C = 2.0 A; I _B = 0.5 A; T _{mb} = 25 °C; Fig. 8 ; Fig. 9		-	0.2	0.6	V
		I _C = 4.0 A; I _B = 1.0 A; T _{mb} = 25 °C; Fig. 8 ; Fig. 9		-	0.3	1	V
V _{BEsat}	base-emitter saturation voltage	I _C = 1.0 A; I _B = 0.2 A; T _{mb} = 25 °C; Fig. 10		-	0.85	1.2	V
		I _C = 2.0 A; I _B = 0.5 A; T _{mb} = 25 °C; Fig. 10		-	0.92	1.6	V
h _{FE}	DC current gain	I _C = 1 A; V _{CE} = 5 V; T _{mb} = 25 °C; Fig. 11		12	20	40	
		I _C = 2 A; V _{CE} = 5 V; T _{mb} = 25 °C; Fig. 11		10	17	28	
Dynamic characteristics							
t _s	storage time	I _C = 2 A; I _{Bon} = 0.4 A; I _{Boff} = -0.4 A; R _L = 75 Ω; T _{mb} = 25 °C; resistive load; Fig. 12 ; Fig. 13		-	2.7	4	μs
		I _C = 2 A; I _{Bon} = 0.4 A; V _{BB} = -5 V; L _B = 1 μH; T _{mb} = 25 °C; inductive load; Fig. 14 ; Fig. 15		-	1.2	2	μs
		I _C = 2 A; I _{Bon} = 0.4 A; V _{BB} = -5 V; L _B = 1 μH; T _{mb} = 100 °C; inductive load; Fig. 14 ; Fig. 15		-	1.4	4	μs
t _f	fall time	I _C = 2 A; I _{Bon} = 0.4 A; I _{Boff} = -0.4 A; R _L = 75 Ω; T _{mb} = 25 °C; resistive load; Fig. 12 ; Fig. 13		-	0.3	0.9	μs
		I _C = 2 A; I _{Bon} = 0.4 A; V _{BB} = -5 V; L _B = 1 μH; T _{mb} = 25 °C; inductive load; Fig. 14 ; Fig. 15		-	0.1	0.5	μs
		I _C = 2 A; I _{Bon} = 0.4 A; V _{BB} = -5 V; L _B = 1 μH; T _{mb} = 100 °C; inductive load; Fig. 14 ; Fig. 15		-	0.16	0.9	μs

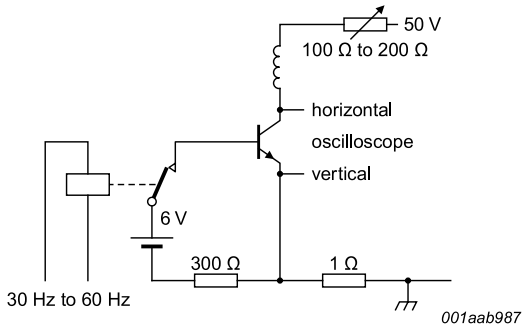


Fig. 6. Test circuit for collector-emitter sustaining voltage

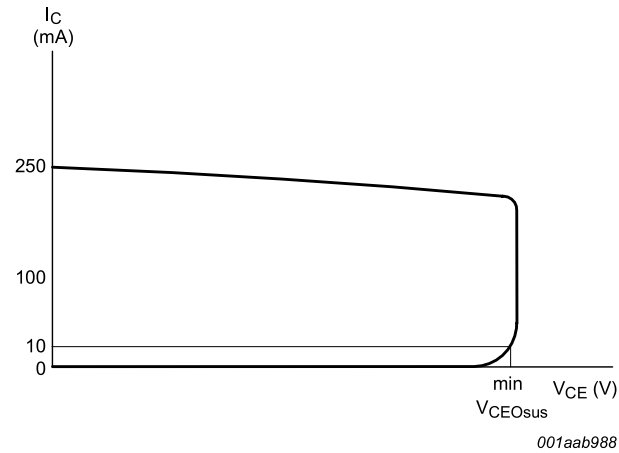


Fig. 7. Oscilloscope display for collector-emitter sustaining voltage test waveform

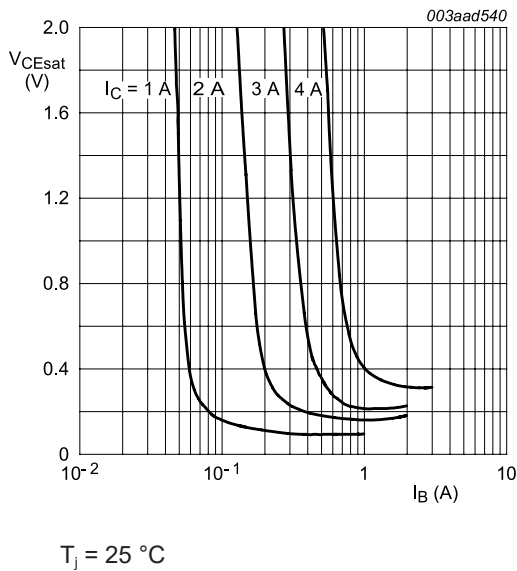


Fig. 8. Collector-emitter saturation voltage; typical values

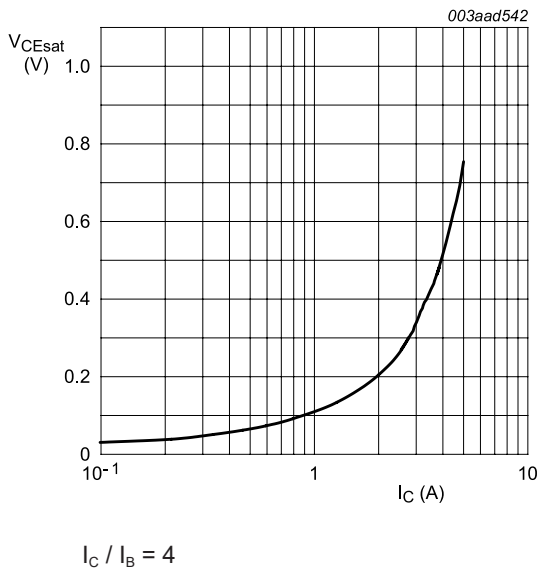


Fig. 9. Collector-emitter saturation voltage as a function of collector current; typical values

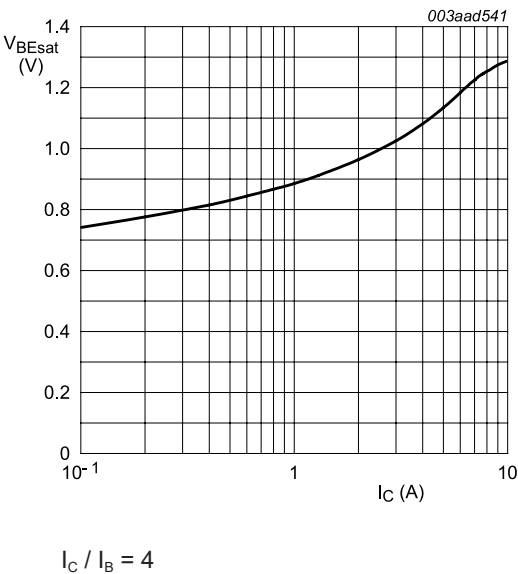


Fig. 10. Base-emitter saturation voltage; typical values

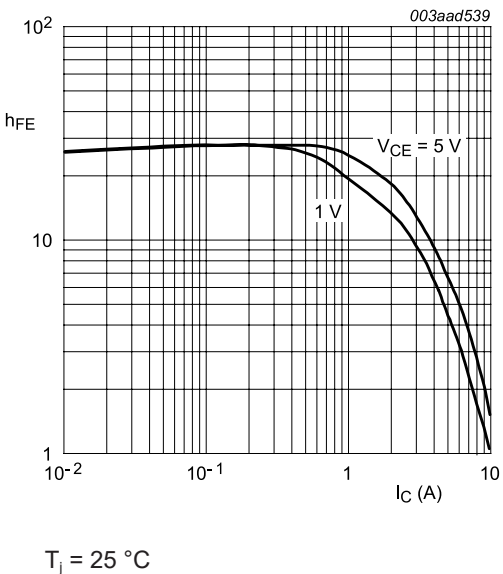
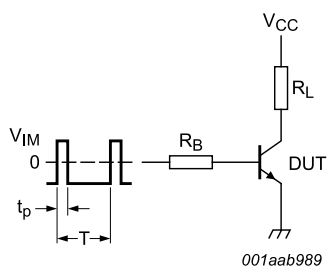


Fig. 11. DC current gain as a function of collector current; typical values



$V_{IM} = -6$ to $+8$ V; $V_{CC} = 250$ V; $t_p = 20\text{ }\mu\text{s}$;
 $\delta = t_p / T = 0.01$
 R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig. 12. Test circuit for resistive load switching

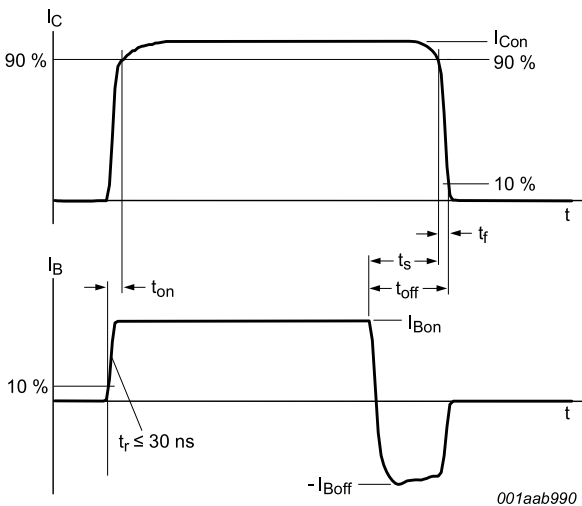
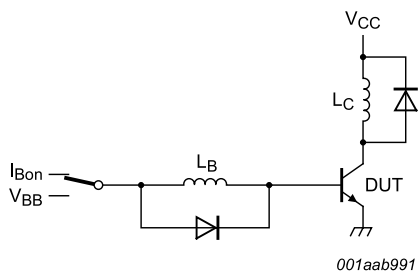


Fig. 13. Switching times waveforms for resistive load



$V_{CC} = 300\text{ V}$; $V_{BB} = -5\text{ V}$; $L_C = 200\text{ }\mu\text{H}$; $L_B = 1\text{ }\mu\text{H}$

Fig. 14. Test circuit for inductive load switching

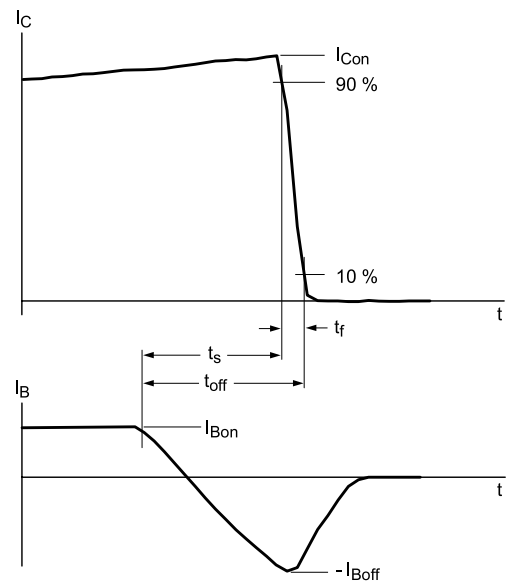


Fig. 15. Switching times waveforms for inductive load

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