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# 24 MHz Rail-to-Rail Amplifiers with Shutdown Option

# AD8646/AD8647/AD8648

## FEATURES

**Offset voltage: 2.5 mV maximum**
**Single-supply operation: 2.7 V to 5.5 V**
**Low noise: 8 nV/√Hz**
**Wide bandwidth: 24 MHz**
**Slew rate: 11 V/µs**
**Short-circuit output current: 120 mA**
**No phase reversal**
**Low input bias current: 1 pA**
**Low supply current per amplifier: 2 mA maximum**
**Unity gain stable**

## APPLICATIONS

**Battery-powered instruments**
**Multipole filters**
**ADC front ends**
**Sensors**
**Barcode scanners**
**ASIC input or output amplifiers**
**Audio amplifiers**
**Photodiode amplifiers**
**Datapath/mux/switch control**

## PIN CONFIGURATIONS

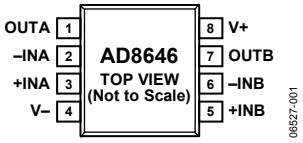



*Figure 1. 8-Lead SOIC and MSOP*

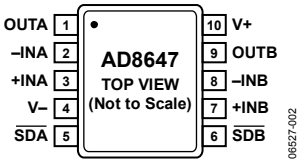



*Figure 2. 10-Lead MSOP*

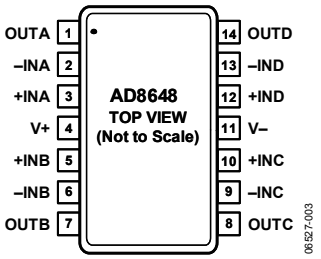



*Figure 3. 14-Lead SOIC and TSSOP*

## GENERAL DESCRIPTION

The AD8646 and the AD8647 are the dual, and the AD8648 is the quad, rail-to-rail, input and output, single-supply amplifiers featuring low offset voltage, wide signal bandwidth, low input voltage, and low current noise. The AD8647 also has a low power shutdown function.

The combination of 24 MHz bandwidth, low offset, low noise, and very low input bias current makes these amplifiers useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from the combination of performance features. AC applications benefit from the wide bandwidth and low distortion. TheAD8646/AD8647/AD8648 offer high output drive capability, which is excellent for audio line drivers and other low impedance applications.

Applications include portable and low powered instrumentation, audio amplification for portable devices, portable phone headsets, barcode scanners, and multipole filters. The ability to swing rail to rail at both the input and output enables designers to buffer CMOS ADCs, DACs, ASICs, and other wide output swing devices in single-supply systems.

**Rev. B**
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## REVISION HISTORY

***Revision History: AD8646/AD8647/AD8648***

**10/07—Revision B: Initial Combined Version**

***Revision History: AD8646***

**10/07—Rev. 0 to Rev. B**

Combined with AD8648 ..... Universal
Added AD8647 ..... Universal
Deleted Figure 4 and Figure 7 ..... 7
Deleted Figure 33 ..... 11

**8/07—Revision 0: Initial Version**

***Revision History: AD8648***

**10/07—Rev. A to Rev. B**

Combined with AD8646 ..... Universal
Added AD8647 ..... Universal
Deleted Figure 7 ..... 6
Deleted Figure 11 ..... 7
Deleted Figure 16 and Figure 17 ..... 8
Deleted Figure 24 ..... 9
Deleted Figure 27, Figure 28, Figure 31, and Figure 32 ..... 10

**6/07—Rev. 0 to Rev. A**

Changes to General Description ..... 1
Updated Outline Dimensions ..... 12
Changes to Ordering Guide ..... 12

**1/06—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{SY}$ = 5 V, $V_{CM}$ = $V_{SY}$/2, $T_A$ = +25°C, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | $V_{OS}$ | $V_{CM}$ = 0 V to 5V | | 0.6 | 2.5 | mV |
| | | −40°C < $T_A$ < +125°C | | | 3.2 | mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | −40°C < $T_A$ < +125°C | | 1.8 | 7.5 | µV/°C |
| Input Bias Current | $I_B$ | | | 0.3 | 1 | pA |
| | | −40°C < $T_A$ < +85°C | | | 50 | pA |
| | | −40°C < $T_A$ < +125°C | | | 550 | pA |
| Input Offset Current | $I_{OS}$ | | | 0.1 | 0.5 | pA |
| | | −40°C < $T_A$ < +85°C | | | 50 | pA |
| | | −40°C < $T_A$ < +125°C | | | 250 | pA |
| Input Voltage Range | $V_{CM}$ | | 0 | | 5 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = 0 V to 5 V | 67 | 84 | | dB |
| Large Signal Voltage Gain | $A_{VO}$ | $R_L$ = 2 kΩ, $V_O$ = 0.5 V to 4.5 V | 104 | 116 | | dB |
| Input Capacitance | | | | | | |
| Differential | $C_{DIFF}$ | | | 2.5 | | pF |
| Common Mode | $C_{CM}$ | | | 6.7 | | pF |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | $V_{OH}$ | $I_{OUT}$ = 1 mA | 4.98 | 4.99 | | V |
| | | −40°C < $T_A$ < +125°C | 4.90 | | | V |
| | | $I_{OUT}$ = 10 mA | 4.85 | 4.92 | | V |
| | | −40°C < $T_A$ < +125°C | 4.70 | | | V |
| Output Voltage Low | $V_{OL}$ | $I_{OUT}$ = 1 mA | | 8.4 | 20 | mV |
| | | −40°C < $T_A$ < +125°C | | | 40 | mV |
| | | $I_{OUT}$ = 10 mA | | 78 | 145 | mV |
| | | −40°C < $T_A$ < +125°C | | | 200 | mV |
| Output Current | $I_{sc}$ | Short circuit | | ±120 | | mA |
| Closed-Loop Output Impedance | $Z_{OUT}$ | At 1 MHz, $A_V$ = 1 | | 5 | | Ω |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_{SY}$ = 2.7 V to 5.5 V | 63 | 80 | | dB |
| Supply Current per Amplifier | $I_{SY}$ | | | 1.5 | 2.0 | mA |
| | | −40°C < $T_A$ < +125°C | | | 2.5 | mA |
| Supply Current Shutdown Mode (AD8647) | $I_{SD}$ | Shutdown of both amplifiers (AD8647 only) | | 10 | | nA |
| | | −40°C < $T_A$ < +125°C | | | 1 | µA |
| SHUTDOWN INPUTS (AD8647) | | | | | | |
| Logic High Voltage (Enabled) | $V_{INH}$ | −40°C < $T_A$ < +125°C | +2.0 | | | V |
| Logic Low Voltage (Power-Down) | $V_{INL}$ | −40°C < $T_A$ < +125°C | | | +0.8 | V |
| Logic Input Current (Per Pin) | $I_{IN}$ | −40°C < $T_A$ < +125°C | | | 1 | µA |
| Output Pin Leakage Current | | −40°C < $T_A$ < +125°C (shutdown active) | | 1 | | nA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L$ = 2 kΩ | | 11 | | V/µs |
| Gain Bandwidth Product | GBP | | | 24 | | MHz |
| Phase Margin | $Ø_m$ | | | 74 | | Degrees |
| Settling Time | $t_s$ | To 0.1% | | 0.5 | | µs |
| Amplifier Turn-On Time (AD8647) | $t_{on}$ | 25°C, $A_V$ = 1, $R_L$ = 1 kΩ (see Figure 44) | | 1 | | µs |
| Amplifier Turn-Off Time (AD8647) | $t_{off}$ | 25°C, $A_V$ = 1, $R_L$ = 1 kΩ (see Figure 45) | | 1 | | µs |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| NOISE PERFORMANCE | | | | | | |
| Peak-to-Peak Noise | $e_n$ p-p | 0.1 Hz to 10 Hz | | 2.3 | | μV |
| Voltage Noise Density | $e_n$ | f = 1 kHz | | 8 | | nV/√Hz |
| | | f = 10 kHz | | 6 | | nV/√Hz |
| Channel Separation | CS | f = 10 kHz | | −115 | | dB |
| | | f = 100 kHz | | −110 | | dB |
| Total Harmonic Distortion Plus Noise | THD + N | V p-p = 0.1 V, $R_L$ = 600 Ω, f = 25 kHz, $T_A$ = 25°C | | | | |
| | | $A_V$ = +1 | | 0.010 | | % |
| | | $A_V$ = −10 | | 0.021 | | % |

$V_{SY}$ = 2.7 V, $V_{CM}$ = $V_{SY}$/2, $T_A$ = +25°C, unless otherwise noted.

**Table 2.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | $V_{OS}$ | $V_{CM}$ = 0 V to 2.7 V | | 0.6 | 2.5 | mV |
| | | −40°C < $T_A$ < +125°C | | | 3.2 | mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | −40°C < $T_A$ < +125°C | | 1.8 | 7.0 | µV/°C |
| Input Bias Current | $I_B$ | | | 0.2 | 1 | pA |
| | | −40°C < $T_A$ < +85°C | | | 50 | pA |
| | | −40°C < $T_A$ < +125°C | | | 550 | pA |
| Input Offset Current | $I_{OS}$ | | | 0.1 | 0.5 | pA |
| | | −40°C < $T_A$ < +85°C | | | 50 | pA |
| | | −40°C < $T_A$ < +125°C | | | 250 | pA |
| Input Voltage Range | $V_{CM}$ | | 0 | | 2.7 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = 0 V to 2.7 V | 62 | 79 | | dB |
| Large Signal Voltage Gain | $A_{VO}$ | $R_L$ = 2 kΩ, $V_O$ = 0.5 V to 2.2 V | 95 | 102 | | dB |
| Input Capacitance | | | | | | |
| Differential | $C_{DIFF}$ | | | 2.5 | | pF |
| Common Mode | $C_{CM}$ | | | 7.8 | | pF |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | $V_{OH}$ | $I_{OUT}$ = 1 mA | 2.65 | 2.68 | | V |
| | | −40°C < $T_A$ < +125°C | 2.60 | | | V |
| Output Voltage Low | $V_{OL}$ | $I_{OUT}$ = 1 mA | | 11 | 25 | mV |
| | | −40°C < $T_A$ < +125°C | | | 30 | mV |
| Output Current | $I_{OUT}$ | Short circuit | | ±63 | | mA |
| Closed-Loop Output Impedance | $Z_{OUT}$ | At 1 MHz, $A_V$ = 1 | | 5 | | Ω |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_{SY}$ = 2.7 V to 5.5 V | 63 | 80 | | dB |
| Supply Current per Amplifier | $I_{SY}$ | | | 1.6 | 2.0 | mA |
| | | −40°C < $T_A$ < +125°C | | | 2.5 | mA |
| Supply Current Shutdown Mode (AD8647) | $I_{SD}$ | Shutdown of both amplifiers (AD8647 only) | | 10 | | nA |
| | | −40°C < $T_A$ < +125°C | | | 1 | µA |
| SHUTDOWN INPUTS (AD8647) | | | | | | |
| Logic High Voltage (Enabled) | $V_{INH}$ | −40°C < $T_A$ < +125°C | +2.0 | | | V |
| Logic Low Voltage (Power-Down) | $V_{INL}$ | −40°C < $T_A$ < +125°C | | | +0.8 | V |
| Logic Input Current (Per Pin) | $V_{IN}$ | −40°C < $T_A$ < +125°C | | | 1 | µA |
| Output Pin Leakage Current | | −40°C < $T_A$ < +125°C (shutdown active) | | 1 | | nA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L$ = 2 kΩ | | 11 | | V/µs |
| Gain Bandwidth Product | GBP | | | 24 | | MHz |
| Phase Margin | $Ø_m$ | | | 53 | | Degrees |
| Settling Time | $t_s$ | To 0.1% | | 0.3 | | µs |
| Amplifier Turn-On Time (AD8647) | $t_{on}$ | 25°C, $A_V$ = 1, $R_L$ = 1 kΩ (see Figure 41) | | 1.2 | | µs |
| Amplifier Turn-Off Time (AD8647) | $t_{off}$ | 25°C, $A_V$ = 1, $R_L$ = 1 kΩ (see Figure 42) | | 1 | | µs |
| NOISE PERFORMANCE | | | | | | |
| Peak-to-Peak Noise | $e_n$ p-p | 0.1 Hz to 10 Hz | | 2.3 | | µV |
| Voltage Noise Density | $e_n$ | f = 1 kHz | | 8 | | nV/√Hz |
| | | f = 10 kHz | | 6 | | nV/√Hz |
| Channel Separation | CS | f = 10 kHz | | −115 | | dB |
| | | f = 100 kHz | | −110 | | dB |

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 6 V |
| Input Voltage | GND to $V_{SY}$ |
| Differential Input Voltage | ±3 V |
| Output Short Circuit to GND | Indefinite |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | −40°C to +125°C |
| Lead Temperature (Soldering 60 sec) | 300°C |
| Junction Temperature | 150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 4. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 8-Lead SOIC_N | 125 | 43 | °C/W |
| 8-Lead MSOP | 210 | 45 | °C/W |
| 10-Lead MSOP | 200 | 44 | °C/W |
| 14-Lead SOIC_N | 120 | 36 | °C/W |
| 14-Lead TSSOP | 180 | 35 | °C/W |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

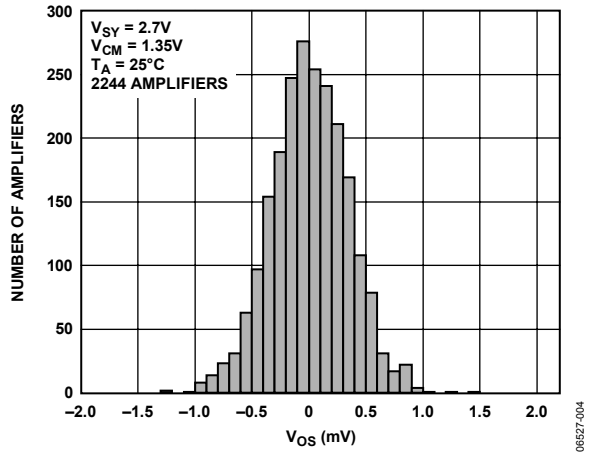



Figure 4. Input Offset Voltage Distribution

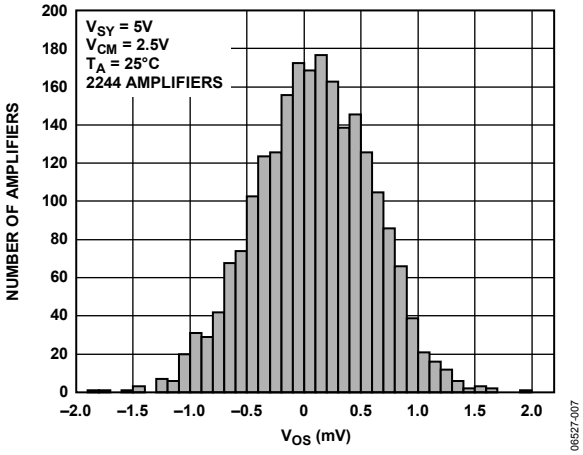



Figure 7. Input Offset Voltage Distribution

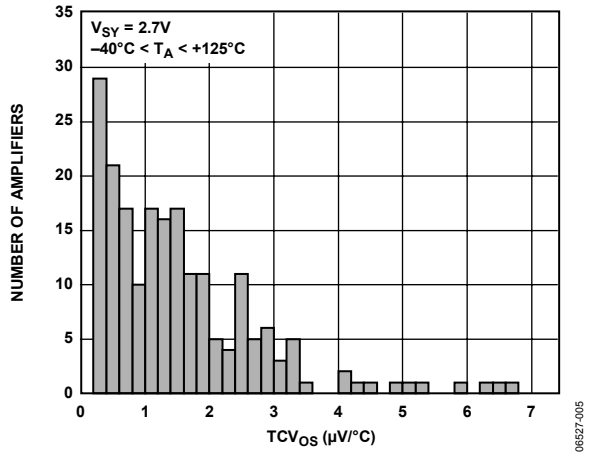



Figure 5. $V_{OS}$ Drift ($TCV_{OS}$) Distribution

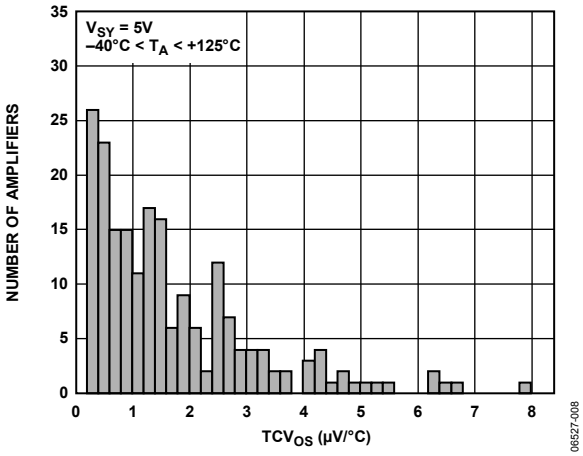



Figure 8. $V_{OS}$ Drift ($TCV_{OS}$) Distribution

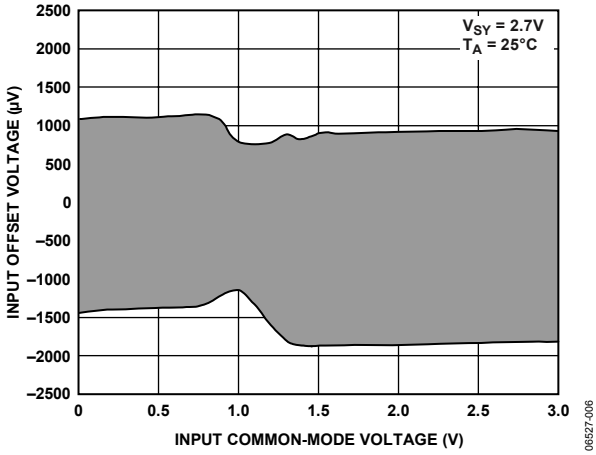



Figure 6. Input Offset Voltage vs. Input Common-Mode Voltage

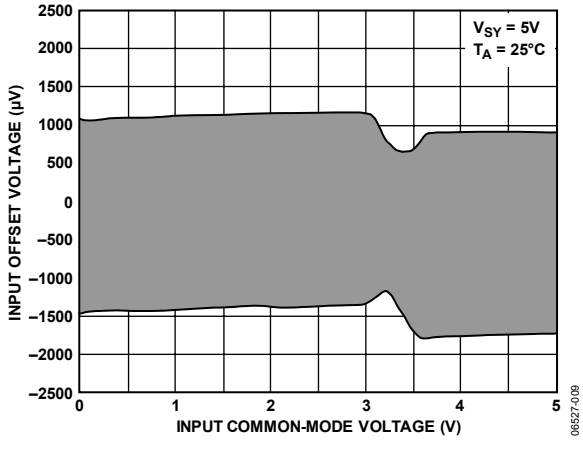



Figure 9. Input Offset Voltage vs. Input Common-Mode Voltage

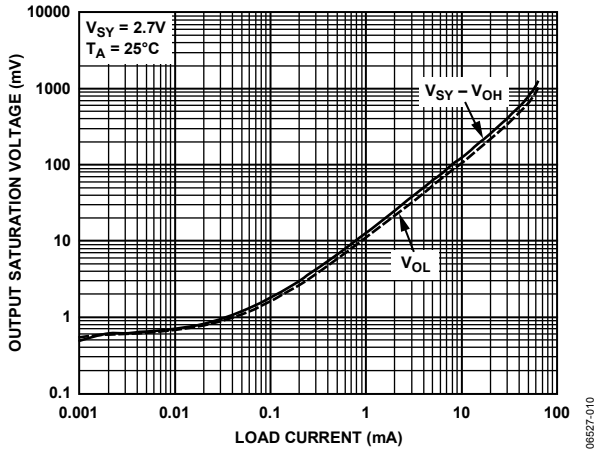



*Figure 10. Output Saturation Voltage vs. Load Current*

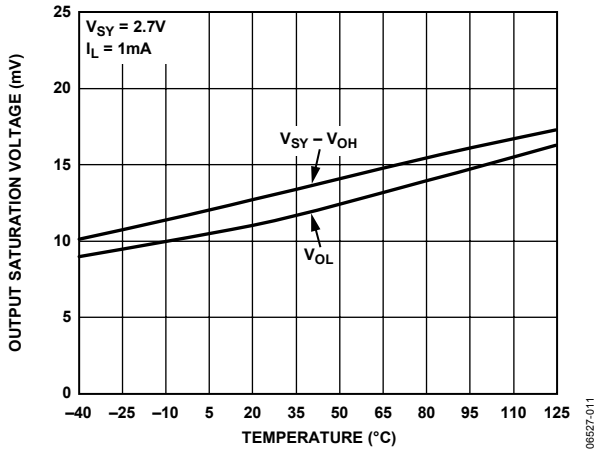



*Figure 11. Output Saturation Voltage vs. Temperature*

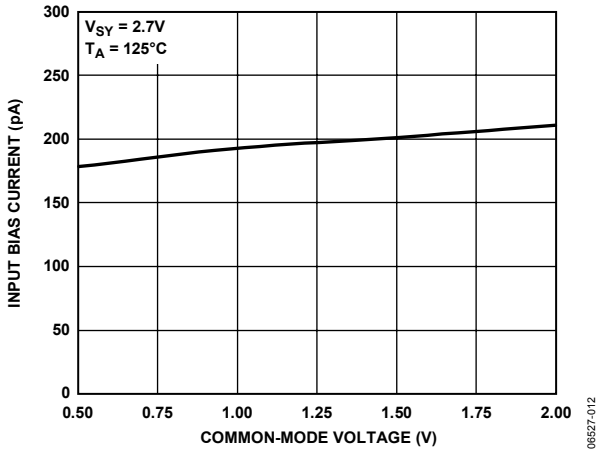



*Figure 12. Input Bias Current vs. Common-Mode Voltage*

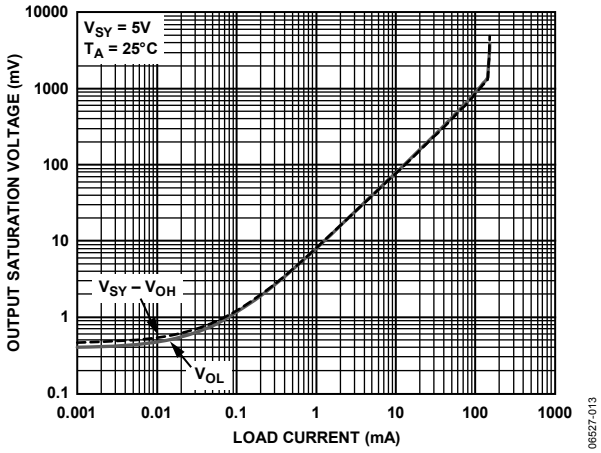



*Figure 13. Output Saturation Voltage vs. Load Current*

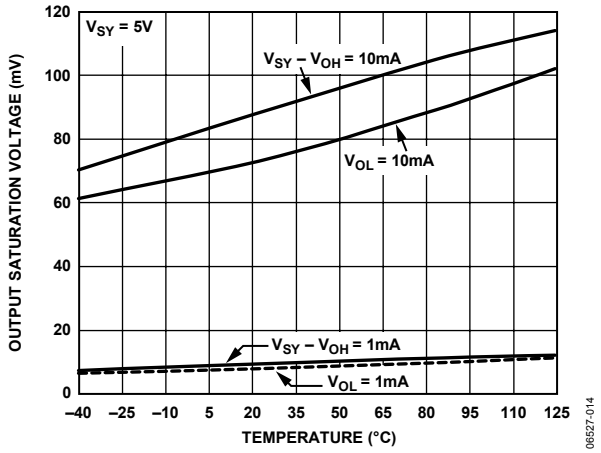



*Figure 14. Output Saturation Voltage vs. Temperature*

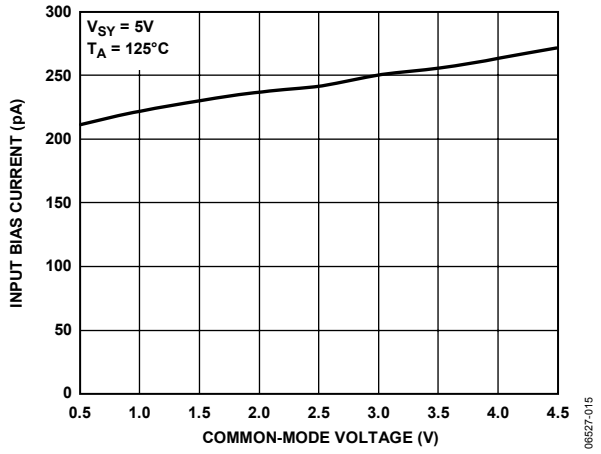



*Figure 15. Input Bias Current vs. Common-Mode Voltage*

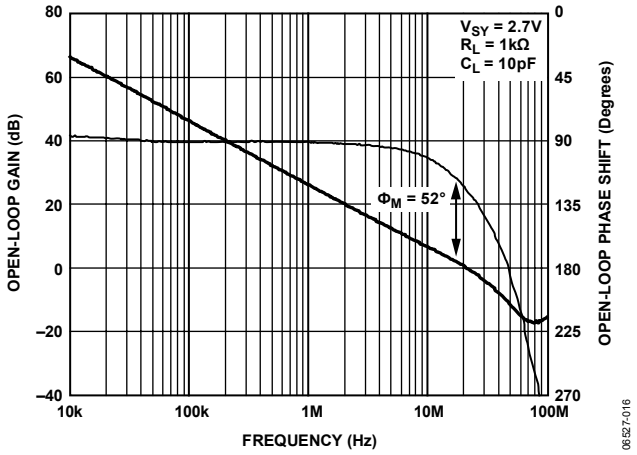



Figure 16. Open-Loop Gain and Phase vs. Frequency

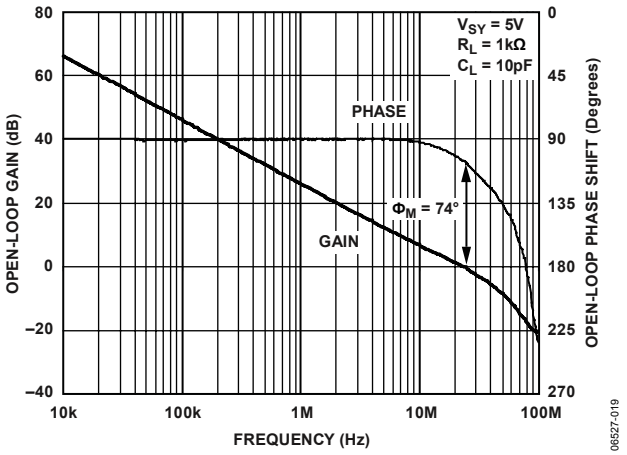



Figure 19. Open-Loop Gain and Phase vs. Frequency

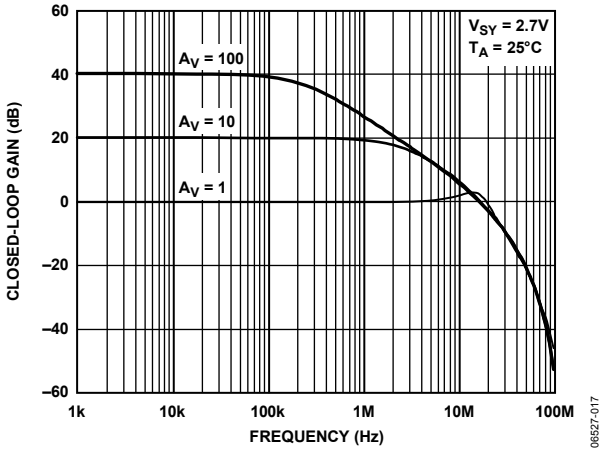



Figure 17. Closed-Loop Gain vs. Frequency

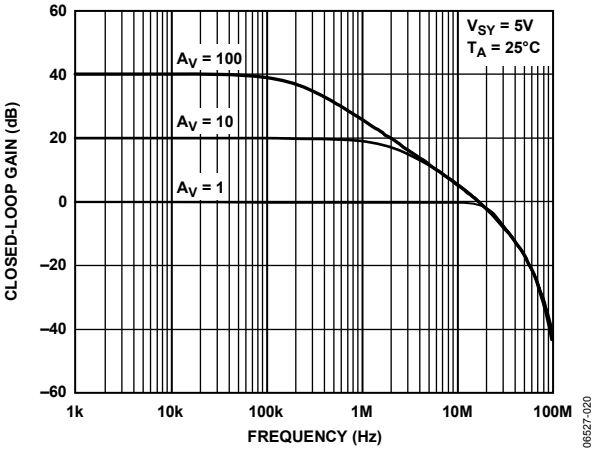



Figure 20. Closed-Loop Gain vs. Frequency

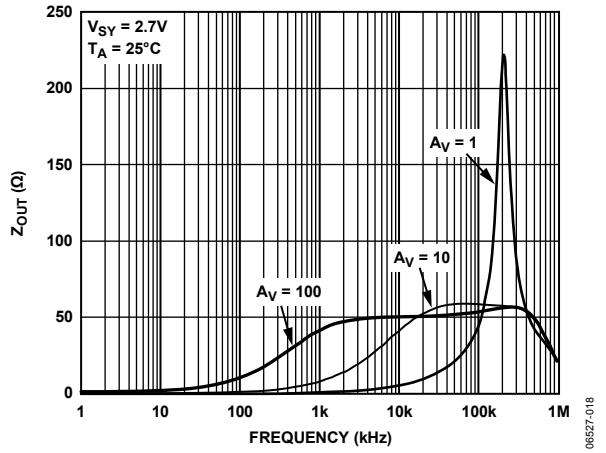



Figure 18. $Z_{OUT}$ vs. Frequency

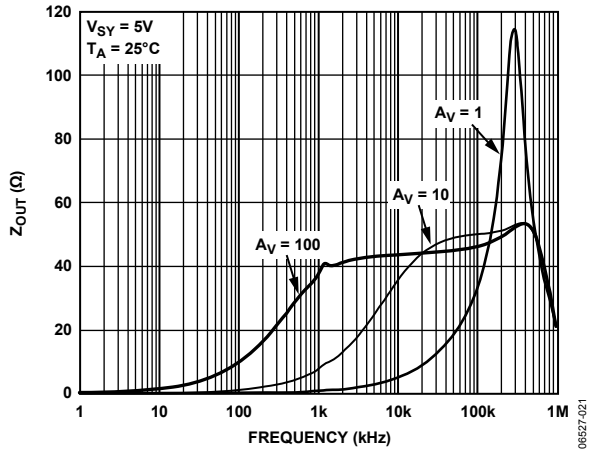



Figure 21. $Z_{OUT}$ vs. Frequency

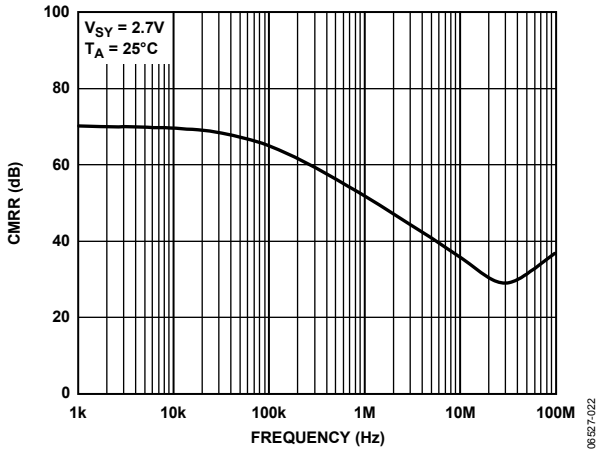



Figure 22. CMRR vs. Frequency

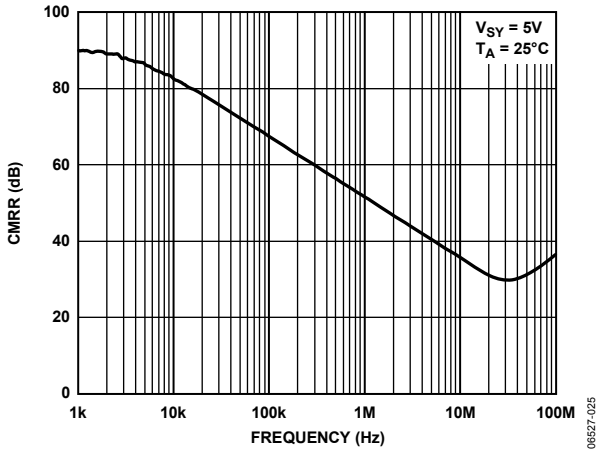



Figure 25. CMRR vs. Frequency

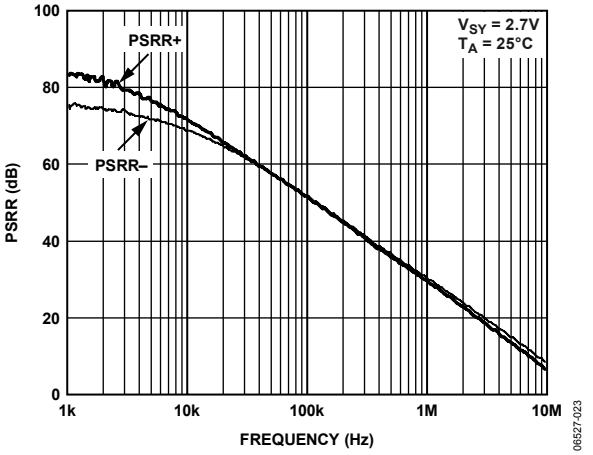



Figure 23. PSRR vs. Frequency

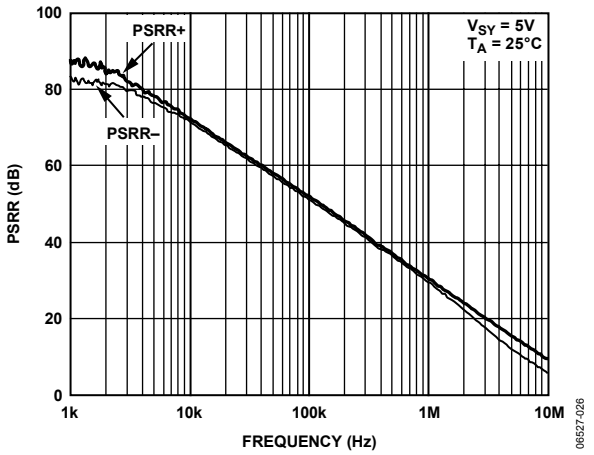



Figure 26. PSRR vs. Frequency

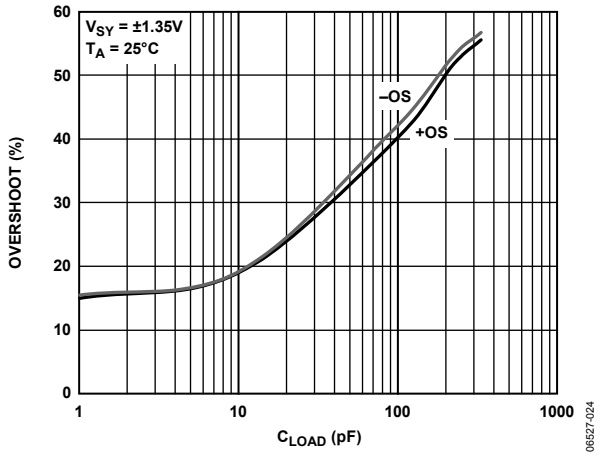



Figure 24. Overshoot vs. Load Capacitance

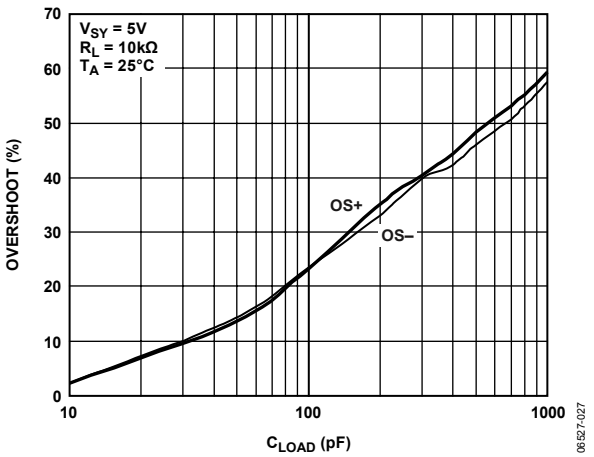



Figure 27. Overshoot vs. Load Capacitance

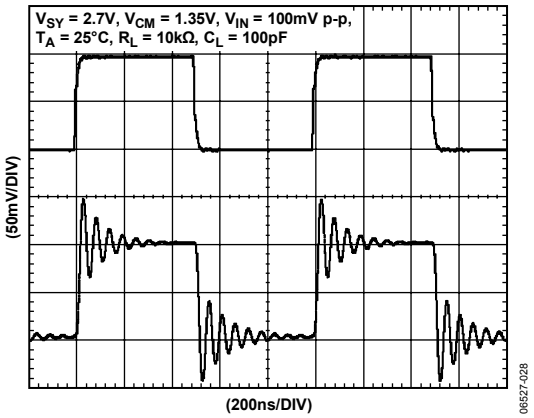



Figure 28. Small-Signal Transient Response

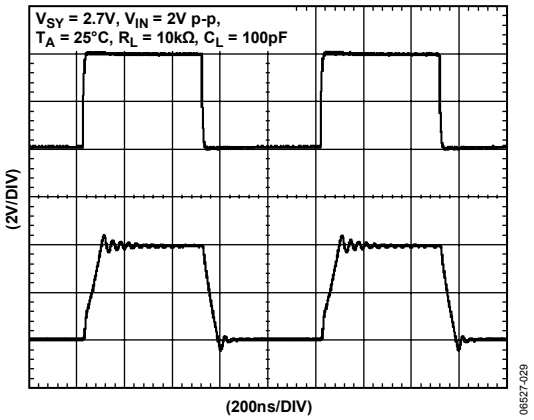



Figure 29. Large-Signal Transient Response

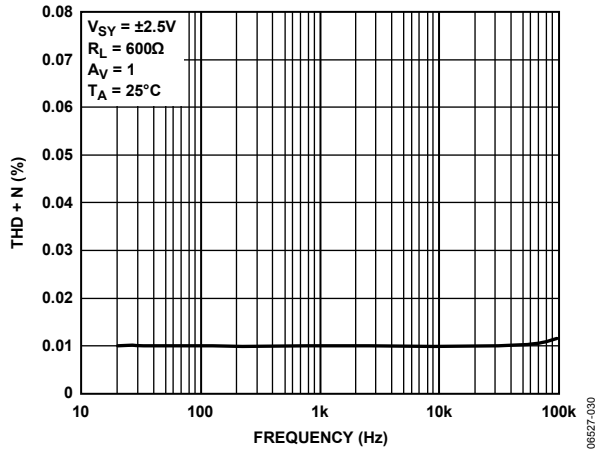



Figure 30. THD + Noise vs. Frequency

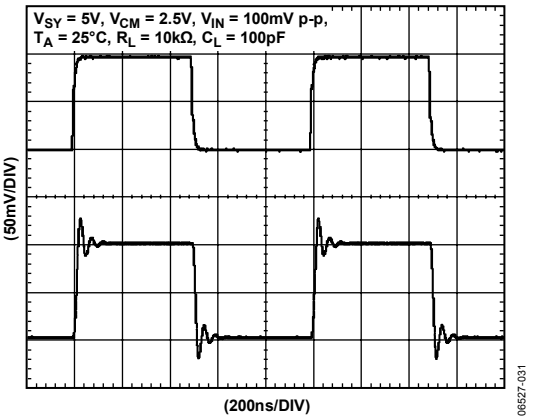



Figure 31. Small-Signal Transient Response

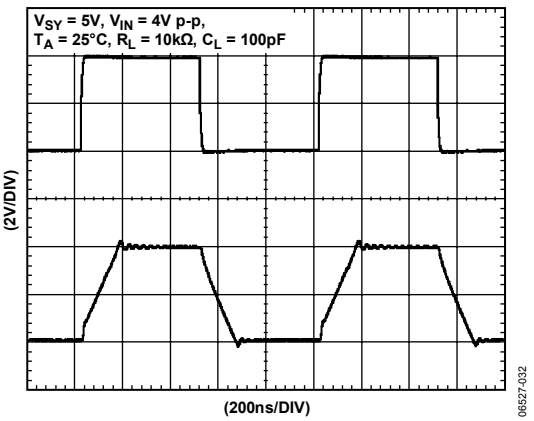



Figure 32. Large-Signal Transient Response

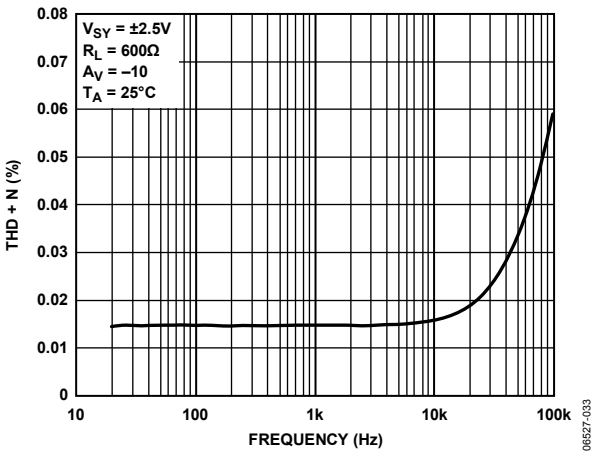



Figure 33. THD + Noise vs. Frequency

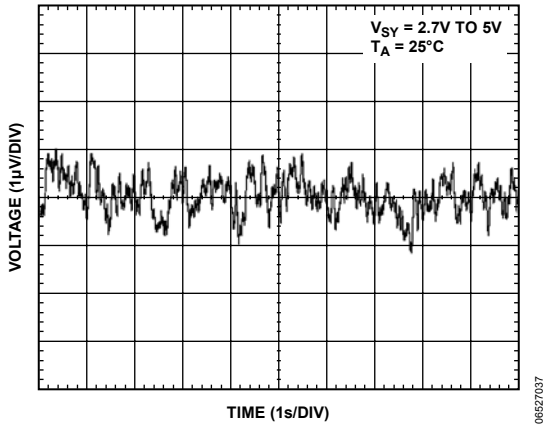



Figure 34. 0.1 Hz to 10 Hz Voltage Noise

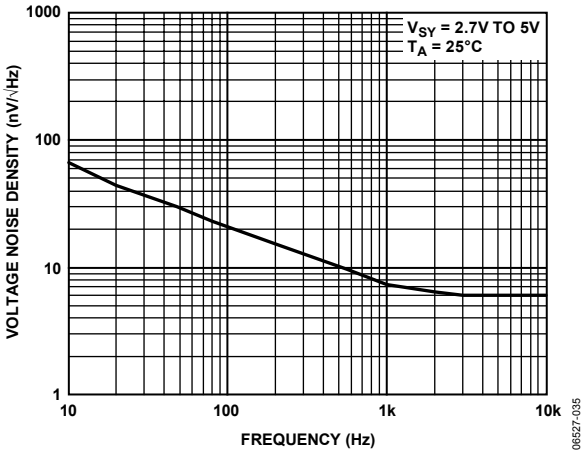



Figure 35. Voltage Noise Density vs. Frequency

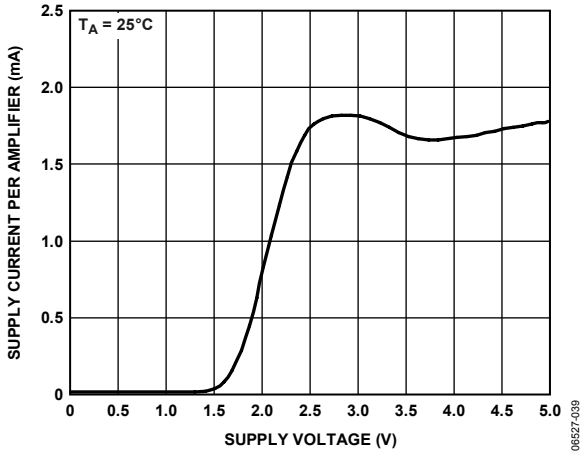



Figure 36. Supply Current per Amplifier vs. Supply Voltage

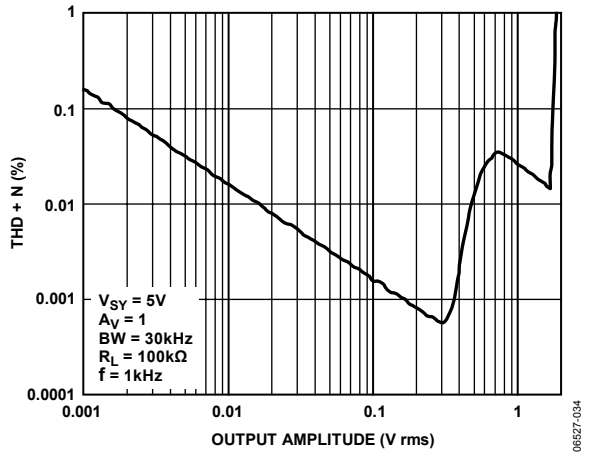



Figure 37. THD + Noise vs. Output Amplitude

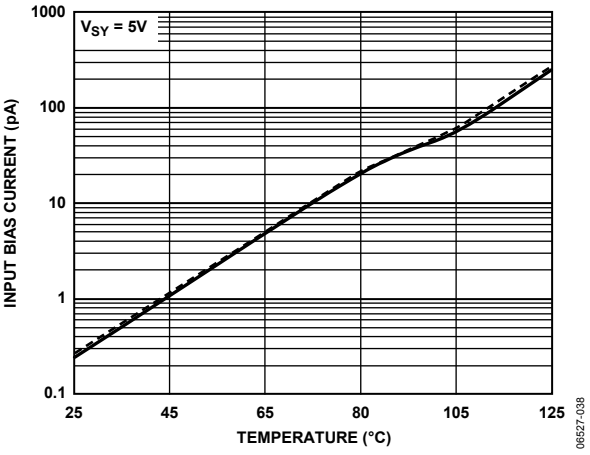



Figure 38. Input Bias Current vs. Temperature

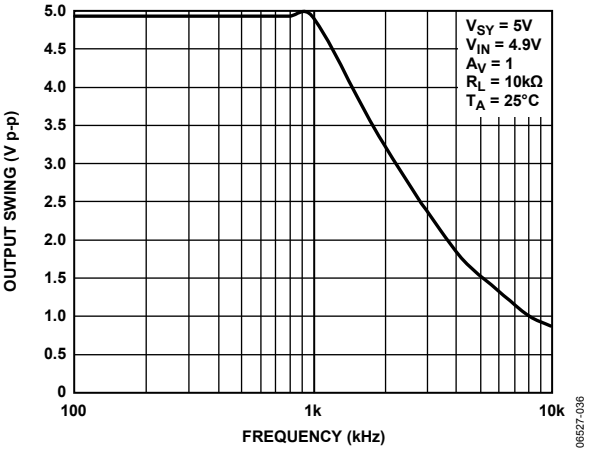



Figure 39. Maximum Output Swing vs. Frequency

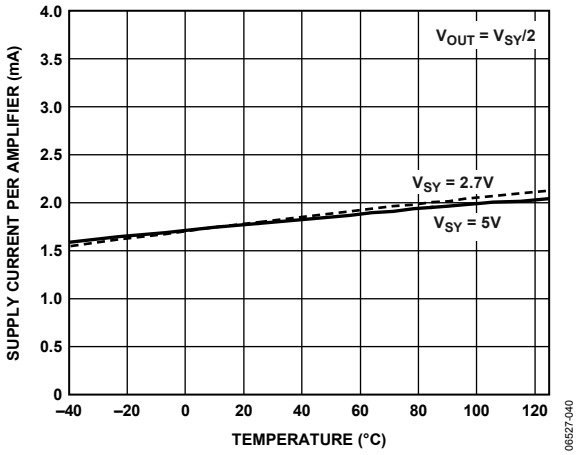



Figure 40. Supply Current per Amplifier vs. Temperature

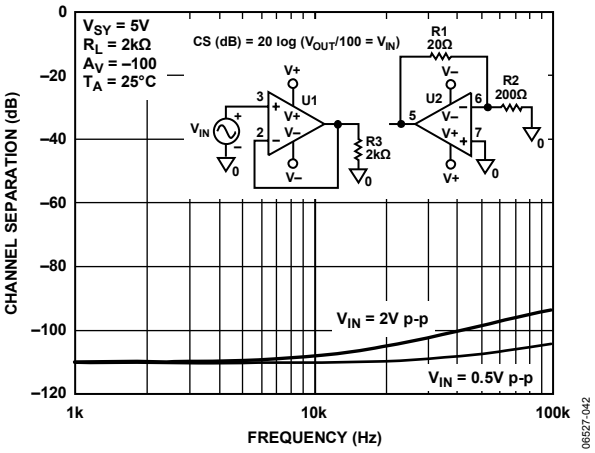



Figure 43. Channel Separation

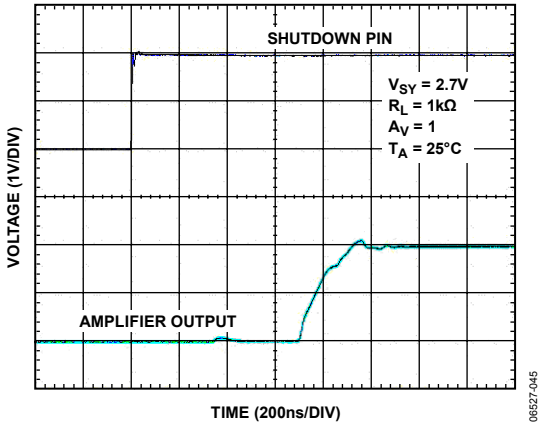



Figure 41. Turn-On Time

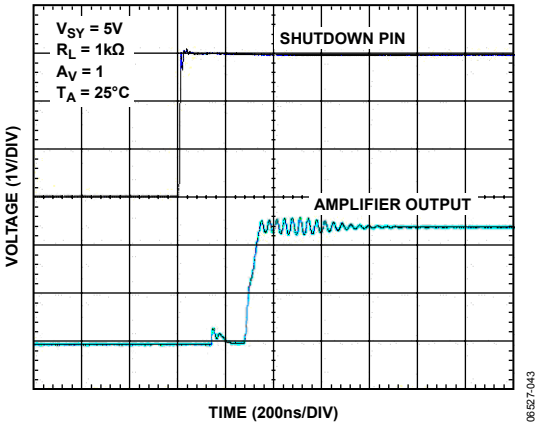



Figure 44. Turn-On Time

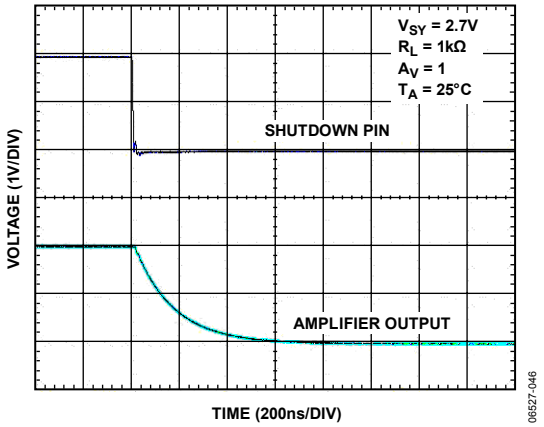



Figure 42. Turn-Off Time

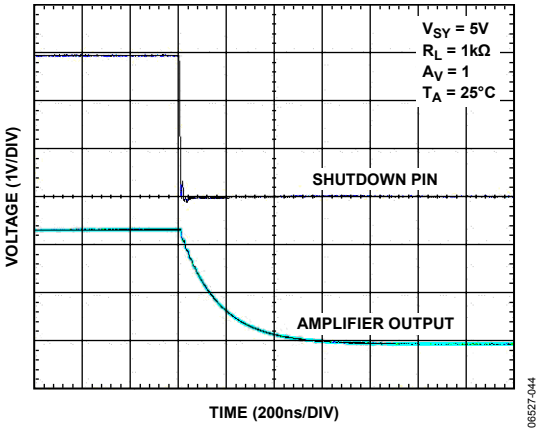



Figure 45. Turn-Off Time

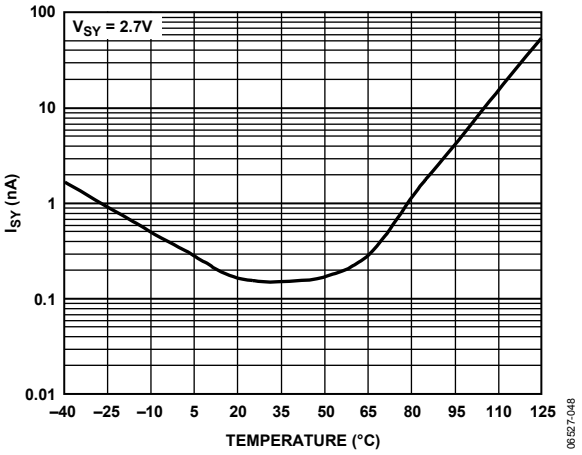



*Figure 46. Supply Current with Op-Amp Shutdown vs. Temperature*

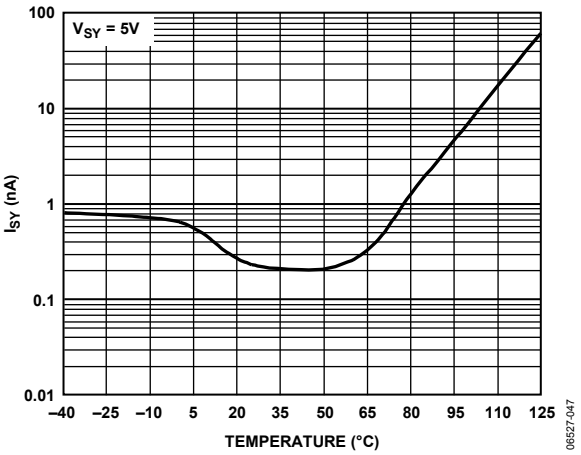



*Figure 47. Supply Current with Op-Amp Shutdown vs. Temperature*

# THEORY OF OPERATION

## POWER-DOWN OPERATION

The shutdown function of the AD8647 is referenced to the negative supply voltage of the operational amplifier. A logic level high (> 2.0 V) enables the device, while a logic level low (< 0.8 V) disables the device and places the output in a high impedance condition. Several outputs can be wire-OR'ed, thus eliminating a multiplexer. The logic input is a high impedance CMOS input. If dual or split supplies are used, the logic signals must be properly referred to the negative supply voltage.

## MULTIPLEXING OPERATION

Because each op amp has a separate logic input enable pin, the outputs can be connected together if it can be guaranteed that only one op amp is active at any time. By connecting the op amps as shown in Figure 48, a multiplexer can be eliminated. With the reasonably short turn-on and turn-off times, low frequency signal paths can be smoothly selected. The turn-off time is slightly faster than the turn-on time so, even when using sections from two different packages, the overlap is less than 300 nanoseconds.

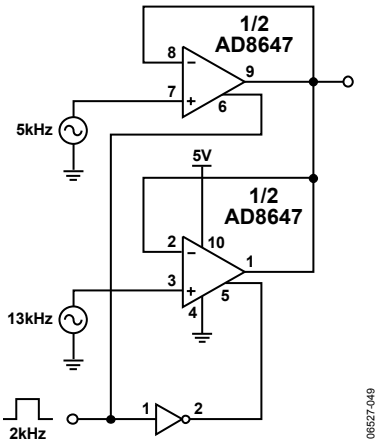



*Figure 48. AD8647 Output Switching*

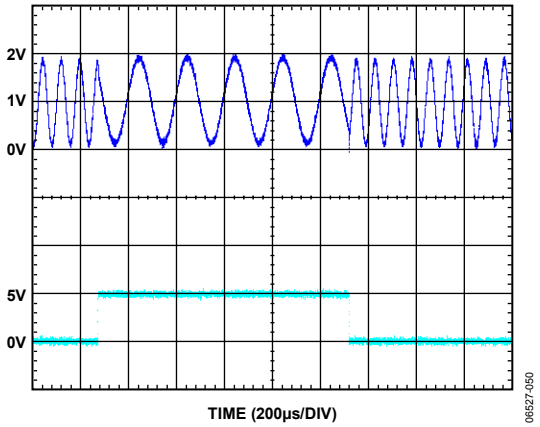
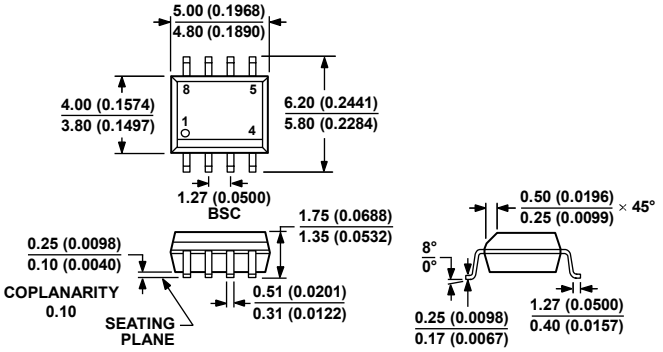



*Figure 49. Switching Waveforms*

# OUTLINE DIMENSIONS

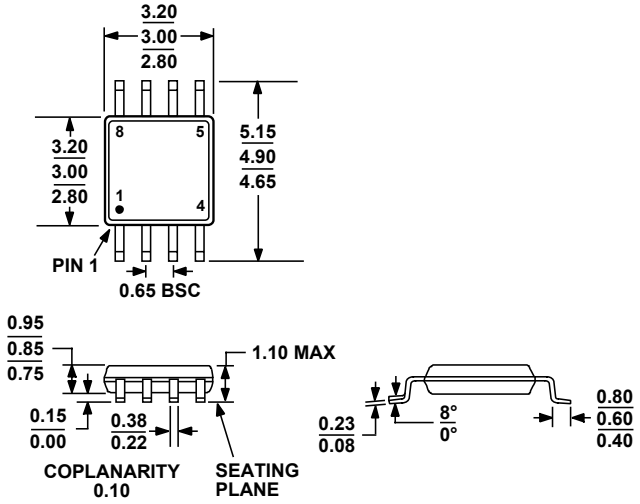



**COMPLIANT TO JEDEC STANDARDS MS-012-AA**

**CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.**

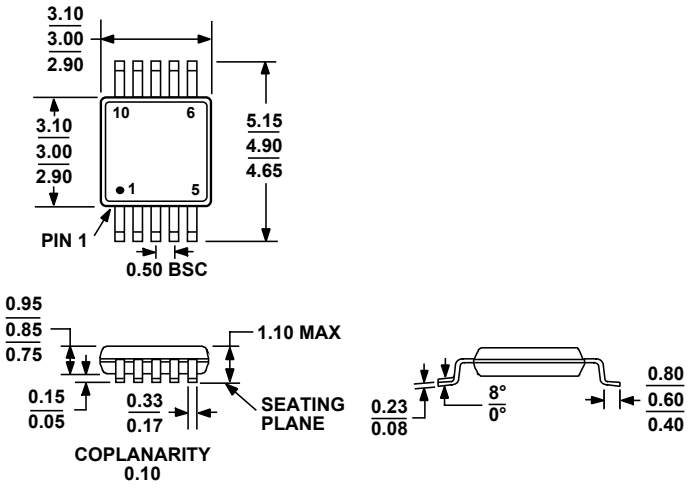
012407-A

*Figure 50. 8-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*(R-8)*
*Dimensions shown in millimeters and (inches)*



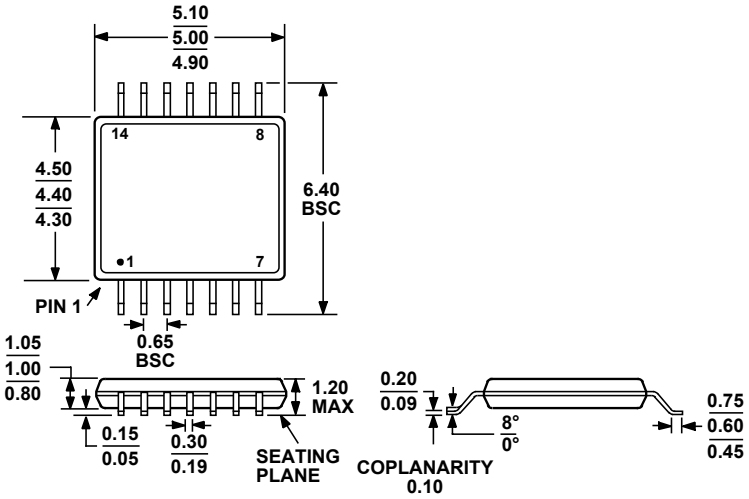

**COMPLIANT TO JEDEC STANDARDS MO-187-AA**

*Figure 51. 8-Lead Mini Small Outline Package [MSOP]*
*(RM-8)*
*Dimensions shown in millimeters*



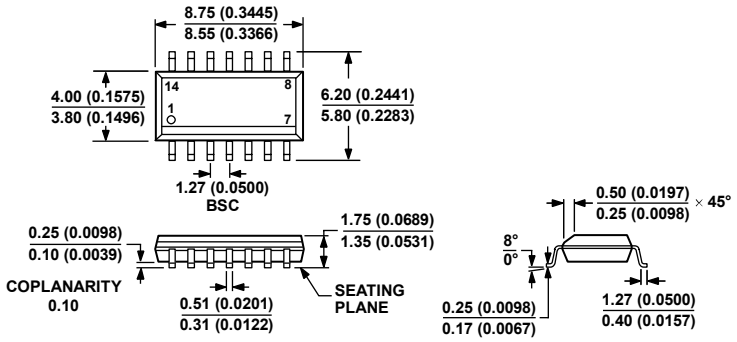

COMPLIANT TO JEDEC STANDARDS MO-187-BA

*Figure 52. 10 Lead Mini Small Outline Package [MSOP]*
*(RM-10)*
*Dimensions shown in millimeters*




COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

*Figure 53. 14-Lead Thin Shrink Small Outline Package [TSSOP]*
*(RU-14)*
*Dimensions shown in millimeters*




COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

*Figure 54. 14-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*(R-14)*
*Dimensions shown in millimeters and (inches)*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|
| AD8646ARZ[1] | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| AD8646ARZ-REEL[1] | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| AD8646ARZ-REEL7[1] | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| AD8646ARMZ-R2[1] | −40°C to +125°C | 8-Lead MSOP | RM-8 | A1V |
| AD8646ARMZ-REEL[1] | −40°C to +125°C | 8-Lead MSOP | RM-8 | A1V |
| AD8647ARMZ-R2[1] | −40°C to +125°C | 10-Lead MSOP | RM-10 | A1W |
| AD8647ARMZ-REEL[1] | −40°C to +125°C | 10-Lead MSOP | RM-10 | A1W |
| AD8648ARZ[1] | −40°C to +125°C | 14-Lead SOIC_N | R-14 | |
| AD8648ARZ-REEL[1] | −40°C to +125°C | 14-Lead SOIC_N | R-14 | |
| AD8648ARZ-REEL7[1] | −40°C to +125°C | 14-Lead SOIC_N | R-14 | |
| AD8648ARUZ[1] | −40°C to +125°C | 14-Lead TSSOP | RU-14 | |
| AD8648ARUZ-REEL[1] | −40°C to +125°C | 14-Lead TSSOP | RU-14 | |

[1] Z = RoHS Compliant Part.

## NOTES

## NOTES

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