24-Bit ADC with Built-in Temperature Sensor (HX710A)

24-Bit ADC with (DVDD-AVDD) Voltage Difference Detection (HX710B)

DESCRIPTION

Based on Avia Semiconductor's patented technology, HX710(A/B) is a precision 24-bit analog-to-digital converter (ADC) with built-in temperature sensor (HX710A) or DVDD, AVDD voltage difference detection (HX710B). It's designed for weigh scales and industrial control applications to interface directly with a bridge sensor.

The input low-noise amplifier (PGA) has a fixed gain of 128, corresponding to a full-scale differential input voltage of ±20mV, when a 5V reference voltage is connected to the VREF pin. On chip oscillator provides the system clock without any external component. On-chip power-on-reset circuitry simplifies digital interface initialization. There is no programming needed for the internal registers. All controls to the HX710 are through the pins.

FEATURES

- **On-chip temperature measurement (HX701A)**
- **DVDD and AVDD supply voltage difference measurement (HX701B)**
- **On-chip low noise amplifier with a gain of 128**
- **On-chip oscillator requiring no external component**
- **On-chip power-on-reset**
- **Simple digital control and serial interface: pin-driven controls, no programming needed**
- **Selectable 10SPS or 40SPS output data rate**
- **Simultaneous 50 and 60Hz supply rejection**
- **Current consumption:**
  normal operation < 1.2mA, power down < 1uA
- **Operation supply voltage range: 2.6 ~ 5.5V**
- **Operation temperature range: -40 ~ +85℃**
- **8 pin SOP-8 package**

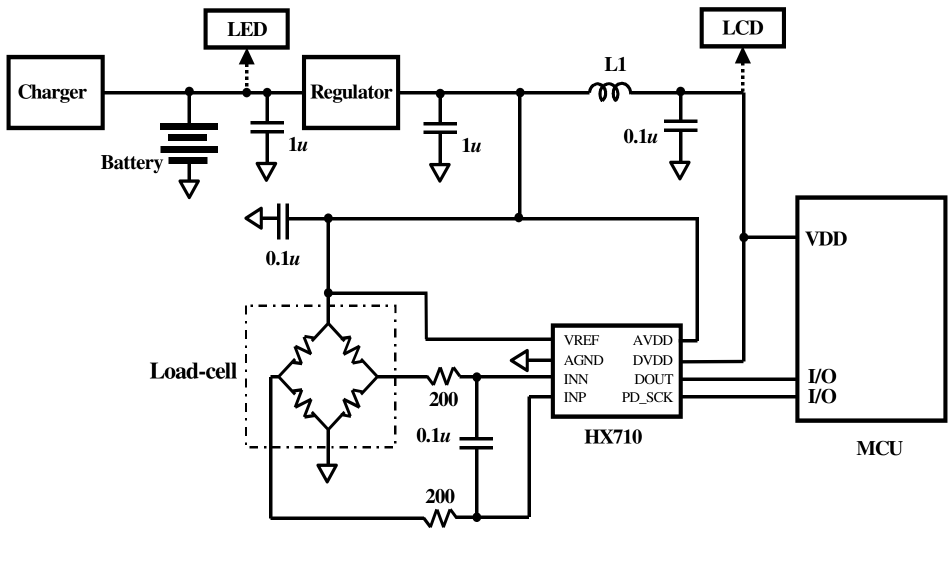
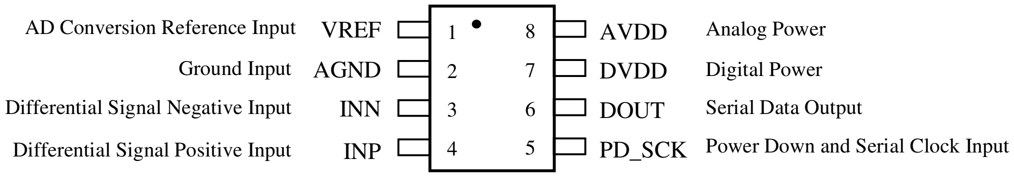


Fig. 1 Typical weigh scale application block diagram using HX710(a/b)

Pin Description



SOP-8 Package

Pin #	Name	Function	Description
1	VREF	Analog Input	Reference input voltage: 1.8 ~ 5.5V (<=AVDD)
2	AGND	Ground	Analog Ground
3	INN	Analog Input	Differential signal negative input
4	INP	Analog Input	Differential signal positive input
5	PD_SCK	Digital Input	Power down control (high active) and serial clock input
6	DOUT	Digital Output	Serial data output
7	DVDD	Power	Digital supply: 2.6 ~ 5.5V (DVDD >= AVDD)
8	AVDD	Power	Analog supply: 2.6 ~ 5.5V

Table 1 Pin Description

KEY ELECTRICAL CHARACTERISTICS

Parameter	Notes	MIN	TYP	MAX	UNIT
Full scale differential input voltage range	V(inp)-V(inn)		±0.0039*VREF		mV
Effective-Number-of-Bits (ENBs) [1]	Gain=128, Rate=10SPS		19.5		Bits
	Gain=128, Rate=40SPS		18.4		
Noise-Free Bits (NFBs) [2]	Gain=128, Rate=10SPS		17.1		
	Gain=128, Rate=40SPS		16.0		
Integral Nonlinearity （INL）	Differential input, end-point fit		±0.001		%of *FSR*
Common mode input range		AGND+0.9		AVDD-1.3	V
VREF input voltage range		1.8		AVDD	
Output data rate			10/40		Hz
Output data coding	2's complement	800000		7FFFFF	HEX
Output settling time [3]			400/100		ms
Input offset			0.01		mV
Input referred noise			50		nV(rms)
Temperature drift	Input offset		±15		nV/℃
	Gain		±7		ppm/℃
Input common mode rejection			100		dB
Power supply rejection			100		dB
Power supply voltage	DVDD	2.6		5.5	V
	AVDD	2.6		5.5	V
Analog supply current	Normal		1100		µA
	Power down		0.3		
Digital supply current	Normal		100		µA
	Power down		0.2		

（1）(2) ENBs = ln(*FSR*/*RMS Noise*)/ln(2), NFBs = ln(*FSR*/*Peak-to-Peak Noise*)/ln(2). *FSR* is full-scale input or output. *RMS Noise* corresponds to input or output RMS noise. *Peak-to-Peak Noise* corresponds to input or output peak-to-peak noise.

（3）Settling time refers to the time from power up, reset, input channel change and gain change to valid stable output data.

Table 2 Key Electrical Characteristics

Analog Input

The differential input is designed to interface directly with a bridge sensor's differential output. It has a fixed gain of 128. The large gains are needed to accommodate the small output signal from the sensor. When a 5V reference is used at the VREF pin, the full-scale differential input voltage range is ±20mV.

Power Supply Options

Digital power supply (DVDD) can be connected directly to AVDD supply. But it should be the same or similar voltage as the MCU power supply to ensure proper communication with the MCU.

If battery output is directly connected to DVDD pin and a regulator output is used for AVDD supply, battery output voltage can be detected by detecting the voltage difference between DVDD and AVDD pins (HX710B).

A/D conversion reference voltage (VREF) should be connected to load-cell's supply voltage. It can be connected directly to AVDD or through a resistor to reduce the power consumption by the load-cell.

Clock Source, Output Data Rate and Format

HX710 uses the on-chip oscillator as clock source. The nominal output data rate is 10 or 40SPS.

The output 24 bits of data is in 2's complement format. When input differential signal goes out of the 24-bit range, the output data will be saturated at 800000h (MIN) or 7FFFFFh (MAX), until the input signal comes back to the input range.

Temperature Measurement

HX710A has an on-chip temperature sensor that can be used to measure system temperature for temperature related system level compensation. It has an effective 15-bit accuracy. Typical measurement resolution is about 20.4 LSB readings/℃ (15 bits).

The on chip digital temperature sensor has significant chip-to-chip variations in offset and gain. When using it for absolute temperature readings, these need to be calibrated out. However, if it's used for temperature related system performance improvement, it's not necessary to calibrate out gain and offset.

Serial Interface

Pin PD_SCK and DOUT are used for data retrieval, input selection, output data rate selection and power down controls.

When output data is not ready for retrieval, digital output pin DOUT is high. Serial clock input PD_SCK should be low. When DOUT goes to low, it indicates data is ready for retrieval. By applying 25~27 positive clock pulses at the PD_SCK pin, data is shifted out from the DOUT output pin. Each PD_SCK pulse shifts out one bit, starting with the MSB bit first, until all 24 bits are shifted out. The 25th pulse at PD_SCK input will pull DOUT pin back to high (Fig.2).

Input selection and output data rate selection is controlled by the number of the input PD_SCK pulses (Table 3). PD_SCK clock pulses should not be less than 25 or more than 27 within one conversion period, to avoid causing serial communication error.

PD_SCK Pulses	Input	Data Rate
25	Differential input	10 Hz
26	Temperature (HX710A)	40 Hz
26	DVDD-AVDD (HX710B)	40Hz
27	Differential input	40 Hz

Table 3 Input and Data Rate Selection

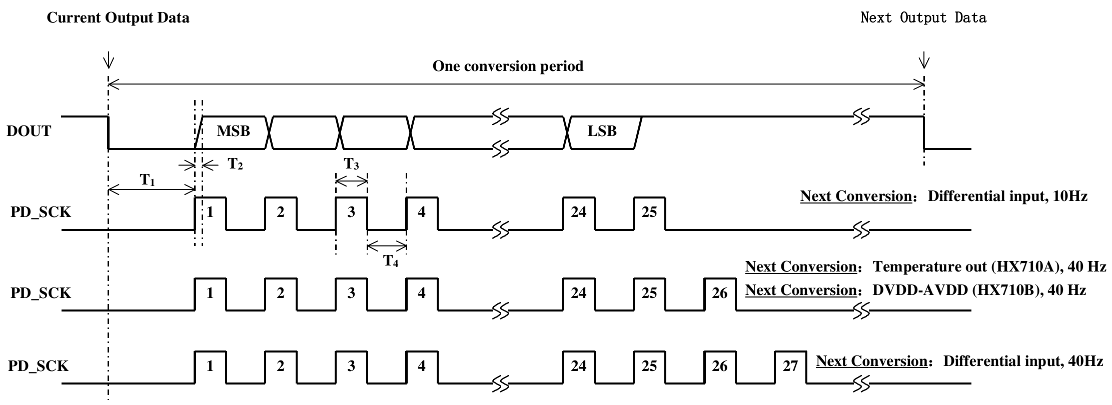


Fig.2 Data output, input and data rate selection timing and control

Symbol	Note	MIN	TYP	MAX	Unit
T_1	DOUT falling edge to PD_SCK rising edge	0.1			μs
T_2	PD_SCK rising edge to DOUT data ready			0.1	μs
T_3	PD_SCK high time	0.2	1	50	μs
T_4	PD_SCK low time	0.2	1		μs

Reset and Power-Down

When chip is powered up, on-chip power on rest circuitry will reset the chip.

Pin PD_SCK input is used to power down the HX710. When PD_SCK Input is low, chip is in normal working mode.

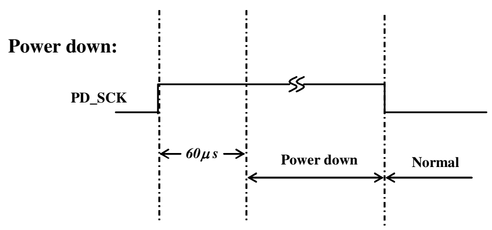


Fig.3 Power down control

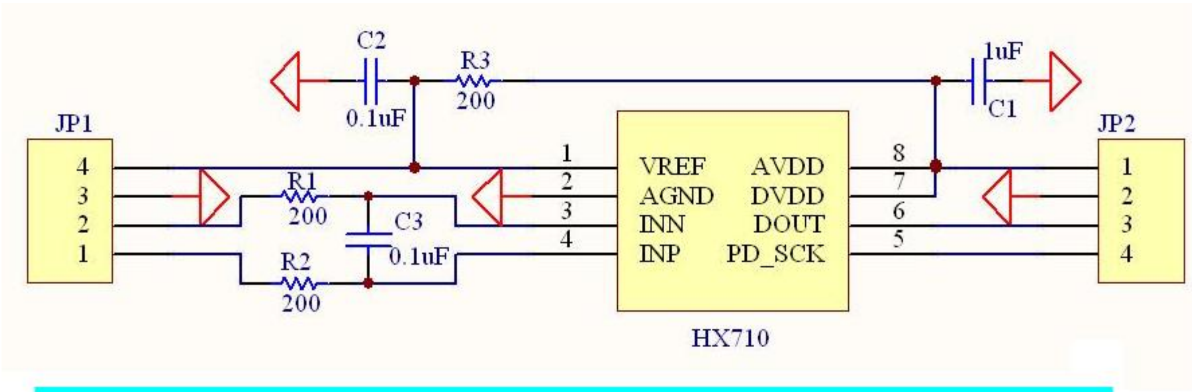
When PD_SCK pin changes from low to high and stays at high for longer than 60μs, HX710 enters power down mode (Fig.3). When PD_SCK returns to low, chip will return back to the setup conditions before power down and enter normal operation mode.

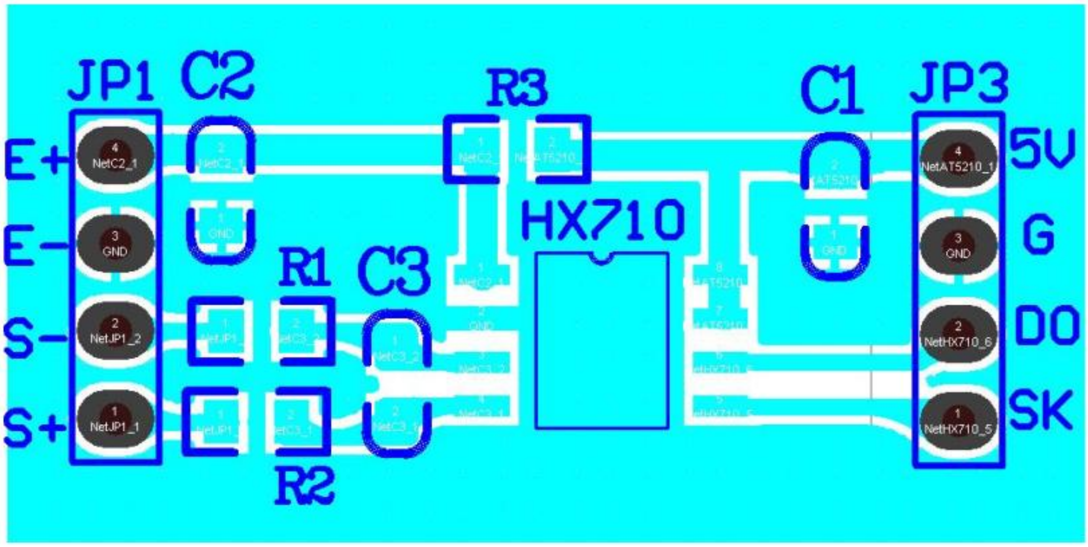
If PD_SCK pulse number is changed during the current conversion period, power down should be executed after current conversion period is completed. This is to ensure the change is saved before power down. When chip returns back to normal operation from power down, it will return to the set up conditions of the last change.

Application Example

Fig.1 is a typical weigh scale application using HX710(AB).

Reference PCB Board Design (Single layer)





Reference Driver (Assembly)

```
/*--------------------------------------------------------------------
Call from ASM:      LCALL   ReaAD
Call from C:    extern unsigned long ReadAD(void);
                  .
                  .
                 unsigned long data;
                 data=ReadAD();
                  .
                  .
----------------------------------------------------------------------*/
PUBLIC        ReadAD
HX710ROM      segment  code
rseg          HX710ROM

sbit           ADDO = P1.5;
```

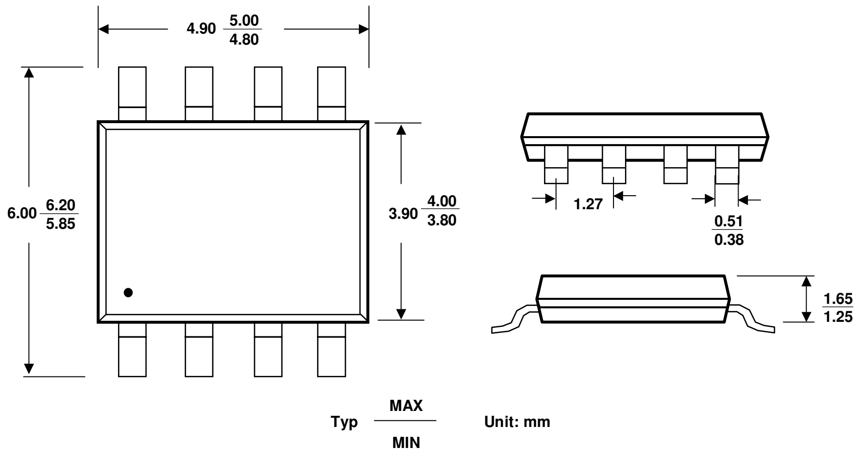
```
sbit          ADSK = P0.0;
/*---------------------------------------------------
 OUT:   R4, R5, R6, R7   R7=>LSB
---------------------------------------------------*/
ReadAD:
    CLR     ADSK               //AD Enable (PD_SCK set low)
    SETB    ADDO               //Enable 51CPU I/O
    JB      ADDO,$             //AD conversion completed?
    MOV     R4,#24
ShiftOut:
    SETB    ADSK               //PD_SCK set high (positive pulse)
    NOP
    CLR     ADSK               //PD_SCK set low
    MOV     C,ADDO             //read on bit
    XCH     A,R7               //move data
    RLC     A
    XCH     A,R7
    XCH     A,R6
    RLC     A
    XCH     A,R6
    XCH     A,R5
    RLC     A
    XCH     A,R5
    DJNZ    R4,ShiftOut         //moved 24BIT?
    SETB    ADSK
    NOP
    CLR     ADSK
    RET
    END
```

Reference Driver (C)

```
//---------------------------------------------------------------------
sbit   ADDO = P1^5;
sbit   ADSK = P0^0;
unsigned long ReadCount(void){
  unsigned long Count;
  unsigned char i;
  ADDO=1;
  ADSK=0;
  Count=0;
  while(ADDO);
  for (i=0;i<24;i++){
    ADSK=1;
    Count=Count<<1;
    ADSK=0;
    if(ADDO) Count++;
  }
```

```
  ADSK=1;
  Count=Count^0x800000;
  ADSK=0;
  return(Count);
}
```

Package Dimensions



SOP-8 Package