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74HC08; 74HCT08

Quad 2-input AND gate

Rev. 8 — 10 August 2021

Product data sheet

1. General description

The 74HC08; 74HCT08 is a quad 2-input AND gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- · High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Input levels:
 - For 74HC08: CMOS level
 - For 74HCT08: TTL level
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- · Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

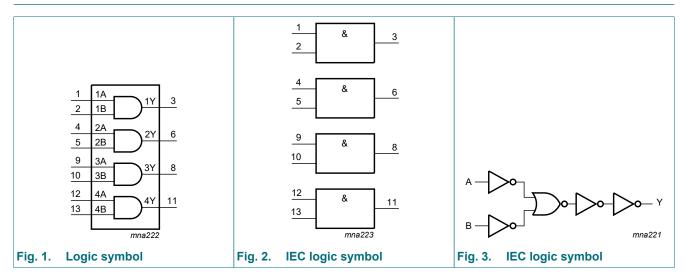
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC08D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads;	SOT108-1
74HCT08D			body width 3.9 mm	
74HC08PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads;	SOT402-1
74HCT08PW			body width 4.4 mm	
74HC08BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced	SOT762-1
74HCT08BQ			very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	

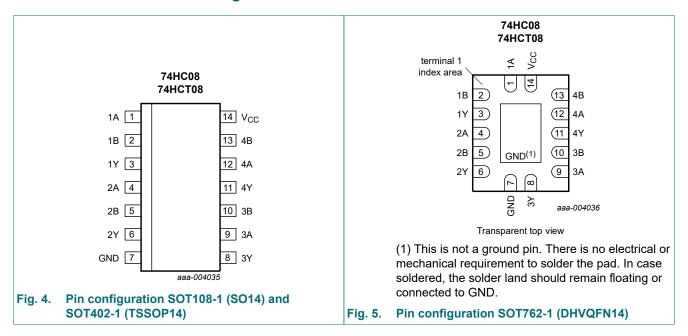


4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Table 2. I ill description		
Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don't \ care.$

Input		Output
nA	nB	nY
L	L	L
L	Н	L
Н	L	L
Н	Н	Н

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I _{OK}	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
Io	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 \text{ to } +85 ^{\circ}\text{C}$ [2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

For SOT402-1 (TSSOP14) package: Ptot derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: Ptot derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		74HC08			Unit		
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V_{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0 \text{ V}$	-	-	83	-	-	-	ns/V

^[2] For SOT108-1 (SO14) package: Ptot derates linearly with 10.1 mW/K above 100 °C.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C			°C to 5 °C		°C to 5 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC08						'				
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1	-	±1	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions		25 °C			°C to 5 °C		°C to 5 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HCT08	3									
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 5.2 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1	-	±1	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
ΔI _{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A};$ other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	60	216	-	270	-	294	μΑ
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

 $GND = 0 \ V; \ C_L = 50 \ pF;$ for test circuit see Fig. 7.

Symbol	Parameter	Conditions		25 °C			°C to 5 °C	_	°C to 5 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC08										
t _{pd}	propagation	nA, nB to nY; see Fig. 6 [1]								
	delay	V _{CC} = 2.0 V	-	25	90	-	115	-	135	ns
		V _{CC} = 4.5 V	-	9	18	-	23	-	27	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	7	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	7	15	-	20	-	23	ns
t _t	transition time	see <u>Fig. 6</u> [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C _{PD}	power dissipation capacitance	per package; [3] $V_I = GND \text{ to } V_{CC}$	-	10	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C				°C to 5 °C	-40 °C to +125 °C		Unit	
				Min	Тур	Max	Min	Max	Min	Max	
74HCT08	3				•		•	•	•		
t _{pd}	propagation	nA, nB to nY; see Fig. 6	[1]								
	delay	V _{CC} = 4.5 V		-	14	24	-	30	-	36	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$		-	11	-	-	-	-	-	ns
t _t	transition time	V _{CC} = 4.5 V; see <u>Fig. 6</u>	[2]	-	7	15	-	19	-	22	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} - 1.5 V	[3]	-	20	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PHL} and t_{PLH} .
- t_t is the same as t_{THL} and t_{TLH} . C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

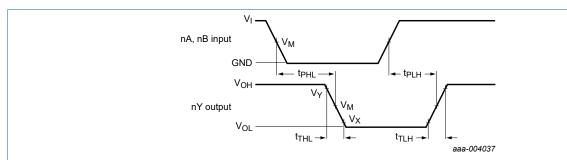
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$

10.1. Waveforms and test circuit



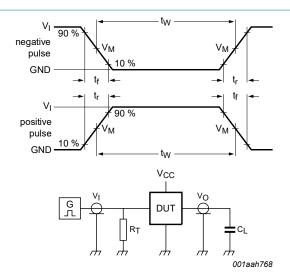
Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Input to output propagation delays

Table 8. Measurement points

Туре	Input	Output		
	V _M	V _M	V _X	V _Y
74HC08	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}
74HCT08	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}



Test data is given in Table 9.

Definitions test circuit:

 R_{T} = termination resistance should be equal to output impedance Z_{o} of the pulse generator.

 C_L = load capacitance including jig and probe capacitance.

Fig. 7. Test circuit for measuring switching times

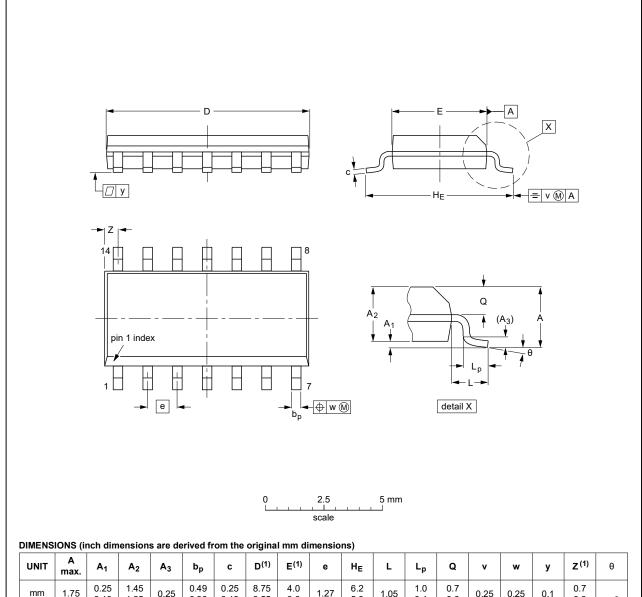
Table 9. Test data

Туре	Input		Load	Test
	VI	t _r , t _f	CL	
74HC08	V _{CC}	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}
74HCT08	3.0 V	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

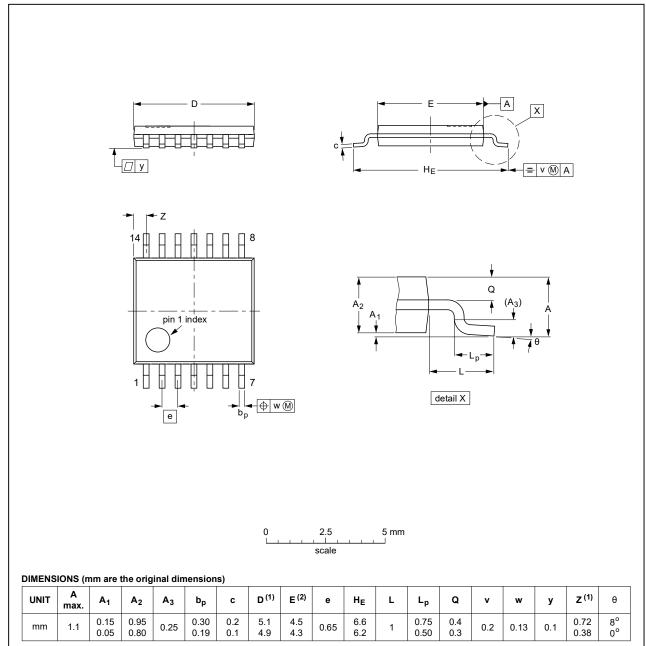
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN	ISSUE DATE	
	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012				99-12-27 03-02-19

Fig. 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE	REFERENCES			EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT402-1		MO-153				99-12-27 03-02-18

Fig. 9. Package outline SOT402-1 (TSSOP14)

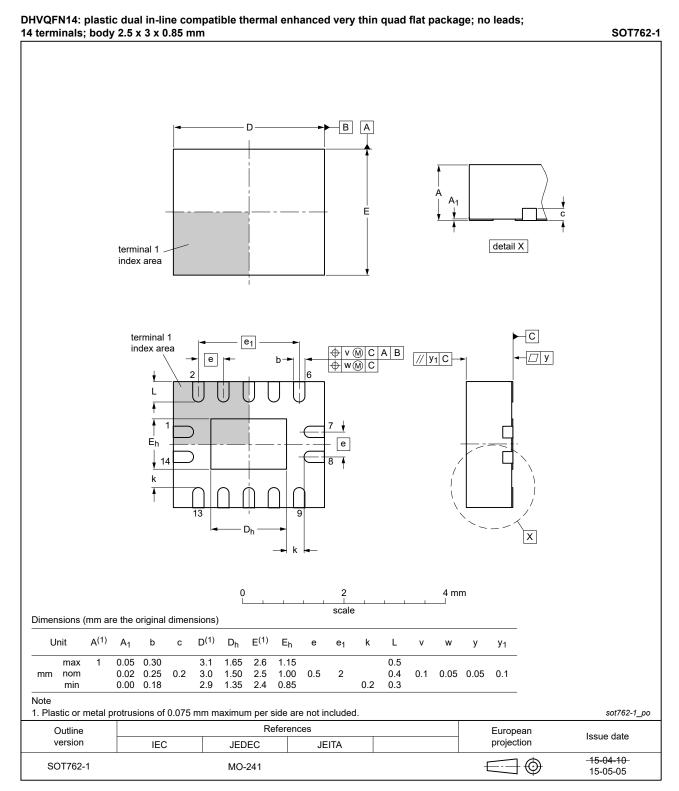


Fig. 10. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74HC_HCT08 v.8	20210810	Product data sheet	-	74HC_HCT08 v.7		
Modifications:	 Section 2 updated. Type numbers 74HC08DB and 74HCT08DB (SOT337-1/SSOP14) removed. 					
74HC_HCT08 v.7	20200416	Product data sheet	-	74HC_HCT08 v.6		
Modifications:	• <u>Table 4</u> : Der	<u>Table 4</u> : Derating values for P _{tot} total power dissipation updated.				
74HC_HCT08 v.6	20170613	Product data sheet	-	74HC_HCT08 v.5		
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 					
74HC_HCT08 v.5	20151130	Product data sheet	-	74HC_HCT08 v.4		
Modifications:	Type numbers 74HC08N and 74HCT08N (SOT27-1) removed.					
74HC_HCT08 v.4	20120906	Product data sheet	-	74HC_HCT08 v.3		
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 					
74HC_HCT08 v.3	20030725	Product specification	-	74HC_HCT08_CNV v.2		
74HC_HCT08_CNV v.2	19970826	Product specification	-	-		

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Data sheet status

Document status [1][2]	Product status [3]	Definition	
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.	
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