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EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x
Replacement guide

About this document

Scope and purpose

This application note is a step-by-step guide to replace dual-channel low-side drivers available on the market with the industry-standard **EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x**, and how to design with the latest small and versatile 6-pin SOT-23 package.

Intended audience

This document is intended for R&D engineers, application engineers, and hardware designers.

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1 Introduction to the 2EDN family

The EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x is a family of dual-channel low-side gate driver ICs from Infineon. The EiceDRIVER™ 2EDNxx3x family features two independent, non-isolated, low-side driving channels, with maximum peak output current of 5 A, and two possible undervoltage lockout (UVLO) protection levels, typically 4.2 V and 8 V.

Proper selection of a gate driver IC requires comparison of the main parameters. Influencers of gate driver choice are current capability, switching speed, package size and level of integration, such as the number of driving stages and safety features integrated into the IC. Furthermore, pin-to-pin compatibility is often a required feature for gate driver ICs to allow for using similar gate driver ICs from different manufacturers in the assembly line. In this case the devices should have similar features, identical footprints and compatible pinouts.

1.1 EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x portfolio

Table 1 presents an overview of the EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x family portfolio.

Table 1 EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x family overview

Peak output current	Inputs	DSO-8 package		TSSOP-8 package		WSON-8 package	SOT-23-6 package
		4 V UVLO	8 V UVLO	4 V UVLO	8 V UVLO	4 V UVLO	4 V UVLO
5 A	Non-inverting	2EDN7534F	2EDN8534F	2EDN7534R	2EDN8534R	2EDN7534G	2EDN7534B
	Inverting	2EDN7533F	2EDN8533F	2EDN7533R	2EDN8533R	–	2EDN7533B
4 A	Non-inverting	2EDN7434F	–	2EDN7434R	–	–	–

1.2 Available packages

The EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x family is offered in the following package variants:

- DSO-8, TSSOP-8 and WSON-8 are industry-standard packages, which allow pin-to-pin compatibility with other gate driver ICs available on the market and backward compatibility with legacy EiceDRIVER™ 2EDN families
- A new SOT23-6 small form-factor package reduces the driving stage size while retaining the same electrical performance, allowing better optimization of the driving loop

Table 2 Available packages and respective body size

DSO-8 **8-pin package with leads** **(4.94 x 3.94 mm body size)**	
TSSOP-8 **8-pin package with leads** **(3 x 3 mm body size)**	
WSON-8 **8-pin leadless package** **(3 x 3 mm body size)**	
SOT-23-6 **6-pin package with leads** **(2.9 x 1.6 mm body size)**	

2 Description of 2EDN753x/2EDN853x/2EDN743x

The EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x is an advanced dual-channel gate driver family, suited to driving logic and normal-level MOSFETs, and supports OptiMOS™, CoolMOS™ and superjunction MOSFETs, as well as IGBTs and GaN switches.

The control and enable inputs are LV-TTL compatible, and can withstand absolute maximum input voltages from-12 V to +22 V, improving compatibility with similar devices and reducing the required number of components to protect the input pins of the gate driver IC. Furthermore, the inputs prevent latch-up and possible electrical overstress induced by parasitic ground inductances, enhancing overall system reliability.

The two 4.2 V and 8.0 V UVLO options allow selection of the proper protection level depending on the driving voltage required by the switch. In the case of abnormal operation such as a drop in the V_{DD} supply voltage, UVLO protection is triggered, and this prevents the switching device operating in the linear region.

Each channel features a rail-to-rail output stage, able to sink and source up to 5 A peak current, providing very low on-resistance for the driving path. Product versions with peak sink and source currents of 4 A are also available. The channel-to-channel delay matching is typically 1 ns. This allows use of the two channels in parallel to double the peak output current: peak source and sink output current capability of 10 A are possible by using a single 5 A device (EiceDRIVER™ 2EDNx53x) version with two channels in parallel. An industry-leading reverse current robustness eliminates the need for Schottky diodes at the outputs and reduces the component count and cost.

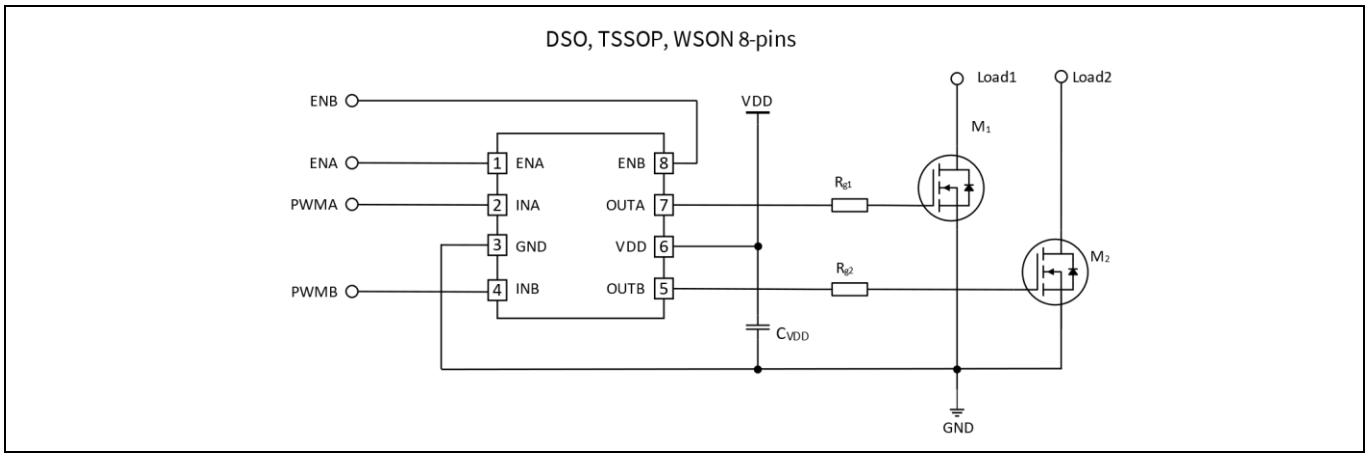


Figure 1 Application example: DSO-8, TSSOP-8 and WSON-8 packages

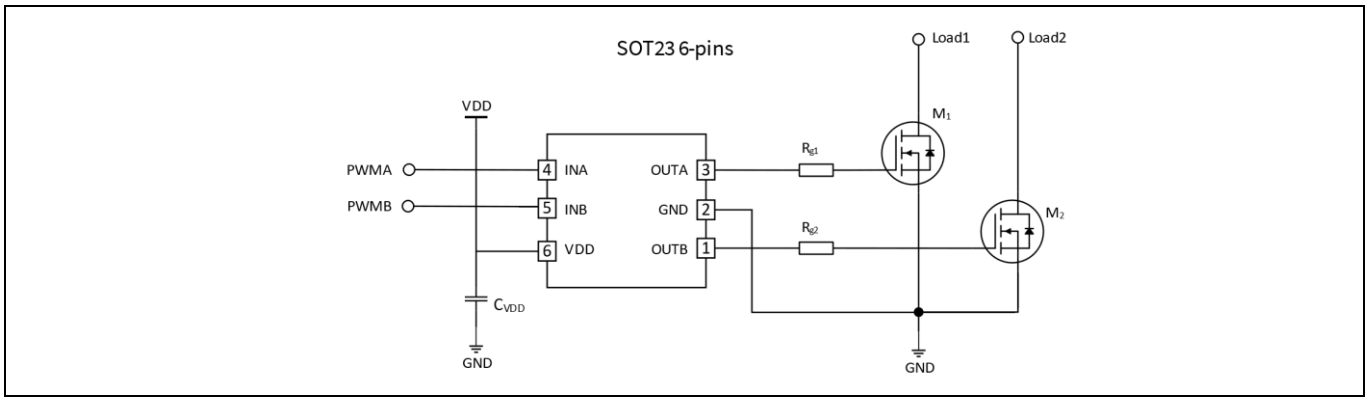


Figure 2 Application example: SOT-23-6 package

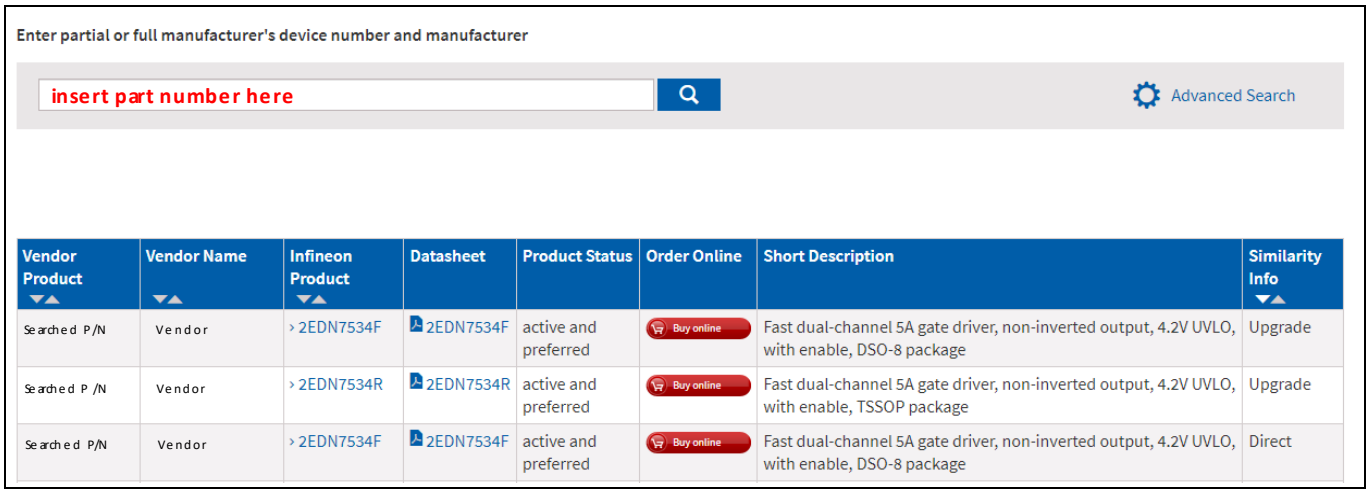
3 Step-by-step replacement procedure

In order to safely replace the existing device, it is recommended to measure key parameters from a golden sample of the original board, and compare them with datasheet parameters to ensure device interoperability.

3.1 Selecting the proper gate driver IC with online cross-reference tool

Infineon offers an online interactive cross-reference tool [3].

In the “search” tab, insert the device’s part number to be replaced. The online cross-reference tool returns the part number of the Infineon EiceDRIVER™ gate driver IC equivalent to the device in use.



Vendor Product	Vendor Name	Infineon Product	Datasheet	Product Status	Order Online	Short Description	Similarity Info
Searched P/N	Vendor	› 2EDN7534F	2EDN7534F	active and preferred	Buy online	Fast dual-channel 5A gate driver, non-inverted output, 4.2V UVLO, with enable, DSO-8 package	Upgrade
Searched P /N	Vendor	› 2EDN7534R	2EDN7534R	active and preferred	Buy online	Fast dual-channel 5A gate driver, non-inverted output, 4.2V UVLO, with enable, TSSOP package	Upgrade
Searched P/N	Vendor	› 2EDN7534F	2EDN7534F	active and preferred	Buy online	Fast dual-channel 5A gate driver, non-inverted output, 4.2V UVLO, with enable, DSO-8 package	Direct

Figure 3 Cross-reference tool research example

Once an initial selection is made, please carefully compare the original gate driver IC datasheet with the EiceDRIVER™ gate driver IC datasheet.

- It is recommended to check package drawings and footprints.
- Compare parametric data from earlier testing with the EiceDRIVER™ gate driver IC datasheet: power supply, inputs, outputs, and timings must be within datasheet limits.

3.2 Verifying the V_{DD} supply voltage range

The EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x family has a maximum operating supply voltage of 20 V.

The minimum operating supply voltage is set by the UVLO function to a typical default value of 4.2 V or 8 V. The UVLO function protects power MOSFETs from running in linear mode with subsequent high-power dissipation.

We recommend a low-ESR ceramic bypass capacitor of 100 nF or greater between the GND and V_{DD} pins.

Table 3 Supply voltage parameters to be verified

Parameter	Symbol	Note
Supply voltage	V_{DD}	Verify maximum operating V_{DD} = 20 V
Supply voltage	V_{DD}	Verify minimum operating V_{DD} is above the selected UVLO threshold Refer to UVLO tables in datasheet [2]
V_{DD} quiescent current	I_{VDDqu1} I_{VDDqu2}	Power supply must provide more than 1.2 mA under quiescent conditions (no switching)
V_{DD} maximum current	I_{VDDmax}	Verify that power supply is capable of providing enough DC current at maximum switching frequency and maximum V_{DD} voltage in the application

3.3 Verifying the PWM input dynamics and configuration

The EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x family is available in two different input logic configurations of the PWM pins (INA and INB):

1. Direct (or non-inverting): the output stages are driven according to the PWM positive inputs logic (INA and INB). The two PWM inputs INA and INB have an internal pull-down resistor connected to GND.
2. Inverting: the output stages are driven with inverted logic with respect to the PWM inputs (INA and INB). The two PWM inputs INA and INB have an internal pull-up resistor connected to V_{DD}.

The different input logic configurations are shown in **Figure 4**.

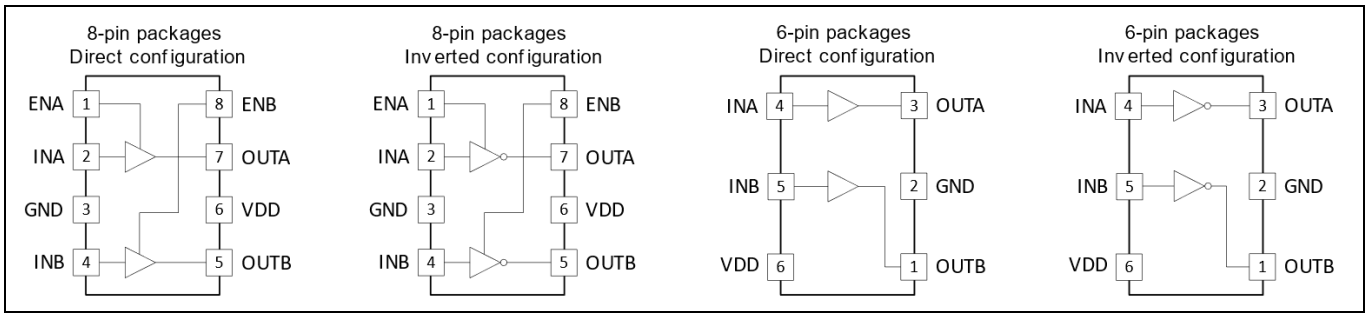


Figure 4 Input configurations

The internal pull-down (pull-up) resistors prevent turn-on of the driven switches during power up in case of a high impedance condition on the input pins.

The enable inputs ENA and ENB of the DSO-8, TSSOP-8 and WSON-8 packages are internally pulled up to V_{DD} (i.e., the driver is enabled when enable pins are left open). The small form-factor SOT-23-6 package is provided without ENA and ENB pins, resulting in an always-active condition when the V_{DD} is above the UVLO threshold.

All input pins (INA, INB, ENA, and ENB) are compatible with LV-TTL levels (typical V_{INH} = 2.1 V; V_{INL} = 1.2 V), providing a typical hysteresis of 0.9 V, independently of the supply voltage V_{DD}.

All input pins (INA, INB, ENA, and ENB) have an extended operating voltage range from -10 V to 20 V, with absolute maximum rating ranging from -12 V to 22 V. This prevents cross current during GND shifts, and allows for reduction of the number of external components on the gate driver IC input pins.

Parameters to be verified are described in **Table 4**.

Table 4 Input pin (INA, INB, ENA, ENB) parameters to be verified

Parameter	Symbol	Note
Input and enable low level	V_{INL} V_{ENL}	Verify maximum voltage level and noise margin Recommended noise margin for input signals greater than 200 mV
Input and enable high level	V_{INH} V_{ENH}	Verify minimum voltage level and noise margin Recommended noise margin for input signals greater than 200 mV
Input and enable rise/fall time	$t_{IN,\ RISE}$ $t_{IN,\ FALL}$	If channels A and B run in parallel mode, the rise/fall times of the input signals must be less than 100 ns (10 to 90 percent) to avoid cross conduction currents in the device output stages

3.4 Verifying the input, output and V_{gs} behavior

The EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x family has two rail-to-rail output stages achieved with complementary MOS transistors, which can provide a maximum sinking/sourcing current of 5 A (4 A peak output current versions are also available).

The output impedances for the sourcing p-channel MOS have typical values of 0.8 Ω for 2EDN753x and 2EDN853x and 1.0 Ω for 2EDN743x. The output impedances for the sinking n-channel MOS transistor have typical values of 0.6 Ω for 2EDN753x and 2EDN853x and 0.8 Ω for 2EDN743x. The use of a p-channel sourcing transistor is crucial for achieving rail-to-rail behavior. Gate drive outputs are actively tied to GND by the nMOS in case of floating ENx or INx inputs, or during start-up or power-down transients if the supply voltage is below the UVLO threshold.

When qualifying designs with compatible devices it could happen that the V_{gs} behavior during turn-on and turn-off transients is different. This could be related to a different implementation of the output stage inside the gate driver IC, which could lead to different output on-resistances, slew rates or timing behaviors. It is recommended to measure the MOSFET V_{gs} voltage (see nodes B1 and B2 in **Figure 5**) due to a change in the input signal (see nodes A1 and A2 in **Figure 5**). Changing the gate resistor R_g allows the user to tune and equalize the timing and slope of the V_{gs} signal between the different gate driver ICs qualified for the design.

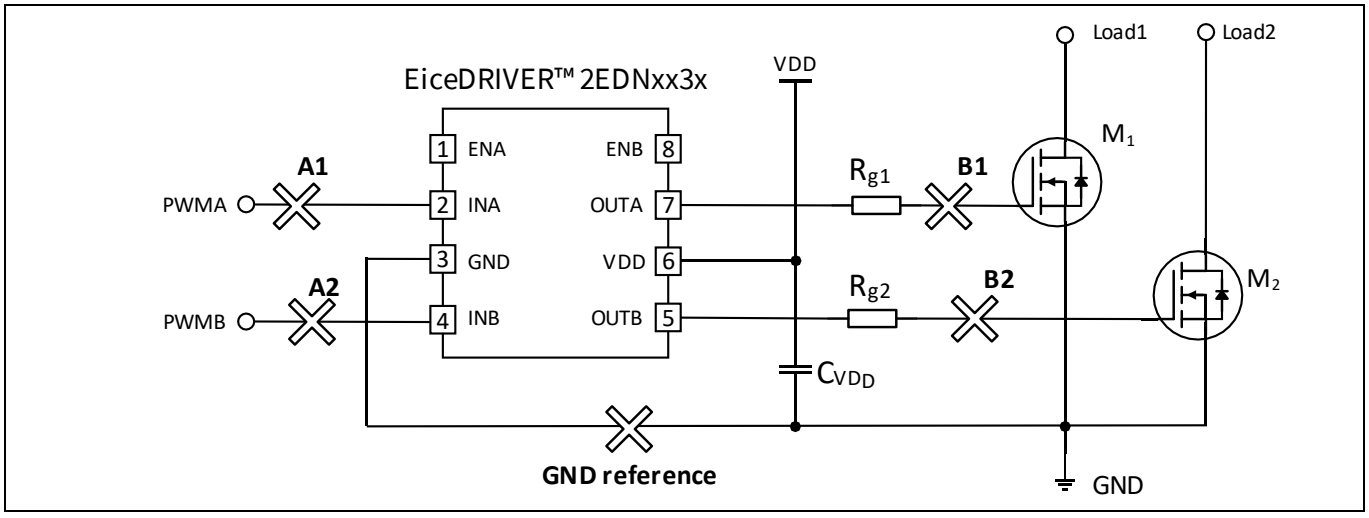


Figure 5 Probing points to verify the driving behavior of A1, A2, B1 and B2

3.5 Verifying PCB connections

Besides EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x, other gate driver ICs available on the market have industry-standard DSO-8, TSSOP-8 and WSON-8 packages. Some of them have no internal connection on the enable pins Pin 1 and Pin 8 (i.e., ENA and ENB pins are not connected internally). If components with not-connected Pin 1 and Pin 8 are also qualified as alternative devices, the following must be verified:

Table 5 Verification of enable pins status

Pin 1 and Pin 8 PCB connection	Consequence	Corrective action
Pads of Pin 1 and Pin 8 are not connected on the PCB	Pin 1 and Pin 8 floating	No action needed. EiceDRIVER™ 2EDN has 400 kΩ internal pull-up resistor
Pads of Pin 1 and Pin 8 are connected to V_{DD}	ENA = ENB = V_{DD}	No action needed. EiceDRIVER™ 2EDN is enabled
Pads of Pin 1 and Pin 8 are connected to GND	ENA = ENB = GND	EiceDRIVER™ 2EDN is disabled via ENA and ENB pins. PCB rework is required

In case enable pins ENA and ENB are not used, a space-efficient solution is to use **EiceDRIVER™ 2EDN7534B** (non-inverting) or **EiceDRIVER™ 2EDN7533B** (inverting) in a 6-pin SOT-23-6 package. 2EDN7534B and 2EDN7533B feature the same performance in a smaller 6-pin package, and enable improvements in the gate driving loop as well as better placement of the gate driver IC and PCB layout versatility.

SOT-23-6 **6-pin package with leads** (2.9 x 1.6 mm body size)	

3.6 Design validation test

After the device functionality has been checked at the ambient temperature, as an additional safety measure it is recommended to run a product validation test on a controlled production batch according to the relevant company's rules to verify functionality over the whole temperature range.

References

[1] Infineon Technologies AG: *EiceDRIVER™ 2EDN gate driver for MOSFETs*; Product page; **Available online**

[2] Infineon Technologies AG: *EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x*; Datasheet; **Available online**

[3] Infineon Technologies AG: *Infineon – cross-reference tool*; **Available online**

Revision history

Document revision	Date	Description of changes
V 1.0	2022-11-18	Initial release

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Edition 2022-11-18

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
AN_2211_PL21_2211_171017

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