EN: This Datasheet/Document is presented by the manufacturer.

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Features

- Single 2.5V or 2.7V to 3.6V Supply
- RapidS® Serial Interface: 66 MHz Maximum Clock Frequency
  - SPI Compatible Modes 0 and 3
- User Configurable Page Size
  - 256 Bytes per Page
  - 264 Bytes per Page
- Page Program Operation
  - Intelligent Programming Operation
  - 2,048 Pages (256/264 Bytes/Page) Main Memory
- Flexible Erase Options
  - Page Erase (256 Bytes)
  - Block Erase (2 Kbytes)
  - Sector Erase (64 Kbytes)
  - Chip Erase (4 Mbits)
- Two SRAM Data Buffers (256/264 Bytes)
  - Allows Receiving of Data while Reprogramming the Flash Array
- Continuous Read Capability through Entire Array
  - Ideal for Code Shadowing Applications
- Low-power Dissipation
  - 7 mA Active Read Current Typical
  - 25 µA Standby Current Typical
  - 5 µA Deep Power-down Typical
- Hardware and Software Data Protection Features
  - Individual Sector
- Sector Lockdown for Secure Code and Data Storage
  - Individual Sector
- Security: 128-byte Security Register
  - 64-byte User Programmable Space
  - Unique 64-byte Device Identifier
- JEDEC Standard Manufacturer and Device ID Read
- 100,000 Program/Erase Cycles Per Page Minimum
- Data Retention – 20 Years
- Industrial Temperature Range
- Green (Pb/Halide-free/RoHS Compliant) Packaging Options

4-megabit 2.5-volt or 2.7-volt DataFlash®

AT45DB041D

1. Description

The AT45DB041D is a 2.5V or 2.7V, serial-interface Flash memory ideally suited for a wide variety of digital voice-, image-, program code- and data-storage applications. The AT45DB041D supports RapidS serial interface for applications requiring very high speed operations. RapidS serial interface is SPI compatible for frequencies up to 66 MHz. Its 4,325,376 bits of memory are organized as 2,048 pages of 256 bytes or 264 bytes each. In addition to the main memory, the AT45DB041D also contains two SRAM buffers of 256/264 bytes each. The buffers allow the receiving of data while a page in the main Memory is being reprogrammed, as well as writing a continuous data stream. EEPROM emulation (bit or byte alterability) is easily handled with a self-contained three step read-modify-write operation. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the DataFlash uses a RapidS serial interface to sequentially access its data. The simple sequential access dramatically reduces active pin count, facilitates hardware layout,

3595H–DFLASH–03/07

increases system reliability, minimizes switching noise, and reduces package size. The device is optimized for use in many commercial and industrial applications where high-density, low-pin count, low-voltage and low-power are essential.

To allow for simple in-system reprogrammability, the AT45DB041D does not require high input voltages for programming. The device operates from a single power supply, 2.5V to 3.6V or 2.7V to 3.6V, for both the program and read operations. The AT45DB041D is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming and erase cycles are self-timed.

2. Pin Configurations and Pinouts

Table 2-1. Pin Configurations

Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	**Chip Select:** Asserting the $\overline{CS}$ pin selects the device. When the $\overline{CS}$ pin is deasserted, the device will be deselected and normally be placed in the standby mode (not Deep Power-Down mode), and the output pin (SO) will be in a high-impedance state. When the device is deselected, data will not be accepted on the input pin (SI). A high-to-low transition on the $\overline{CS}$ pin is required to start an operation, and a low-to-high transition is required to end an operation. When ending an internally self-timed operation such as a program or erase cycle, the device will not enter the standby mode until the completion of the operation.	Low	Input
SCK	**Serial Clock:** This pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command, address, and input data present on the SI pin is always latched on the rising edge of SCK, while output data on the SO pin is always clocked out on the falling edge of SCK.	–	Input
SI	**Serial Input:** The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched on the rising edge of SCK. If the SER/$\overline{BYTE}$ pin is always driven low, the SI pin should be a “no connect”.	–	Input
SO	**Serial Output:** The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK. If the SER/$\overline{BYTE}$ pin is always driven low, the SO pin should be a “no connect”.	–	Output
$\overline{WP}$	**Write Protect:** When the $\overline{WP}$ pin is asserted, all sectors specified for protection by the Sector Protection Register will be protected against program and erase operations regardless of whether the Enable Sector Protection command has been issued or not. The $\overline{WP}$ pin functions independently of the software controlled protection method. After the $\overline{WP}$ pin goes low, the content of the Sector Protection Register cannot be modified. If a program or erase command is issued to the device while the $\overline{WP}$ pin is asserted, the device will simply ignore the command and perform no operation. The device will return to the idle state once the $\overline{CS}$ pin has been deasserted. The Enable Sector Protection command and Sector Lockdown command, however, will be recognized by the device when the $\overline{WP}$ pin is asserted. The $\overline{WP}$ pin is internally pulled-high and may be left floating if hardware controlled protection will not be used. However, it is recommended that the $\overline{WP}$ pin also be externally connected to V_{CC} whenever possible.	Low	Input
RESET	**Reset:** A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level. The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. If this pin and feature are not utilized it is recommended that the $\overline{RESET}$ pin be driven high externally.	Low	Input
V_{CC}	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	–	Power
GND	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.	–	Ground

Figure 2-1. MLF Top View

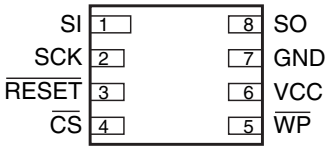
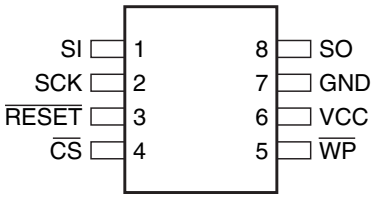
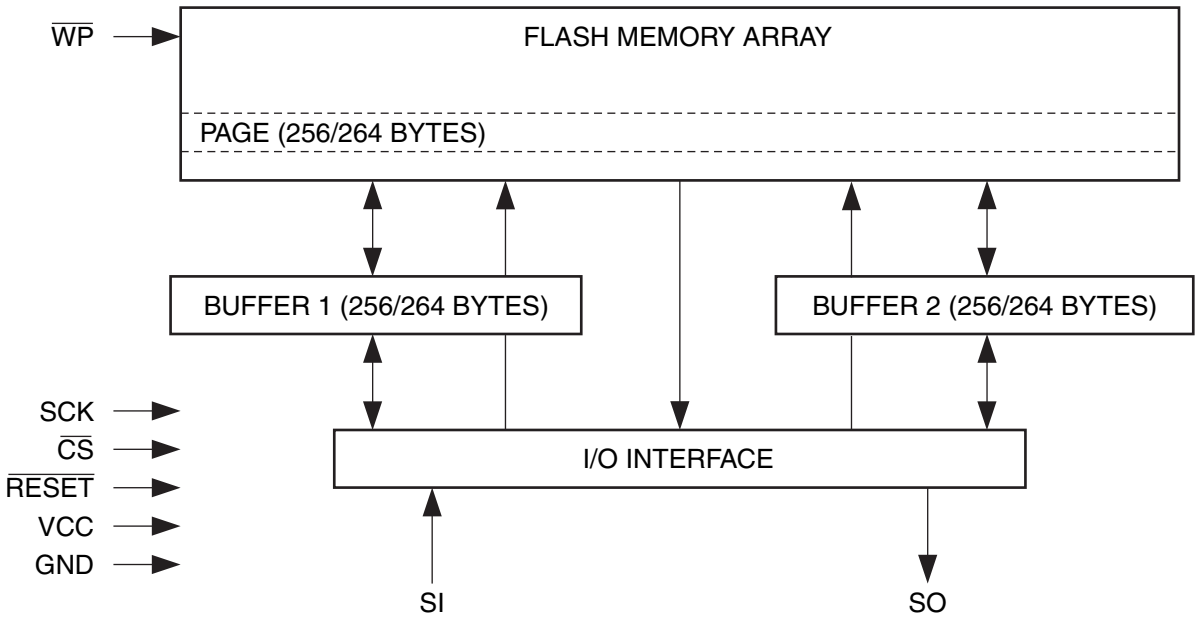


Figure 2-2. SOIC Top View



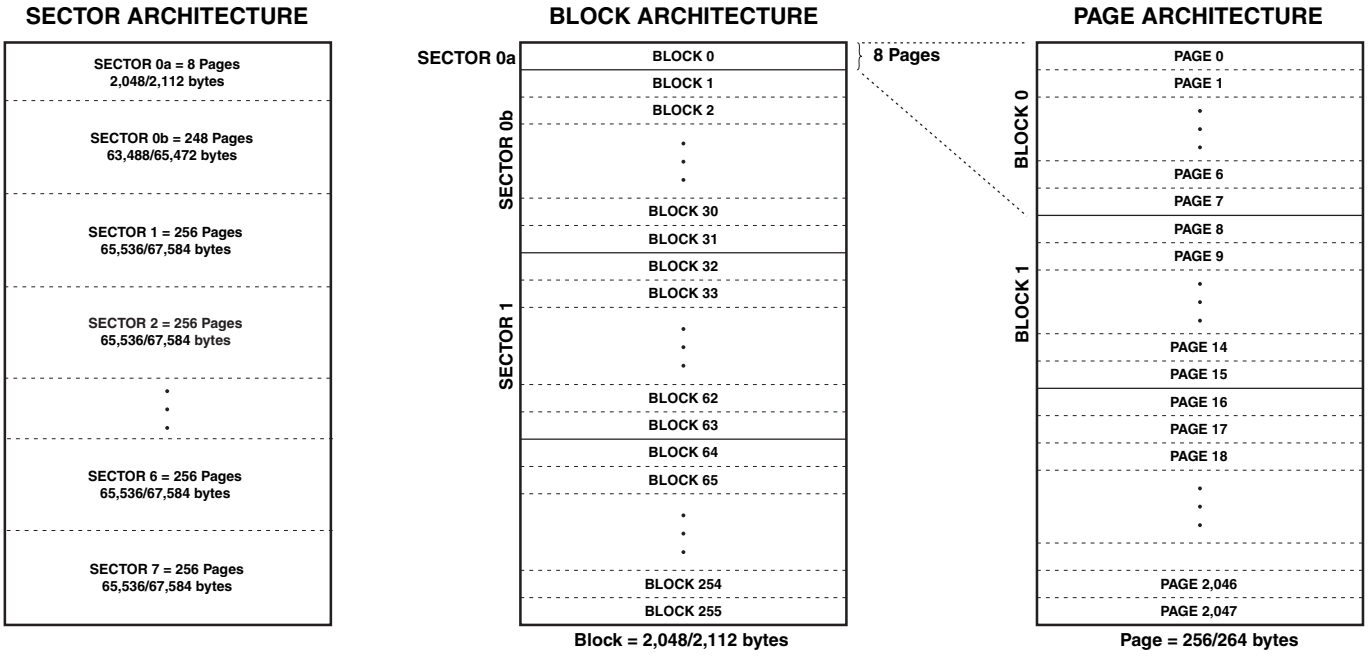
3. Block Diagram



4. Memory Array

To provide optimal flexibility, the memory array of the AT45DB041D is divided into three levels of granularity comprising of sectors, blocks, and pages. The “Memory Architecture Diagram” illustrates the breakdown of each level and details the number of pages per sector and block. All program operations to the DataFlash occur on a page-by-page basis. The erase operations can be performed at the chip, sector, block or page level.

Figure 4-1. Memory Architecture Diagram



5. Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Tables 15-1 through 15-7. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Buffer addressing for the DataFlash standard page size (264 bytes) is referenced in the datasheet using the terminology BEA8 - BFA0 to denote the 9 address bits required to designate a byte address within a buffer. Main memory addressing is referenced using the terminology PA10 - PA0 and BA8 - BA0, where PA10 - PA0 denotes the 11 address bits required to designate a page address and BA8 - BA0 denotes the 9 address bits required to designate a byte address within the page.

For the “Power of 2” binary page size (256 bytes), the Buffer addressing is referenced in the datasheet using the conventional terminology BFA7 - BFA0 to denote the 8 address bits required to designate a byte address within a buffer. Main memory addressing is referenced using the terminology A18 - A0, where A18 - A8 denotes the 11 address bits required to designate a page address and A7 - A0 denotes the 8 address bits required to designate a byte address within a page.

6. Read Commands

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two SRAM data buffers. The DataFlash supports RapidS protocols for Mode 0 and Mode 3. Please refer to the “Detailed Bit-level Read Timing” diagrams in this datasheet for details on the clock cycle sequences for each mode.

6.1 Continuous Array Read (Legacy Command – E8H): Up to 66 MHz

By supplying an initial starting address for the main memory array, the Continuous Array Read command can be utilized to sequentially read a continuous stream of data from the device by simply providing a clock signal; no additional addressing information or control signals need to be provided. The DataFlash incorporates an internal address counter that will automatically increment on every clock cycle, allowing one continuous read operation without the need of additional address sequences. To perform a continuous read from the DataFlash standard page size (264 bytes), an opcode of E8H must be clocked into the device followed by three address bytes (which comprise the 24-bit page and byte address sequence) and 4 don’t care bytes. The first 11 bits (PA10 - PA0) of the 20-bit address sequence specify which page of the main memory array to read, and the last 9 bits (BA8 - BA0) of the 20-bit address sequence specify the starting byte address within the page. To perform a continuous read from the binary page size (256 bytes), the opcode (E8H) must be clocked into the device followed by three address bytes and 4 don’t care bytes. The first 11 bits (A18 - A8) of the 19-bits sequence specify which page of the main memory array to read, and the last 8 bits (A7 - A0) of the 19-bits address sequence specify the starting byte address within the page. The don’t care bytes that follow the address bytes are needed to initialize the read operation. Following the don’t care bytes, additional clock pulses on the SCK pin will result in data being output on the SO (serial output) pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don’t care bytes, and the reading of data. When the end of a page in main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR1} specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

6.2 Continuous Array Read (High Frequency Mode – 0BH): Up to 66 MHz

This command can be used with the serial interface to read the main memory array sequentially in high speed mode for any clock frequency up to the maximum specified by f_{CAR1}. To perform a continuous read array with the page size set to 264 bytes, the $\overline{CS}$ must first be asserted then an opcode 0BH must be clocked into the device followed by three address bytes and a dummy byte. The first 11 bits (PA10 - PA0) of the 20-bit address sequence specify which page of the main memory array to read, and the last 9 bits (BA8 - BA0) of the 20-bit address sequence specify the starting byte address within the page. To perform a continuous read with the page size set to 256 bytes, the opcode, 0BH, must be clocked into the device followed by three address bytes (A18 - A0) and a dummy byte. Following the dummy byte, additional clock pulses on the SCK pin will result in data being output on the SO (serial output) pin.

The CS pin must remain low during the loading of the opcode, the address bytes, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array. A low-to-high transition on the CS pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR1} specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

6.3 Continuous Array Read (Low Frequency Mode: 03H): Up to 33 MHz

This command can be used with the serial interface to read the main memory array sequentially without a dummy byte up to maximum frequencies specified by f_{CAR2}. To perform a continuous read array with the page size set to 264 bytes, the $\overline{CS}$ must first be asserted then an opcode, 03H, must be clocked into the device followed by three address bytes (which comprise the 24-bit page and byte address sequence). The first 11 bits (PA10 - PA0) of the 20-bit address sequence specify which page of the main memory array to read, and the last 9 bits (BA8 - BA0) of the 20-bit address sequence specify the starting byte address within the page. To perform a continuous read with the page size set to 256 bytes, the opcode, 03H, must be clocked into the device followed by three address bytes (A18 - A0). Following the address bytes, additional clock pulses on the SCK pin will result in data being output on the SO (serial output) pin.

The CS pin must remain low during the loading of the opcode, the address bytes, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array. A low-to-high transition on the CS pin will terminate the read operation and tri-state the output pin (SO). The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

6.4 Main Memory Page Read

A main memory page read allows the user to read data directly from any one of the 2,048 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read from the DataFlash standard page size (264 bytes), an opcode of D2H must be clocked into the device followed by three address bytes (which comprise the 24-bit page and byte address sequence) and 4 don't care bytes. The first 11 bits (PA10 - PA0) of the 20-bit address sequence specify the page in main memory to be read, and the last 9 bits (BA8 - BA0) of the 20-bit address sequence specify the starting byte address within that page. To start a page read from the binary page size (256 bytes), the opcode D2H must be clocked into the device followed by three address bytes and 4 don't care bytes. The first 11 bits (A18 - A8) of the 19-bits sequence specify which page of the main memory array to read, and the last 8 bits (A7 - A0) of the 19-bits address sequence specify the starting byte address within the page. The don't care bytes that follow the address bytes are sent to initialize the read operation. Following the don't care bytes, additional pulses on SCK result in data being output on the SO (serial output) pin. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don't care bytes, and the reading of data. When the end of a page in main

memory is reached, the device will continue reading back at the beginning of the same page. A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Main Memory Page Read is defined by the f_{SCK} specification. The Main Memory Page Read bypasses both data buffers and leaves the contents of the buffers unchanged.

6.5 Buffer Read

The SRAM data buffers can be accessed independently from the main memory array, and utilizing the Buffer Read Command allows data to be sequentially read directly from the buffers. Four opcodes, D4H or D1H for buffer 1 and D6H or D3H for buffer 2 can be used for the Buffer Read Command. The use of each opcode depends on the maximum SCK frequency that will be used to read data from the buffer. The D4H and D6H opcode can be used at any SCK frequency up to the maximum specified by f_{CAR1}. The D1H and D3H opcode can be used for lower frequency read operations up to the maximum specified by f_{CAR2}.

To perform a buffer read from the DataFlash standard buffer (264 bytes), the opcode must be clocked into the device followed by three address bytes comprised of 15 don't care bits and 9 buffer address bits (BFA8 - BFA0). To perform a buffer read from the binary buffer (256 bytes), the opcode must be clocked into the device followed by three address bytes comprised of 16 don't care bits and 8 buffer address bits (BFA7 - BFA0). Following the address bytes, one don't care byte must be clocked in to initialize the read operation. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don't care bytes, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO).

7. Program and Erase Commands

7.1 Buffer Write

Data can be clocked in from the input pin (SI) into either buffer 1 or buffer 2. To load data into the DataFlash standard buffer (264 bytes), a 1-byte opcode, 84H for buffer 1 or 87H for buffer 2, must be clocked into the device, followed by three address bytes comprised of 15 don't care bits and 9 buffer address bits (BFA8 - BFA0). The 9 buffer address bits specify the first byte in the buffer to be written. To load data into the binary buffers (256 bytes each), a 1-byte opcode 84H for buffer 1 or 87H for buffer 2, must be clocked into the device, followed by three address bytes comprised of 16 don't care bits and 8 buffer address bits (BFA7 - BFA0). The 8 buffer address bits specify the first byte in the buffer to be written. After the last address byte has been clocked into the device, data can then be clocked in on subsequent clock cycles. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low-to-high transition is detected on the $\overline{CS}$ pin.

7.2 Buffer to Main Memory Page Program with Built-in Erase

Data written into either buffer 1 or buffer 2 can be programmed into the main memory. A 1-byte opcode, 83H for buffer 1 or 86H for buffer 2, must be clocked into the device. For the DataFlash standard page size (264 bytes), the opcode must be followed by three address bytes consist of 4 don't care bits, 11 page address bits (PA10 - PA0) that specify the page in the main memory to be written and 9 don't care bits. To perform a buffer to main memory page program with built-in erase for the binary page size (256 bytes), the opcode 83H for buffer 1 or 86H for buffer 2, must be clocked into the device followed by three address bytes consisting of 5 don't care bits

11 page address bits (A18 - A8) that specify the page in the main memory to be written and 8 don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory (the erased state is a logic 1) and then program the data stored in the buffer into the specified page in main memory. Both the erase and the programming of the page are internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

7.3 Buffer to Main Memory Page Program without Built-in Erase

A previously-erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. A 1-byte opcode, 88H for buffer 1 or 89H for buffer 2, must be clocked into the device. For the DataFlash standard page size (264 bytes), the opcode must be followed by three address bytes consist of 4 don't care bits, 11 page address bits (PA10 - PA0) that specify the page in the main memory to be written and 9 don't care bits. To perform a buffer to main memory page program without built-in erase for the binary page size (256 bytes), the opcode 88H for buffer 1 or 89H for buffer 2, must be clocked into the device followed by three address bytes consisting of 5 don't care bits, 11 page address bits (A18 - A8) that specify the page in the main memory to be written and 8 don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously erased using one of the erase commands (Page Erase or Block Erase). The programming of the page is internally self-timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the part is busy.

7.4 Page Erase

The Page Erase command can be used to individually erase any page in the main memory array allowing the Buffer to Main Memory Page Program to be utilized at a later time. To perform a page erase in the DataFlash standard page size (264 bytes), an opcode of 81H must be loaded into the device, followed by three address bytes comprised of 4 don't care bits, 11 page address bits (PA10 - PA0) that specify the page in the main memory to be erased and 9 don't care bits. To perform a page erase in the binary page size (256 bytes), the opcode 81H must be loaded into the device, followed by three address bytes consist of 5 don't care bits, 11 page address bits (A18 - A8) that specify the page in the main memory to be erased and 8 don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will erase the selected page (the erased state is a logical 1). The erase operation is internally self-timed and should take place in a maximum time of t_{PE}. During this time, the status register will indicate that the part is busy.

7.5 Block Erase

A block of eight pages can be erased at one time. This command is useful when large amounts of data has to be written into the device. This will avoid using multiple Page Erase Commands. To perform a block erase for the DataFlash standard page size (264 bytes), an opcode of 50H must be loaded into the device, followed by three address bytes comprised of 4 don't care bits, 8 page address bits (PA10 - PA3) and 12 don't care bits. The 8 page address bits are used to specify which block of eight pages is to be erased. To perform a block erase for the binary page size (256 bytes), the opcode 50H must be loaded into the device, followed by three address bytes consisting of 5 don't care bits, 8 page address bits (A18 - A11) and 11 don't care bits. The 9 page address bits are used to specify which block of eight pages is to be erased. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will erase the selected block of eight pages. The erase operation is internally self-timed and should take place in a maximum time of t_{BE}. During this time, the status register will indicate that the part is busy.

Table 7-1. Block Erase Addressing

PA10/ A18	PA9/ A17	PA8/ A16	PA7/ A15	PA6/ A14	PA5/ A13	PA4/ A12	PA3/ A11	PA2/ A10	PA1/ A9	PA0/ A8	Block
0	0	0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	0	0	1	X	X	X	1
0	0	0	0	0	0	1	0	X	X	X	2
0	0	0	0	0	0	1	1	X	X	X	3
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	0	0	X	X	X	252
1	1	1	1	1	1	0	1	X	X	X	253
1	1	1	1	1	1	1	0	X	X	X	254
1	1	1	1	1	1	1	1	X	X	X	255

7.6 Sector Erase

The Sector Erase command can be used to individually erase any sector in the main memory. There are 8 sectors and only one sector can be erased at one time. To perform sector 0a or sector 0b erase for the DataFlash standard page size (264 bytes), an opcode of 7CH must be loaded into the device, followed by three address bytes comprised of 4 don't care bits, 8 page address bits (PA10 - PA3) and 12 don't care bits. To perform a sector 1-7 erase, the opcode 7CH must be loaded into the device, followed by three address bytes comprised of 4 don't care bits, 3 page address bits (PA10 - PA8) and 17 don't care bits. To perform sector 0a or sector 0b erase for the binary page size (256 bytes), an opcode of 7CH must be loaded into the device, followed by three address bytes comprised of 5 don't care bit and 8 page address bits (A18 - A11) and 11 don't care bits. To perform a sector 1-15 erase, the opcode 7CH must be loaded into the device, followed by three address bytes comprised of 5 don't care bit and 3 page address bits (A18 - A16) and 17 don't care bits. The page address bits are used to specify any valid address location within the sector which is to be erased. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will erase the selected sector. The erase operation is internally self-timed and should take place in a maximum time of t_{SE}. During this time, the status register will indicate that the part is busy.

Table 7-2. Sector Erase Addressing

PA10/ A18	PA9/ A17	PA8/ A16	PA7/ A15	PA6/ A14	PA5/ A13	PA4/ A12	PA3/ A11	PA2/ A10	PA1/ A9	PA0/ A8	Sector
0	0	0	0	0	0	0	0	X	X	X	0a
0	0	0	0	0	0	0	1	X	X	X	0b
0	0	1	X	X	X	X	X	X	X	X	1
0	1	0	X	X	X	X	X	X	X	X	2
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
1	0	0	X	X	X	X	X	X	X	X	4
1	0	1	X	X	X	X	X	X	X	X	5
1	1	0	X	X	X	X	X	X	X	X	6
1	1	1	X	X	X	X	X	X	X	X	7

7.7 Chip Erase[1]

The entire main memory can be erased at one time by using the Chip Erase command.

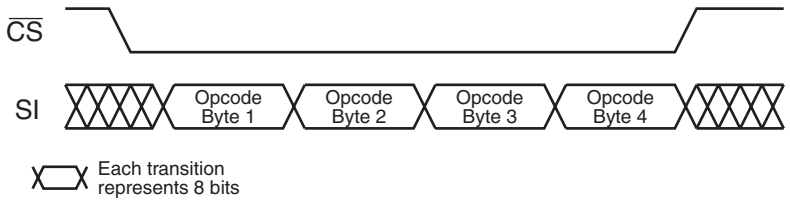
To execute the Chip Erase command, a 4-byte command sequence C7H, 94H, 80H and 9AH must be clocked into the device. Since the entire memory array is to be erased, no address bytes need to be clocked into the device, and any data clocked in after the opcode will be ignored. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin can be deasserted to start the erase process. The erase operation is internally self-timed and should take place in a time of t_{CE}. During this time, the Status Register will indicate that the device is busy.

The Chip Erase command will not affect sectors that are protected or locked down; the contents of those sectors will remain unchanged. Only those sectors that are not protected or locked down will be erased.

The $\overline{WP}$ pin can be asserted while the device is erasing, but protection will not be activated until the internal erase cycle completes.

Command	Byte 1	Byte 2	Byte 3	Byte 4
Chip Erase	C7H	94H	80H	9AH

Figure 7-1. Chip Erase



Note: 1. Refer to the errata regarding Chip Erase on page 52.

7.8 Main Memory Page Program Through Buffer

This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-in Erase operations. Data is first clocked into buffer 1 or buffer 2 from the input pin (SI) and then programmed into a specified page in the main memory. To perform a main memory page program through buffer for the DataFlash standard page size (264 bytes), a 1-byte opcode, 82H for buffer 1 or 85H for buffer 2, must first be clocked into the device, followed by three address bytes. The address bytes are comprised of 4 don't care bits, 11 page address bits, (PA10 - PA0) that select the page in the main memory where data is to be written, and 9 buffer address bits (BFA8 - BFA0) that select the first byte in the buffer to be written. To perform a main memory page program through buffer for the binary page size (256 bytes), the opcode 82H for buffer 1 or 85H for buffer 2, must be clocked into the device followed by three address bytes consisting of 5 don't care bits, 11 page address bits (A18 - A8) that specify the page in the main memory to be written, and 8 buffer address bits (BFA7 - BFA0) that selects the first byte in the buffer to be written. After all address bytes are clocked in, the part will take data from the input pins and store it in the specified data buffer. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low-to-high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into that memory page. Both the erase and the programming of the page are internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

8. Sector Protection

Two protection methods, hardware and software controlled, are provided for protection against inadvertent or erroneous program and erase cycles. The software controlled method relies on the use of software commands to enable and disable sector protection while the hardware controlled method employs the use of the Write Protect ($\overline{WP}$) pin. The selection of which sectors that are to be protected or unprotected against program and erase operations is specified in the nonvolatile Sector Protection Register. The status of whether or not sector protection has been enabled or disabled by either the software or the hardware controlled methods can be determined by checking the Status Register.

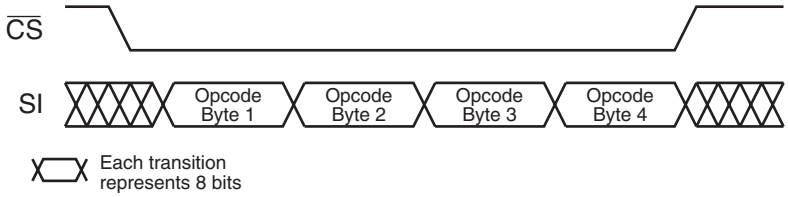
8.1 Software Sector Protection

8.1.1 Enable Sector Protection Command

Sectors specified for protection in the Sector Protection Register can be protected from program and erase operations by issuing the Enable Sector Protection command. To enable the sector protection using the software controlled method, the $\overline{CS}$ pin must first be asserted as it would be with any other command. Once the $\overline{CS}$ pin has been asserted, the appropriate 4-byte command sequence must be clocked in via the input pin (SI). After the last bit of the command sequence has been clocked in, the $\overline{CS}$ pin must be deasserted after which the sector protection will be enabled.

Command	Byte 1	Byte 2	Byte 3	Byte 4
Enable Sector Protection	3DH	2AH	7FH	A9H

Figure 8-1. Enable Sector Protection

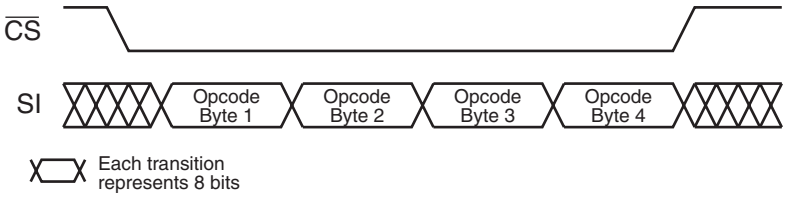


8.1.2 Disable Sector Protection Command

To disable the sector protection using the software controlled method, the $\overline{CS}$ pin must first be asserted as it would be with any other command. Once the $\overline{CS}$ pin has been asserted, the appropriate 4-byte sequence for the Disable Sector Protection command must be clocked in via the input pin (SI). After the last bit of the command sequence has been clocked in, the $\overline{CS}$ pin must be deasserted after which the sector protection will be disabled. The $\overline{WP}$ pin must be in the deasserted state; otherwise, the Disable Sector Protection command will be ignored.

Command	Byte 1	Byte 2	Byte 3	Byte 4
Disable Sector Protection	3DH	2AH	7FH	9AH

Figure 8-2. Disable Sector Protection



8.1.3 Various Aspects About Software Controlled Protection

Software controlled protection is useful in applications in which the $\overline{WP}$ pin is not or cannot be controlled by a host processor. In such instances, the $\overline{WP}$ pin may be left floating (the $\overline{WP}$ pin is internally pulled high) and sector protection can be controlled using the Enable Sector Protection and Disable Sector Protection commands.

If the device is power cycled, then the software controlled protection will be disabled. Once the device is powered up, the Enable Sector Protection command should be reissued if sector protection is desired and if the $\overline{WP}$ pin is not used.

9. Hardware Controlled Protection

Sectors specified for protection in the Sector Protection Register and the Sector Protection Register itself can be protected from program and erase operations by asserting the $\overline{WP}$ pin and keeping the pin in its asserted state. The Sector Protection Register and any sector specified for protection cannot be erased or reprogrammed as long as the $\overline{WP}$ pin is asserted. In order to modify the Sector Protection Register, the $\overline{WP}$ pin must be deasserted. If the $\overline{WP}$ pin is permanently connected to GND, then the content of the Sector Protection Register cannot be changed. If the $\overline{WP}$ pin is deasserted, or permanently connected to V_{CC}, then the content of the Sector Protection Register can be modified.

The $\overline{WP}$ pin will override the software controlled protection method but only for protecting the sectors. For example, if the sectors were not previously protected by the Enable Sector Protection command, then simply asserting the $\overline{WP}$ pin would enable the sector protection within the maximum specified t_{WPE} time. When the $\overline{WP}$ pin is deasserted; however, the sector protection would no longer be enabled (after the maximum specified t_{WPD} time) as long as the Enable Sector Protection command was not issued while the $\overline{WP}$ pin was asserted. If the Enable Sector Protection command was issued before or while the $\overline{WP}$ pin was asserted, then simply deasserting the $\overline{WP}$ pin would not disable the sector protection. In this case, the Disable Sector Protection command would need to be issued while the $\overline{WP}$ pin is deasserted to disable the sector protection. The Disable Sector Protection command is also ignored whenever the $\overline{WP}$ pin is asserted.

A noise filter is incorporated to help protect against spurious noise that may inadvertently assert or deassert the $\overline{WP}$ pin.

The table below details the sector protection status for various scenarios of the $\overline{WP}$ pin, the Enable Sector Protection command, and the Disable Sector Protection command.

Figure 9-1. $\overline{WP}$ Pin and Protection Status

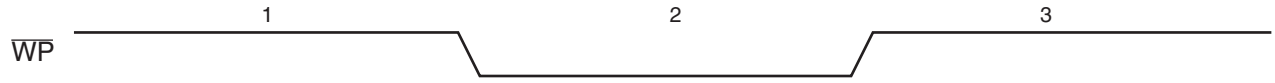


Table 9-1. $\overline{WP}$ Pin and Protection Status

Time Period	$\overline{WP}$ Pin	Enable Sector Protection Command	Disable Sector Protection Command	Sector Protection Status	Sector Protection Register
1	High	Command Not Issued Previously – Issue Command	X Issue Command –	Disabled Disabled Enabled	Read/Write Read/Write Read/Write
2	Low	X	X	Enabled	Read Only
3	High	Command Issued During Period 1 or 2 – Issue Command	Not Issued Yet Issue Command –	Enabled Disabled Enabled	Read/Write Read/Write Read/Write

9.1 Sector Protection Register

The nonvolatile Sector Protection Register specifies which sectors are to be protected or unprotected with either the software or hardware controlled protection methods. The Sector Protection Register contains 8 bytes of data, of which byte locations 0 through 7 contain values that specify whether sectors 0 through 7 will be protected or unprotected. The Sector Protection Register is user modifiable and must first be erased before it can be reprogrammed. Table 9-3 illustrates the format of the Sector Protection Register.:

Table 9-2. Sector Protection Register

Sector Number	0 (0a, 0b)	1 to 7
Protected	See Table 9-3	FFH
Unprotected		00H

Table 9-3. Sector 0 (0a, 0b)

	0a	0b			
	(Page 0-7)	(Page 8-255)			
	Bit 7, 6	Bit 5, 4	Bit 3, 2	Bit 1, 0	Data Value
Sectors 0a, 0b Unprotected	00	00	xx	xx	0xH
Protect Sector 0a	11	00	xx	xx	CxH
Protect Sector 0b (Page 8-255)	00	11	xx	xx	3xH
Protect Sectors 0a (Page 0-7), 0b (Page 8-255)(1)	11	11	xx	xx	FxH

Note: 1. The default value for bytes 0 through 15 when shipped from Atmel® is 00H.
x = don't care.

9.1.1 Erase Sector Protection Register Command

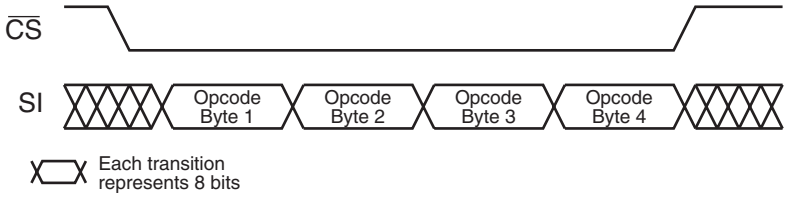
In order to modify and change the values of the Sector Protection Register, it must first be erased using the Erase Sector Protection Register command.

To erase the Sector Protection Register, the $\overline{CS}$ pin must first be asserted as it would be with any other command. Once the $\overline{CS}$ pin has been asserted, the appropriate 4-byte opcode sequence must be clocked into the device via the SI pin. The 4-byte opcode sequence must start with 3DH and be followed by 2AH, 7FH, and CFH. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed erase cycle. The erasing of the Sector Protection Register should take place in a time of t_{PE}, during which time the Status Register will indicate that the device is busy. If the device is powered-down before the completion of the erase cycle, then the contents of the Sector Protection Register cannot be guaranteed.

The Sector Protection Register can be erased with the sector protection enabled or disabled. Since the erased state (FFH) of each byte in the Sector Protection Register is used to indicate that a sector is specified for protection, leaving the sector protection enabled during the erasing of the register allows the protection scheme to be more effective in the prevention of accidental programming or erasing of the device. If for some reason an erroneous program or erase command is sent to the device immediately after erasing the Sector Protection Register and before the register can be reprogrammed, then the erroneous program or erase command will not be processed because all sectors would be protected.

Command	Byte 1	Byte 2	Byte 3	Byte 4
Erase Sector Protection Register	3DH	2AH	7FH	CFH

Figure 9-2. Erase Sector Protection Register



9.1.2 Program Sector Protection Register Command

Once the Sector Protection Register has been erased, it can be reprogrammed using the Program Sector Protection Register command.

To program the Sector Protection Register, the $\overline{CS}$ pin must first be asserted and the appropriate 4-byte opcode sequence must be clocked into the device via the SI pin. The 4-byte opcode sequence must start with 3DH and be followed by 2AH, 7FH, and FCH. After the last bit of the opcode sequence has been clocked into the device, the data for the contents of the Sector Protection Register must be clocked in. As described in Section 9.1, the Sector Protection Register contains 8 bytes of data, so 8 bytes must be clocked into the device. The first byte of data corresponds to sector 0, the second byte corresponds to sector 1, and so on with the last byte of data corresponding to sector 7.

After the last data byte has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed program cycle. The programming of the Sector Protection Register should take place in a time of t_P, during which time the Status Register will indicate that the device is busy. If the device is powered-down during the program cycle, then the contents of the Sector Protection Register cannot be guaranteed.

If the proper number of data bytes is not clocked in before the $\overline{CS}$ pin is deasserted, then the protection status of the sectors corresponding to the bytes not clocked in can not be guaranteed. For example, if only the first two bytes are clocked in instead of the complete 8 bytes, then the protection status of the last 6 sectors cannot be guaranteed. Furthermore, if more than 8 bytes of data is clocked into the device, then the data will wrap back around to the beginning of the register. For instance, if 9 bytes of data are clocked in, then the 9th byte will be stored at byte location 0 of the Sector Protection Register.

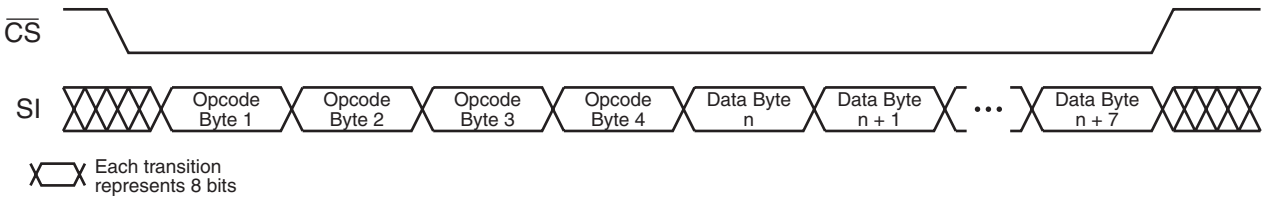
If a value other than 00H or FFH is clocked into a byte location of the Sector Protection Register, then the protection status of the sector corresponding to that byte location cannot be guaranteed. For example, if a value of 17H is clocked into byte location 2 of the Sector Protection Register, then the protection status of sector 2 cannot be guaranteed.

The Sector Protection Register can be reprogrammed while the sector protection enabled or disabled. Being able to reprogram the Sector Protection Register with the sector protection enabled allows the user to temporarily disable the sector protection to an individual sector rather than disabling sector protection completely.

The Program Sector Protection Register command utilizes the internal SRAM buffer 1 for processing. Therefore, the contents of the buffer 1 will be altered from its previous state when this command is issued.

Command	Byte 1	Byte 2	Byte 3	Byte 4
Program Sector Protection Register	3DH	2AH	7FH	FCH

Figure 9-3. Program Sector Protection Register



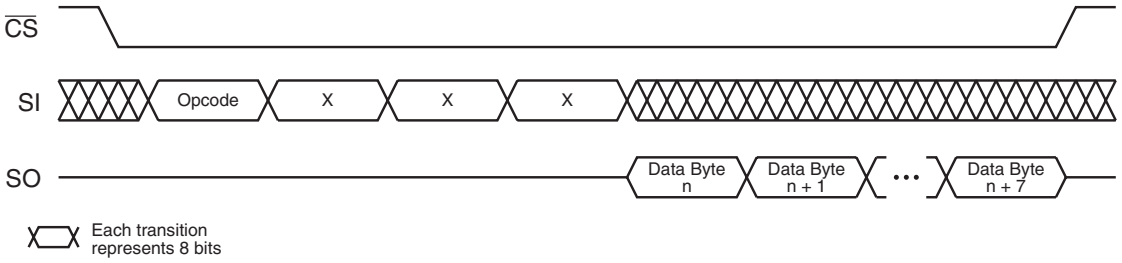
9.1.3 Read Sector Protection Register Command

To read the Sector Protection Register, the $\overline{CS}$ pin must first be asserted. Once the $\overline{CS}$ pin has been asserted, an opcode of 32H and 3 dummy bytes must be clocked in via the SI pin. After the last bit of the opcode and dummy bytes have been clocked in, any additional clock pulses on the SCK pins will result in data for the content of the Sector Protection Register being output on the SO pin. The first byte corresponds to sector 0 (0a, 0b), the second byte corresponds to sector 1 and the last byte (byte 8) corresponds to sector 7. Once the last byte of the Sector Protection Register has been clocked out, any additional clock pulses will result in undefined data being output on the SO pin. The $\overline{CS}$ must be deasserted to terminate the Read Sector Protection Register operation and put the output into a high-impedance state.

Command	Byte 1	Byte 2	Byte 3	Byte 4
Read Sector Protection Register	32H	xxH	xxH	xxH

Note: xx = Dummy Byte

Figure 9-4. Read Sector Protection Register



9.1.4 Various Aspects About the Sector Protection Register

The Sector Protection Register is subject to a limit of 10,000 erase/program cycles. Users are encouraged to carefully evaluate the number of times the Sector Protection Register will be modified during the course of the applications' life cycle. If the application requires that the Sector Protection Register be modified more than the specified limit of 10,000 cycles because the application needs to temporarily unprotect individual sectors (sector protection remains enabled while the Sector Protection Register is reprogrammed), then the application will need to limit this practice. Instead, a combination of temporarily unprotecting individual sectors along with disabling sector protection completely will need to be implemented by the application to ensure that the limit of 10,000 cycles is not exceeded.

10. Security Features

10.1 Sector Lockdown

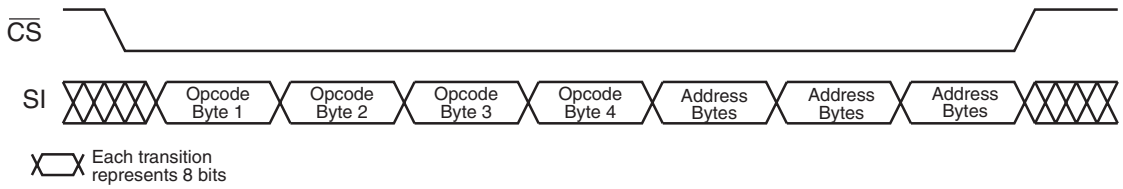
The device incorporates a Sector Lockdown mechanism that allows each individual sector to be permanently locked so that it becomes read only. This is useful for applications that require the ability to permanently protect a number of sectors against malicious attempts at altering program code or security information. **Once a sector is locked down, it can never be erased or programmed, and it can never be unlocked.**

To issue the Sector Lockdown command, the $\overline{CS}$ pin must first be asserted as it would be for any other command. Once the $\overline{CS}$ pin has been asserted, the appropriate 4-byte opcode sequence must be clocked into the device in the correct order. The 4-byte opcode sequence must start with 3DH and be followed by 2AH, 7FH, and 30H. After the last byte of the command sequence has been clocked in, then three address bytes specifying any address within the sector to be locked down must be clocked into the device. After the last address bit has been clocked in, the $\overline{CS}$ pin must then be deasserted to initiate the internally self-timed lockdown sequence.

The lockdown sequence should take place in a maximum time of t_P, during which time the Status Register will indicate that the device is busy. If the device is powered-down before the completion of the lockdown sequence, then the lockdown status of the sector cannot be guaranteed. In this case, it is recommended that the user read the Sector Lockdown Register to determine the status of the appropriate sector lockdown bits or bytes and reissue the Sector Lockdown command if necessary.

Command	Byte 1	Byte 2	Byte 3	Byte 4
Sector Lockdown	3DH	2AH	7FH	30H

Figure 10-1. Sector Lockdown



10.1.1 Sector Lockdown Register

Sector Lockdown Register is a nonvolatile register that contains 16 bytes of data, as shown below:

Sector Number	0 (0a, 0b)	1 to 7
Locked	See Below	FFH
Unlocked		00H

Table 10-1. Sector 0 (0a, 0b)

	0a (Page 0-7) Bit 7, 6	0b (Page 8-255) Bit 5, 4	Bit 3, 2	Bit 1, 0	Data Value
Sectors 0a, 0b Unlocked	00	00	00	00	00H
Sector 0a Locked (Page 0-7)	11	00	00	00	C0H
Sector 0b Locked (Page 8-255)	00	11	00	00	30H
Sectors 0a, 0b Locked (Page 0-255)	11	11	00	00	F0H

10.1.2 Reading the Sector Lockdown Register

The Sector Lockdown Register can be read to determine which sectors in the memory array are permanently locked down. To read the Sector Lockdown Register, the $\overline{CS}$ pin must first be asserted. Once the $\overline{CS}$ pin has been asserted, an opcode of 35H and 3 dummy bytes must be clocked into the device via the SI pin. After the last bit of the opcode and dummy bytes have been clocked in, the data for the contents of the Sector Lockdown Register will be clocked out on the SO pin. The first byte corresponds to sector 0 (0a, 0b) the second byte corresponds to sector 1 and the las byte (byte 8) corresponds to sector 7. After the last byte of the Sector Lockdown Register has been read, additional pulses on the SCK pin will simply result in undefined data being output on the SO pin.

Deasserting the $\overline{CS}$ pin will terminate the Read Sector Lockdown Register operation and put the SO pin into a high-impedance state.

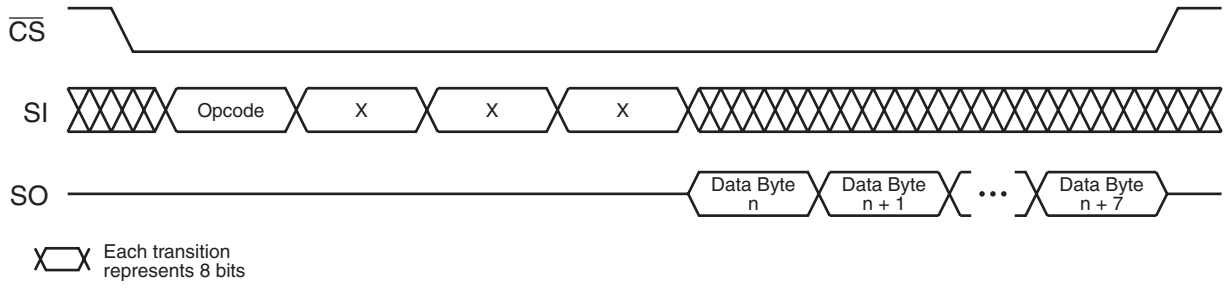
Table 10-2 details the values read from the Sector Lockdown Register.

Table 10-2. Sector Lockdown Register

Command	Byte 1	Byte 2	Byte 3	Byte 4
Read Sector Lockdown Register	35H	xxH	xxH	xxH

Note: xx = Dummy Byte

Figure 10-2. Read Sector Lockdown Register



10.2 Security Register

The device contains a specialized Security Register that can be used for purposes such as unique device serialization or locked key storage. The register is comprised of a total of 128 bytes that is divided into two portions. The first 64 bytes (byte locations 0 through 63) of the Security Register are allocated as a one-time user programmable space. Once these 64 bytes have been programmed, they cannot be reprogrammed. The remaining 64 bytes of the register (byte locations 64 through 127) are factory programmed by Atmel and will contain a unique value for each device. The factory programmed data is fixed and cannot be changed.

Table 10-3. Security Register

	Security Register Byte Number									
	0	**1**	**• • •**	**62**	**63**	**64**	**65**	**• • •**	**126**	**127**
Data Type	One-time User Programmable					Factory Programmed By Atmel				

10.2.1 Programming the Security Register

The user programmable portion of the Security Register does not need to be erased before it is programmed.

To program the Security Register, the $\overline{CS}$ pin must first be asserted and the appropriate 4-byte opcode sequence must be clocked into the device in the correct order. The 4-byte opcode sequence must start with 9BH and be followed by 00H, 00H, and 00H. After the last bit of the opcode sequence has been clocked into the device, the data for the contents of the 64-byte user programmable portion of the Security Register must be clocked in.

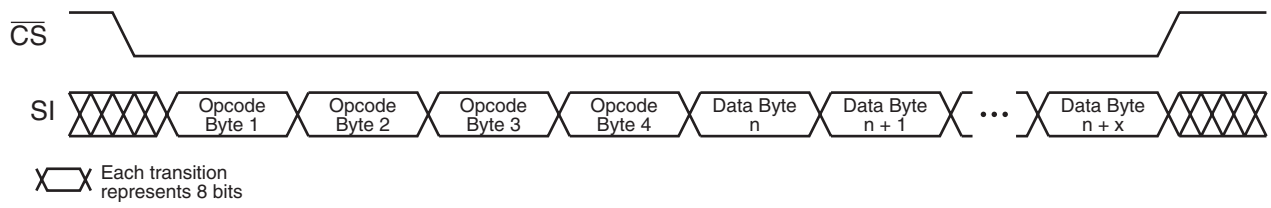
After the last data byte has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed program cycle. The programming of the Security Register should take place in a time of t_P, during which time the Status Register will indicate that the device is busy. If the device is powered-down during the program cycle, then the contents of the 64-byte user programmable portion of the Security Register cannot be guaranteed.

If the full 64 bytes of data is not clocked in before the $\overline{CS}$ pin is deasserted, then the values of the byte locations not clocked in cannot be guaranteed. For example, if only the first two bytes are clocked in instead of the complete 64 bytes, then the remaining 62 bytes of the user programmable portion of the Security Register cannot be guaranteed. Furthermore, if more than 64 bytes of data is clocked into the device, then the data will wrap back around to the beginning of the register. For instance, if 65 bytes of data are clocked in, then the 65th byte will be stored at byte location 0 of the Security Register.

The user programmable portion of the Security Register can only be programmed one time. Therefore, it is not possible to only program the first two bytes of the register and then program the remaining 62 bytes at a later time.

The Program Security Register command utilizes the internal SRAM buffer 1 for processing. Therefore, the contents of the buffer 1 will be altered from its previous state when this command is issued.

Figure 10-3. Program Security Register

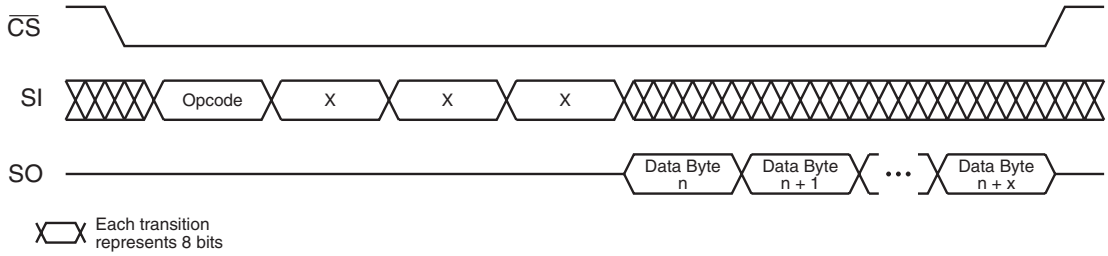


10.2.2 Reading the Security Register

The Security Register can be read by first asserting the $\overline{CS}$ pin and then clocking in an opcode of 77H followed by three dummy bytes. After the last don't care bit has been clocked in, the content of the Security Register can be clocked out on the SO pins. After the last byte of the Security Register has been read, additional pulses on the SCK pin will simply result in undefined data being output on the SO pins.

Deasserting the $\overline{CS}$ pin will terminate the Read Security Register operation and put the SO pins into a high-impedance state.

Figure 10-4. Read Security Register



11. Additional Commands

11.1 Main Memory Page to Buffer Transfer

A page of data can be transferred from the main memory to either buffer 1 or buffer 2. To start the operation for the DataFlash standard page size (264 bytes), a 1-byte opcode, 53H for buffer 1 and 55H for buffer 2, must be clocked into the device, followed by three address bytes comprised of 4 don't care bits, 11 page address bits (PA10 - PA0), which specify the page in main memory that is to be transferred, and 9 don't care bits. To perform a main memory page to buffer transfer for the binary page size (256 bytes), the opcode 53H for buffer 1 or 55H for buffer 2, must be clocked into the device followed by three address bytes consisting of 5 don't care bits, 11 page address bits (A18 - A8) which specify the page in the main memory that is to be transferred, and 8 don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode and the address bytes from the input pin (SI). The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed.

11.2 Main Memory Page to Buffer Compare

A page of data in main memory can be compared to the data in buffer 1 or buffer 2. To initiate the operation for the DataFlash standard page size, a 1-byte opcode, 60H for buffer 1 and 61H for buffer 2, must be clocked into the device, followed by three address bytes consisting of 4 don't care bits, 11 page address bits (PA10 - PA0) that specify the page in the main memory that is to be compared to the buffer, and 9 don't care bits. To start a main memory page to buffer compare for a binary page size, the opcode 60H for buffer 1 or 61H for buffer 2, must be clocked into the device followed by three address bytes consisting of 5 don't care bits, 11 page address bits (A18 - A8) that specify the page in the main memory that is to be compared to the buffer, and 8 don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode and

the address bytes from the input pin (SI). On the low-to-high transition of the $\overline{CS}$ pin, the data bytes in the selected main memory page will be compared with the data bytes in buffer 1 or buffer 2. During this time (t_{COMP}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

11.3 Auto Page Rewrite

This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion within a sector. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-in Erase. A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) is programmed back into its original page of main memory. To start the rewrite operation for the DataFlash standard page size (264 bytes), a 1-byte opcode, 58H for buffer 1 or 59H for buffer 2, must be clocked into the device, followed by three address bytes comprised of 4 don't care bits, 11 page address bits (PA10-PA0) that specify the page in main memory to be rewritten and 9 don't care bits. To initiate an auto page rewrite for a binary page size (256 bytes), the opcode 58H for buffer 1 or 59H for buffer 2, must be clocked into the device followed by three address bytes consisting of 5 don't care bits, 11 page address bits (A18 - A8) that specify the page in the main memory that is to be written and 8 don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

If a sector is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 25-1 (page 45) is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in a sector, then the programming algorithm shown in Figure 25-2 (page 46) is recommended. Each page within a sector must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations in that sector.

11.4 Status Register Read

The status register can be used to determine the device's ready/busy status, page size, a Main Memory Page to Buffer Compare operation result, the Sector Protection status or the device density. The Status Register can be read at any time, including during an internally self-timed program or erase operation. To read the status register, the $\overline{CS}$ pin must be asserted and the opcode of D7H must be loaded into the device. After the opcode is clocked in, the 1-byte status register will be clocked out on the output pin (SO), starting with the next clock cycle. The data in the status register, starting with the MSB (bit 7), will be clocked out on the SO pin during the next eight clock cycles. After the one byte of the status register has been clocked out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled). The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. Since the data in the status register is constantly updated, the user must toggle SCK pin to check the ready/busy status. There are several operations that can cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program, Main Memory Page Program through Buffer, Page Erase, Block Erase, Sector Erase, Chip Erase and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

Bit 1 in the Status Register is used to provide information to the user whether or not the sector protection has been enabled or disabled, either by software-controlled method or hardware-controlled method. A logic 1 indicates that sector protection has been enabled and logic 0 indicates that sector protection has been disabled.

Bit 0 in the Status Register indicates whether the page size of the main memory array is configured for “power of 2” binary page size (256 bytes) or the DataFlash standard page size (264 bytes). If bit 0 is a 1, then the page size is set to 256 bytes. If bit 0 is a 0, then the page size is set to 264 bytes.

The device density is indicated using bits 5, 4, 3, and 2 of the status register. For the AT45DB041D, the four bits are 0111 The decimal value of these four binary bits does not equate to the device density; the four bits represent a combinational code relating to differing densities of DataFlash devices. The device density is not the same as the density code indicated in the JEDEC device ID information. The device density is provided only for backward compatibility.

Table 11-1. Status Register Format

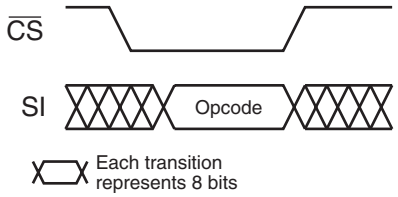
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{\text{BUSY}}$	COMP	0	1	1	1	PROTECT	PAGE SIZE

12. Deep Power-down

After initial power-up, the device will default in standby mode. The Deep Power-down command allows the device to enter into the lowest power consumption mode. To enter the Deep Power-down mode, the $\overline{CS}$ pin must first be asserted. Once the $\overline{CS}$ pin has been asserted, an opcode of B9H command must be clocked in via input pin (SI). After the last bit of the command has been clocked in, the $\overline{CS}$ pin must be de-asserted to initiate the Deep Power-down operation. After the $\overline{CS}$ pin is de-asserted, the will device enter the Deep Power-down mode within the maximum t_{EDPD} time. Once the device has entered the Deep Power-down mode, all instructions are ignored except for the Resume from Deep Power-down command.

Command	Opcode
Deep Power-down	B9H

Figure 12-1. Deep Power-down

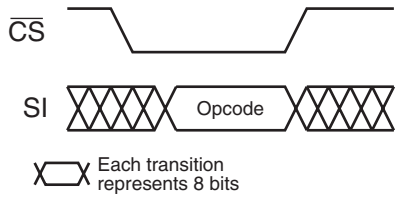


12.1 Resume from Deep Power-down

The Resume from Deep Power-down command takes the device out of the Deep Power-down mode and returns it to the normal standby mode. To Resume from Deep Power-down mode, the $\overline{CS}$ pin must first be asserted and an opcode of ABH command must be clocked in via input pin (SI). After the last bit of the command has been clocked in, the $\overline{CS}$ pin must be de-asserted to terminate the Deep Power-down mode. After the $\overline{CS}$ pin is de-asserted, the device will return to the normal standby mode within the maximum t_{RDPD} time. The $\overline{CS}$ pin must remain high during the t_{RDPD} time before the device can receive any commands. After resuming form Deep Power-down, the device will return to the normal standby mode.

Command	Opcode
Resume from Deep Power-down	ABH

Figure 12-2. Resume from Deep Power-Down



13. “Power of 2” Binary Page Size Option

“Power of 2” binary page size Configuration Register is a user-programmable nonvolatile register that allows the page size of the main memory to be configured for binary page size (256 bytes) or the DataFlash standard page size (264 bytes). **The “power of 2” page size is a one-time programmable configuration register and once the device is configured for “power of 2” page size, it cannot be reconfigured again.** The devices are initially shipped with the page size set to 264 bytes.

For the binary “power of 2” page size to become effective, the following steps must be followed:

1. Program the one-time programmable configuration resister using opcode sequence 3DH, 2AH, 80H and A6H (please see Section 13.1).
2. Power cycle the device (i.e. power down and power up again).
3. The page for the binary page size can now be programmed.

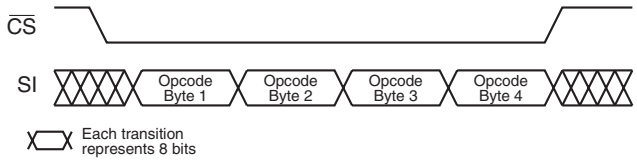
If the above steps are not followed to set the page size prior to page programming, incorrect data during a read operation may be encountered.

13.1 Programming the Configuration Register

To program the Configuration Register for “power of 2” binary page size, the $\overline{CS}$ pin must first be asserted as it would be with any other command. Once the $\overline{CS}$ pin has been asserted, the appropriate 4-byte opcode sequence must be clocked into the device in the correct order. The 4-byte opcode sequence must start with 3DH and be followed by 2AH, 80H, and A6H. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed program cycle. The programming of the Configuration Register should take place in a time of t_P, during which time the Status Register will indicate that the device is busy. The device must be power-cycled after the completion of the program cycle to set the “power of 2” page size. If the device is powered-down before the completion of the program cycle, then setting the Configuration Register cannot be guaranteed. However, the user should check bit 0 of the status register to see whether the page size was configured for binary page size. If not, the command can be re-issued again.

Command	Byte 1	Byte 2	Byte 3	Byte 4
Power of Two Page Size	3DH	2AH	80H	A6H

Figure 13-1. Erase Sector Protection Register



14. Manufacturer and Device ID Read

Identification information can be read from the device to enable systems to electronically query and identify the device while it is in system. The identification method and the command opcode comply with the JEDEC standard for “Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices”. The type of information that can be read from the device includes the JEDEC defined Manufacturer ID, the vendor specific Device ID, and the vendor specific Extended Device Information.

To read the identification information, the $\overline{CS}$ pin must first be asserted and the opcode of 9FH must be clocked into the device. After the opcode has been clocked in, the device will begin outputting the identification data on the SO pin during the subsequent clock cycles. The first byte

that will be output will be the Manufacturer ID followed by two bytes of Device ID information. The fourth byte output will be the Extended Device Information String Length, which will be 00H indicating that no Extended Device Information follows. As indicated in the JEDEC standard, reading the Extended Device Information String Length and any subsequent data is optional.

Deasserting the $\overline{CS}$ pin will terminate the Manufacturer and Device ID Read operation and put the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

14.1 Manufacturer and Device ID Information

14.1.1 Byte 1 – Manufacturer ID

Hex Value	JEDEC Assigned Code							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1FH	0	0	0	1	1	1	1	1

Manufacturer ID	1FH = Atmel

14.1.2 Byte 2 – Device ID (Part 1)

Hex Value	Family Code			Density Code				
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
24H	0	0	1	0	0	1	0	0

Family Code	001 = DataFlash
Density Code	00100 = 16-Mbit

14.1.3 Byte 3 – Device ID (Part 2)

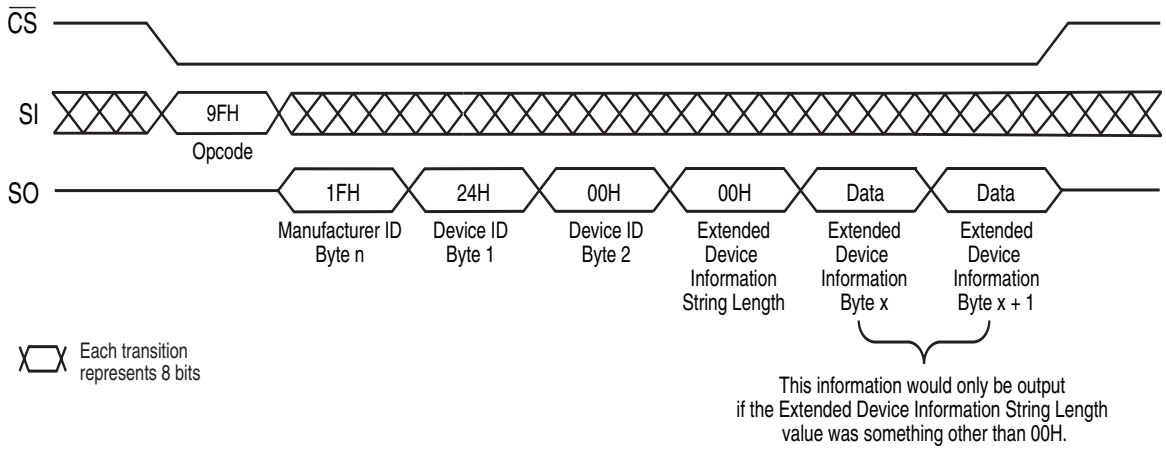
Hex Value	MLC Code			Product Version Code				
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	0	0	0	0	0	0	0	0

MLC Code	000 = 1-bit/Cell Technology
Product Version	00000 = Initial Version

14.1.4 Byte 4 – Extended Device Information String Length

Hex Value	Byte Count							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	0	0	0	0	0	0	0	0

Byte Count	00H = 0 Bytes of Information



Note: Based on JEDEC publication 106 (JEP106), Manufacturer ID data can be comprised of any number of bytes. Some manufacturers may have Manufacturer ID codes that are two, three or even four bytes long with the first byte(s) in the sequence being 7FH. A system should detect code 7FH as a "Continuation Code" and continue to read Manufacturer ID bytes. The first non-7FH byte would signify the last byte of Manufacturer ID data. For Atmel (and some other manufacturers), the Manufacturer ID data is comprised of only one byte.

14.2 Operation Mode Summary

The commands described previously can be grouped into four different categories to better describe which commands can be executed at what times.

Group A commands consist of:

1. Main Memory Page Read
2. Continuous Array Read
3. Read Sector Protection Register
4. Read Sector Lockdown Register
5. Read Security Register

Group B commands consist of:

1. Page Erase
2. Block Erase
3. Sector Erase
4. Chip Erase
5. Main Memory Page to Buffer 1 (or 2) Transfer
6. Main Memory Page to Buffer 1 (or 2) Compare
7. Buffer 1 (or 2) to Main Memory Page Program with Built-in Erase
8. Buffer 1 (or 2) to Main Memory Page Program without Built-in Erase
9. Main Memory Page Program through Buffer 1 (or 2)
10. Auto Page Rewrite

Group C commands consist of:

1. Buffer 1 (or 2) Read
2. Buffer 1 (or 2) Write
3. Status Register Read
4. Manufacturer and Device ID Read

Group D commands consist of:

1. Erase Sector Protection Register
2. Program Sector Protection Register
3. Sector Lockdown
4. Program Security Register

If a Group A command is in progress (not fully completed), then another command in Group A, B, C, or D should not be started. However, during the internally self-timed portion of Group B commands, any command in Group C can be executed. The Group B commands using buffer 1 should use Group C commands using buffer 2 and vice versa. Finally, during the internally self-timed portion of a Group D command, only the Status Register Read command should be executed.

15. Command Tables

Table 15-1. Read Commands

Command	Opcode
Main Memory Page Read	D2H
Continuous Array Read (Legacy Command)	E8H
Continuous Array Read (Low Frequency)	03H
Continuous Array Read (High Frequency)	0BH
Buffer 1 Read (Low Frequency)	D1H
Buffer 2 Read (Low Frequency)	D3H
Buffer 1 Read	D4H
Buffer 2 Read	D6H

Table 15-2. Program and Erase Commands

Command	Opcode
Buffer 1 Write	84H
Buffer 2 Write	87H
Buffer 1 to Main Memory Page Program with Built-in Erase	83H
Buffer 2 to Main Memory Page Program with Built-in Erase	86H
Buffer 1 to Main Memory Page Program without Built-in Erase	88H
Buffer 2 to Main Memory Page Program without Built-in Erase	89H
Page Erase	81H
Block Erase	50H
Sector Erase	7CH
Chip Erase	C7H, 94H, 80H, 9AH
Main Memory Page Program Through Buffer 1	82H
Main Memory Page Program Through Buffer 2	85H

Table 15-3. Protection and Security Commands

Command	Opcode
Enable Sector Protection	3DH + 2AH + 7FH + A9H
Disable Sector Protection	3DH + 2AH + 7FH + 9AH
Erase Sector Protection Register	3DH + 2AH + 7FH + CFH
Program Sector Protection Register	3DH + 2AH + 7FH + FCH
Read Sector Protection Register	32H
Sector Lockdown	3DH + 2AH + 7FH + 30H
Read Sector Lockdown Register	35H
Program Security Register	9BH + 00H + 00H + 00H
Read Security Register	77H

Table 15-4. Additional Commands

Command	Opcode
Main Memory Page to Buffer 1 Transfer	53H
Main Memory Page to Buffer 2 Transfer	55H
Main Memory Page to Buffer 1 Compare	60H
Main Memory Page to Buffer 2 Compare	61H
Auto Page Rewrite through Buffer 1	58H
Auto Page Rewrite through Buffer 2	59H
Deep Power-down	B9H
Resume from Deep Power-down	ABH
Status Register Read	D7H
Manufacturer and Device ID Read	9FH

Table 15-5. Legacy Commands[1]

Command	Opcode
Buffer 1 Read	54H
Buffer 2 Read	56H
Main Memory Page Read	52H
Continuous Array Read	68H
Status Register Read	57H

Note: 1. These legacy commands are not recommended for new designs.

Table 15-6. Detailed Bit-level Addressing Sequence for Binary Page Size (256 Bytes)

Page Size = 256 bytes									Address Byte								Address Byte								Address Byte								Additional Don't Care Bytes
Opcode	Opcode								Reserved	Reserved	Reserved	Reserved	Reserved	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
03h	0	0	0	0	0	0	1	1	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
0Bh	0	0	0	0	1	0	1	1	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	1
50h	0	1	0	1	0	0	0	0	x	x	x	x	x	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	x	x	x	N/A
53h	0	1	0	1	0	0	1	1	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	N/A
55h	0	1	0	1	0	1	0	1	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	N/A
58h	0	1	0	1	1	0	0	0	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	N/A
59h	0	1	0	1	1	0	0	1	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	N/A
60h	0	1	1	0	0	0	0	0	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	N/A
61h	0	1	1	0	0	0	0	1	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	N/A
77h	0	1	1	1	0	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	N/A
7Ch	0	1	1	1	1	1	0	0	x	x	x	x	x	A	A	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	N/A
81h	1	0	0	0	0	0	0	1	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	N/A
82h	1	0	0	0	0	0	1	0	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
83h	1	0	0	0	0	0	1	1	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	N/A
84h	1	0	0	0	0	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	A	A	A	A	A	A	A	N/A
85h	1	0	0	0	0	1	0	1	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
86h	1	0	0	0	0	1	1	0	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	N/A
87h	1	0	0	0	0	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	A	A	A	A	A	A	A	N/A
88h	1	0	0	0	1	0	0	0	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	N/A
89h	1	0	0	0	1	0	0	1	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	N/A
9Fh	1	0	0	1	1	1	1	1	N/A								N/A								N/A								N/A
B9h	1	0	1	1	1	0	0	1	N/A								N/A								N/A								N/A
ABh	1	0	1	0	1	0	1	1	N/A								N/A								N/A								N/A
D1h	1	1	0	1	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	A	A	A	A	A	A	A	A	N/A
D2h	1	1	0	1	0	0	1	0	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	4
D3h	1	1	0	1	0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	A	A	A	A	A	A	A	A	N/A
D4h	1	1	0	1	0	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	A	A	A	A	A	A	A	A	1
D6h	1	1	0	1	0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	A	A	A	A	A	A	A	A	1
D7h	1	1	0	1	0	1	1	1	N/A								N/A								N/A								N/A
E8h	1	1	1	0	1	0	0	0	x	x	x	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	4

Notes: x = Don't Care

Table 15-7. Detailed Bit-level Addressing Sequence for Standard DataFlash Page Size (264 Bytes)

Page Size = 264 bytes									Address Byte								Address Byte								Address Byte								Additional Don't Care Bytes
Opcode	Opcode								Reserved	Reserved	Reserved	Reserved	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	BA0	BA8	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	
03h	0	0	0	0	0	0	1	1	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	N/A
0Bh	0	0	0	0	1	0	1	1	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	1
50h	0	1	0	1	0	0	0	0	x	x	x	x	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	x	N/A
53h	0	1	0	1	0	0	1	1	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	N/A
55h	0	1	0	1	0	1	0	1	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	N/A
58h	0	1	0	1	1	0	0	0	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	N/A
59h	0	1	0	1	1	0	0	1	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	N/A
60h	0	1	1	0	0	0	0	0	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	N/A
61h	0	1	1	0	0	0	0	1	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	N/A
77h	0	1	1	1	0	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	N/A
7Ch	0	1	1	1	1	1	0	0	x	x	x	x	P	P	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	N/A
81h	1	0	0	0	0	0	0	1	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	N/A
82h	1	0	0	0	0	0	1	0	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	N/A
83h	1	0	0	0	0	0	1	1	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	N/A
84h	1	0	0	0	0	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	N/A
85h	1	0	0	0	0	1	0	1	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	N/A
86h	1	0	0	0	0	1	1	0	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	N/A
87h	1	0	0	0	0	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	N/A
88h	1	0	0	0	1	0	0	0	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	N/A
89h	1	0	0	0	1	0	0	1	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	N/A
9Fh	1	0	0	1	1	1	1	1	N/A								N/A								N/A								N/A
B9h	1	0	1	1	1	0	0	1	N/A								N/A								N/A								N/A
ABh	1	0	1	0	1	0	1	1	N/A								N/A								N/A								N/A
D1h	1	1	0	1	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	N/A
D2h	1	1	0	1	0	0	1	0	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	4
D3h	1	1	0	1	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	N/A
D4h	1	1	0	1	0	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	1
D6h	1	1	0	1	0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	1
D7h	1	1	0	1	0	1	1	1	N/A								N/A								N/A								N/A
E8h	1	1	1	0	1	0	0	0	x	x	x	x	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	4

Notes: P = Page Address Bit B = Byte/Buffer Address Bit x = Don't Care

16. Power-on/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to Mode 3. In addition, the output pin (SO) will be in a high impedance state, and a high-to-low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The mode (Mode 3 or Mode 0) will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state.

16.1 Initial Power-up/Reset Timing Restrictions

At power up, the device must not be selected until the supply voltage reaches the V_{CC} (min.) and further delay of t_{VCSL}. During power-up, the internal Power-on Reset circuitry keeps the device in reset mode until the V_{CC} rises above the Power-on Reset threshold value (V_{POR}). At this time, all operations are disabled and the device does not respond to any commands. After power up is applied and the V_{CC} is at the minimum operating voltage V_{CC} (min.), the t_{VCSL} delay is required before the device can be selected in order to perform a read operation.

Similarly, the t_{PUW} delay is required after the V_{CC} rises above the Power-on Reset threshold value (V_{POR}) before the device can perform a write (Program or Erase) operation. After initial power-up, the device will default in Standby mode.

Symbol	Parameter	Min	Typ	Max	Units
t_{VCSL}	V_{CC} (min.) to Chip Select low	50			µs
t_{PUW}	Power-Up Device Delay before Write Allowed			20	ms
V_{POR}	Power-ON Reset Voltage	1.5		2.5	V

17. System Considerations

The RapidS serial interface is controlled by the clock SCK, serial input SI and chip select $\overline{CS}$ pins. These signals must rise and fall monotonically and be free from noise. Excessive noise or ringing on these pins can be misinterpreted as multiple edges and cause improper operation of the device. The PC board traces must be kept to a minimum distance or appropriately terminated to ensure proper operation. If necessary, decoupling capacitors can be added on these pins to provide filtering against noise glitches.

As system complexity continues to increase, voltage regulation is becoming more important. A key element of any voltage regulation scheme is its current sourcing capability. Like all Flash memories, the peak current for DataFlash occur during the programming and erase operation. The regulator needs to supply this peak current requirement. An under specified regulator can cause current starvation. Besides increasing system noise, current starvation during programming or erase can lead to improper operation and possible data corruption.

18. Electrical Specifications

Table 18-1. Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 18-2. DC and AC Operating Range

		AT45DB041D (2.5V Version)	AT45DB041D
Operating Temperature (Case)	Ind.	-40°C to 85°C	-40°C to 85°C
V_{CC} Power Supply		2.5V to 3.6V	2.7V to 3.6V

Table 18-3. DC Characteristics

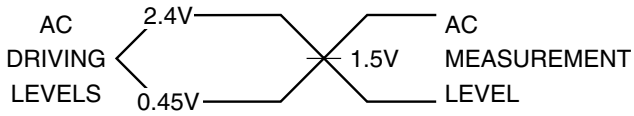
Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DP}	Deep Power-down Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		5	10	µA
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		25	50	µA
I_{CC1} (1)	Active Current, Read Operation	f = 20 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		7	10	mA
		f = 33 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		8	12	mA
		f = 50 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		10	14	mA
		f = 66 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		11	15	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		12	17	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input Low Voltage				V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

Notes: 1. I_{CC1} during a buffer read is 20 mA maximum @ 20 MHz.
2. All inputs are 5 volts tolerant.

Table 18-4. AC Characteristics – RapidS/Serial Interface

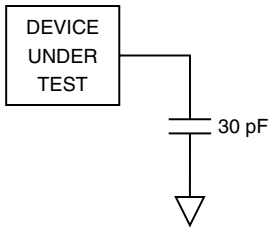
Symbol	Parameter	AT45DB041D (2.5V Version)			AT45DB041D			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK}	SCK Frequency			50			66	MHz
f_{CAR1}	SCK Frequency for Continuous Array Read			50			66	MHz
f_{CAR2}	SCK Frequency for Continuous Array Read (Low Frequency)			33			33	MHz
t_{WH}	SCK High Time	6.8			6.8			ns
t_{WL}	SCK Low Time	6.8			6.8			ns
t_{SCKR}[1]	SCK Rise Time, Peak-to-Peak (Slew Rate)	0.1			0.1			V/ns
t_{SCKF}[1]	SCK Fall Time, Peak-to-Peak (Slew Rate)	0.1			0.1			V/ns
t_{CS}	Minimum $\overline{CS}$ High Time	50			50			ns
t_{CSS}	$\overline{CS}$ Setup Time	5			5			ns
t_{CSH}	$\overline{CS}$ Hold Time	5			5			ns
t_{SU}	Data In Setup Time	2			2			ns
t_H	Data In Hold Time	3			3			ns
t_{HO}	Output Hold Time	0			0			ns
t_{DIS}	Output Disable Time			8			6	ns
t_V	Output Valid			8			6	ns
t_{WPE}	$\overline{WP}$ Low to Protection Enabled			1			1	µs
t_{WPD}	$\overline{WP}$ High to Protection Disabled			1			1	µs
t_{EDPD}	$\overline{CS}$ High to Deep Power-down Mode			3			3	µs
t_{RDPD}	$\overline{CS}$ High to Standby Mode			30			30	µs
t_{XFR}	Page to Buffer Transfer Time			400			400	µs
t_{comp}	Page to Buffer Compare Time			400			400	µs
t_{EP}	Page Erase and Programming Time (256/264 bytes)		14	35		14	35	ms
t_P	Page Programming Time (256/264 bytes)		2	4		2	4	ms
t_{PE}	Page Erase Time (256/264 bytes)		13	32		13	32	ms
t_{BE}	Block Erase Time (2,048/2,112 bytes)		30	75		30	75	ms
t_{SE}	Sector Erase Time (65,536/67,584 bytes)		1.6	5		1.6	5	s
t_{CE}	Chip Erase Time		TBD	TBD		TBD	TBD	s
t_{RST}	$\overline{RESET}$ Pulse Width	10			10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1			1	µs

19. Input Test Waveforms and Measurement Levels



t_R, t_F < 2 ns (10% to 90%)

20. Output Test Load

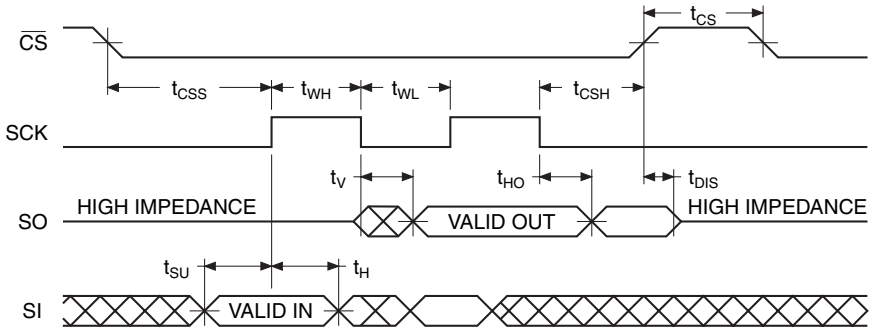


21. AC Waveforms

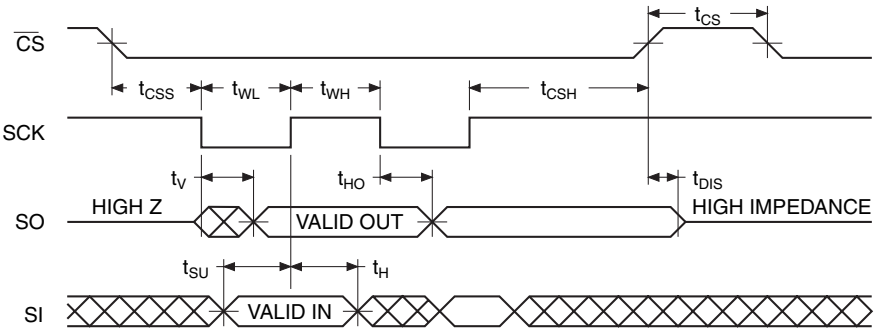
Six different timing waveforms are shown on page 36. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. In both cases, output SO becomes valid while the SCK signal is still low (SCK low time is specified as t_{WL}). Timing waveforms 1 and 2 conform to RapidS serial interface but for frequencies up to 66 MHz. Waveforms 1 and 2 are compatible with SPI Mode 0 and SPI Mode 3, respectively.

Waveform 3 and waveform 4 illustrate general timing diagram for RapidS serial interface. These are similar to waveform 1 and waveform 2, except that output SO is not restricted to become valid during the t_{WL} period. These timing waveforms are valid over the full frequency range (maximum frequency = 66 MHz) of the RapidS serial case.

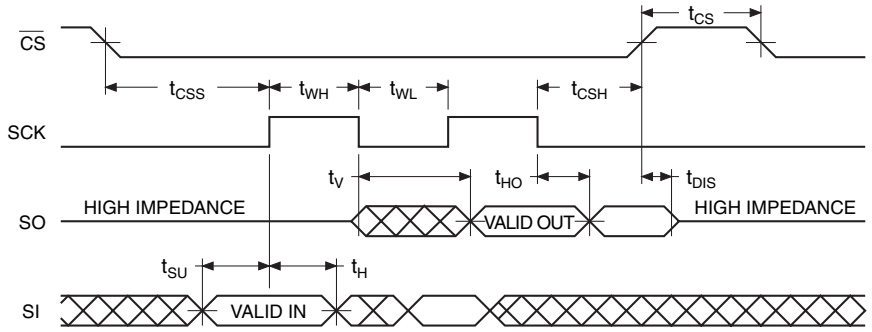
21.1 Waveform 1 – SPI Mode 0 Compatible (for Frequencies up to 66 MHz)



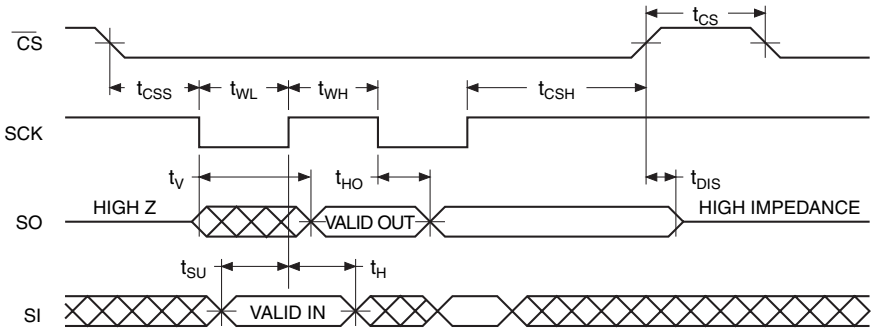
21.2 Waveform 2 – SPI Mode 3 Compatible (for Frequencies up to 66 MHz)



21.3 Waveform 3 – RapidS Mode 0 (F_{MAX} = 66 MHz)



21.4 Waveform 4 – RapidS Mode 3 (F_{MAX} = 66 MHz)

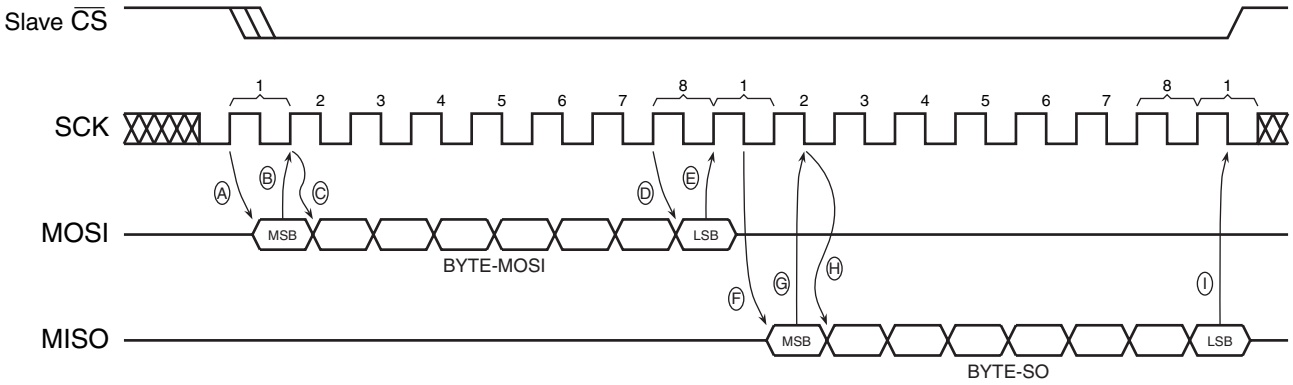


21.5 Utilizing the RapidS Function

To take advantage of the RapidS function's ability to operate at higher clock frequencies, a full clock cycle must be used to transmit data back and forth across the serial bus. The DataFlash is designed to always clock its data out on the falling edge of the SCK signal and clock data in on the rising edge of SCK.

For full clock cycle operation to be achieved, when the DataFlash is clocking data out on the falling edge of SCK, the host controller should wait until the next falling edge of SCK to latch the data in. Similarly, the host controller should clock its data out on the rising edge of SCK in order to give the DataFlash a full clock cycle to latch the incoming data in on the next rising edge of SCK.

Figure 21-1. RapidS Mode

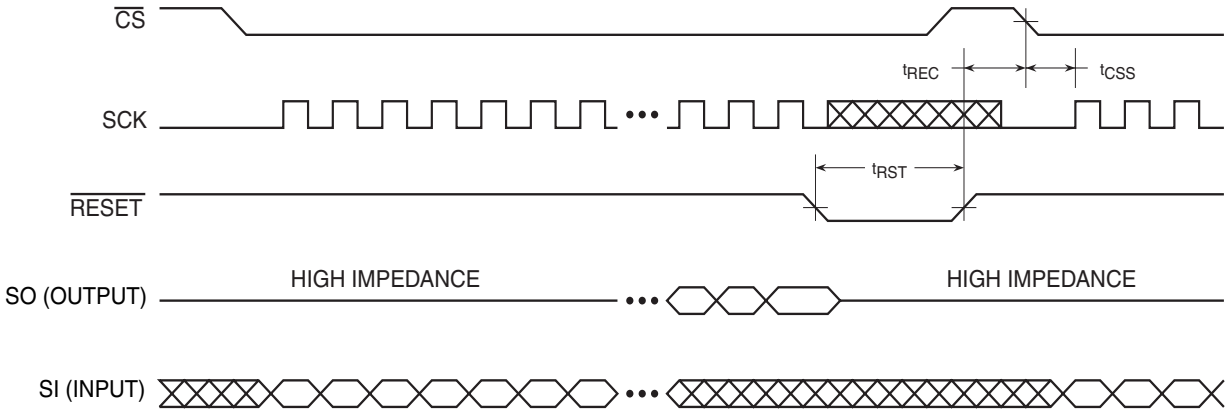


MOSI = Master Out, Slave In
MISO = Master In, Slave Out
The Master is the host controller and the Slave is the DataFlash

The Master always clocks data out on the rising edge of SCK and always clocks data in on the falling edge of SCK.
The Slave always clocks data out on the falling edge of SCK and always clocks data in on the rising edge of SCK.

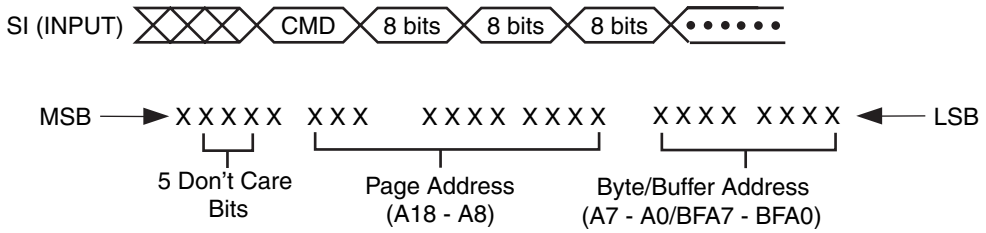
A. Master clocks out first bit of BYTE-MOSI on the rising edge of SCK.
B. Slave clocks in first bit of BYTE-MOSI on the next rising edge of SCK.
C. Master clocks out second bit of BYTE-MOSI on the same rising edge of SCK.
D. Last bit of BYTE-MOSI is clocked out from the Master.
E. Last bit of BYTE-MOSI is clocked into the slave.
F. Slave clocks out first bit of BYTE-SO.
G. Master clocks in first bit of BYTE-SO.
H. Slave clocks out second bit of BYTE-SO.
I. Master clocks in last bit of BYTE-SO.

21.6 Reset Timing

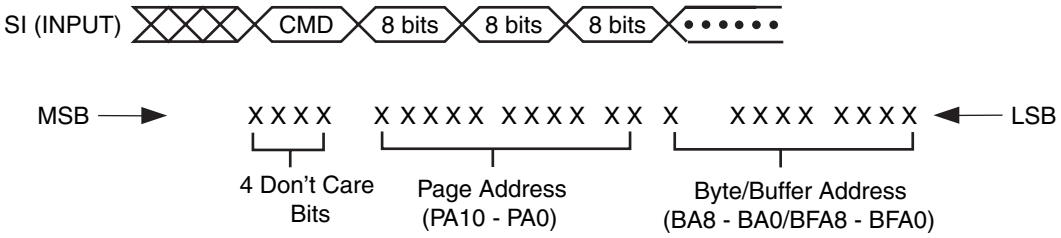


Note: The $\overline{CS}$ signal should be in the high state before the $\overline{RESET}$ signal is deasserted.

21.7 Command Sequence for Read/Write Operations for Page Size 256 Bytes (Except Status Register Read, Manufacturer and Device ID Read)

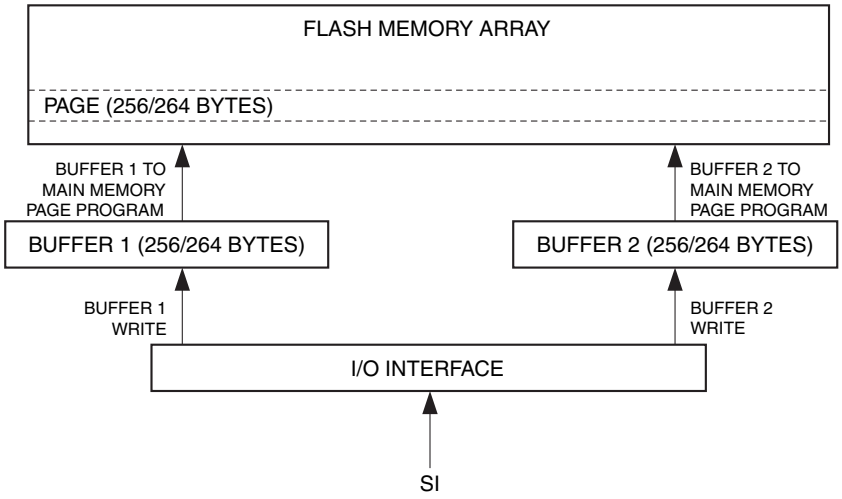


21.8 Command Sequence for Read/Write Operations for Page Size 264 Bytes (Except Status Register Read, Manufacturer and Device ID Read)

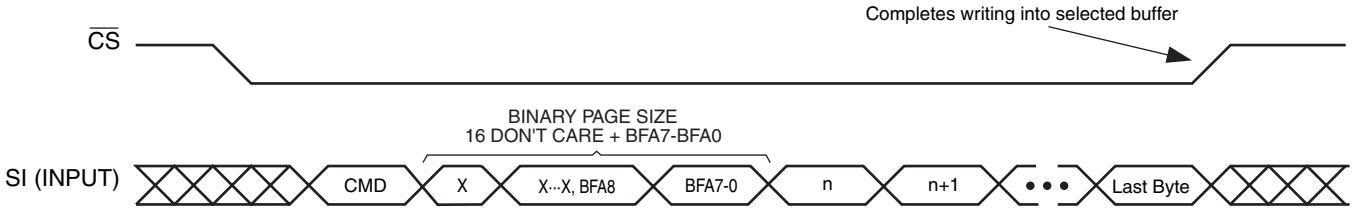


22. Write Operations

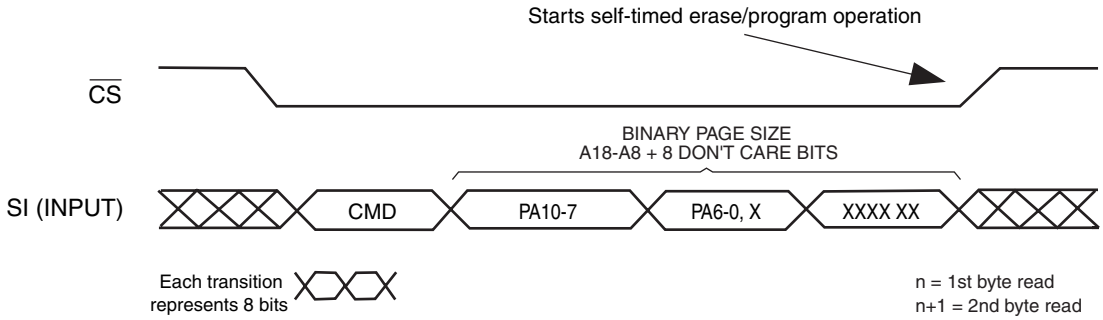
The following block diagram and waveforms illustrate the various write sequences available.



22.1 Buffer Write

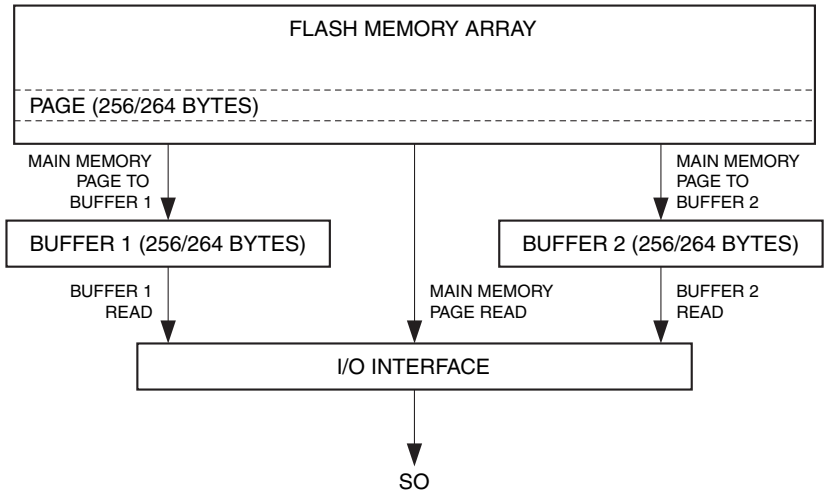


22.2 Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)

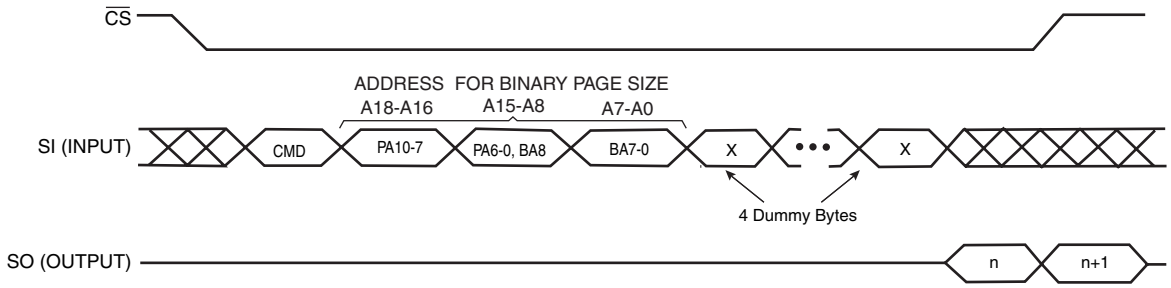


23. Read Operations

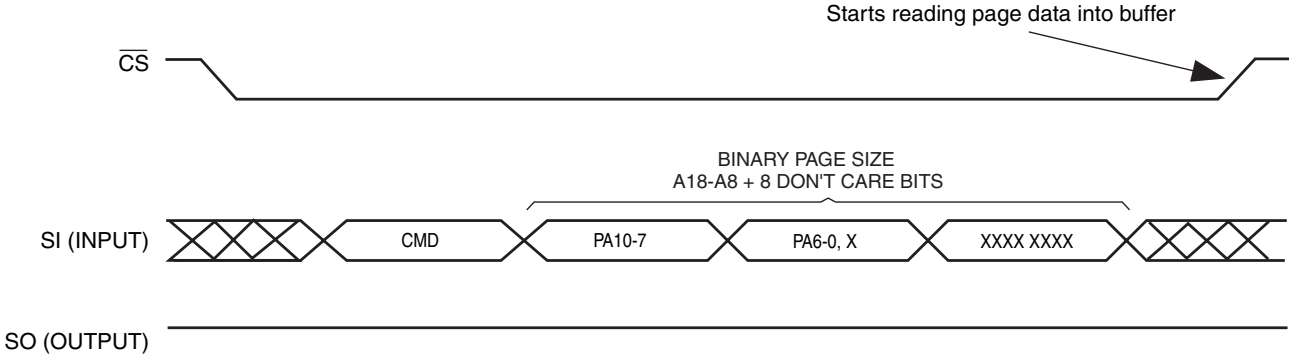
The following block diagram and waveforms illustrate the various read sequences available.



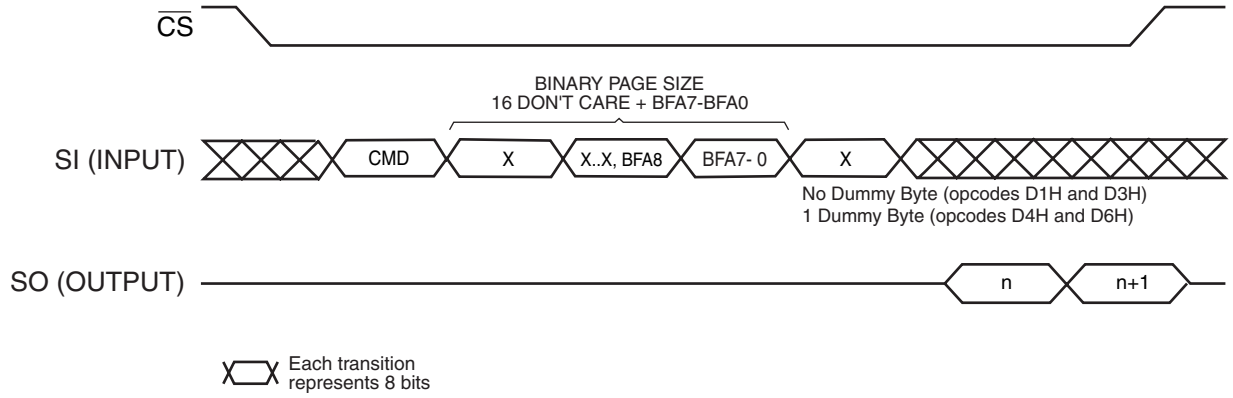
23.1 Main Memory Page Read



23.2 Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)

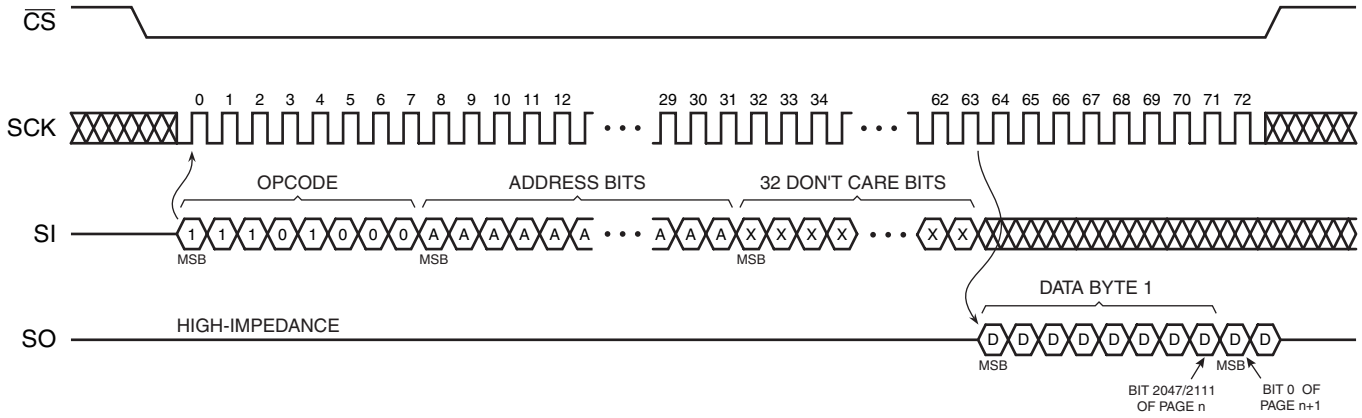


23.3 Buffer Read

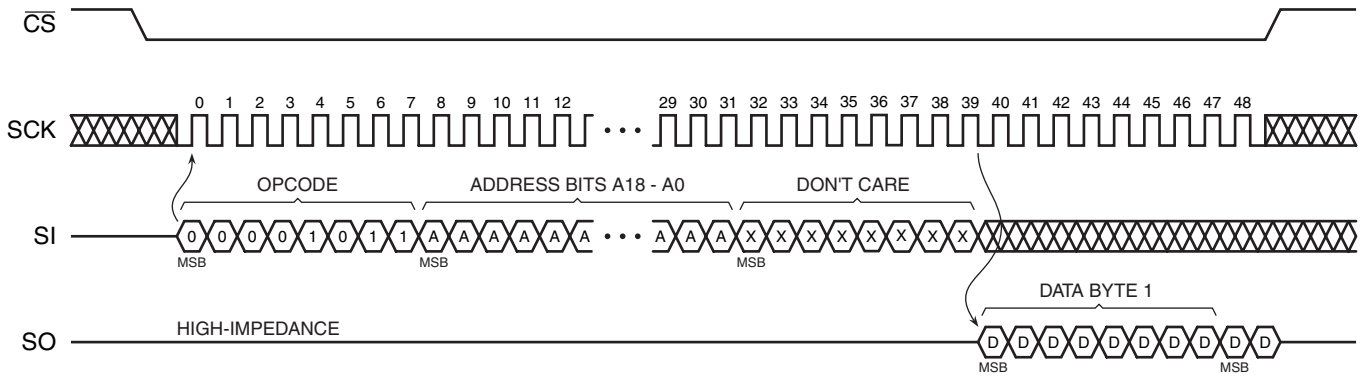


24. Detailed Bit-level Read Waveform – RapidS Serial Interface Mode 0/Mode 3

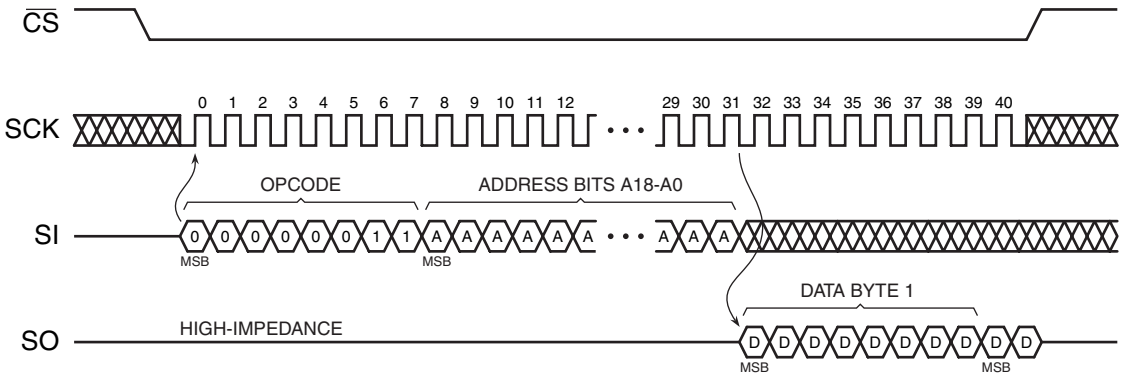
24.1 Continuous Array Read (Legacy Opcode E8H)



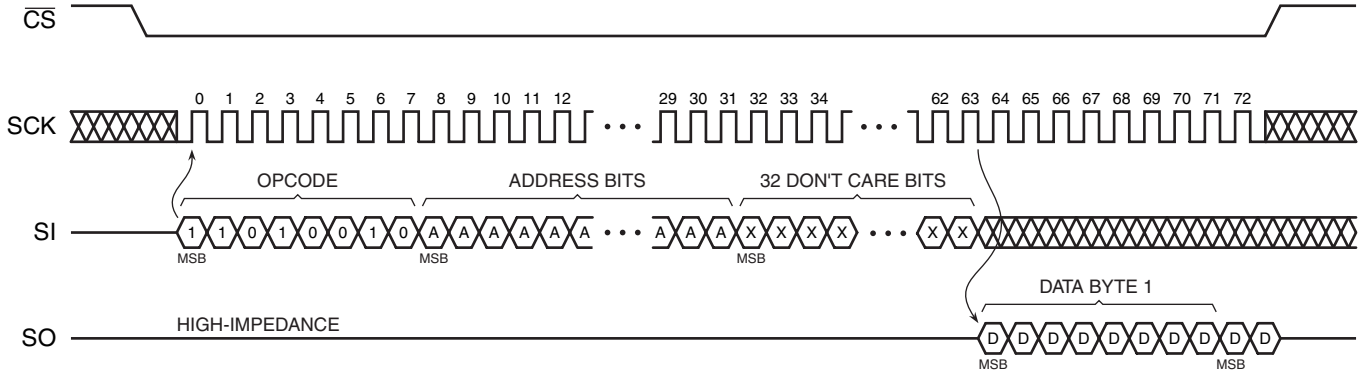
24.2 Continuous Array Read (Opcode 0BH)



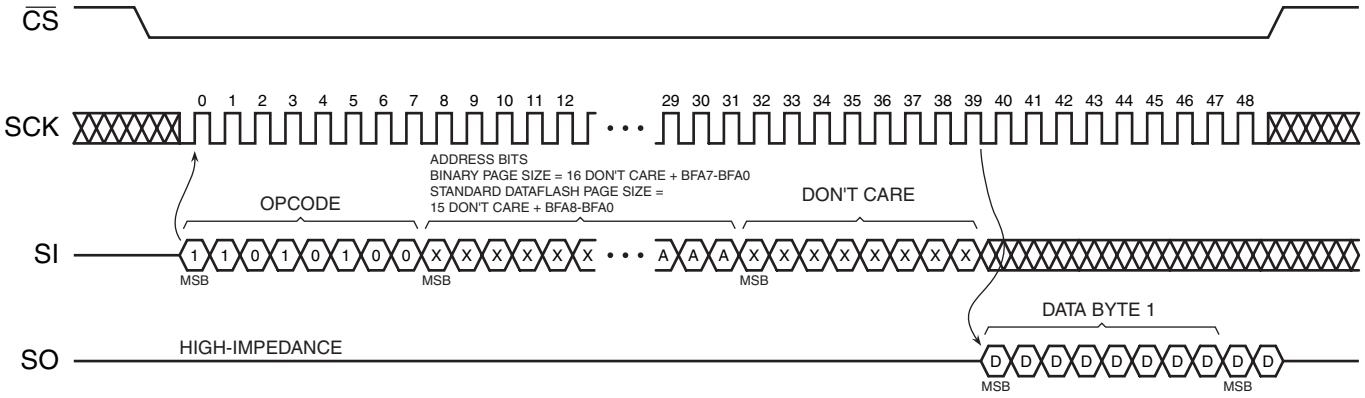
24.3 Continuous Array Read (Low Frequency: Opcode 03H)



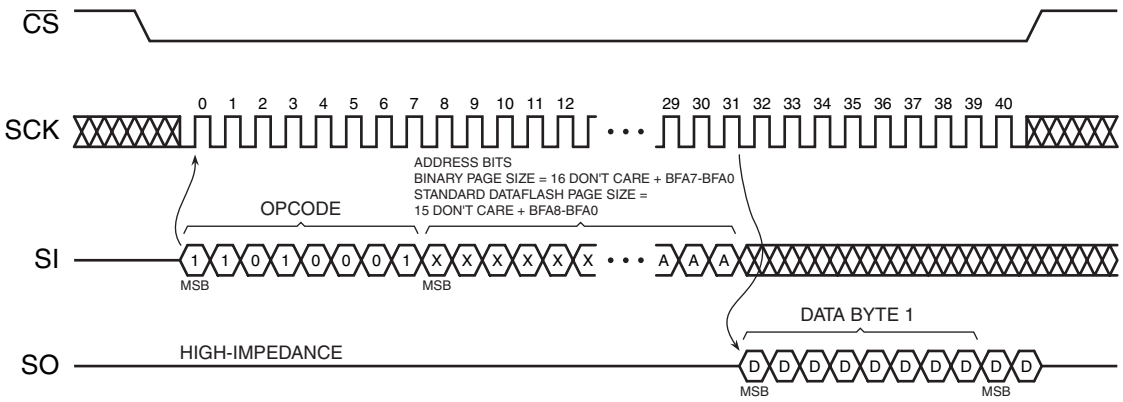
24.4 Main Memory Page Read (Opcode: D2H)



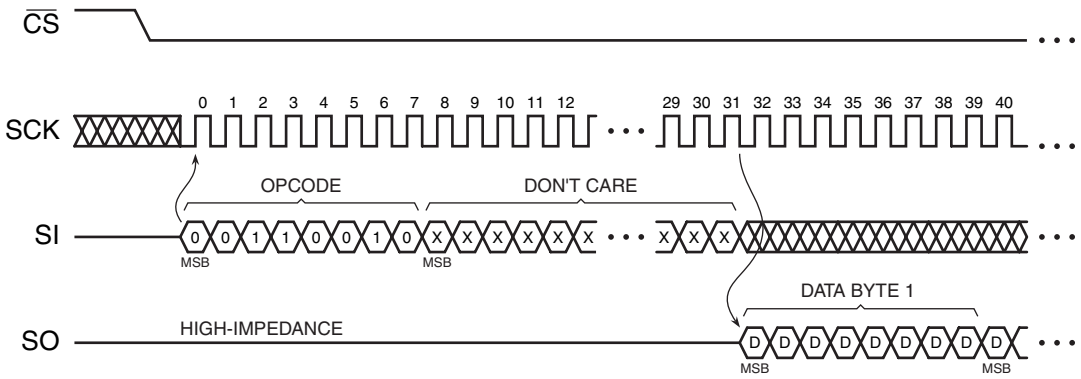
24.5 Buffer Read (Opcode D4H or D6H)



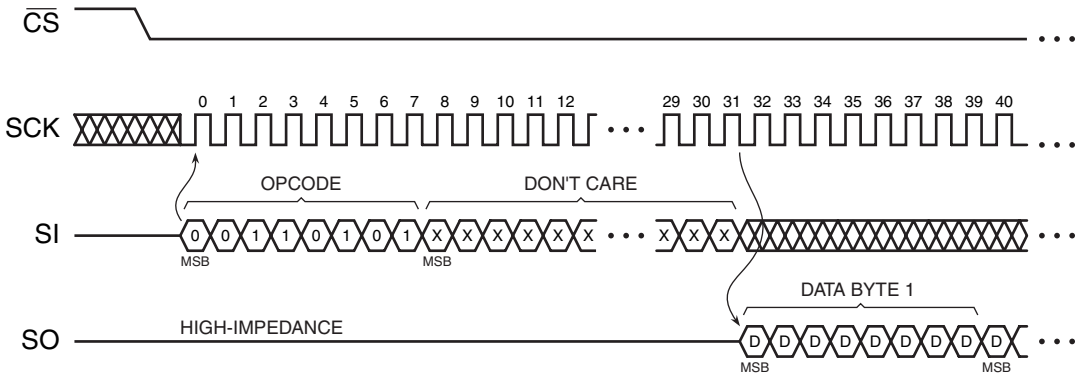
24.6 Buffer Read (Low Frequency: Opcode D1H or D3H)



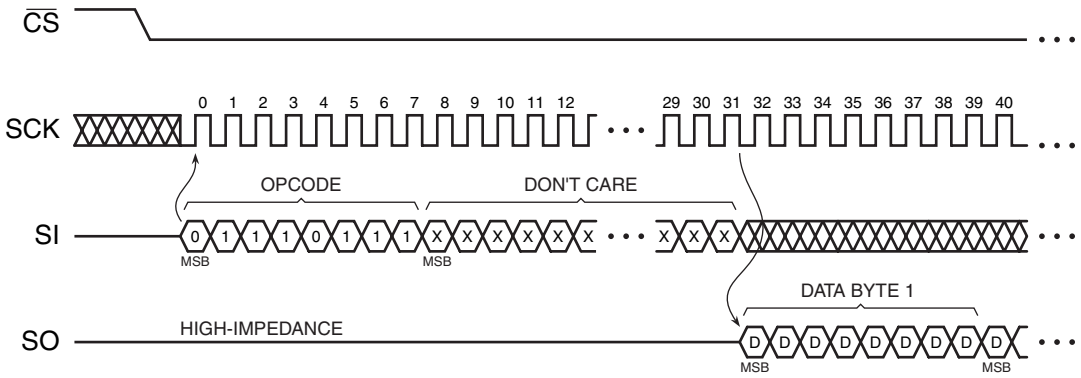
24.7 Read Sector Protection Register (Opcode 32H)



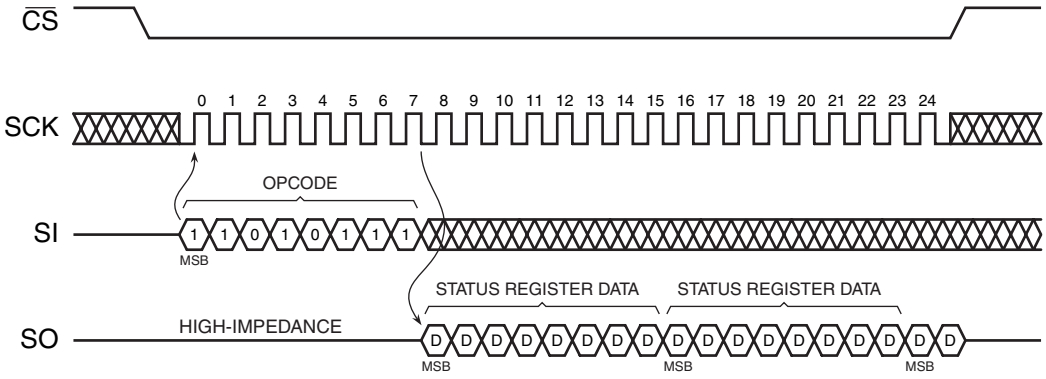
24.8 Read Sector Lockdown Register (Opcode 35H)



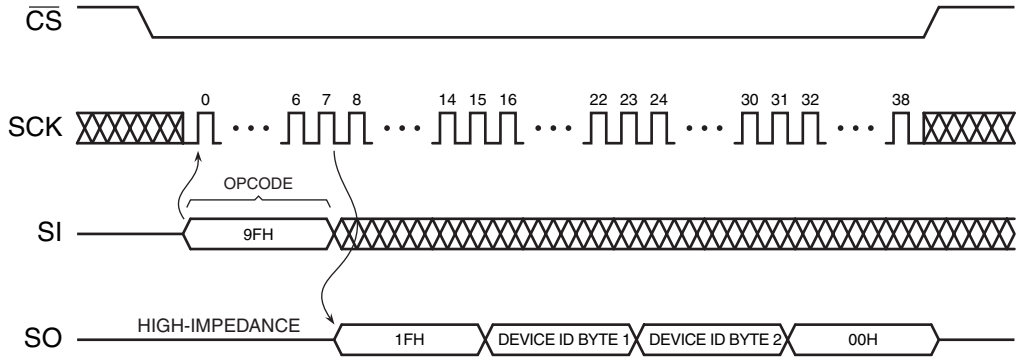
24.9 Read Security Register (Opcode 77H)



24.10 Status Register Read (Opcode D7H)



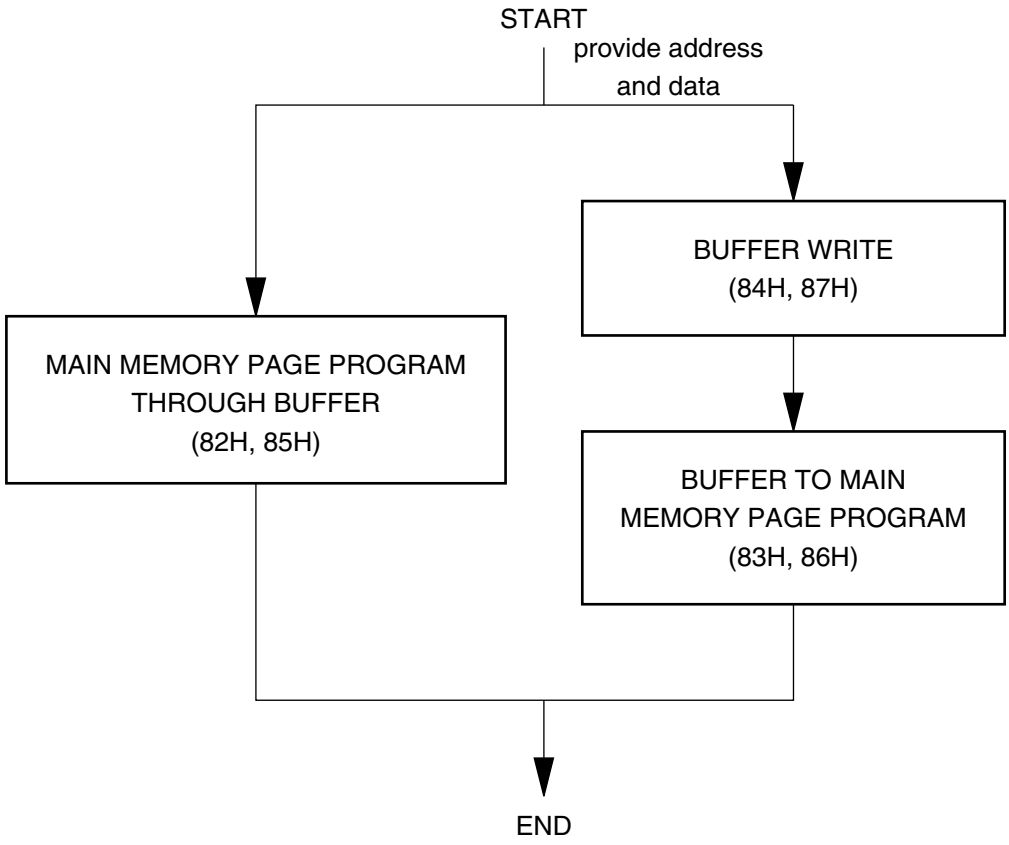
24.11 Manufacturer and Device Read (Opcode 9FH)



Note: Each transition shown for SI and SO represents one byte (8 bits)

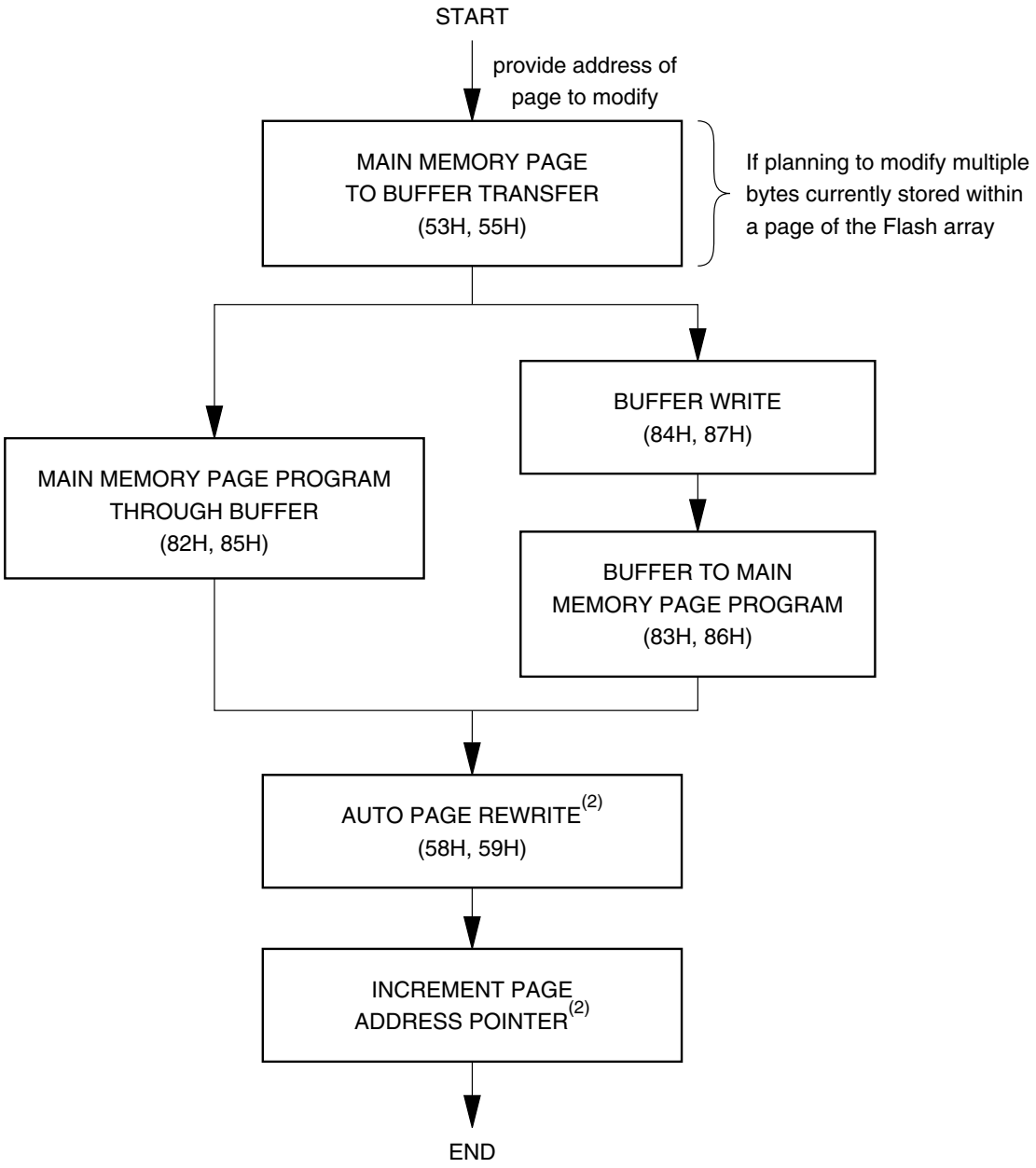
25. Auto Page Rewrite Flowchart

Figure 25-1. Algorithm for Programming or Reprogramming of the Entire Array Sequentially



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array.

Figure 25-2. Algorithm for Randomly Modifying Data



Notes:
1. To preserve data integrity, each page of a DataFlash sector must be updated/rewritten at least once within every 10,000 cumulative page erase and program operations.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low-power applications may choose to wait until 10,000 cumulative page erase and program operations have accumulated before rewriting all pages of the sector. See application note AN-4 (“Using Atmel’s Serial DataFlash”) for more details.

26. Ordering Information

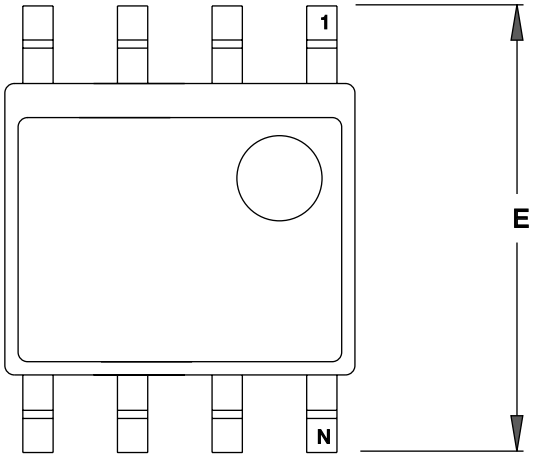
26.1 Green Package Options (Pb/Halide-free/RoHS Compliant)

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
66	15	0.05	AT45DB041D-SSU	8S1	Industrial (-40°C to 85°C)
			AT45DB041D-SU	8S2	
			AT45DB041D-MU	8M1-A	
50	15	0.05	AT45DB041D-SSU-2.5	8S1	
			AT45DB041D-SU-2.5	8S2	
			AT45DB041D-MU-2.5	8M1-A	

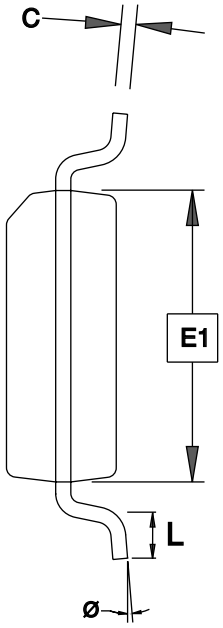
Package Type	
8S1	8-lead, 0.150” Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8S2	8-lead, 0.209” Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)
8M1-A	8-lead, 6 mm x 5 mm Very Thin Micro Lead-frame Package (MLF)

27. Packaging Information

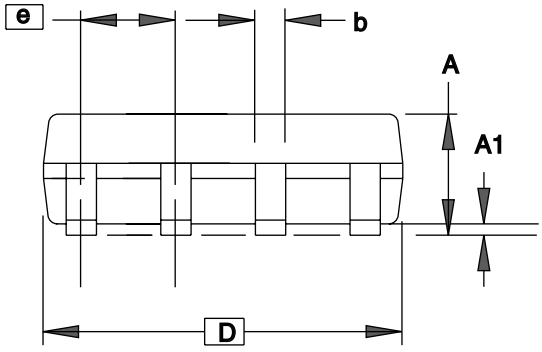
27.1 8S1 – JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

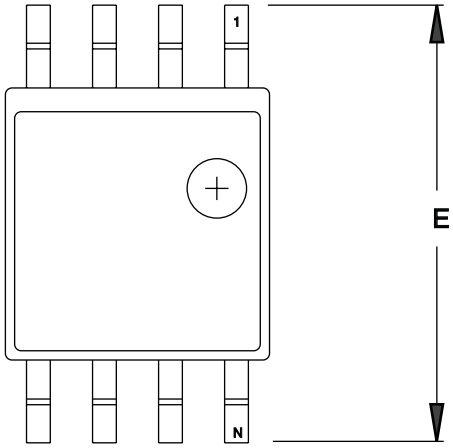
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
θ	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

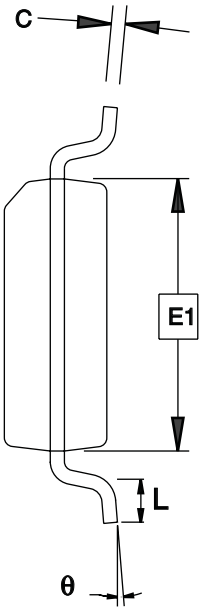
3/17/05

	TITLE	DRAWING NO.	REV.
1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	8S1	C

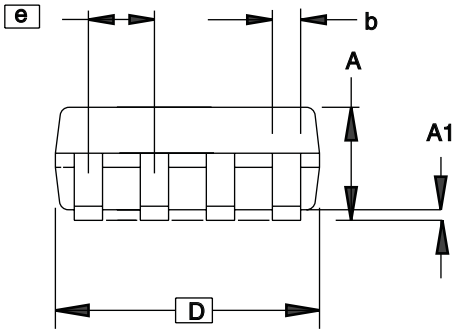
27.2 8S2 – EIAJ SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

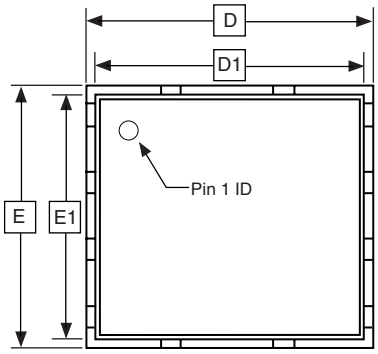
SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	5
C	0.15		0.35	5
D	5.13		5.35	
E1	5.18		5.40	2, 3
E	7.70		8.26	
L	0.51		0.85	
θ	0°		8°	
e	1.27 BSC			4

Notes: 1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs are not included.
3. It is recommended that upper and lower cavities be equal. If they are different, the larger dimension shall be regarded.
4. Determines the true geometric position.
5. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

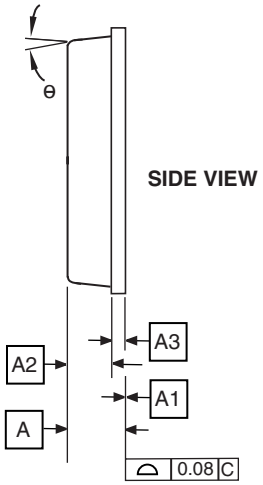
4/7/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8S2**, 8-lead, 0.209" Body, Plastic Small Outline Package (EIAJ)	8S2	D

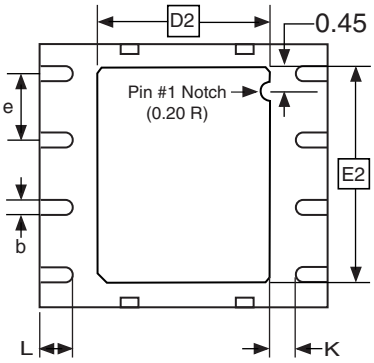
27.3 8M1-A – MLF



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	0.85	1.00	
A1	–	–	0.05	
A2		0.65 TYP		
A3		0.20 TYP		
b	0.35	0.40	0.48	
D	5.90	6.00	6.10	
D1	5.70	5.75	5.80	
D2	3.20	3.40	3.60	
E	4.90	5.00	5.10	
E1	4.70	4.75	4.80	
E2	3.80	4.00	4.20	
e		1.27		
L	0.50	0.60	0.75	
θ	–	–	12°	
K	0.25	–	–	

9/8/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8M1-A,** 8-pad, 6 x 5 x 1.00 mm Body, Very Thin Dual Flat Package No Lead (MLF)	8M1-A	C

28. Revision History

Revision Level – Revision Date	History
A – October 2005	Initial Release
B – March 2006	Added “Preliminary”. Added text, in “Programming the Configuration Register”, to indicate that power cycling is required to switch to “power of 2” page size after the opcode enable has been executed. Added “Legacy Commands” table.
C – June 2006	Corrected typographical errors.
D – July 2006	Corrected typographical errors.
E – August 2006	Added errata regarding Chip Erase.
F – November 2006	Removed “Preliminary”.
G – February 2007	Removed RDY/$\overline{\text{BUSY}}$ pin references.
H – March 2007	Changed page size description from 512 to 256 in Table 15-6. Changed page size description from 528 to 264 in Table 15-7. Added additional text for “power of 2” binary page size option.

29. Errata

29.1 Chip Erase

29.1.1 Issue

In a certain percentage of units, the Chip Erase feature may not function correctly and may adversely affect device operation. Therefore, it is recommended that the Chip Erase commands (opcodes C7H, 94H, 80H, and 9AH) not be used.

29.1.2 Workaround

Use Block Erase (opcode 50H) as an alternative. The Block Erase function is not affected by the Chip Erase issue.

29.1.3 Resolution

The Chip Erase feature may be fixed with a new revision of the device. Please contact Atmel for the estimated availability of devices with the fix.

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