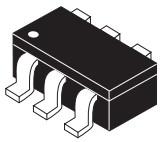
EN: This Datasheet/Document is presented by the manufacturer.

Please visit our website for pricing and availability at www.hestore.hu.

USBLC6-4

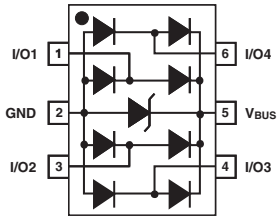
Very low capacitance ESD protection

Datasheet - production data



SOT23-6L

Figure 1. Functional diagram



Features

- 4 data-line protection
- Protects V_{BUS}
- Very low capacitance: 3 pF typ.
- Peak pulse power (8/20 µs): 130 W typ.
- SOT23-6L package
- RoHS compliant

Benefits

- Very low capacitance between lines to GND for optimized data integrity and speed
- Low PCB space consumption, 9 mm² maximum foot print
- Enhanced ESD protection: IEC 61000-4-2 level 4 compliance guaranteed at device level, hence greater immunity at system level
- ESD protection of V_{BUS}: allows ESD current flowing to ground when ESD event occurs on data line
- High reliability offered by monolithic integration
- Low leakage current for longer operation of battery powered devices
- Fast response time
- Consistent D+ / D- signal balance:
  - Best capacitance matching tolerance I/O to GND = 0.015 pF
  - Compliant with USB 2.0 requirements < 1 pF

Complies with the following standards

- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)

Applications

- USB 2.0 ports up to 480 Mb/s (high speed)
- Backwards compatible with USB 1.1 low and full speed
- Ethernet port: 10/100 Mb/s
- SIM card protection
- Video line protection
- Portable electronics

Description

The USBLC6-4 is a monolithic application specific device dedicated to ESD protection of high speed interfaces, such as USB 2.0, Ethernet links and video lines.

Its very low line capacitance secures a high level of signal integrity without compromising in protecting sensitive chips against the most stringent characterized ESD strikes.

This is information on a product in full production. www.st.com

1 Characteristics

Table 1. Absolute ratings

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 air discharge IEC 61000-4-2 contact discharge MIL STD883C-Method 3015-6	15 15 25	kV
T_{stg}	Storage temperature range		-55 to +150	°C
T_j	Operating junction temperature range		-40 to +125	°C
T_L	Lead solder temperature (10 seconds duration)		260	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{RM}	Leakage current	V_{RM} = 5.25 V		10	150	nA
V_{BR}	Breakdown voltage between V_{BUS} and GND	I_R = 1 mA	6		10	V
V_F	Forward voltage	I_F = 10 mA			0.86	V
V_{CL}	Clamping voltage	I_{PP} = 1 A, 8/20 µs Any I/O pin to GND			12	V
		I_{PP} = 5 A, 8/20 µs Any I/O pin to GND			17	V
$C_{i/o-GND}$	Capacitance between I/O and GND	V_R = 1.65 V		3	4	pF
$\Delta C_{i/o-GND}$				0.015		
$C_{i/o-i/o}$	Capacitance between I/O	V_R = 1.65 V		1.85	2.7	pF
$\Delta C_{i/o-i/o}$				0.04		

Figure 2. Capacitance versus voltage (typical values)

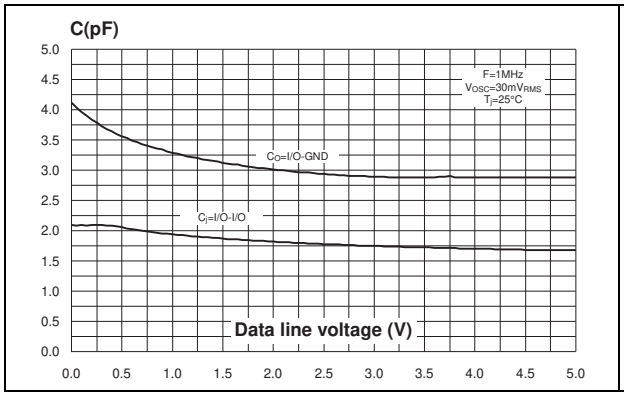


Figure 3. Line capacitance versus frequency (typical values)

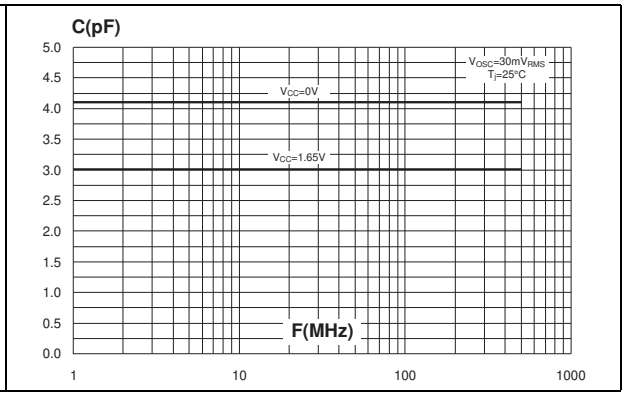


Figure 4. Relative variation of leakage current versus junction temperature (typical values)

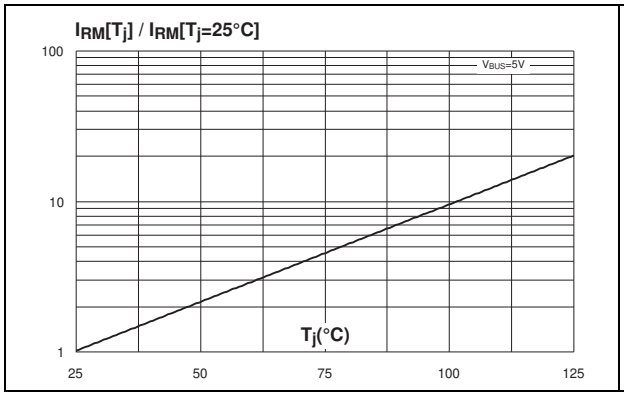
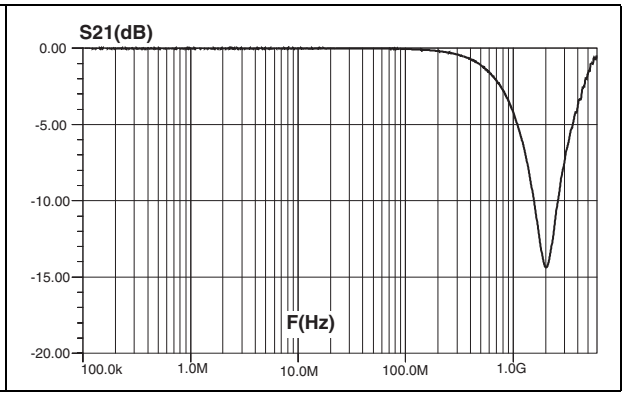


Figure 5. Frequency response



2 Technical information

2.1 Surge protection

The USBLC6-4SC6 is particularly optimized to provide surge protection based on the rail to rail topology.

The clamping voltage V_{CL} can be calculated as follows:

$V_{CL}+ = V_{TRANSIL} + V_F$ for positive surges

$V_{CL}- = - V_F$ for negative surges

with: $V_F = V_T + R_d.I_p$

(V_F forward drop voltage, V_T forward drop threshold voltage

Calculation example

We assume that the value of the dynamic resistance of the clamping diode is typically:

$R_d = 0.5\ \Omega$ and $V_T = 1.1$ V.

For an IEC 61000-4-2 surge level 4 (Contact Discharge: $V_g = 8$ kV, $R_g = 330\ \Omega$), $V_{BUS} = +5$ V, and if in a first approximation, we assume that:

$I_p = V_g / R_g = 24$ A.

So, we find:

$V_{CL}+ = +31.2$ V

$V_{CL}- = -13.1$ V

Note: The calculations do not take into account phenomena due to parasitic inductances.

2.2 Surge protection application example

If we consider that the connections from the pin V_{BUS} to V_{CC}, from I/O to data line and from GND to PCB GND plane are implemented as racks 10 mm long and 0.5 mm large, we can assume that the parasitic inductances L_{VBUS} $L_{I/0}$ and L_{GND} of these tracks are about 6 nH. So, when an IEC 61000-4-2 surge occurs, due to the rise time of this spike ($t_r = 1$ ns), the voltage V_{CL} has an extra value equal to $L_{I/0}$·dI/dt, + L_{GND}·dI/dt

The dI/dt is calculated as:

$dI/dt = I_p/t_r = 24$ A/ns

The overvoltage due to the parasitic inductances is:

$L_{I/0}$·dI/dt, = L_{GND}·dI/dt = 6 x 24 = 144 V

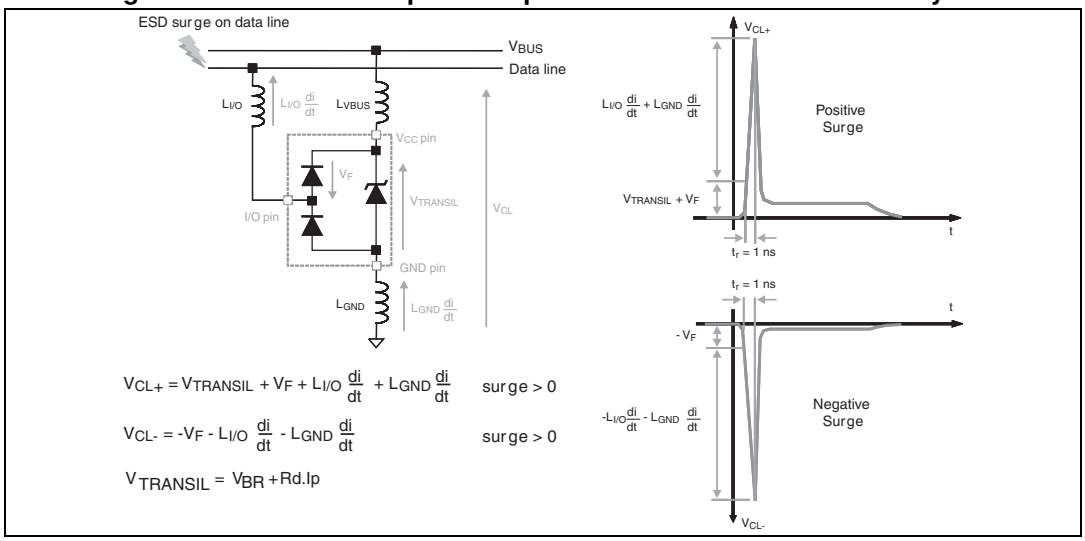
By taking into account the effect of these parasitic inductances due to unsuitable layout, the clamping voltage will be:

$V_{CL}+ = +31.2 + 144 + 144 = 319.2$ V

$V_{CL}- = -13.1 - 144 -144 = -301.1$ V

We can significantly reduce this phenomena with simple layout optimization. It is for this reason that some recommendations have to be followed (see *2.3: How to ensure good ESD protection*).

Figure 6. ESD behavior: parasitic phenomena due to unsuitable layout



2.3 How to ensure good ESD protection

While the USBLC6-4SC6 provides high immunity to ESD surge, efficient protection depends on the layout of the board. In the same way, with the rail to rail topology, the track from data lines to I/O pins, from V_{CC} to the V_{BUS} pin and from GND plane to GND pin must be as short as possible to avoid overvoltages due to parasitic phenomena (see *Figure 7* and *Figure 8* for layout considerations)

Figure 7. ESD behavior: optimized layout and addition of a capacitance of 100 nF

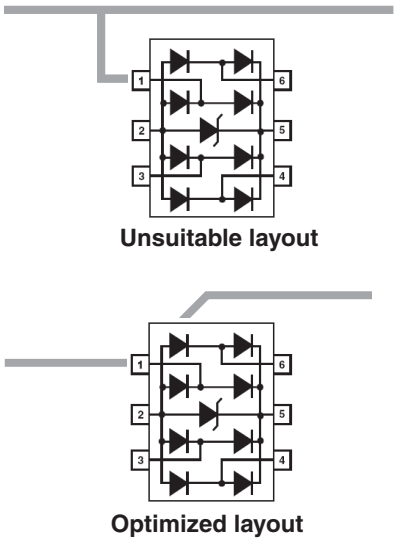


Figure 8. ESD behavior: measurement conditions (with coupling capacitance)

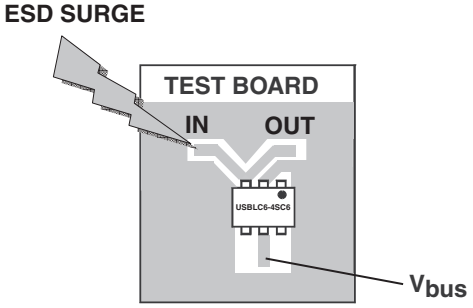


Figure 9. Remaining voltage after the USBLC6-4SC6 during positive ESD surge

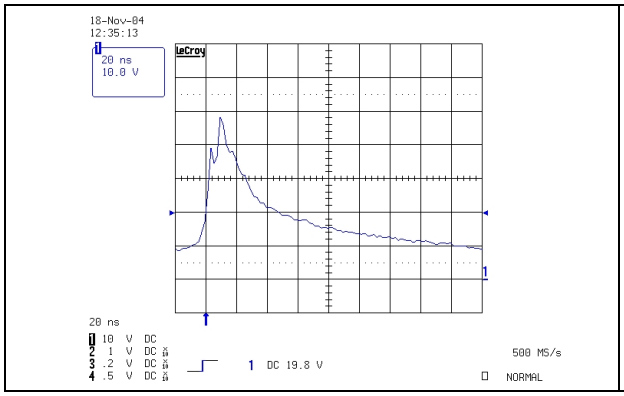
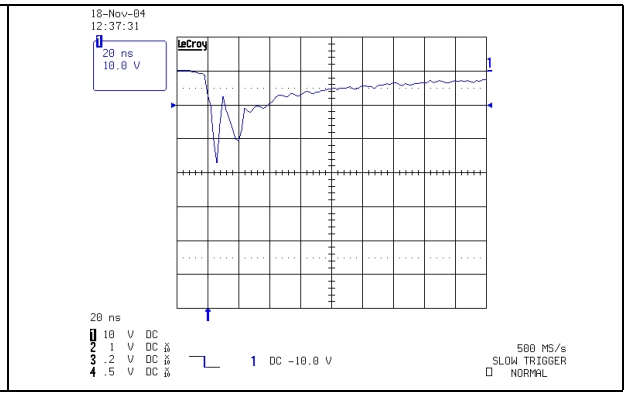


Figure 10. Remaining voltage after the USBLC6-4SC6 during negative ESD surge



Note: The measurements have been done with the USBLC6-4SC6 in open circuit.

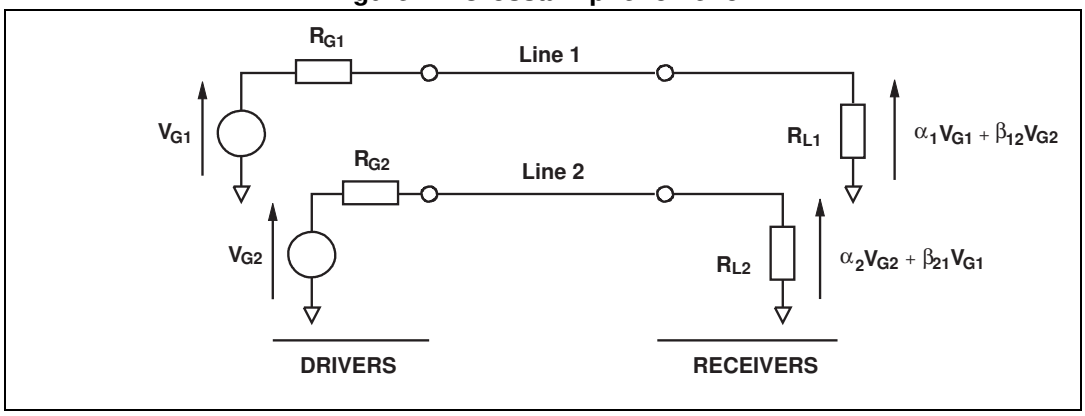
Important:

A good precaution to take is to put the protection device as close as possible to the disturbance source (generally the connector).

2.4 Crosstalk behavior

2.4.1 Crosstalk phenomenon

Figure 11. Crosstalk phenomenon



The crosstalk phenomenon is due to the coupling between 2 lines. The coupling factor ($\beta 12$ or $\beta 21$) increases when the gap across lines decreases, particularly in silicon dice. In the above example the expected signal on load R_{L2} is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21} V_{G1}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ).

Figure 12. Analog crosstalk measurements

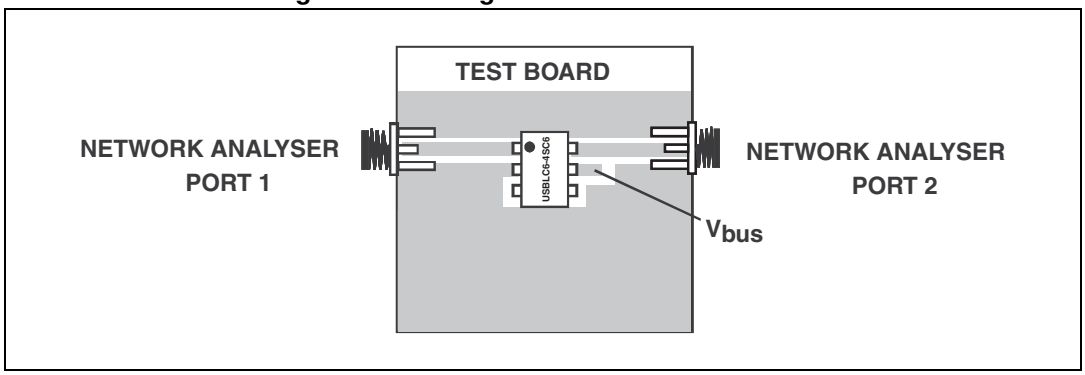
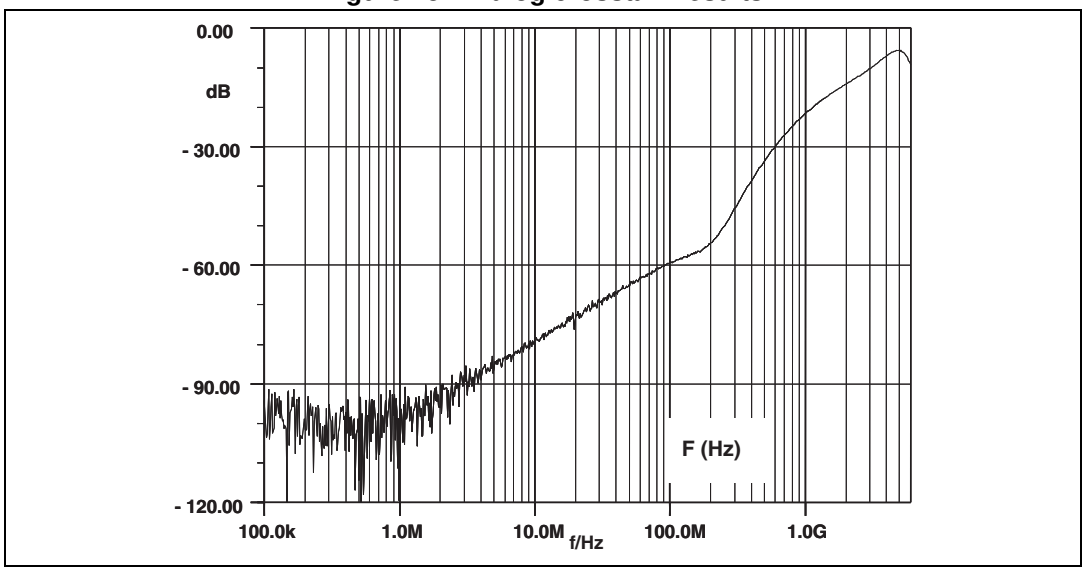


Figure 12. shows the measurement circuit for the analog application. In usual frequency range of analog signals (up to 240 MHz) the effect on disturbed line is less than -55 dB (see *Figure 13.*).

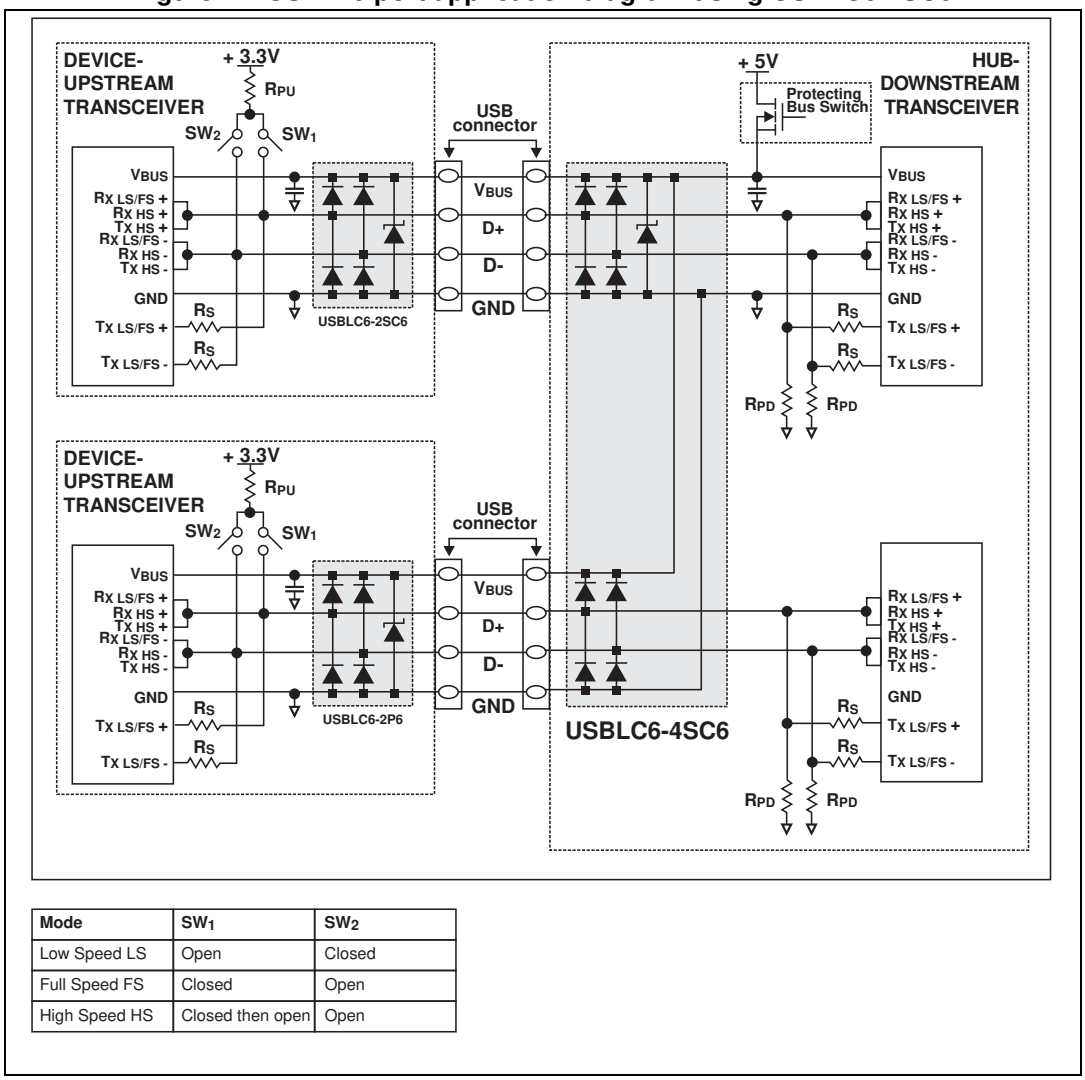
Figure 13. Analog crosstalk results



As the USBLC6-4SC6 is designed to protect high speed data lines, it must ensure a good transmission of operating signals. The frequency response (*Figure 5.*) gives attenuation information and shows that the USBLC6-4SC6 is well suitable for data line transmission up to 480 Mbit/s while it works as a filter for undesirable signals like GSM (900 MHz) frequencies, for instance.

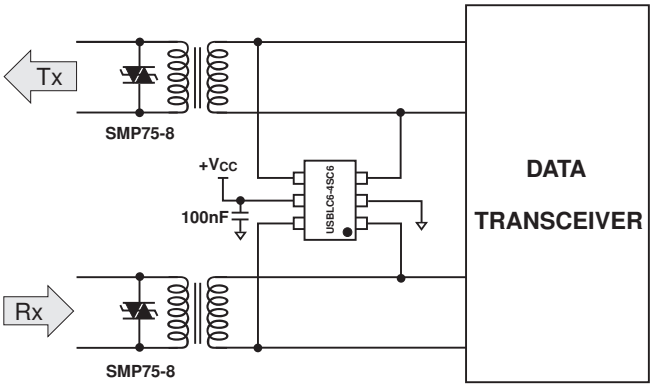
2.5 Application examples

Figure 14. USB 2.0 port application diagram using USBLC6-4SC6



Mode	SW_1	SW_2
Low Speed LS	Open	Closed
Full Speed FS	Closed	Open
High Speed HS	Closed then open	Open

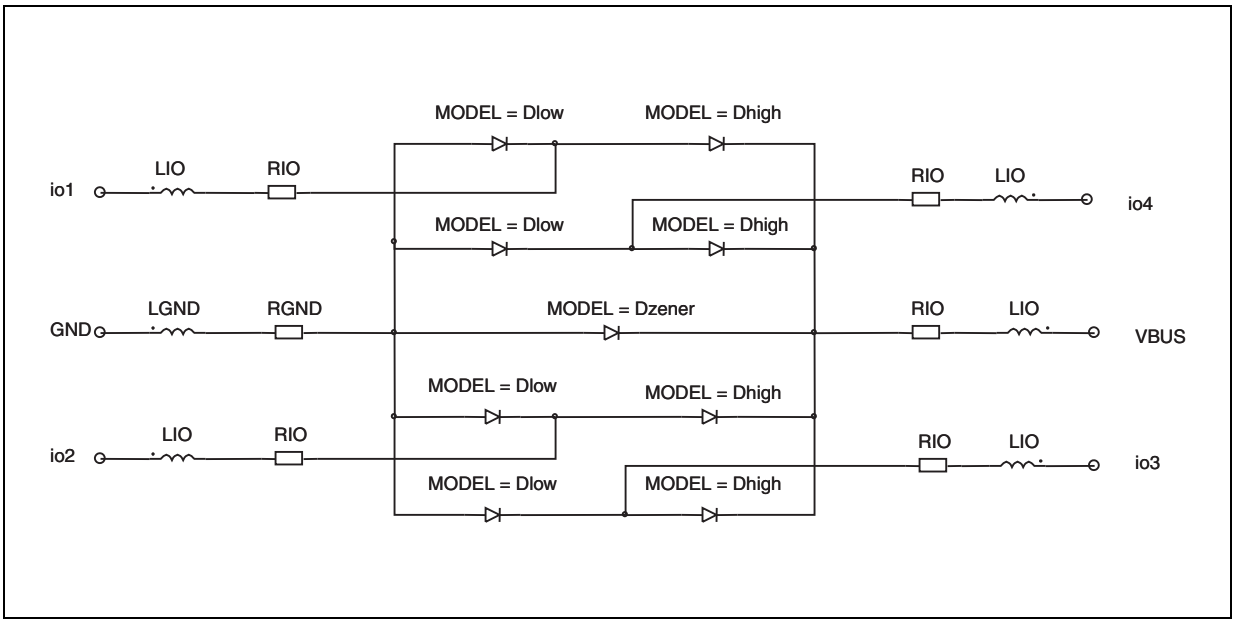
Figure 15. T1/E1/Ethernet protection



2.6 PSPICE model

Figure 16. shows the PSPICE model of one USBLC6-4SC6 cell. In this model, the diodes are defined by the PSPICE parameters given in *Figure 17.*

Figure 16. PSPICE model



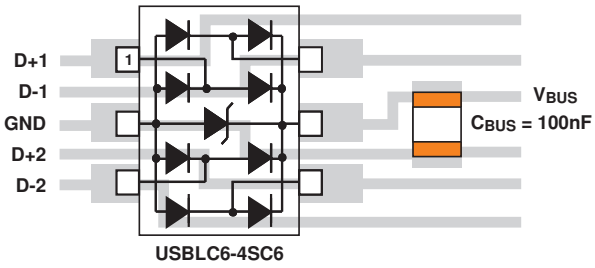
Note: This simulation model is available only for an ambient temperature of 27 °C.

Figure 17. PSPICE parameters

	Dlow	Dhigh	Dzener
BV	50	50	7.3
CJ0	2.4p	2.4p	20p
IBV	1m	1m	1m
IKF	0.038	0.018	2.42
IS	55.2p	2.27f	3.21p
ISR	100p	100p	100p
N	1.62	1.13	1.24
M	0.3333	0.3333	0.3333
RS	0.38	0.63	0.42
VJ	0.6	0.6	0.6
TT	0.1u	0.1u	0.1u

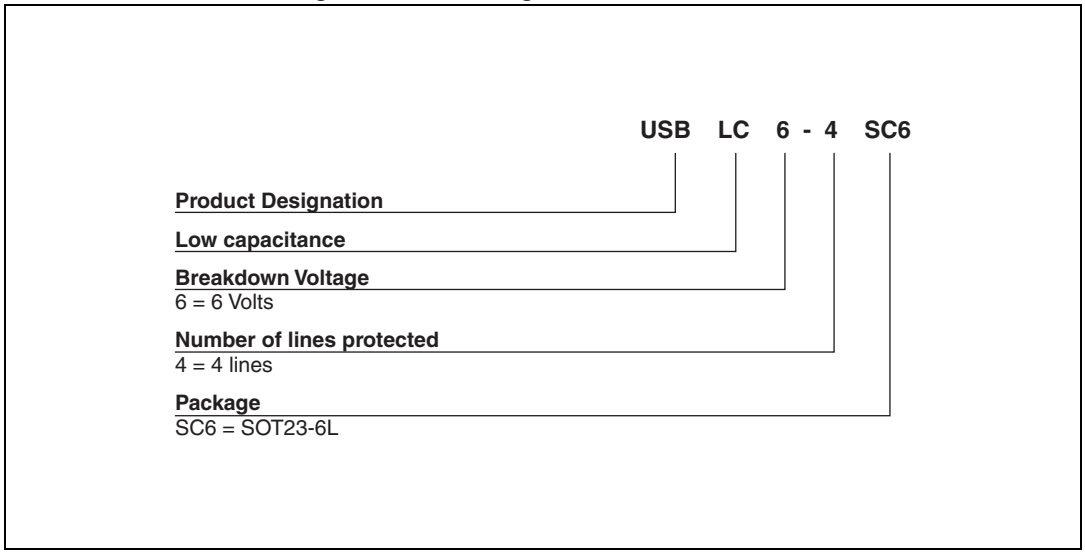
LIO	710p
RIO	100m
LGND	430p
RGND	50m

Figure 18. USBLC6-4SC6 PCB layout considerations



3 Ordering information scheme

Figure 19. Ordering information scheme

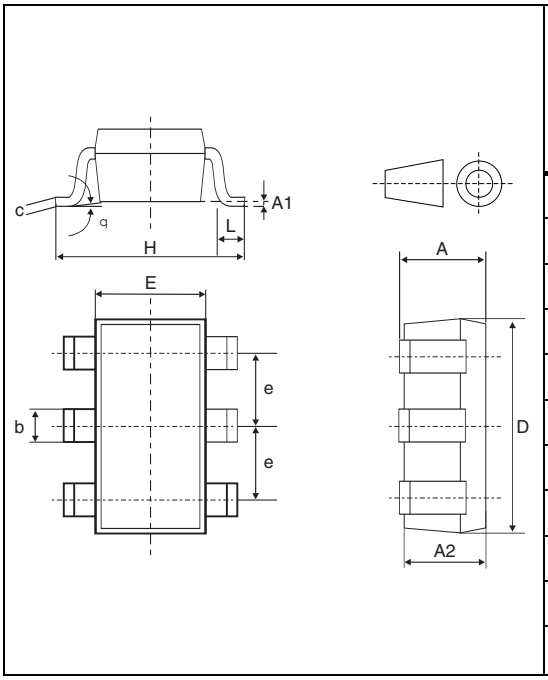


4 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 3. SOT23-6L package dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1	0		0.10	0		0.004
A2	0.90		1.30	0.035		0.051
b	0.35		0.50	0.014		0.02
C	0.09		0.20	0.004		0.008
D	2.80		3.05	0.110		0.120
E	1.50		1.75	0.059		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.10		0.60	0.004		0.024
θ	0°		10°	0°		10°

Figure 20. SOT23-6L footprint (mm)

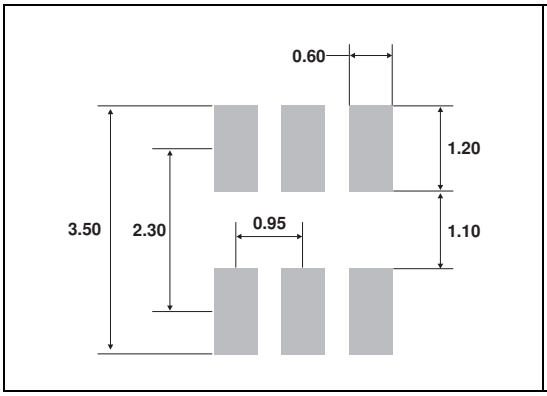
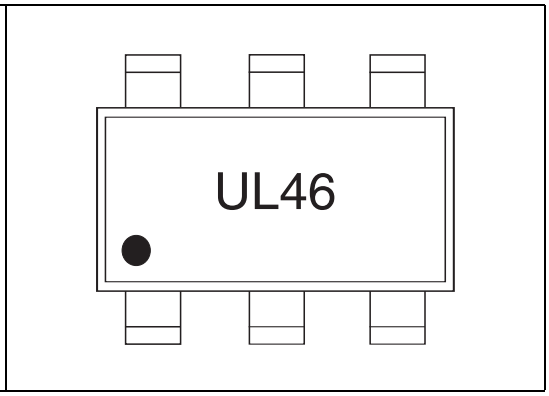


Figure 21. SOT23-6L marking



5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
USBLC6-4SC6	UL46	SOT23-6L	16.7 mg	3000	Tape and reel

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
10-Dec-2004	1	First issue.
28-Feb-2005	2	Minor layout update. No content change.
04-Feb-2008	3	Updated operating junction temperature range in absolute ratings, page 2. Updated Section 2: Technical information. Updated marking illustration Figure 21. Reformatted to current standard.
23-Sep-2011	4	Updated leakage current at V_{RM} = 5.25 V as specified in USB standard. Updated marking illustration Figure 21.
13-Oct-2015	5	Updated features in cover page and *Table 2*.
26-Oct-2015	6	Updated features in cover page.
03-Nov-2015	7	Minor text changes.

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