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74HC4046A; 74HCT4046A

Phase-locked loop with VCO

Rev. 3 — 8 June 2016 Product data sheet

1. General description

The 74HC4046A; 74HCT4046A is a high-speed Si-gate CMOS device. It is specified in compliance with JEDEC standard no 7A.

2. Features and benefits

- Low power consumption
- VCO-Inhibit control for ON/OFF keying and for low standby power consumption
- Center frequency up to 17 MHz (typical) at V_{CC} = 4.5 V
- Choice of three phase comparators:
  - PC1: EXCLUSIVE-OR
  - PC2: Edge-triggered J-K flip-flop
  - PC3: Edge-triggered RS flip-flop
- Excellent Voltage Controlled Oscillator (VCO) linearity
- Low frequency drift with supply voltage and temperature variations
- Operating power supply voltage range:
  - VCO section 3.0 V to 6.0 V
  - Digital section 2.0 V to 6.0 V
- Zero voltage offset due to operational amplifier buffering
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

3. Applications

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control

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4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
74HC4046AD	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4046AD			
74HC4046ADB	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT4046ADB			
74HC4046APW	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Block diagram

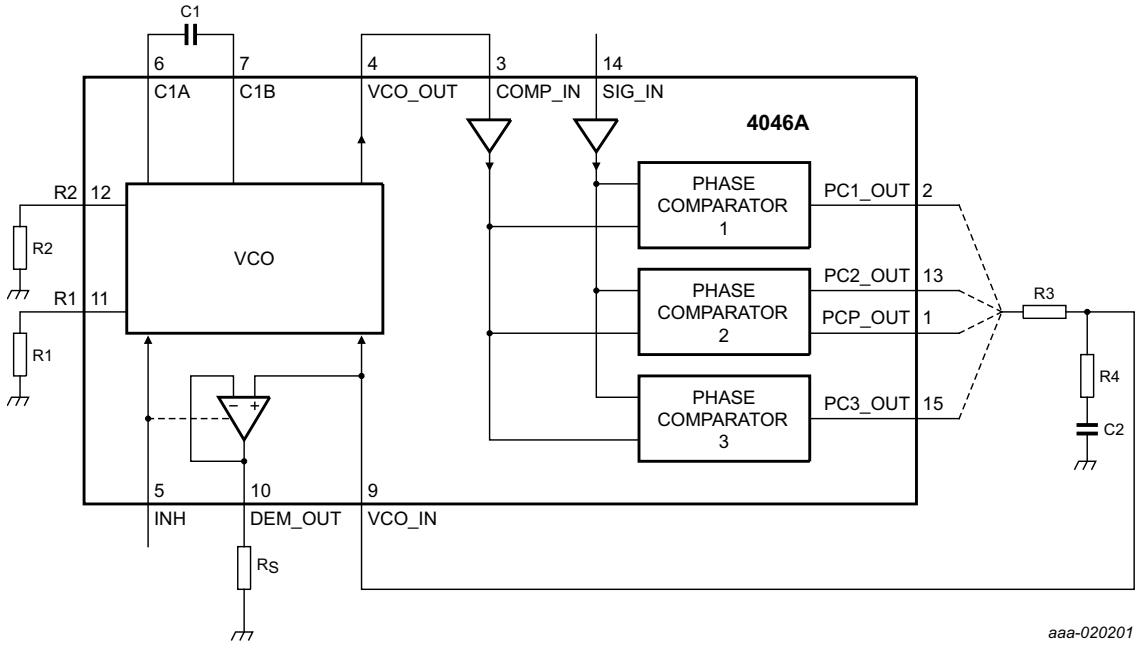

Fig 1. Block diagram

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6. Functional diagram

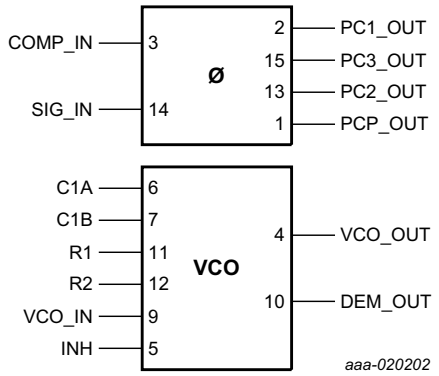

Fig 2. Logic symbol

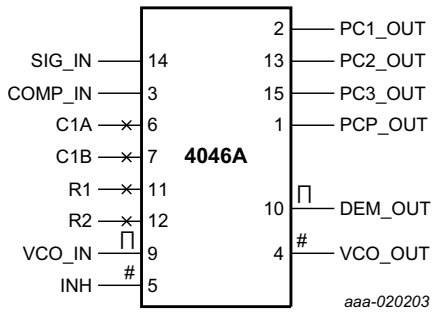

Fig 3. IEC logic symbol

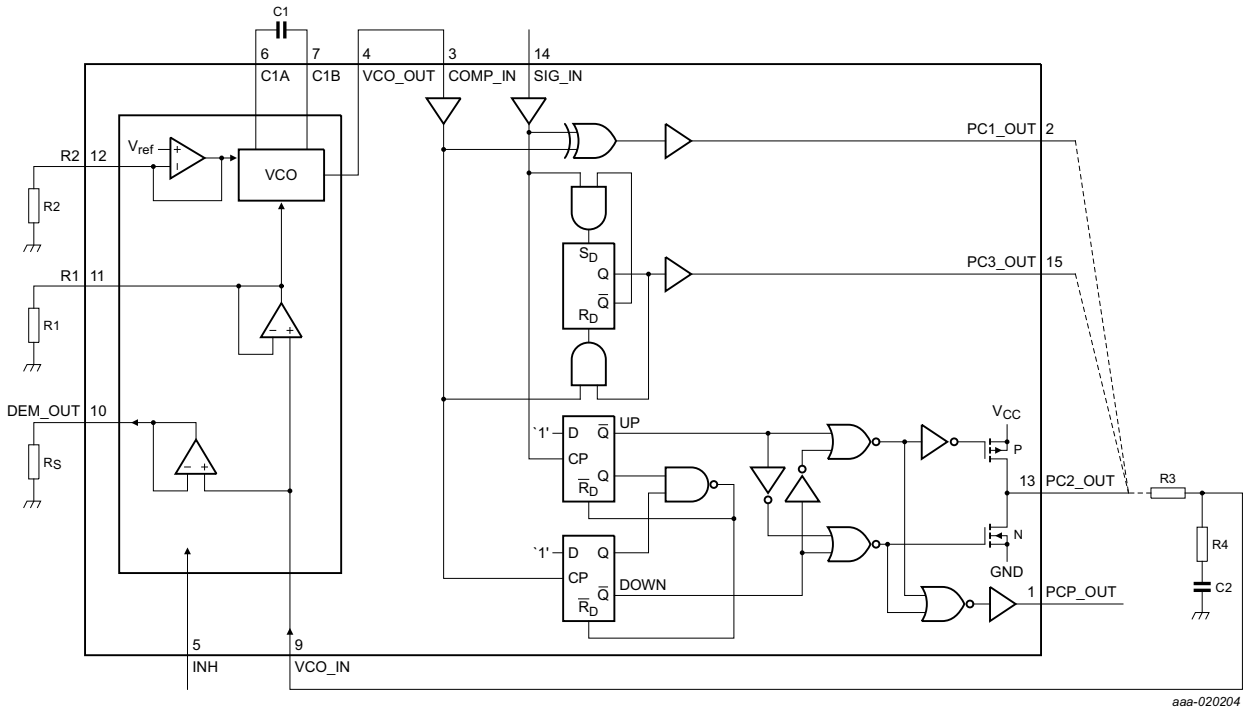

Fig 4. Logic diagram

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7. Pinning information

7.1 Pinning

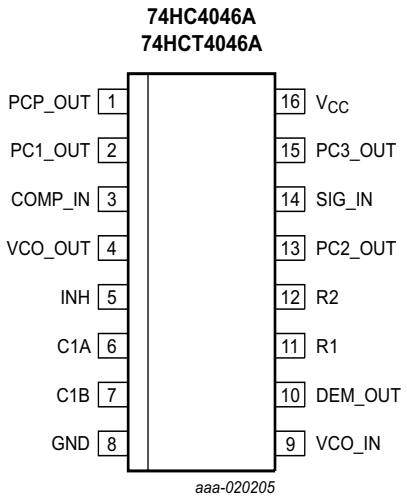

Fig 5. Pin configuration

7.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
PCP_OUT	1	phase comparator pulse output
PC1_OUT	2	phase comparator 1 output
COMP_IN	3	comparator input
VCO_OUT	4	VCO output
INH	5	inhibit input
C1A	6	capacitor C1 connection A
C1B	7	capacitor C1 connection B
GND	8	ground (0 V)
VCO_IN	9	VCO input
DEM_OUT	10	demodulator output
R1	11	resistor R1 connection
R2	12	resistor R2 connection
PC2_OUT	13	phase comparator 2 output
SIG_IN	14	signal input
PC3_OUT	15	phase comparator 3 output
V_{CC}	16	supply voltage

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8. Functional description

The 74HC4046A; 74HCT4046A is a phase-locked-loop circuit that comprises a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2 and PC3). It has a common signal input amplifier and a common comparator input (see Figure 1). The signal input can be directly coupled to a large voltage signal, or indirectly coupled (with a series capacitor) to a small voltage signal. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the 74HC4046A; 74HCT4046A forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op amp techniques.

8.1 VCO

The VCO requires one external capacitor C1 (between pins C1A and C1B) and one external resistor R1 (between pins R1 and GND). Alternatively, it requires two external resistors R1 and R2 (between pins R1 and GND, and R2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if necessary (see Figure 4).

The high input impedance of the VCO simplifies the design of the low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin DEM_OUT. In contrast to conventional techniques, where the DEM_OUT voltage is one threshold voltage lower than the VCO input voltage, the DEM_OUT voltage equals the VCO input. If DEM_OUT is used, a series resistor (R_s) should be connected from pin DEM_OUT to GND; if unused, DEM_OUT should be left open. The VCO output (pin VCO_OUT) can be connected directly to the comparator input (pin COMP_IN), or connected via a frequency divider. When the VCO input DC level is held constant, the VCO output signal has a duty cycle of 50 % (maximum expected deviation 1 %). A LOW-level at the inhibit input (pin INH) enables the VCO and demodulator, while a HIGH-level turns both off to minimize standby power consumption.

The only difference between the 74HC4046A and 74HCT4046A is the input level specification of the INH input. This input disables the VCO section. The sections of the comparator are identical, so that there is no difference in the SIG_IN or COMP_IN inputs between the 74HC4046A and 74HCT4046A.

8.2 Phase comparators

The input signal can be coupled to the self-biasing amplifier at pin SIG_IN, when the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

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8.2.1 Phase Comparator 1 (PC1)

This circuit is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f_i) must have a 50 % duty cycle to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is:

$$V_{DEM_OUT} = \frac{V_{CC}}{\pi}(\Phi_{SIG_IN} - \Phi_{COMP_IN})$$

where:

V_{DEM_OUT} is the demodulator output at pin DEM_OUT

$V_{DEM_OUT} = V_{PC1_OUT}$ (via low-pass filter)

The phase comparator gain is: $K_p = \frac{V_{CC}}{\pi}(V/r)$

PC1 is fed to the VCO input via the low-pass filter and seen at the demodulator output at pin DEM_OUT (V_{DEM_OUT}). The average output voltage from PC1 is the result of the phase differences of signals (SIG_IN) and the comparator input (COMP_IN). These phase differences are shown in Figure 6. The average of V_{DEM_OUT} is equal to $0.5V_{CC}$ when there is no signal or noise at SIG_IN. Using this input, the VCO oscillates at the center frequency (f_0). Typical waveforms for the PC1 loop locked at f_0 are shown in Figure 7.

The frequency capture range ($2f_c$) is defined as the frequency range of input signals on which the PLL locks when it was initially out-of-lock. The frequency lock range ($2f_L$) is the frequency range of the input signals on which the loop stays locked when it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration remains locked even with very noisy input signals. Typical behavior of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO center frequency.

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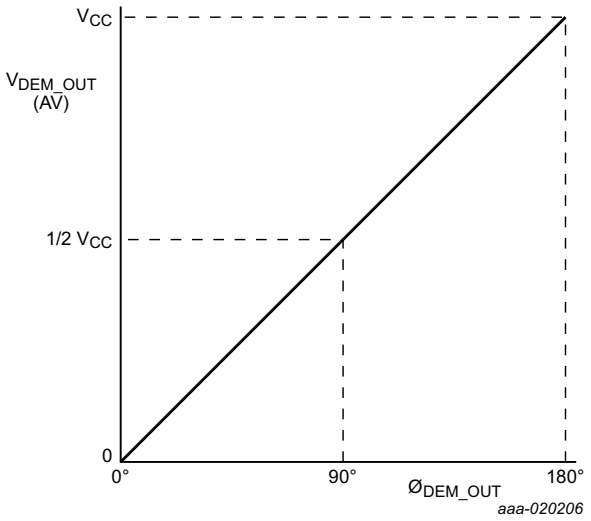

$$V_{DEM_OUT} = V_{PC1_OUT} = \frac{V_{CC}}{\pi}(\Phi_{SIG_IN} - \Phi_{COMP_IN})$$

$$\Phi_{DEM_OUT} = (\Phi_{SIG_IN} - \Phi_{COMP_IN})$$

Fig 6. Phase comparator 1; average output voltage as a function of input phase difference

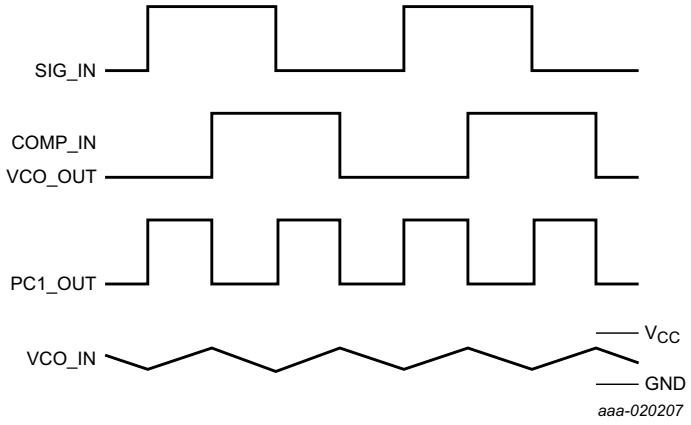

Fig 7. Typical waveforms for PLL using phase comparator 1; loop-locked at f_0

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8.2.2 Phase Comparator 2 (PC2)

PC2 is a positive edge-triggered phase and frequency detector. When the PLL uses this comparator, positive signal transitions control the loop and the duty cycles of SIG_IN and COMP_IN are not important. PC2 comprises two D-type flip-flops, control gating and a 3-state output stage. The circuit functions as an up-down counter (see Figure 4) where SIG_IN causes an up-count and COMP_IN a down count. The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed, is:

$$V_{DEM_OUT} = \frac{V_{CC}}{4\pi}(\Phi_{SIG_IN} - \Phi_{COMP_IN})$$

where:

V_{DEM_OUT} is the demodulator output at pin DEM_OUT

$V_{DEM_OUT} = V_{PC2_OUT}$ (via low-pass filter)

The phase comparator gain is: $K_p = \frac{V_{CC}}{4\pi}(V/r)$

V_{DEM_OUT} is the resultant of the initial phase differences of SIG_IN and COMP_IN as shown in Figure 8. Typical waveforms for the PC2 loop locked at f_o are shown in Figure 9.

When the SIG_IN and COMP_IN frequencies are equal but the phase of SIG_IN leads that of COMP_IN, the p-type output driver at PC2_OUT is held 'ON'. The time that it is held ÓN' corresponds to the phase difference (Φ_{DEM_OUT}). When the phase of SIG_IN lags that of COMP_IN, the n-type driver is held 'ON'.

When the SIG_IN frequency is higher than the COMP_IN frequency, the p-type output driver is held 'ON' for most of the input signal cycle time. For the remainder of the cycle time, both n- and p-type drivers are 'OFF' (3-state). If the SIG_IN frequency is lower than the COMP_IN frequency, then it is the n-type driver that is held 'ON' for most of the cycle. The voltage at capacitor (C2) of the low-pass filter, connected to PC2_OUT, varies until the phase and frequency of the signal and comparator inputs are equal. At this stable point, the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO_IN input is in a high-impedance state. In this condition, the signal at the phase comparator pulse output (PCP_OUT) is a HIGH level and can be used for indicating a locked condition.

Thus for PC2 no phase difference exists between SIG_IN and COMP_IN over the full frequency range of the VCO. The power dissipation due to the low-pass filter is reduced because both n- and p-type output drivers are 'OFF' for most of the signal input cycle. The PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_IN the VCO adjust, via PC2, to its lowest frequency.

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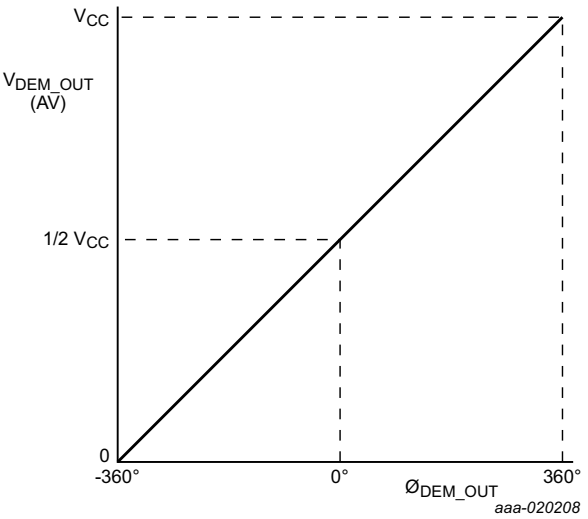

$$V_{DEM_OUT} = V_{PC2_OUT} = \frac{V_{CC}}{\pi}(\Phi_{SIG_IN} - \Phi_{COMP_IN})$$

$$\Phi_{DEM_OUT} = (\Phi_{SIG_IN} - \Phi_{COMP_IN})$$

Fig 8. Phase comparator 2; average output voltage as a function of input phase difference

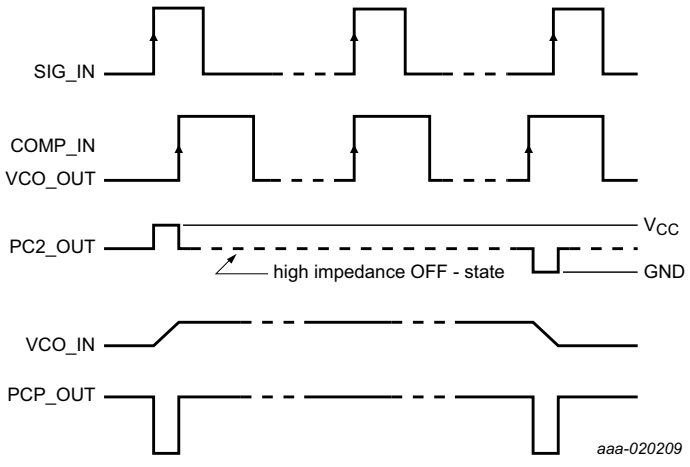

Fig 9. Typical waveforms for PLL using phase comparator 2; loop-locked at f_0

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8.2.3 Phase Comparator 3 (PC3)

PC3 is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, positive signal transitions control the loop and the duty factors of SIG_IN and COMP_IN are not important. The transfer characteristic of PC3, assuming ripple ($f_r = f_i$) is suppressed, is:

$$V_{DEM_OUT} = \frac{V_{CC}}{2\pi}(\Phi_{SIG_IN} - \Phi_{COMP_IN})$$

where:

V_{DEM_OUT} is the demodulator output at pin DEM_OUT

$V_{DEM_OUT} = V_{PC3_OUT}$ (via low-pass filter)

The phase comparator gain is: $K_p = \frac{V_{CC}}{2\pi}(V/r)$

PC3 is fed to the VCO via the low-pass filter and seen at the demodulator output at pin DEM_OUT. The average output from PC3 is the resultant of the phase differences of SIG_IN and COMP_IN, see Figure 10. Typical waveforms for the PC3 loop locked at f_o are shown in Figure 11.

The phase-to-output response characteristic of PC3 (Figure 10) differs from PC2 in that the phase angle between SIG_IN and COMP_IN varies between 0° and 360°. It is 180° at the center frequency. Also PC3 gives a greater voltage swing than PC2 for input phase differences. As a result, the ripple content of the VCO input signal is higher. The PLL lock range for this type of phase comparator and the capture range are dependent on the low-pass filter. With no signal present at SIG_IN, the VCO adjusts to its lowest frequency via PC3.

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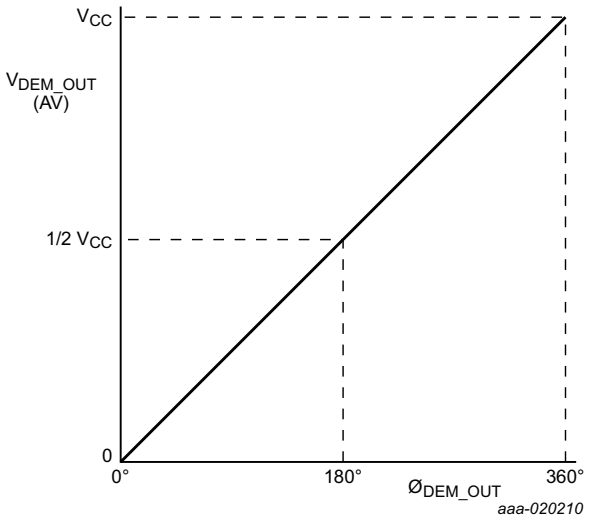

$$V_{DEM_OUT} = V_{PC3_OUT} = \frac{V_{CC}}{\pi}(\Phi_{SIG_IN} - \Phi_{COMP_IN})$$

$$\Phi_{DEM_OUT} = (\Phi_{SIG_IN} - \Phi_{COMP_IN})$$

Fig 10. Phase comparator 3; average output voltage as a function of input phase difference

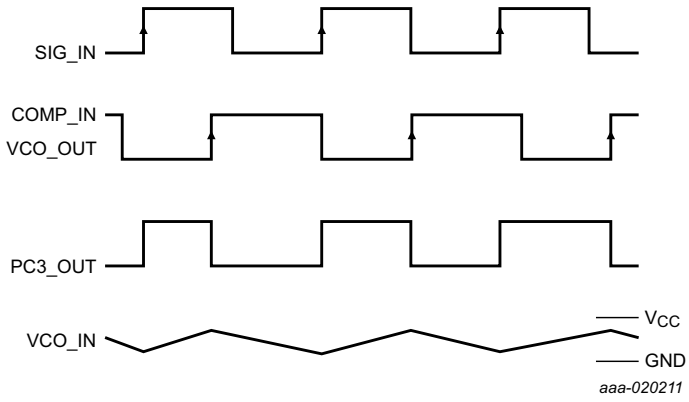

Fig 11. Typical waveforms for PLL using phase comparator 3; loop-locked at f_0

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9. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		−50	-	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C			
		SO16 and (T)SSOP16 [1]	-	500	mW

[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

10. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4046A			74HCT4046A			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		3.0	5.0	6.0	4.5	5.0	5.5	V
		when VCO is not used	2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	pin INH							
		V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V
T_{amb}	ambient temperature		−40	+25	+125	−40	+25	+125	°C

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11. Static characteristics

11.1 Static characteristics 74HC4046A

Table 5. Static characteristics 74HC4046A

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Phase comparator section; T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	pins SIG_IN, COMP_IN; DC coupled				
		V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	pins SIG_IN, COMP_IN; DC coupled				
		V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	pins PCP_OUT, PCn_OUT; V_I = V_{IH} or V_{IL}				
		I_O = −20 μA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = −4 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	pins PCP_OUT, PCn_OUT; V_I = V_{IH} or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_I	input leakage current	pins SIG_IN, COMP_IN; V_I = V_{CC} or GND				
		V_{CC} = 2.0 V	-	-	±3	μA
		V_{CC} = 3.0 V	-	-	±7	μA
		V_{CC} = 4.5 V	-	-	±18	μA
		V_{CC} = 6.0 V	-	-	±30	μA
I_{OZ}	OFF-state output current	pin PC2_OUT; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND				
		V_{CC} = 6.0 V	-	-	±0.5	μA
R_I	input resistance	pins SIG_IN, COMP_IN; V_I at self-bias operating point; ΔV_I = 0.5 V; see Figure 12, 13 and 14				
		V_{CC} = 3.0 V	-	800	-	kΩ
		V_{CC} = 4.5 V	-	250	-	kΩ
		V_{CC} = 6.0 V	-	150	-	kΩ

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Table 5. Static characteristics 74HC4046A

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCO section; T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	pin INH				
		V_{CC} = 3.0 V	2.1	1.7	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	pin INH				
		V_{CC} = 3.0 V	-	1.3	0.9	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	pin VCO_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = −20 μA; V_{CC} = 3.0 V	2.9	3.0	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = −4 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	pin VCO_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 3.0 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
		pins C1A, C1B; $V_I = V_{IH}$ or V_{IL}				
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.40	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.40	V
I_I	input leakage current	pins INH, VCO_IN; $V_I = V_{CC}$ or GND				
		V_{CC} = 6.0 V	-	-	±0.1	μA
R1	resistor 1	V_{CC} = 3.0 V to 6.0 V [1]	3	-	300	kΩ
R2	resistor 2	V_{CC} = 3.0 V to 6.0 V [1]	3	-	300	kΩ
C1	capacitor 1	V_{CC} = 3.0 V to 6.0 V	40	-	no limit	pF
V_{VCO_IN}	voltage on pin VCO_IN	over the range specified for R1; for linearity see Figure 22 and 23				
		V_{CC} = 3.0 V	1.1	-	1.9	V
		V_{CC} = 4.5 V	1.1	-	3.4	V
		V_{CC} = 6.0 V	1.1	-	4.9	V

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Table 5. Static characteristics 74HC4046A

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Demodulator section; T_{amb} = 25 °C						
R_s	series resistance	at R_s > 300 kΩ, the leakage current can influence V_{DEM_OUT}				
		V_{CC} = 3.0 V to 6.0 V	50	-	300	kΩ
V_{offset}	offset voltage	VCO_IN to V_{DEM_OUT}; $V_I = V_{VCO_IN} = 0.5V_{CC}$; values taken over R_s range; see Figure 15				
		V_{CC} = 3.0 V	-	±30	-	mV
		V_{CC} = 4.5 V	-	±20	-	mV
		V_{CC} = 6.0 V	-	±10	-	mV
R_{dyn}	dynamic resistance	DEM_OUT; $V_{DEM_OUT} = 0.5V_{CC}$				
		V_{CC} = 3.0 V to 6.0 V	-	25	-	Ω
General; T_{amb} = 25 °C						
I_{CC}	supply current	VCO disabled; pins COMP_IN, INH and SIG_IN at V_{CC}; pin VCO_IN at GND; I_I at pins COMP_IN and SIGN_IN to be excluded				
		V_{CC} = 6.0 V	-	-	8.0	µA
C_I	input capacitance	pin INH	-	3.5	-	pF
Phase comparator section; T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	pins SIG_IN, COMP_IN; DC coupled				
		V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	pins SIG_IN, COMP_IN; DC coupled				
		V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	pins PCP_OUT, PCn_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V
V_{OL}	LOW-level output voltage	pins PCP_OUT, PCn_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V

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Table 5. Static characteristics 74HC4046A

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	input leakage current	pins SIG_IN, COMP_IN; $V_I = V_{CC}$ or GND				
		V_{CC} = 2.0 V	-	-	±4	μA
		V_{CC} = 3.0 V	-	-	±9	μA
		V_{CC} = 4.5 V	-	-	±23	μA
		V_{CC} = 6.0 V	-	-	±38	μA
I_{OZ}	OFF-state output current	pin PC2_OUT; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND				
		V_{CC} = 6.0 V	-	-	±5	μA
VCO section; T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	pin INH				
		V_{CC} = 3.0 V	2.1	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	pin INH				
		V_{CC} = 3.0 V	-	-	0.9	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	pin VCO_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = –20 μA; V_{CC} = 3.0 V	2.9	-	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V
V_{OL}	LOW-level output voltage	pin VCO_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 3.0 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
		pins C1A, C1B; $V_I = V_{IH}$ or V_{IL}				
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.47	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.47	V
I_I	input leakage current	pins INH, VCO_IN; $V_I = V_{CC}$ or GND				
		V_{CC} = 6.0 V	-	-	±1	μA
General; T_{amb} = –40 °C to +85 °C						
I_{CC}	supply current	VCO disabled; pins COMP_IN, INH and SIG_IN at V_{CC}; pin VCO_IN at GND; I_I at pins COMP_IN and SIGN_IN to be excluded				
		V_{CC} = 6.0 V	-	-	80.0	μA

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Table 5. Static characteristics 74HC4046A

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Phase comparator section; T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	pins SIG_IN, COMP_IN; DC coupled				
		V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	pins SIG_IN, COMP_IN; DC coupled				
		V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	pins PCP_OUT, PCn_OUT; V_I = V_{IH} or V_{IL}				
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.2	-	-	V
V_{OL}	LOW-level output voltage	pins PCP_OUT, PCn_OUT; V_I = V_{IH} or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_I	input leakage current	pins SIG_IN, COMP_IN; V_I = V_{CC} or GND				
		V_{CC} = 2.0 V	-	-	±5	μA
		V_{CC} = 3.0 V	-	-	±11	μA
		V_{CC} = 4.5 V	-	-	±27	μA
		V_{CC} = 6.0 V	-	-	±45	μA
I_{OZ}	OFF-state output current	pin PC2_OUT; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND				
		V_{CC} = 6.0 V	-	-	±10	μA
VCO section; T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	pin INH				
		V_{CC} = 3.0 V	2.1	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	pin INH				
		V_{CC} = 3.0 V	-	-	0.9	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V

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Table 5. Static characteristics 74HC4046A

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	pin VCO_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = –20 μA; V_{CC} = 3.0 V	2.9	-	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.2	-	-	V
V_{OL}	LOW-level output voltage	pin VCO_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 3.0 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
		pins C1A, C1B; $V_I = V_{IH}$ or V_{IL}				
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.54	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.54	V
I_I	input leakage current	pins INH, VCO_IN; $V_I = V_{CC}$ or GND				
		V_{CC} = 6.0 V	-	-	±1	μA
General; T_{amb} = –40 °C to +125 °C						
I_{CC}	supply current	VCO disabled; pins COMP_IN, INH and SIG_IN at V_{CC}; pin VCO_IN at GND; I_I at pins COMP_IN and SIGN_IN to be excluded				
		V_{CC} = 6.0 V	-	-	160.0	μA

[1] The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/ or R2 are/is > 10 kΩ.

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11.2 Static characteristics 74HCT4046A

Table 6. Static characteristics 74HCT4046A

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Phase comparator section; T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	pins SIG_IN, COMP_IN; DC coupled				
		V_{CC} = 4.5 V	3.15	2.4	-	V
V_{IL}	LOW-level input voltage	pins SIG_IN, COMP_IN; DC coupled				
		V_{CC} = 4.5 V	-	2.1	1.35	V
V_{OH}	HIGH-level output voltage	pins PCP_OUT, PCn_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = −4 μA; V_{CC} = 4.5 V	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	pins PCP_OUT, PCn_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
I_I	input leakage current	pins SIG_IN, COMP_IN; $V_I = V_{CC}$ or GND				
		V_{CC} = 5.5 V	-	-	±30	μA
I_{OZ}	OFF-state output current	pin PC2_OUT; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND				
		V_{CC} = 5.5 V	-	-	±0.5	μA
R_I	input resistance	pins SIG_IN, COMP_IN; V_I at self-bias operating point; ΔV_I = 0.5 V; see Figure 12, 13 and 14				
		V_{CC} = 4.5 V	-	250	-	kΩ
VCO section; T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	pin INH				
		V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	pin INH				
		V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-level output voltage	pin VCO_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = −4 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	pin VCO_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		pins C1A, C1B; $V_I = V_{IH}$ or V_{IL}				
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.40	V
I_I	input leakage current	pins INH, VCO_IN; V_{CC} = 5.5 V; $V_I = V_{CC}$ or GND	-	-	±0.1	μA
R1	resistor 1	V_{CC} = 4.5 V [1]	3	-	300	kΩ
R2	resistor 2	V_{CC} = 4.5 V [1]	3	-	300	kΩ
C1	capacitor 1	V_{CC} = 4.5 V	40	-	no limit	pF
V_{VCO_IN}	voltage on pin VCO_IN	over the range specified for R1; for linearity see Figure 22 and 23				
		V_{CC} = 4.5 V	1.1	-	3.4	V

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Table 6. Static characteristics 74HCT4046A

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Demodulator section; T_{amb} = 25 °C						
R_s	series resistance	at R_s > 300 kΩ, the leakage current can influence V_{DEM_OUT}				
		V_{CC} = 4.5 V	50	-	300	kΩ
V_{offset}	offset voltage	VCO_IN to V_{DEM_OUT}; $V_I = V_{VCO_IN} = 0.5V_{CC}$; values taken over R_s range; see Figure 15				
		V_{CC} = 4.5 V	-	±20	-	mV
R_{dyn}	dynamic resistance	DEM_OUT; $V_{DEM_OUT} = 0.5V_{CC}$				
		V_{CC} = 4.5 V	-	25	-	Ω
General; T_{amb} = 25 °C						
I_{CC}	supply current	VCO disabled; pins COMP_IN, INH and SIG_IN at V_{CC}; pin VCO_IN at GND; I_I at pins COMP_IN and SIGN_IN to be excluded				
		V_{CC} = 6 V	-	-	8.0	µA
ΔI_{CC}	additional supply current	pin INH; $V_I = V_{CC} - 2.1$ V; pins COMP_IN and SIG_IN at V_{CC}; pin VCO_IN at GND; I_I at pins COMP_IN and SIGN_IN to be excluded				
		V_{CC} = 4.5 V to 5.5 V	-	100	360	µA
C_I	input capacitance	pin INH	-	3.5	-	pF
Phase comparator section; T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	pins SIG_IN, COMP_IN; DC coupled				
		V_{CC} = 4.5 V	3.15	-	-	V
V_{IL}	LOW-level input voltage	pins SIG_IN, COMP_IN; DC coupled				
		V_{CC} = 4.5 V	-	-	1.35	V
V_{OH}	HIGH-level output voltage	pins PCP_OUT, PCn_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.84	-	-	V
V_{OL}	LOW-level output voltage	pins PCP_OUT, PCn_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.33	V
I_I	input leakage current	pins SIG_IN, COMP_IN; $V_I = V_{CC}$ or GND				
		V_{CC} = 5.5 V	-	-	±38	µA
I_{OZ}	OFF-state output current	pin PC2_OUT; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND				
		V_{CC} = 5.5 V	-	-	±5	µA

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Table 6. Static characteristics 74HCT4046A

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCO section; T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	pin INH				
		V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	pin INH				
		V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	pin VCO_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.84	-	-	V
V_{OL}	LOW-level output voltage	pin VCO_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.33	V
		pins C1A, C1B; $V_I = V_{IH}$ or V_{IL}				
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.47	V
I_I	input leakage current	pins INH, VCO_IN; $V_I = V_{CC}$ or GND				
		V_{CC} = 5.5 V	-	-	±1	μA
General; T_{amb} = –40 °C to +85 °C						
I_{CC}	supply current	VCO disabled; pins COMP_IN, INH and SIG_IN at V_{CC}; pin VCO_IN at GND; I_I at pins COMP_IN and SIGN_IN to be excluded				
		V_{CC} = 6 V	-	-	80.0	μA
ΔI_{CC}	additional supply current	pin INH; $V_I = V_{CC}$ – 2.1 V; pins COMP_IN and SIG_IN at V_{CC}; pin VCO_IN at GND; I_I at pins COMP_IN and SIGN_IN to be excluded				
		V_{CC} = 4.5 V to 5.5 V	-	-	450	μA
Phase comparator section; T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	pins SIG_IN, COMP_IN; DC coupled				
		V_{CC} = 4.5 V	3.15	-	-	V
V_{IL}	LOW-level input voltage	pins SIG_IN, COMP_IN; DC coupled				
		V_{CC} = 4.5 V	-	-	1.35	V
V_{OH}	HIGH-level output voltage	pins PCP_OUT, PCn_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.7	-	-	V
V_{OL}	LOW-level output voltage	pins PCP_OUT, PCn_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.4	V
I_I	input leakage current	pins SIG_IN, COMP_IN; $V_I = V_{CC}$ or GND				
		V_{CC} = 5.5 V	-	-	±45	μA
I_{OZ}	OFF-state output current	pin PC2_OUT; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND				
		V_{CC} = 5.5 V	-	-	±10	μA

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Table 6. Static characteristics 74HCT4046A

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCO section; T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	pin INH				
		V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	pin INH				
		V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	pin VCO_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.7	-	-	V
V_{OL}	LOW-level output voltage	pin VCO_OUT; $V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.4	V
		pins C1A, C1B; $V_I = V_{IH}$ or V_{IL}				
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.54	V
I_I	input leakage current	pins INH, VCO_IN; $V_I = V_{CC}$ or GND				
		V_{CC} = 5.5 V	-	-	±1	μA
General; T_{amb} = –40 °C to +125 °C						
I_{CC}	supply current	VCO disabled; pins COMP_IN, INH and SIG_IN at V_{CC}; pin VCO_IN at GND; I_I at pins COMP_IN and SIGN_IN to be excluded				
		V_{CC} = 6 V	-	-	160.0	μA
ΔI_{CC}	additional supply current	pin INH; $V_I = V_{CC}$ – 2.1 V; pins COMP_IN and SIG_IN at V_{CC}; pin VCO_IN at GND; I_I at pins COMP_IN and SIGN_IN to be excluded				
		V_{CC} = 4.5 V to 5.5 V	-	-	490	μA

[1] The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/ or R2 are/is > 10 kΩ.

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11.3 Graphs

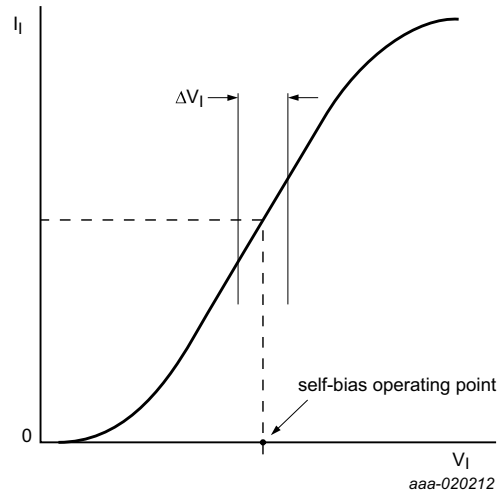


Fig 12. Typical input resistance curve at SIG_IN and COMP_IN

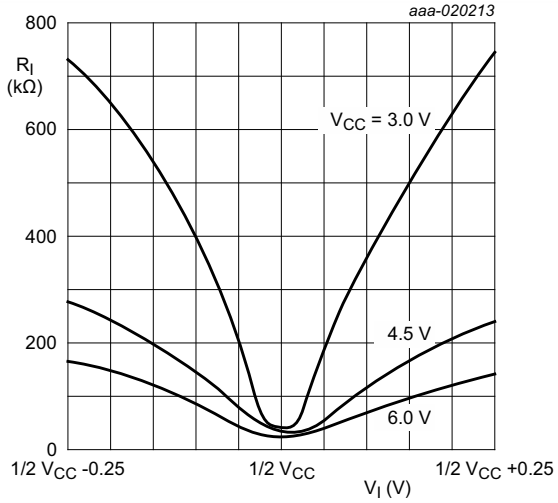


Fig 13. Input resistance at SIG_IN, COMP_IN with ΔV_I = 0.5 V at self-bias point

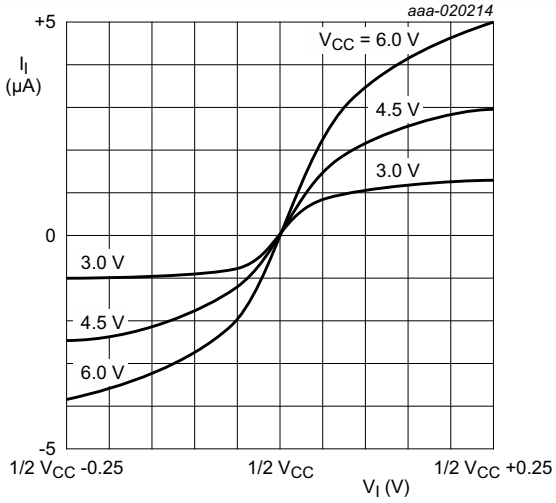
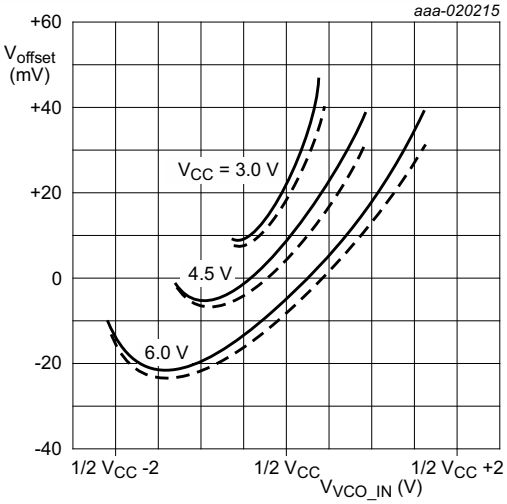


Fig 14. Input current at SIG_IN, COMP_IN with ΔV_I = 0.5 V at self-bias point



___ R_s = 50 kΩ

- - - R_s = 300 kΩ

Fig 15. Offset voltage at demodulator output as a function of VCO_IN and R_s

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12. Dynamic characteristics

12.1 Dynamic characteristics 74HC4046A

Table 7. Dynamic characteristics 74HC4046A[1]

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Phase comparator section; T_{amb} = 25 °C						
t_{pd}	propagation delay	pins SIG_IN, COMP_IN to PC1_OUT; see Figure 16 [1]				
		V_{CC} = 2.0 V	-	63	200	ns
		V_{CC} = 4.5 V	-	23	40	ns
		V_{CC} = 6.0 V	-	18	34	ns
		pins SIG_IN, COMP_IN to PCP_OUT; see Figure 16 [1]				
		V_{CC} = 2.0 V	-	96	340	ns
		V_{CC} = 4.5 V	-	35	68	ns
		V_{CC} = 6.0 V	-	28	58	ns
		pins SIG_IN, COMP_IN to PC3_OUT; see Figure 16 [1]				
		V_{CC} = 2.0 V	-	77	270	ns
		V_{CC} = 4.5 V	-	28	54	ns
		V_{CC} = 6.0 V	-	22	46	ns
t_{en}	enable time	pins SIG_IN, COMP_IN to PC2_OUT; see Figure 17 [1]				
		V_{CC} = 2.0 V	-	83	280	ns
		V_{CC} = 4.5 V	-	30	56	ns
		V_{CC} = 6.0 V	-	24	48	ns
t_{dis}	disable time	pins SIG_IN, COMP_IN to PC2_OUT; see Figure 17 [1]				
		V_{CC} = 2.0 V	-	99	325	ns
		V_{CC} = 4.5 V	-	36	65	ns
		V_{CC} = 6.0 V	-	29	55	ns
t_t	transition time	see Figure 16 [1]				
		V_{CC} = 2.0 V	-	19	75	ns
		V_{CC} = 4.5 V	-	7	15	ns
		V_{CC} = 6.0 V	-	6	13	ns
$V_{i(p-p)}$	peak-to-peak input voltage	pins SIGN_IN, COMP_IN; AC coupled; f_i = 1 MHz				
		V_{CC} = 2.0 V	-	9	-	mV
		V_{CC} = 3.0 V	-	11	-	mV
		V_{CC} = 4.5 V	-	15	-	mV
		V_{CC} = 6.0 V	-	33	-	mV

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Table 7. Dynamic characteristics 74HC4046A[1] *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCO section; T_{amb} = 25 °C						
f_0	center frequency	V_{VCO_IN} = 0.5V_{CC}; duty cycle = 50 %; R1 = 3 kΩ; R2 = ∞ Ω; C1 = 40 pF; see Figure 20 and Figure 21				
		V_{CC} = 3.0 V	7.0	10.0	-	MHz
		V_{CC} = 4.5 V	11.0	17.0	-	MHz
		V_{CC} = 5.0 V	-	19.0	-	MHz
		V_{CC} = 6.0 V	13.0	21.0	-	MHz
Δf/f	relative frequency variation	R1 = 100 kΩ; R2 = ∞ Ω; C1 = 100 pF; see Figure 22 and Figure 23				
		V_{CC} = 3.0 V	-	1.0	-	%
		V_{CC} = 4.5 V	-	0.4	-	%
		V_{CC} = 6.0 V	-	0.3	-	%
δ	duty cycle	pin VCO_OUT; V_{CC} = 3.0 V to 6.0 V	-	50	-	%
General; T_{amb} = 25 °C						
C_{PD}	power dissipation capacitance	[3]	-	24	-	pF
Phase comparator section; T_{amb} = –40 °C to +85 °C						
t_{pd}	propagation delay	pins SIG_IN, COMP_IN to PC1_OUT; see Figure 16 [1]				
		V_{CC} = 2.0 V	-	-	250	ns
		V_{CC} = 4.5 V	-	-	50	ns
		V_{CC} = 6.0 V	-	-	43	ns
		pins SIG_IN, COMP_IN to PCP_OUT; see Figure 16 [1]				
		V_{CC} = 2.0 V	-	-	425	ns
		V_{CC} = 4.5 V	-	-	85	ns
		V_{CC} = 6.0 V	-	-	72	ns
		pins SIG_IN, COMP_IN to PC3_OUT; see Figure 16 [1]				
		V_{CC} = 2.0 V	-	-	340	ns
		V_{CC} = 4.5 V	-	-	68	ns
		V_{CC} = 6.0 V	-	-	58	ns
t_{en}	enable time	pins SIG_IN, COMP_IN to PC2_OUT; see Figure 17 [1]				
		V_{CC} = 2.0 V	-	-	350	ns
		V_{CC} = 4.5 V	-	-	70	ns
		V_{CC} = 6.0 V	-	-	60	ns
t_{dis}	disable time	pins SIG_IN, COMP_IN to PC2_OUT; see Figure 17 [1]				
		V_{CC} = 2.0 V	-	-	405	ns
		V_{CC} = 4.5 V	-	-	81	ns
		V_{CC} = 6.0 V	-	-	69	ns

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Table 7. Dynamic characteristics 74HC4046A[1] *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_t	transition time	see Figure 16 [1]				
		V_{CC} = 2.0 V	-	-	95	ns
		V_{CC} = 4.5 V	-	-	19	ns
		V_{CC} = 6.0 V	-	-	16	ns
VCO section; T_{amb} = –40 °C to +85 °C						
$\Delta f/\Delta T$	frequency variation with temperature	$V_{VCO_IN} = 0.5V_{CC}$; R1 = 100 kΩ; R2 = ∞ kΩ; C1 = 100 pF; see Figure 18 and Figure 19				
		V_{CC} = 3.0 V	-	0.20	-	%/K
		V_{CC} = 4.5 V	-	0.15	-	%/K
		V_{CC} = 6.0 V	-	0.14	-	%/K
Phase comparator section; T_{amb} = –40 °C to +125 °C						
t_{pd}	propagation delay	pins SIG_IN, COMP_IN to PC1_OUT; see Figure 16 [1]				
		V_{CC} = 2.0 V	-	-	300	ns
		V_{CC} = 4.5 V	-	-	60	ns
		V_{CC} = 6.0 V	-	-	51	ns
		pins SIG_IN, COMP_IN to PCP_OUT; see Figure 16 [1]				
		V_{CC} = 2.0 V	-	-	510	ns
		V_{CC} = 4.5 V	-	-	102	ns
		V_{CC} = 6.0 V	-	-	87	ns
		pins SIG_IN, COMP_IN to PC3_OUT; see Figure 16 [1]				
		V_{CC} = 2.0 V	-	-	405	ns
		V_{CC} = 4.5 V	-	-	81	ns
		V_{CC} = 6.0 V	-	-	69	ns
t_{en}	enable time	pins SIG_IN, COMP_IN to PC2_OUT; see Figure 17 [1]				
		V_{CC} = 2.0 V	-	-	420	ns
		V_{CC} = 4.5 V	-	-	84	ns
		V_{CC} = 6.0 V	-	-	71	ns
t_{dis}	disable time	pins SIG_IN, COMP_IN to PC2_OUT; see Figure 17 [1]				
		V_{CC} = 2.0 V	-	-	490	ns
		V_{CC} = 4.5 V	-	-	98	ns
		V_{CC} = 6.0 V	-	-	83	ns

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Table 7. Dynamic characteristics 74HC4046A[1] *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_t	transition time	see Figure 16	[1]				
		V_{CC} = 2.0 V		-	-	110	ns
		V_{CC} = 4.5 V		-	-	22	ns
		V_{CC} = 6.0 V		-	-	19	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}. t_{dis} is the same as t_{PLZ} and t_{PHZ}. t_{en} is the same as t_{PZL} and t_{PZH}. t_t is the same as t_{TLH} and t_{THL}.

[2] Applies to the phase comparator section only (VCO disabled). For power dissipation of the VCO and demodulator sections, see Figure 24, Figure 25 and Figure 26

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = total load switching outputs;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12.2 Dynamic characteristics 74HCT4046A

Table 8. Dynamic characteristics 74HCT4046A[1]

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Phase comparator section; T_{amb} = 25 °C							
t_{pd}	propagation delay	pins SIG_IN, COMP_IN to PC1_OUT; V_{CC} = 4.5 V; see Figure 16	[1]	-	23	40	ns
		pins SIG_IN, COMP_IN to PCP_OUT; V_{CC} = 4.5 V; see Figure 16	[1]	-	35	68	ns
		pins SIG_IN, COMP_IN to PC3_OUT; V_{CC} = 4.5 V; see Figure 16	[1]	-	28	54	ns
t_{en}	enable time	pins SIG_IN, COMP_IN to PC2_OUT; V_{CC} = 4.5 V; see Figure 17	[1]	-	30	56	ns
t_{dis}	disable time	pins SIG_IN, COMP_IN to PC2_OUT; V_{CC} = 4.5 V; see Figure 17	[1]	-	36	65	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 16	[1]	-	7	15	ns
$V_{i(p-p)}$	peak-to-peak input voltage	pins SIGN_IN, COMP_IN; AC coupled; V_{CC} = 4.5 V; f_i = 1 MHz		-	15	-	mV
VCO section; T_{amb} = 25 °C							
f_0	center frequency	V_{VCO_IN} = 0.5V_{CC}; duty cycle = 50 %; R1 = 3 kΩ; R2 = ∞ Ω; C1 = 40 pF; see Figure 20 and Figure 21					
		V_{CC} = 4.5 V		11.0	17.0	-	MHz
		V_{CC} = 5.0 V		-	19.0	-	MHz
Δf/f	relative frequency variation	R1 = 100 kΩ; R2 = ∞ Ω; C1 = 100 pF; V_{CC} = 4.5 V; see Figure 22 and Figure 23		-	0.4	-	%
δ	duty cycle	pin VCO_OUT; V_{CC} = 4.5 V		-	50	-	%

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Table 8. Dynamic characteristics 74HCT4046A[1] *…continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
General; T_{amb} = 25 °C							
C_{PD}	power dissipation capacitance		[2][3]	-	24	-	pF
Phase comparator section; T_{amb} = –40 °C to +85 °C							
t_{pd}	propagation delay	pins SIG_IN, COMP_IN to PC1_OUT; V_{CC} = 4.5 V; see Figure 16	[1]	-	-	50	ns
		pins SIG_IN, COMP_IN to PCP_OUT; V_{CC} = 4.5 V; see Figure 16	[1]	-	-	85	ns
		pins SIG_IN, COMP_IN to PC3_OUT; V_{CC} = 4.5 V; see Figure 16	[1]	-	-	68	ns
t_{en}	enable time	pins SIG_IN, COMP_IN to PC2_OUT; V_{CC} = 4.5 V; see Figure 17	[1]	-	-	70	ns
t_{dis}	disable time	pins SIG_IN, COMP_IN to PC2_OUT; V_{CC} = 4.5 V; see Figure 17	[1]	-	-	81	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 16	[1]	-	-	19	ns
VCO section; T_{amb} = –40 °C to +85 °C							
$\Delta f/\Delta T$	frequency variation with temperature	$V_{VCO_IN} = 0.5V_{CC}$; R1 = 100 kΩ; R2 = ∞ kΩ; C1 = 100 pF; V_{CC} = 4.5 V; see Figure 18b		0.15	-	-	%/K
Phase comparator section; T_{amb} = –40 °C to +125 °C							
t_{pd}	propagation delay	pins SIG_IN, COMP_IN to PC1_OUT; V_{CC} = 4.5 V; see Figure 16	[1]	-	-	60	ns
		pins SIG_IN, COMP_IN to PCP_OUT; V_{CC} = 4.5 V; see Figure 16	[1]	-	-	102	ns
		pins SIG_IN, COMP_IN to PC3_OUT; V_{CC} = 4.5 V; see Figure 16	[1]	-	-	81	ns
t_{en}	enable time	pins SIG_IN, COMP_IN to PC2_OUT; V_{CC} = 4.5 V; see Figure 17	[1]	-	-	84	ns
t_{dis}	disable time	pins SIG_IN, COMP_IN to PC2_OUT; V_{CC} = 4.5 V; see Figure 17	[1]	-	-	98	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 16	[1]	-	-	22	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}. t_{dis} is the same as t_{PLZ} and t_{PHZ}. t_{en} is the same as t_{PZL} and t_{PZH}. t_t is the same as t_{TLH} and t_{THL}.

[2] Applies to the phase comparator section only (VCO disabled). For power dissipation of the VCO and demodulator sections, see Figure 24, Figure 25 and Figure 26

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = total load switching outputs;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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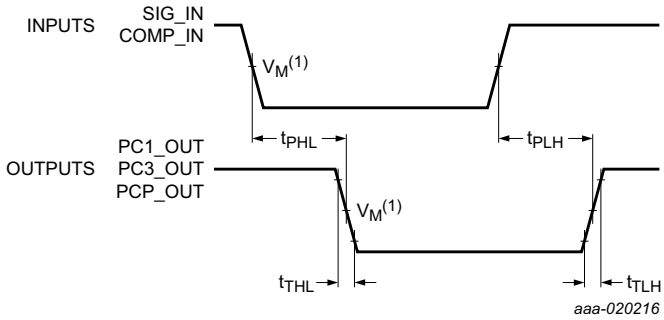
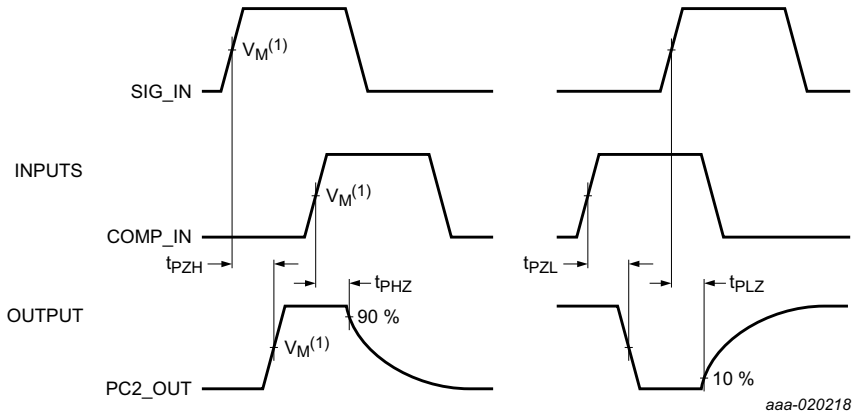
12.3 Waveforms and graphs



$V_M = 0.5V_{CC}$; V_I = GND to V_{CC}.

Fig 16. Waveforms showing input (SIG_IN, COMP_IN) to output (PC1_OUT, PC3_OUT, PCP_OUT) propagation delays and the output transition times



$V_M = 0.5V_{CC}$; V_I = GND to V_{CC}.

Fig 17. Waveforms showing the enable and disable times for PC2_OUT

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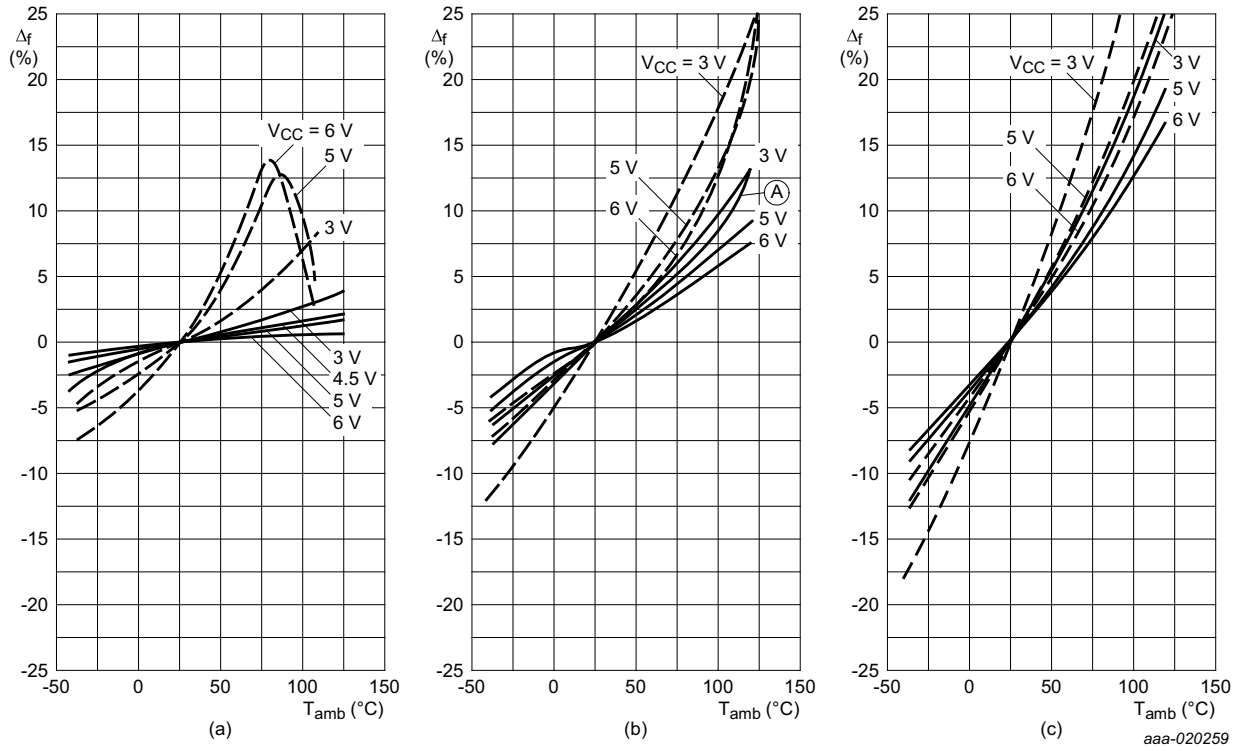

To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

In (b), the frequency stability for R1 = R2 = 10 kΩ at 5 V is also given (curve A). The total VCO bias current sets this curve, and is not simply the addition of the two 10 kΩ stability curves. C1 = 100 pF; $V_{VCO_IN} = 0.5V_{CC}$; This curve is set as follows:

___ Without offset R2 = ∞ kΩ: (a) R1 = 3 kΩ; (b) R1 = 10 kΩ; (c) R1 = 300 kΩ.

- - - With offset R1 = ∞ kΩ: (a) R2 = 3 kΩ; (b) R2 = 10 kΩ; (c) R2 = 300 kΩ.

Fig 18. Frequency stability of the VCO as a function of ambient temperature

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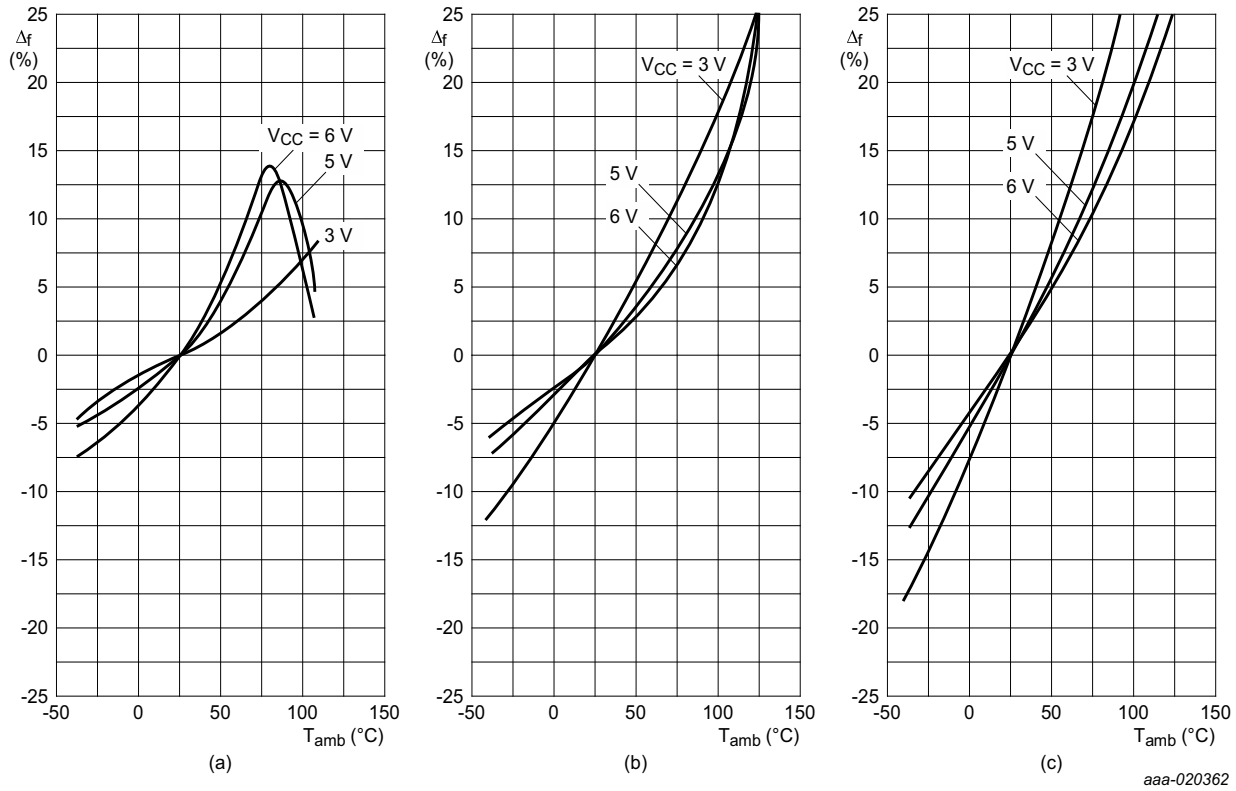

To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

___ With offset; R1 = ∞ kΩ: (a) R2 = 3 kΩ; (b) R2 = 10 kΩ; (c) R2 = 300 kΩ.

Fig 19. Frequency stability of the VCO as a function of ambient temperature

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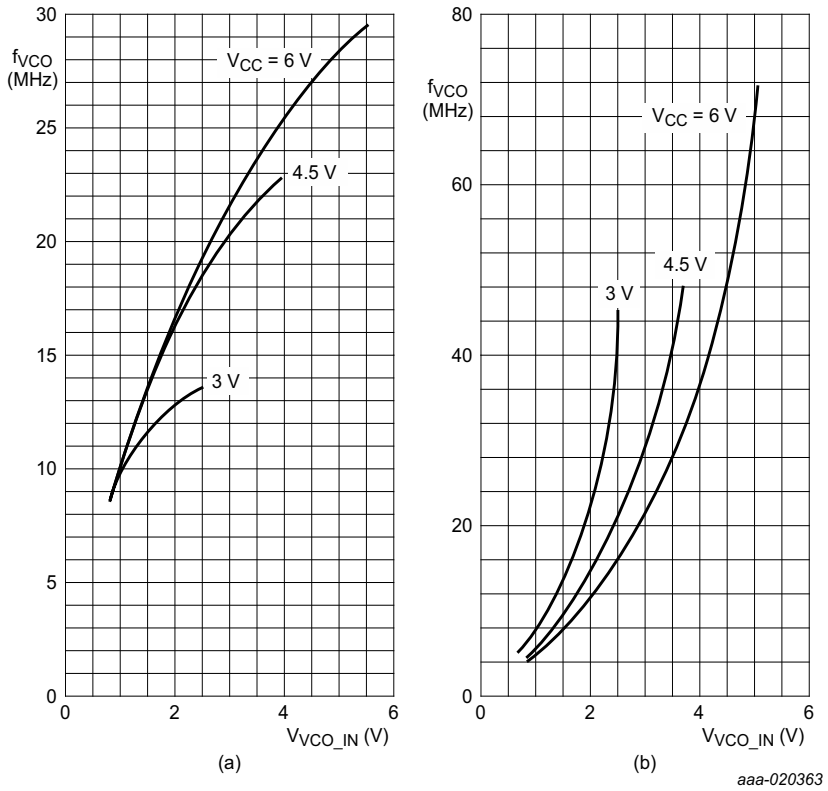

To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

(a) R1 = 3 kΩ; C1 = 40 pF (b) R1 = 3 kΩ; C1 = 100 nF

Fig 20. Graphs showing VCO frequency as a function of the VCO input voltage

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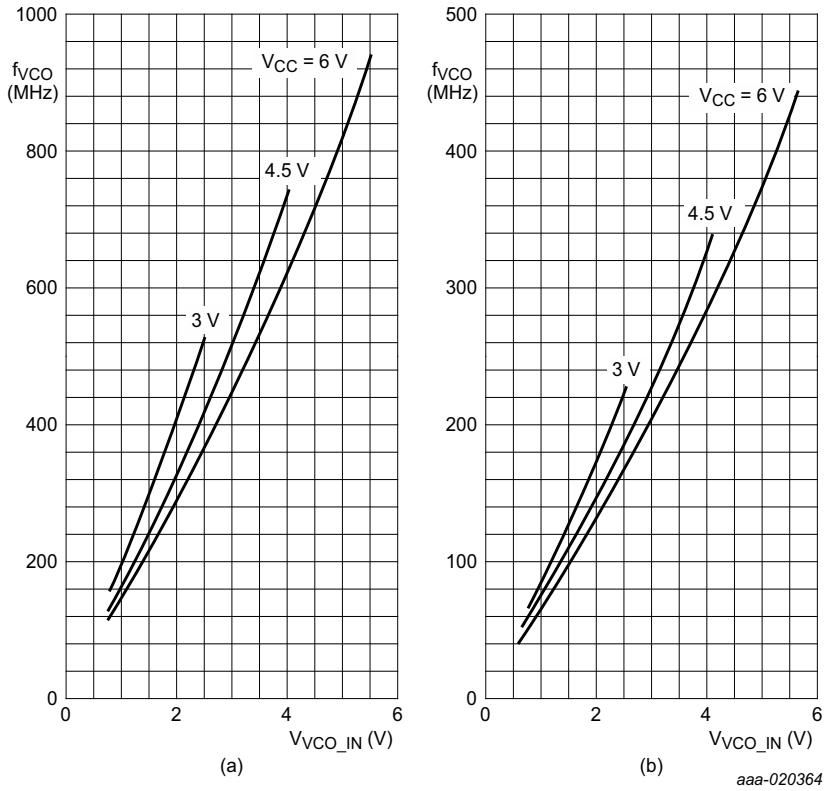

To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

(a) R1 = 300 kΩ; C1 = 40 pF (b) R1 = 300 kΩ; C1 = 100 nF

Fig 21. Graphs showing VCO frequency as a function of the VCO input voltage

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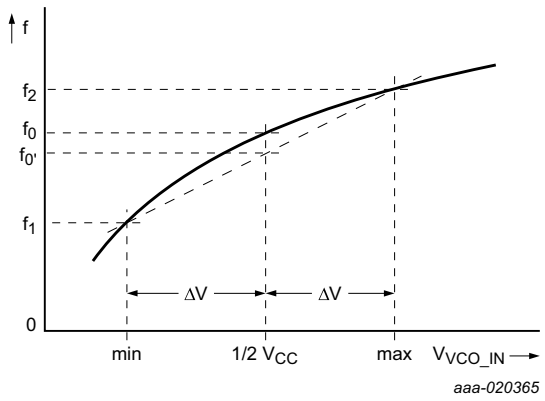
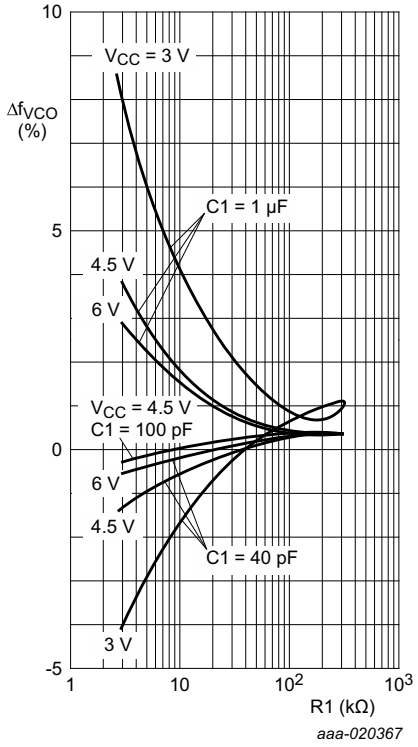


ΔV = 0.5 V over the V_{CC} range.

$$f'_0 = \frac{f_1 + f_2}{2}$$

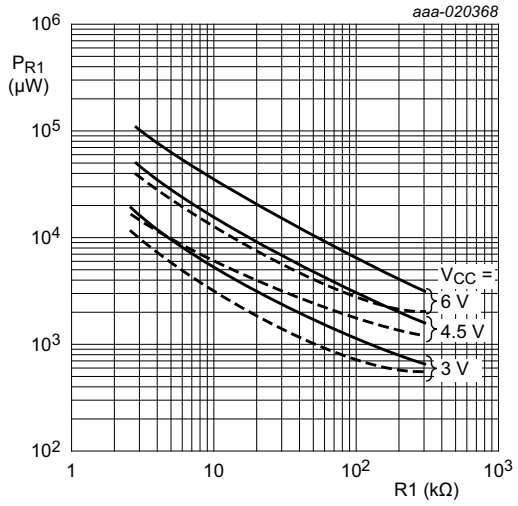
$$\text{linearity} = \frac{f'_0 - f_0}{f'_0} \times 100\ \%$$

Fig 22. Definition of VCO frequency linearity



R2 = ∞ Ω; ΔV = 0.5 V

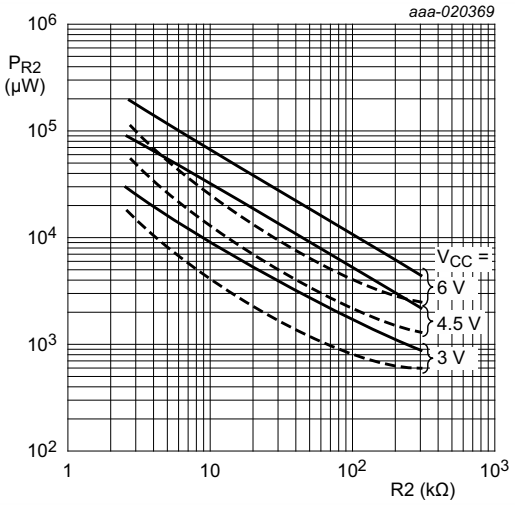
Fig 23. Frequency linearity as a function of R1, C1



R2 = ∞ Ω; C_L = 50 pF; V_{VCO_IN} = 0.5V_{CC}; T_{amb} = 25 °C

___ C1 = 40 pF; - - - C1 = 1 µF

Fig 24. Power dissipation as a function of R1



R1 = ∞ Ω; C_L = 50 pF; V_{VCO_IN} = GND; T_{amb} = 25 °C

___ C1 = 40 pF; - - - C1 = 1 µF

Fig 25. Power dissipation as a function of R2

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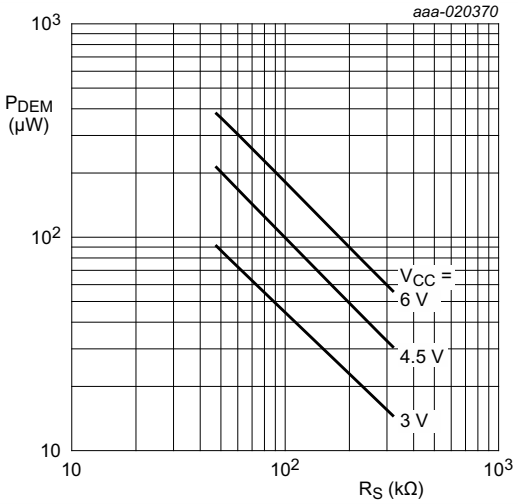

R1 = R2 = ∞ Ω; V_{VCO_IN} = 0.5V_{CC}; T_{amb} = 25 °C

Fig 26. Typical power dissipation of demodulator sections as a function of R_S

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13. Application information

This information is a guide for the approximation of values of external components to be used with the 74HC4046A; 74HCT4046A in a phase-locked-loop system.

References should be made to Figure 30, Figure 31 and Figure 32 as indicated in Table 10.

Values of the selected components should be within the ranges shown in Table 9.

Table 9. Survey of components

Component	Value
R1	between 3 kΩ and 300 kΩ
R2	between 3 kΩ and 300 kΩ
R1 + R2	parallel value > 2.7 kΩ
C1	> 40 pF

Table 10. Design considerations for VCO section

Subject	Phase comparator	Design consideration
VCO frequency **without extra offset**	PC1, PC2 or PC3	VCO frequency characteristic. With R2 = ∞ and R1 within the range 3 kΩ < R1 < 300 kΩ, the characteristics of the VCO operation is as shown in Figure 27a. (Due to R1, C1 time constant a small offset remains when R2 = ∞ Ω).
	PC1	Selection of R1 and C1. Given f_0, determine the values of R1 and C1 using Figure 30.
	PC2 or PC3	Given f_{max} and f_0, determine the values of R1 and C1 using Figure 30; use Figure 32 to obtain $2f_L$ and then use it to calculate f_{min}.
VCO frequency **with extra offset**	PC1, PC2 or PC3	VCO frequency characteristic with R1 and R2 within the ranges 3 kΩ < R1 < 300 kΩ, 3 kΩ < R2 < 300 kΩ. The characteristics of the VCO operation are as shown in Figure 27b.
	PC1, PC2 or PC3	Selection of R1, R2 and C1. Given f_0 and f_L determine the value of product R1C1 by using Figure 32. Calculate f_{off} from the equation $f_{off} = f_0 - 1.6f_L$. Obtain the values of C1 and R2 by using Figure 31. Calculate the value of R1 from the value of C1 and the product R1C1.
PLL conditions **no signal at pin SIG_IN**	PC1	VCO adjusts to f_0 with Φ_{DEM_OUT} = 90° and $V_{VCO_IN} = 0.5V_{CC}$, see Figure 6
	PC2	VCO adjusts to f_0 with Φ_{DEM_OUT} = −360° and V_{VCO_IN} = minimum, see Figure 8
	PC3	VCO adjusts to f_0 with Φ_{DEM_OUT} = −360° and V_{VCO_IN} = minimum, see Figure 10

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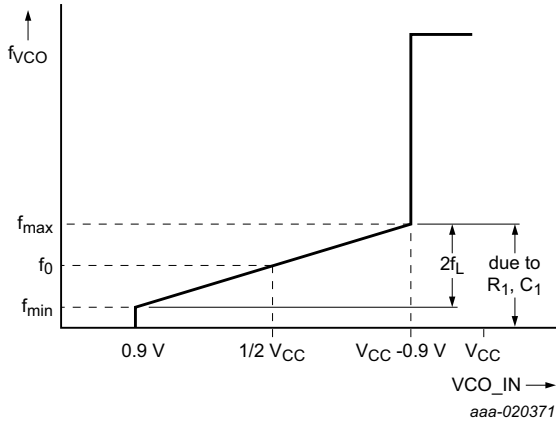
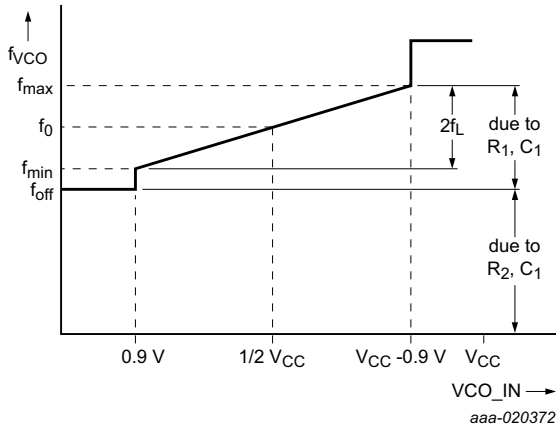


a. Operating without offset; f_0 = center frequency; $2f_L$ = frequency lock range.



b. Operating with offset; f_0 = center frequency; $2f_L$ = frequency lock range.

Fig 27. Frequency characteristic of VCO

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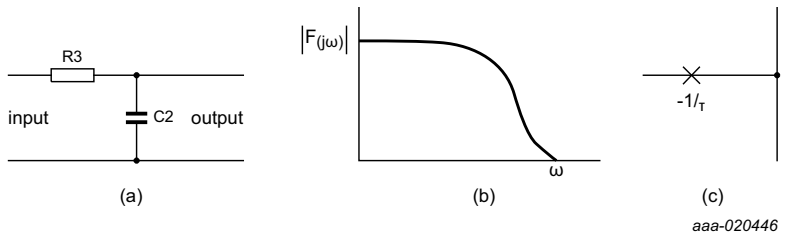
Table 11. General design considerations

Subject	Phase comparator	Design consideration
PLL frequency capture range	PC1, PC2 or PC3	Loop filter component selection, see Figure 28 and 29
PLL locks on harmonics at center frequency	PC1 or PC3	yes
	PC2	no
Noise rejection at signal input	PC1	high
	PC2 or PC3	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$; large ripple content at $\Phi_{DEM_OUT} = 90°$
	PC2	$f_r = f_i$; small ripple content at $\Phi_{DEM_OUT} = 0°$
	PC3	$f_r = f_i$; large ripple content at $\Phi_{DEM_OUT} = 180°$



R3 ≥ 500 Ω.

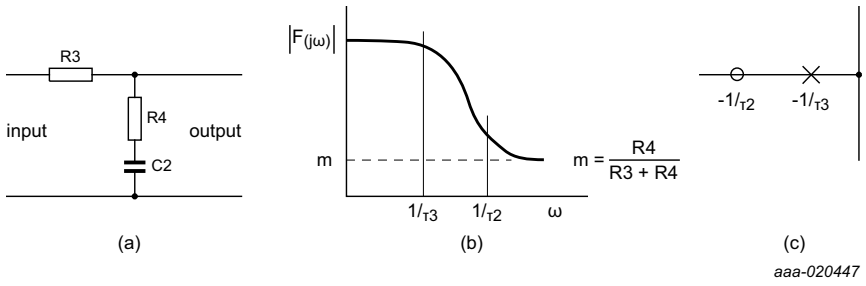
A small capture range ($2f_c$) is obtained if $2f_c = \frac{1}{\pi}\sqrt{2\pi f_L / \tau}$

(a) τ = R3 x C2

(b) amplitude characteristics

(c) pole-zero diagram

Fig 28. Simple loop filter for PLL without offset



R3 + R4 ≥ 500 Ω.

(a) τ1 = R3 x C2; τ2 = R4 x C2; τ3 = (R3 + R4) x C2

(b) amplitude characteristics

(c) pole-zero diagram

Fig 29. Simple loop filter for PLL with offset

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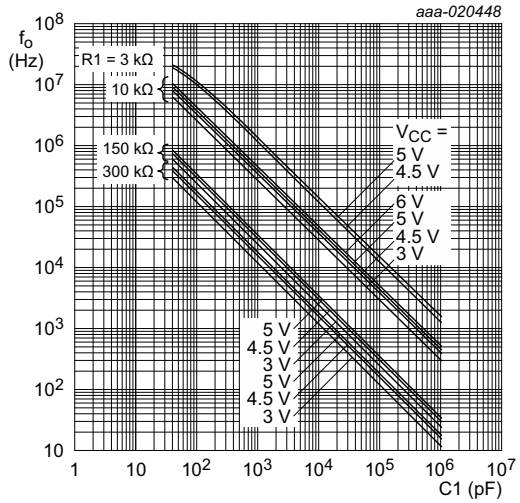
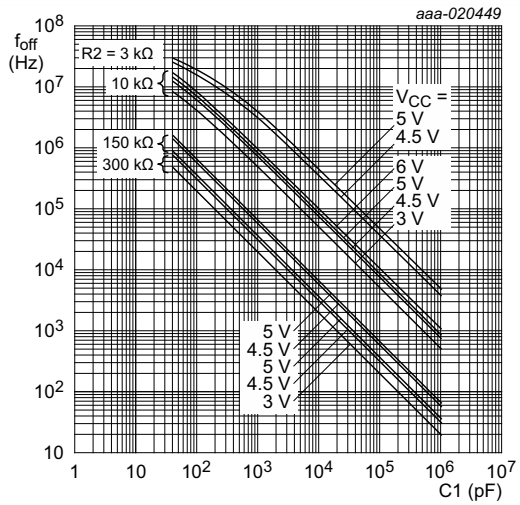


To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.

Interpolation for various values of R1 can be easily calculated because a constant R1C1 product produces almost the same VCO output frequency.

R2 = ∞ Ω; V_{VCO_IN} = 0.5V_{CC}; INH = GND; T_{amb} = 25 °C.

Fig 30. Typical value of VCO center frequency (f_0) as a function of C1



To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.

Interpolation for various values of R2 can be easily calculated because a constant R2C1 product produces almost the same VCO output frequency.

R1 = ∞ Ω; V_{VCO_IN} = 0.5V_{CC}; INH = GND; T_{amb} = 25 °C.

Fig 31. Typical value of frequency offset as a function of C1

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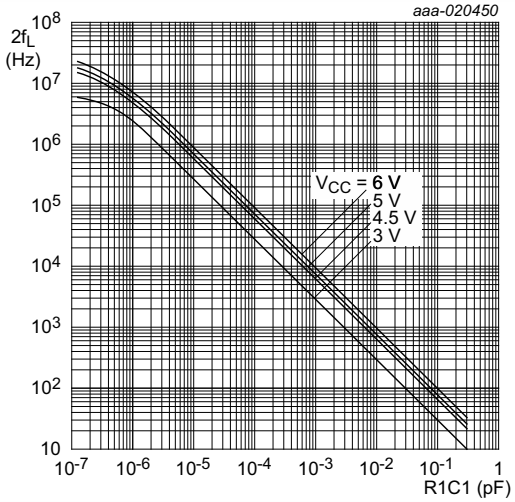

V_{VCO_IN} = 0.9 V to (V_{CC} − 0.9) V; R2 = ∞ Ω.

VCO gain: $K_v = \frac{2f_L}{V_{VCO_IN}\ range} 2\pi(r/s/V)$

Fig 32. Typical frequency lock range ($2f_L$) as a function of the product R1C1

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13.1 PLL design example

The frequency synthesizer used in the design example shown in Figure 33 has the following parameters:

Output frequency: 2 MHz to 3 MHz

Frequency steps: 100 kHz

Settling time: 1 ms

Overshoot: < 20 %

The open loop gain is:

$$H(s) \times G(s) = K_p \times K_f \times K_o \times K_n$$

where:

K_p = phase comparator gain

K_f = low-pass filter transfer gain

K_o = K_v/s VCO gain

K_n = $^1/_n$ divider ratio

The programmable counter ratio K_n can be found as follows:

$$N_{min} = \frac{f_{OUT}}{f_{step}} = \frac{2\ MHz}{100\ kHz} = 20$$

$$N_{max} = \frac{f_{OUT}}{f_{step}} = \frac{3\ MHz}{100\ kHz} = 30$$

The values of R1, R2 and C1; R2 = 10 kΩ (adjustable) set the VCO.

The values can be determined using the information in Table 10 and Table 11.

With f_0 = 2.5 MHz and f_L = 500 kHz, the following values (V_{CC} = 5.0 V) are given:

R1 = 10 kΩ

R2 = 10 kΩ

C1 = 500 pF

The VCO gain is:

$$K_v = \frac{2f_L \times 2\pi}{(V_{CC} - 0.9) - 0.9} = \frac{1\ MHz}{3.2} \times 2\pi \approx 2 \times 10^6\ r/s/V$$

The gain of the phase comparator is:

$$K_p = \frac{V_{CC}}{4 \times \pi} = 0.4\ V/r$$

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The transfer gain of the filter is calculated as follows:

$$K_f = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)\ \mathrm{s}}$$

Where:

$$\tau_1 = R3 \times C2$$

$$\tau_2 = R4 \times C2$$

The characteristic equation is: $1 + H(\mathrm{s}) \times G(\mathrm{s}) = 0$

It results in:

$$S^2 + \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)} \times S + \frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)} = 0$$

The natural frequency ω_n defined as:

$$\omega_n = \sqrt{\frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)}}$$

and the damping value (ζ) given as: $\zeta = \frac{1}{2\omega_n} \times \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)}$

In Figure 34, the output frequency response to a step of input frequency is shown.

The overshoot and settling time percentages are now used to determine ω_n. Figure 34 shows that the damping ratio $\zeta = 0.45$ produces an overshoot of less than 20 % and settle to within 5 % at $\omega_n t = 5$. The required settling time is 1 ms. It results in:

$$\omega_n = \frac{5}{t} = \frac{5}{0.001} = 5 \times 10^3 r/s$$

Rewriting the equation for natural frequency results in:

$$(\tau_1 + \tau_2) = \frac{K_p \times K_v \times K_n}{(\omega_n)^2}$$

The maximum overshoot occurs at N_{max}:

$$(\tau_1 + \tau_2) = \frac{0.4 \times 2 \times 10^6}{5000^2 \times 30} = 0.0011\ \mathrm{s}$$

When C2 = 470 nF, then:

$$R4 = \frac{(\tau_1 + \tau_2) \times 2 \times \omega_n \times \zeta - 1}{K_p \times K_v \times K_n \times C2} = 315\ \Omega$$

R3 can be calculated: $R3 = \frac{\tau_1}{C2} - R4 = 2\ \mathrm{k}\Omega$

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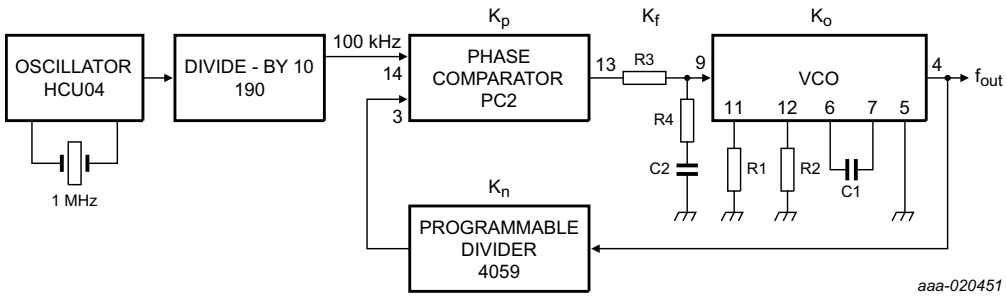


For an extensive description and application example, refer to "*Application note*" ordering number 9398 649 90011.

Fig 33. Frequency synthesizer

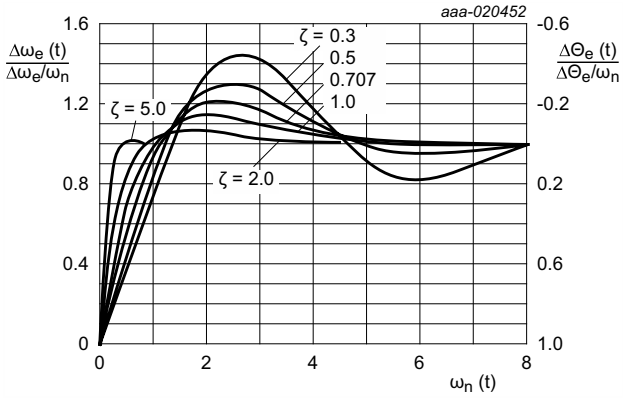
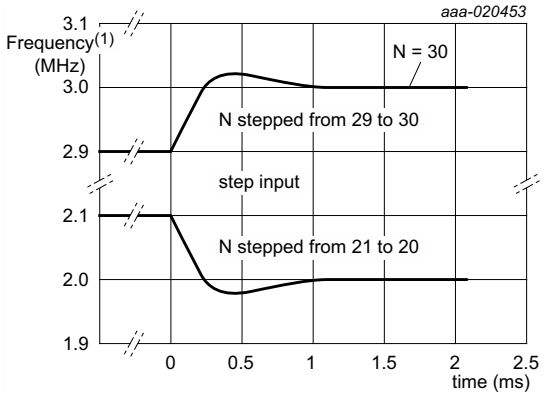


Fig 34. Type 2, second order frequency step response



The output frequency is proportional to the VCO control voltage. As a result, the PLL frequency response can be observed with an oscilloscope by monitoring pin VCO_IN of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin VCO_IN using a simple RC filter. The filter has a long time constant when compared with the phase detector sampling rate but short when compared with the PLL response time.

Fig 35. Frequency compared to the time response

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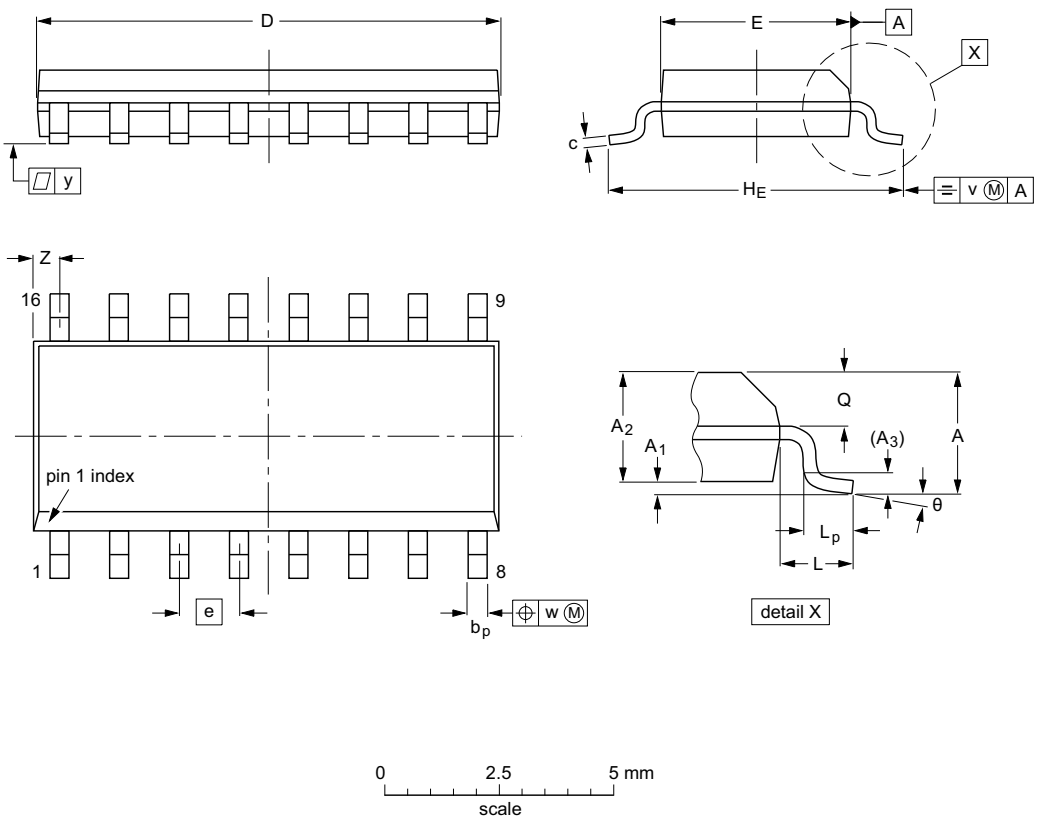
14. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 36. Package outline SOT109-1 (SO16)

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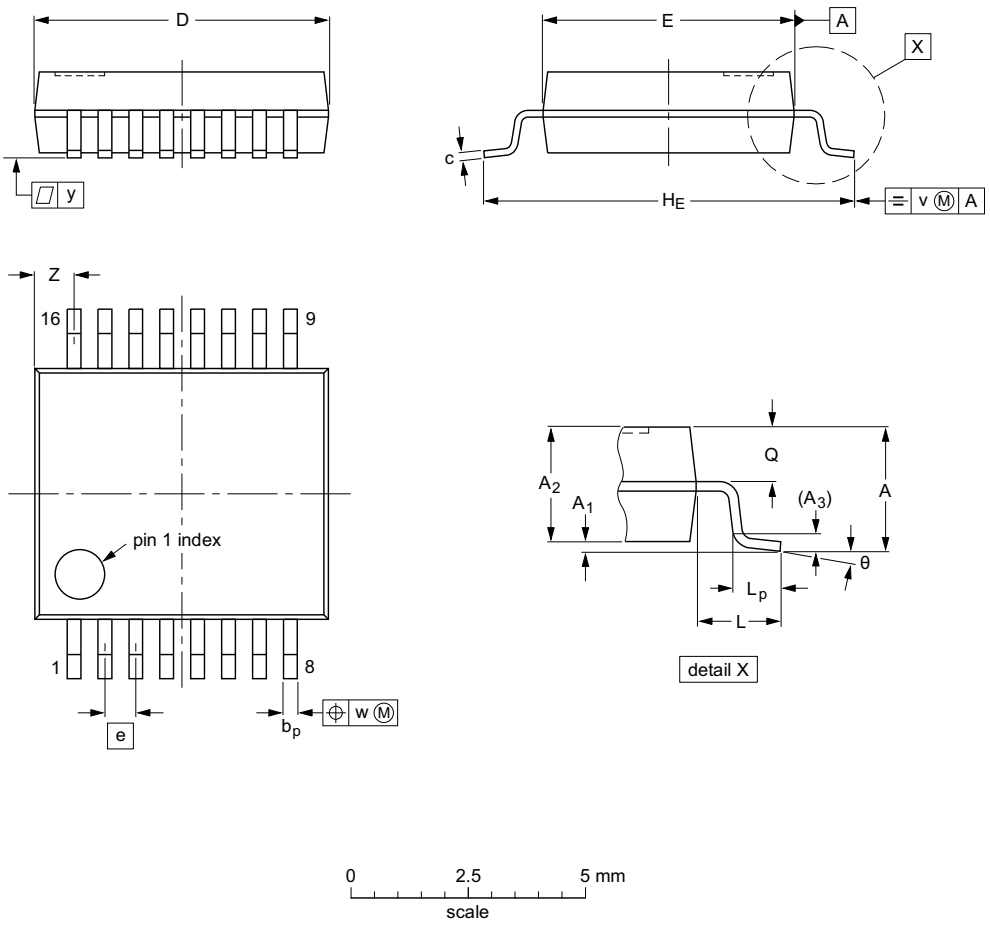
SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 37. Package outline SOT338-1 (SSOP16)

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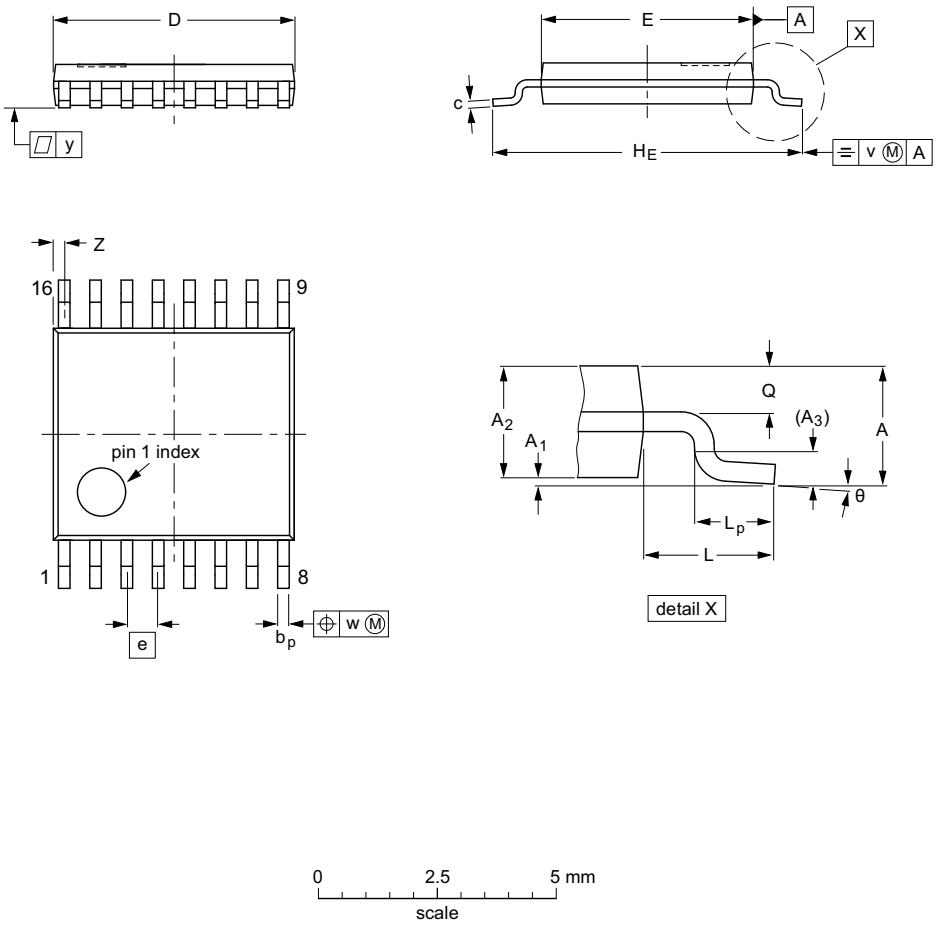
TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 38. Package outline SOT403-1 (TSSOP16)

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15. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductors
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PLL	Phase-Locked Loop
VCO	Voltage Controlled Oscillator

16. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4046A v.3	20160608	Product data sheet	-	74HC_HCT4046A_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT4046A_CNV v.2	19971125	Product specification	-	74HC_HCT4046A v.1
74HC_HCT4046A v.1	19930901	Objective specification	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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