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November 1997 - Revised October 2003

## High-Speed CMOS Logic 7-Stage Binary Ripple Counter

### Features

- Fully Static Operation
- Buffered Inputs
- Common Reset
- Negative Edge Clocking
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The 'HC4024 and 'HCT4024 are 7-stage ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of the stage advances one count on the negative transition of each input pulse; a high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.

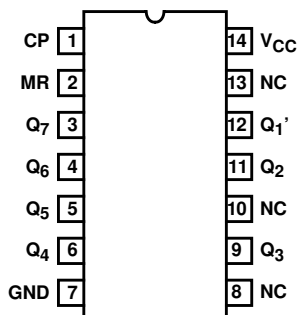
### Ordering Information

| PART NUMBER    | TEMP. RANGE (°C) | PACKAGE      |
|----------------|------------------|--------------|
| CD54HC4024F3A  | -55 to 125       | 14 Ld CERDIP |
| CD54HCT4024F3A | -55 to 125       | 14 Ld CERDIP |
| CD74HC4024E    | -55 to 125       | 14 Ld PDIP   |
| CD74HC4024M    | -55 to 125       | 14 Ld SOIC   |
| CD74HC4024MT   | -55 to 125       | 14 Ld SOIC   |
| CD74HC4024M96  | -55 to 125       | 14 Ld SOIC   |
| CD74HC4024PW   | -55 to 125       | 14 Ld TSSOP  |
| CD74HC4024PWR  | -55 to 125       | 14 Ld TSSOP  |
| CD74HC4024PWT  | -55 to 125       | 14 Ld TSSOP  |
| CD74HCT4024E   | -55 to 125       | 14 Ld PDIP   |
| CD74HCT4024M   | -55 to 125       | 14 Ld SOIC   |

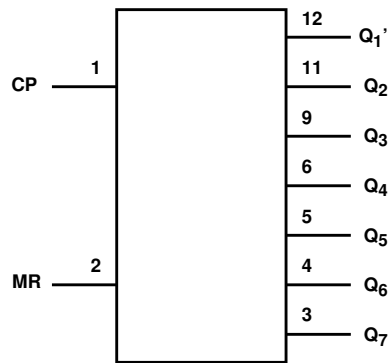
NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

### Pinout

CD54HC4024, CD54HCT4024  
(CERDIP)  
CD74HC4024  
(PDIP, SOIC, TSSOP)  
CD74HCT4024  
(PDIP, SOIC)  
TOP VIEW



## Functional Diagram

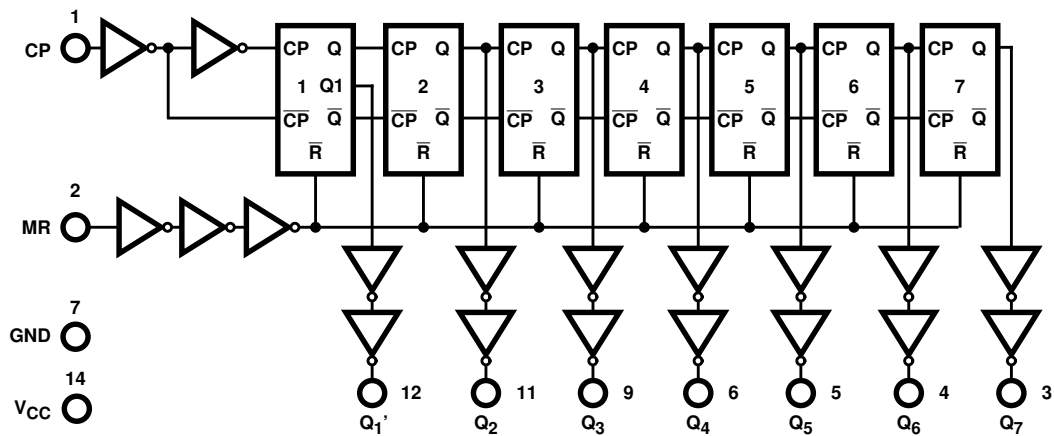


TRUTH TABLE

| CP COUNT | MR | OUTPUT STATE          |
|----------|----|-----------------------|
| ↑        | L  | No Change             |
| ↓        | L  | Advance to Next State |
| X        | H  | All Outputs Are Low   |

H = High Voltage Level, L = Low Voltage Level, X = Don't Care,  
 ↑ = Transition from Low to High Level, ↓ = Transition from High to Low.

## Logic Diagram



# CD54HC4024, CD74HC4024, CD54HCT4024, CD74HCT4024

## Absolute Maximum Ratings

|                                                        |             |
|--------------------------------------------------------|-------------|
| DC Supply Voltage, $V_{CC}$                            | -0.5V to 7V |
| DC Input Diode Current, $I_{IK}$                       |             |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$             | $\pm 20mA$  |
| DC Output Diode Current, $I_{OK}$                      |             |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$             | $\pm 20mA$  |
| DC Output Source or Sink Current per Output Pin, $I_O$ |             |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$             | $\pm 25mA$  |
| DC $V_{CC}$ or Ground Current, $I_{CC}$                | $\pm 50mA$  |

## Thermal Information

|                                          |                                    |
|------------------------------------------|------------------------------------|
| Thermal Resistance (Typical, Note 1)     | $\theta_{JA}$ ( $^{\circ}C/W$ )    |
| E (PDIP) Package                         | 80                                 |
| M (SOIC) Package                         | 86                                 |
| PW (TSSOP) Package                       | 113                                |
| (Maximum Junction Temperature)           | 150 $^{\circ}C$                    |
| Maximum Storage Temperature Range        | -65 $^{\circ}C$ to 150 $^{\circ}C$ |
| Maximum Lead Temperature (Soldering 10s) | 300 $^{\circ}C$                    |
| (SOIC - Lead Tips Only)                  |                                    |

## Operating Conditions

|                                           |                                    |
|-------------------------------------------|------------------------------------|
| Temperature Range ( $T_A$ )               | -55 $^{\circ}C$ to 125 $^{\circ}C$ |
| Supply Voltage Range, $V_{CC}$            |                                    |
| HC Types                                  | .2V to 6V                          |
| HCT Types                                 | .4.5V to 5.5V                      |
| DC Input or Output Voltage, $V_I$ , $V_O$ | 0V to $V_{CC}$                     |
| Input Rise and Fall Time                  |                                    |
| 2V                                        | 1000ns (Max)                       |
| 4.5V                                      | 500ns (Max)                        |
| 6V                                        | 400ns (Max)                        |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL          | TEST CONDITIONS                    |                     | V <sub>CC</sub> (V)    | 25°C |      |      | -40°C TO 85°C |      | -55°C TO 125°C |      | UNITS |     |    |
|-----------------------------------------|-----------------|------------------------------------|---------------------|------------------------|------|------|------|---------------|------|----------------|------|-------|-----|----|
|                                         |                 | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) |                        | MIN  | TYP  | MAX  | MIN           | MAX  | MIN            | MAX  |       |     |    |
| HC TYPES                                |                 |                                    |                     |                        |      |      |      |               |      |                |      |       |     |    |
| High Level Input Voltage                | V <sub>IH</sub> | -                                  | -                   | 2                      | 1.5  | -    | -    | 1.5           | -    | 1.5            | -    | V     |     |    |
|                                         |                 |                                    |                     | 4.5                    | 3.15 | -    | -    | 3.15          | -    | 3.15           | -    | V     |     |    |
|                                         |                 |                                    |                     | 6                      | 4.2  | -    | -    | 4.2           | -    | 4.2            | -    | V     |     |    |
| Low Level Input Voltage                 | V <sub>IL</sub> | -                                  | -                   | 2                      | -    | -    | 0.5  | -             | 0.5  | -              | 0.5  | V     |     |    |
|                                         |                 |                                    |                     | 4.5                    | -    | -    | 1.35 | -             | 1.35 | -              | 1.35 | V     |     |    |
|                                         |                 |                                    |                     | 6                      | -    | -    | 1.8  | -             | 1.8  | -              | 1.8  | V     |     |    |
| High Level Output Voltage<br>CMOS Loads | V <sub>OH</sub> | V <sub>IH</sub> or V <sub>IL</sub> | -0.02               | 2                      | 1.9  | -    | -    | 1.9           | -    | 1.9            | -    | V     |     |    |
|                                         |                 |                                    | -0.02               | 4.5                    | 4.4  | -    | -    | 4.4           | -    | 4.4            | -    | V     |     |    |
|                                         |                 |                                    | -0.02               | 6                      | 5.9  | -    | -    | 5.9           | -    | 5.9            | -    | V     |     |    |
| -                                       |                 |                                    | -                   | -                      | -    | -    | -    | -             | -    | -              | V    |       |     |    |
| -4                                      |                 |                                    | 4.5                 | 3.98                   | -    | -    | 3.84 | -             | 3.7  | -              | V    |       |     |    |
| -5.2                                    |                 |                                    | 6                   | 5.48                   | -    | -    | 5.34 | -             | 5.2  | -              | V    |       |     |    |
| High Level Output Voltage<br>TTL Loads  | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 2                      | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |     |    |
|                                         |                 |                                    | 0.02                | 4.5                    | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |     |    |
|                                         |                 |                                    | 0.02                | 6                      | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |     |    |
| -                                       |                 |                                    | -                   | -                      | -    | -    | -    | -             | -    | -              | V    |       |     |    |
| 4                                       |                 |                                    | 4.5                 | -                      | -    | 0.26 | -    | 0.33          | -    | 0.4            | V    |       |     |    |
| 5.2                                     |                 |                                    | 6                   | -                      | -    | 0.26 | -    | 0.33          | -    | 0.4            | V    |       |     |    |
| Low Level Output Voltage<br>CMOS Loads  | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 2                      | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |     |    |
|                                         |                 |                                    | 0.02                | 4.5                    | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |     |    |
|                                         |                 |                                    | 0.02                | 6                      | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |     |    |
| -                                       |                 |                                    | -                   | -                      | -    | -    | -    | -             | -    | -              | V    |       |     |    |
| 4                                       |                 |                                    | 4.5                 | -                      | -    | 0.26 | -    | 0.33          | -    | 0.4            | V    |       |     |    |
| 5.2                                     |                 |                                    | 6                   | -                      | -    | 0.26 | -    | 0.33          | -    | 0.4            | V    |       |     |    |
| Low Level Output Voltage<br>TTL Loads   | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | -                   | -                      | -    | -    | -    | -             | -    | -              | -    | V     |     |    |
|                                         |                 |                                    | 4                   | 4.5                    | -    | -    | 0.26 | -             | 0.33 | -              | 0.4  | V     |     |    |
|                                         |                 |                                    | 5.2                 | 6                      | -    | -    | 0.26 | -             | 0.33 | -              | 0.4  | V     |     |    |
| Input Leakage Current                   |                 |                                    | I <sub>I</sub>      | V <sub>CC</sub> or GND | -    | 6    | -    | -             | ±0.1 | -              | ±1   | -     | ±1  | μA |
| Quiescent Device Current                |                 |                                    | I <sub>CC</sub>     | V <sub>CC</sub> or GND | 0    | 6    | -    | -             | 8    | -              | 80   | -     | 160 | μA |

**CD54HC4024, CD74HC4024, CD54HCT4024, CD74HCT4024**

**DC Electrical Specifications (Continued)**

| PARAMETER                                                      | SYMBOL                    | TEST CONDITIONS                    |                     | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |     | UNITS |
|----------------------------------------------------------------|---------------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
|                                                                |                           | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX |       |
| HCT TYPES                                                      |                           |                                    |                     |                     |      |     |      |               |      |                |     |       |
| High Level Input Voltage                                       | V <sub>IH</sub>           | -                                  | -                   | 4.5 to 5.5          | 2    | -   | -    | 2             | -    | 2              | -   | V     |
| Low Level Input Voltage                                        | V <sub>IL</sub>           | -                                  | -                   | 4.5 to 5.5          | -    | -   | 0.8  | -             | 0.8  | -              | 0.8 | V     |
| High Level Output Voltage<br>CMOS Loads                        | V <sub>OH</sub>           | V <sub>IH</sub> or V <sub>IL</sub> | -0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -   | V     |
| High Level Output Voltage<br>TTL Loads                         |                           |                                    | -4                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -   | V     |
| Low Level Output Voltage<br>CMOS Loads                         | V <sub>OL</sub>           | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1 | V     |
| Low Level Output Voltage<br>TTL Loads                          |                           |                                    | 4                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4 | V     |
| Input Leakage Current                                          | I <sub>I</sub>            | V <sub>CC</sub> and GND            | 0                   | 5.5                 | -    | -   | ±0.1 | -             | ±1   | -              | ±1  | μA    |
| Quiescent Device Current                                       | I <sub>CC</sub>           | V <sub>CC</sub> or GND             | 0                   | 5.5                 | -    | -   | 8    | -             | 80   | -              | 160 | μA    |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI <sub>CC</sub> (Note 2) | V <sub>CC</sub> -2.1               | -                   | 4.5 to 5.5          | -    | 100 | 360  | -             | 450  | -              | 490 | μA    |

NOTE:

2. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

| INPUT  | UNIT LOADS |
|--------|------------|
| CP, MR | 0.5        |

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

**Prerequisite for Switching Specifications**

| PARAMETER                     | SYMBOL           | V <sub>CC</sub> (V) | 25°C |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|-------------------------------|------------------|---------------------|------|-----|---------------|-----|----------------|-----|-------|
|                               |                  |                     | MIN  | MAX | MIN           | MAX | MIN            | MAX |       |
| HC TYPES                      |                  |                     |      |     |               |     |                |     |       |
| Maximum Input Pulse Frequency | f <sub>MAX</sub> | 2                   | 6    | -   | 5             | -   | 4              | -   | MHz   |
|                               |                  | 4.5                 | 30   | -   | 24            | -   | 20             | -   | MHz   |
|                               |                  | 6                   | 35   | -   | 29            | -   | 24             | -   | MHz   |
| Input Pulse Width             | t <sub>W</sub>   | 2                   | 80   | -   | 100           | -   | 120            | -   | ns    |
|                               |                  | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
|                               |                  | 6                   | 14   | -   | 17            | -   | 20             | -   | ns    |
| Reset Removal Time            | t <sub>REM</sub> | 2                   | 50   | -   | 65            | -   | 75             | -   | ns    |
|                               |                  | 4.5                 | 10   | -   | 13            | -   | 15             | -   | ns    |
|                               |                  | 6                   | 9    | -   | 11            | -   | 13             | -   | ns    |

**CD54HC4024, CD74HC4024, CD54HCT4024, CD74HCT4024**

**Prerequisite for Switching Specifications (Continued)**

| PARAMETER                     | SYMBOL           | V <sub>CC</sub> (V) | 25°C |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|-------------------------------|------------------|---------------------|------|-----|---------------|-----|----------------|-----|-------|
|                               |                  |                     | MIN  | MAX | MIN           | MAX | MIN            | MAX |       |
| Reset Pulse Width             | t <sub>W</sub>   | 2                   | 80   | -   | 100           | -   | 120            | -   | ns    |
|                               |                  | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
|                               |                  | 6                   | 14   | -   | 17            | -   | 20             | -   | ns    |
| HCT TYPES                     |                  |                     |      |     |               |     |                |     |       |
| Maximum Input Pulse Frequency | f <sub>MAX</sub> | 4.5                 | 25   | -   | 20            | -   | 16             | -   | MHz   |
| Input Pulse Width             | t <sub>W</sub>   | 4.5                 | 20   | -   | 25            | -   | 30             | -   | ns    |
| Reset Recovery Time           | t <sub>REC</sub> | 4.5                 | 10   | -   | 13            | -   | 15             | -   | ns    |
| Reset Pulse Width             | t <sub>W</sub>   | 4.5                 | 20   | -   | 25            | -   | 30             | -   | ns    |

**Switching Specifications** Input t<sub>p</sub>, t<sub>f</sub> = 6ns

| PARAMETER                                                    | SYMBOL                                 | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|--------------------------------------------------------------|----------------------------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                                              |                                        |                       |                     | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| HC TYPES                                                     |                                        |                       |                     |      |     |     |               |     |                |     |       |
| Propagation Delay Time<br>(Figure 1)<br><br>CP to Q1' Output | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 140 | -             | 175 | -              | 210 | ns    |
|                                                              |                                        |                       | 4.5                 | -    | -   | 28  | -             | 35  | -              | 42  | ns    |
|                                                              |                                        | C <sub>L</sub> = 15pF | 5                   | -    | 11  | -   | -             | -   | -              | -   | ns    |
|                                                              |                                        | C <sub>L</sub> = 50pF | 6                   | -    | -   | 24  | -             | 30  | -              | 36  | ns    |
| Q <sub>n</sub> to Q <sub>n</sub> + 1                         | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 75  | -             | 95  | -              | 110 | ns    |
|                                                              |                                        |                       | 4.5                 | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
|                                                              |                                        | C <sub>L</sub> = 15pF | 5                   | -    | 6   | -   | -             | -   | -              | -   | ns    |
|                                                              |                                        | C <sub>L</sub> = 50pF | 6                   | -    | -   | 13  | -             | 13  | -              | 19  | ns    |
| MR to Q <sub>n</sub>                                         | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 170 | -             | 215 | -              | 255 | ns    |
|                                                              |                                        |                       | 4.5                 | -    | -   | 34  | -             | 43  | -              | 51  | ns    |
|                                                              |                                        |                       | 5                   | -    | 14  | -   | -             | -   | -              | -   | ns    |
|                                                              |                                        |                       | 6                   | -    | -   | 29  | -             | 27  | -              | 43  | ns    |
| Output Transition Time<br>(Figure 1)                         | t <sub>TLH</sub> , t <sub>THL</sub>    | C <sub>L</sub> = 50pF | 2                   | -    | -   | 75  | -             | 95  | -              | 110 | ns    |
|                                                              |                                        |                       | 4.5                 | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
|                                                              |                                        |                       | 6                   | -    | -   | 13  | -             | 16  | -              | 19  | ns    |
| Input Capacitance                                            | C <sub>IN</sub>                        | C <sub>L</sub> = 50pF | -                   | -    | -   | 10  | -             | 10  | -              | 10  | pF    |
| Power Dissipation Capacitance<br>(Notes 3, 4)                | C <sub>PD</sub>                        | C <sub>L</sub> = 15pF | 5                   | -    | 30  | -   | -             | -   | -              | -   | pF    |
| HCT TYPES                                                    |                                        |                       |                     |      |     |     |               |     |                |     |       |
| Propagation Delay Time<br>(Figure 2)<br><br>CP to Q1' Output | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 40  | -             | 50  | -              | 60  | ns    |
|                                                              |                                        | C <sub>L</sub> = 15pF | 5                   | -    | 17  | -   | -             | -   | -              | -   | ns    |
| Q <sub>n</sub> to Q <sub>n</sub> + 1                         | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
|                                                              |                                        | C <sub>L</sub> = 15pF | 5                   | -    | 6   | -   | -             | -   | -              | -   | ns    |
| MR to Q <sub>n</sub>                                         | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 40  | -             | 50  | -              | 60  | ns    |
|                                                              |                                        | C <sub>L</sub> = 15pF | 5                   | -    | 17  | -   | -             | -   | -              | -   | ns    |

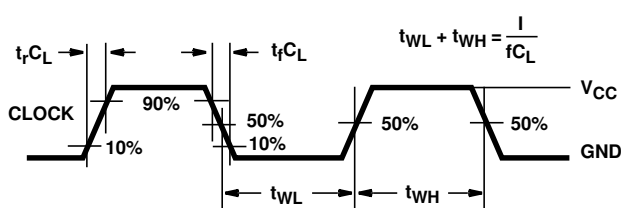
**Switching Specifications** Input  $t_r, t_f = 6\text{ns}$  (Continued)

| PARAMETER                                     | SYMBOL             | TEST CONDITIONS     | $V_{CC}$<br>(V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|-----------------------------------------------|--------------------|---------------------|-----------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                               |                    |                     |                 | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| Output Transition                             | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
| Input Capacitance                             | $C_{IN}$           | $C_L = 15\text{pF}$ | -               | -    | -   | 10  | -             | 10  | -              | 10  | pF    |
| Power Dissipation Capacitance<br>(Notes 3, 4) | $C_{PD}$           | $C_L = 15\text{pF}$ | 5               | -    | 30  | -   | -             | -   | -              | -   | pF    |

NOTES:

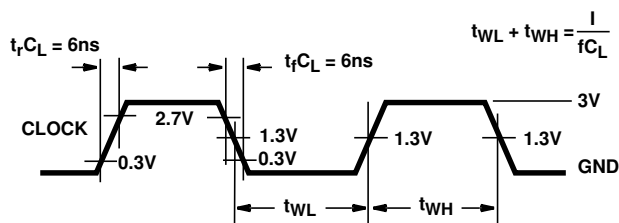
- $C_{PD}$  is used to determine the dynamic power consumption, per package.
- $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_i / M)$  where:  $M = 2^1, 2^2, 2^3, 2^4, 2^5, 2^6, 2^7$   $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

**Test Circuits and Waveforms**



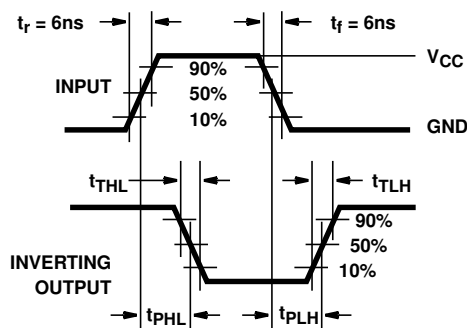
NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**

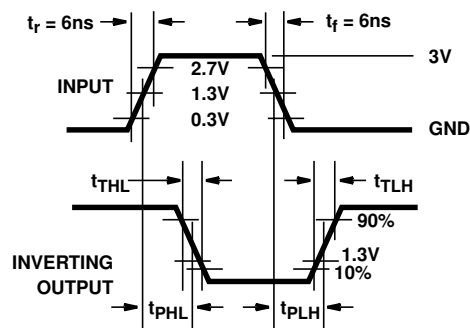


NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**



**FIGURE 3. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**



**FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)     | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD54HC4024F      | ACTIVE        | CDIP         | J                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | CD54HC4024F             | <a href="#">Samples</a> |
| CD54HCT4024F3A   | ACTIVE        | CDIP         | J                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | CD54HCT4024F3A          | <a href="#">Samples</a> |
| CD74HC4024E      | ACTIVE        | PDIP         | N                  | 14   | 25             | RoHS & Green        | NIPDAU                               | N / A for Pkg Type   | -55 to 125   | CD74HC4024E             | <a href="#">Samples</a> |
| CD74HC4024M      | ACTIVE        | SOIC         | D                  | 14   | 50             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | HC4024M                 | <a href="#">Samples</a> |
| CD74HC4024M96    | ACTIVE        | SOIC         | D                  | 14   | 2500           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | HC4024M                 | <a href="#">Samples</a> |
| CD74HC4024MG4    | ACTIVE        | SOIC         | D                  | 14   | 50             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | HC4024M                 | <a href="#">Samples</a> |
| CD74HC4024MT     | ACTIVE        | SOIC         | D                  | 14   | 250            | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | HC4024M                 | <a href="#">Samples</a> |
| CD74HC4024PW     | ACTIVE        | TSSOP        | PW                 | 14   | 90             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | HJ4024                  | <a href="#">Samples</a> |
| CD74HC4024PWR    | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | HJ4024                  | <a href="#">Samples</a> |
| CD74HCT4024E     | ACTIVE        | PDIP         | N                  | 14   | 25             | RoHS &<br>Non-Green | NIPDAU                               | N / A for Pkg Type   | -55 to 125   | CD74HCT4024E            | <a href="#">Samples</a> |
| CD74HCT4024EE4   | ACTIVE        | PDIP         | N                  | 14   | 25             | RoHS &<br>Non-Green | NIPDAU                               | N / A for Pkg Type   | -55 to 125   | CD74HCT4024E            | <a href="#">Samples</a> |
| CD74HCT4024M     | ACTIVE        | SOIC         | D                  | 14   | 50             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | HCT4024M                | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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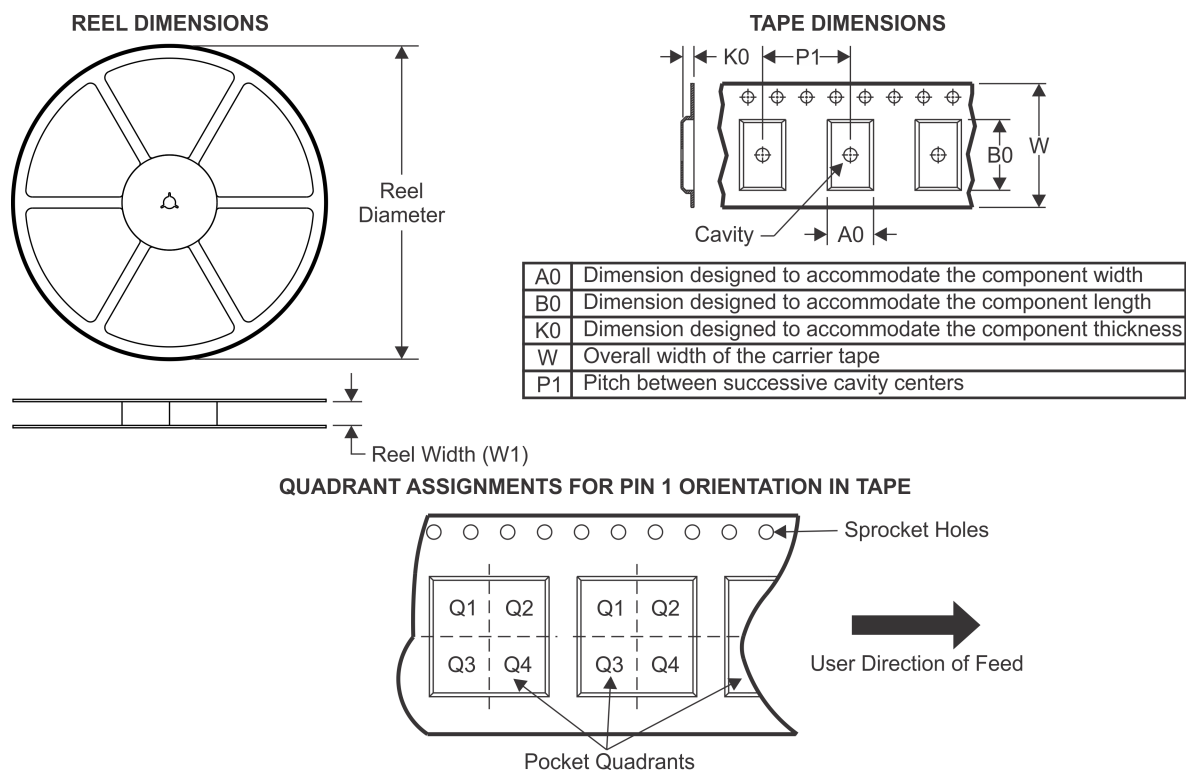
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC4024, CD54HCT4024, CD74HC4024, CD74HCT4024 :**

- Catalog : [CD74HC4024](#), [CD74HCT4024](#)
- Military : [CD54HC4024](#), [CD54HCT4024](#)

**NOTE: Qualified Version Definitions:**

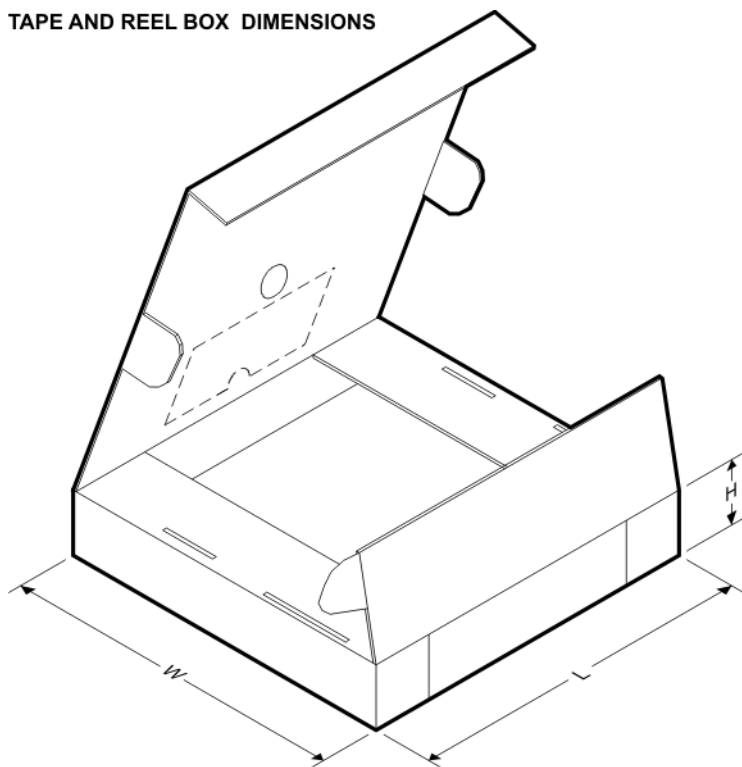
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC4024M96 | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HC4024MT  | SOIC         | D               | 14   | 250  | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HC4024PWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

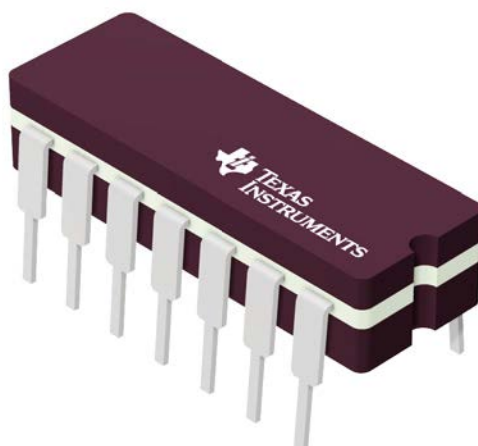
| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC4024M96 | SOIC         | D               | 14   | 2500 | 853.0       | 449.0      | 35.0        |
| CD74HC4024MT  | SOIC         | D               | 14   | 250  | 210.0       | 185.0      | 35.0        |
| CD74HC4024PWR | TSSOP        | PW              | 14   | 2000 | 853.0       | 449.0      | 35.0        |

**J 14**

## GENERIC PACKAGE VIEW

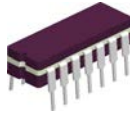
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE

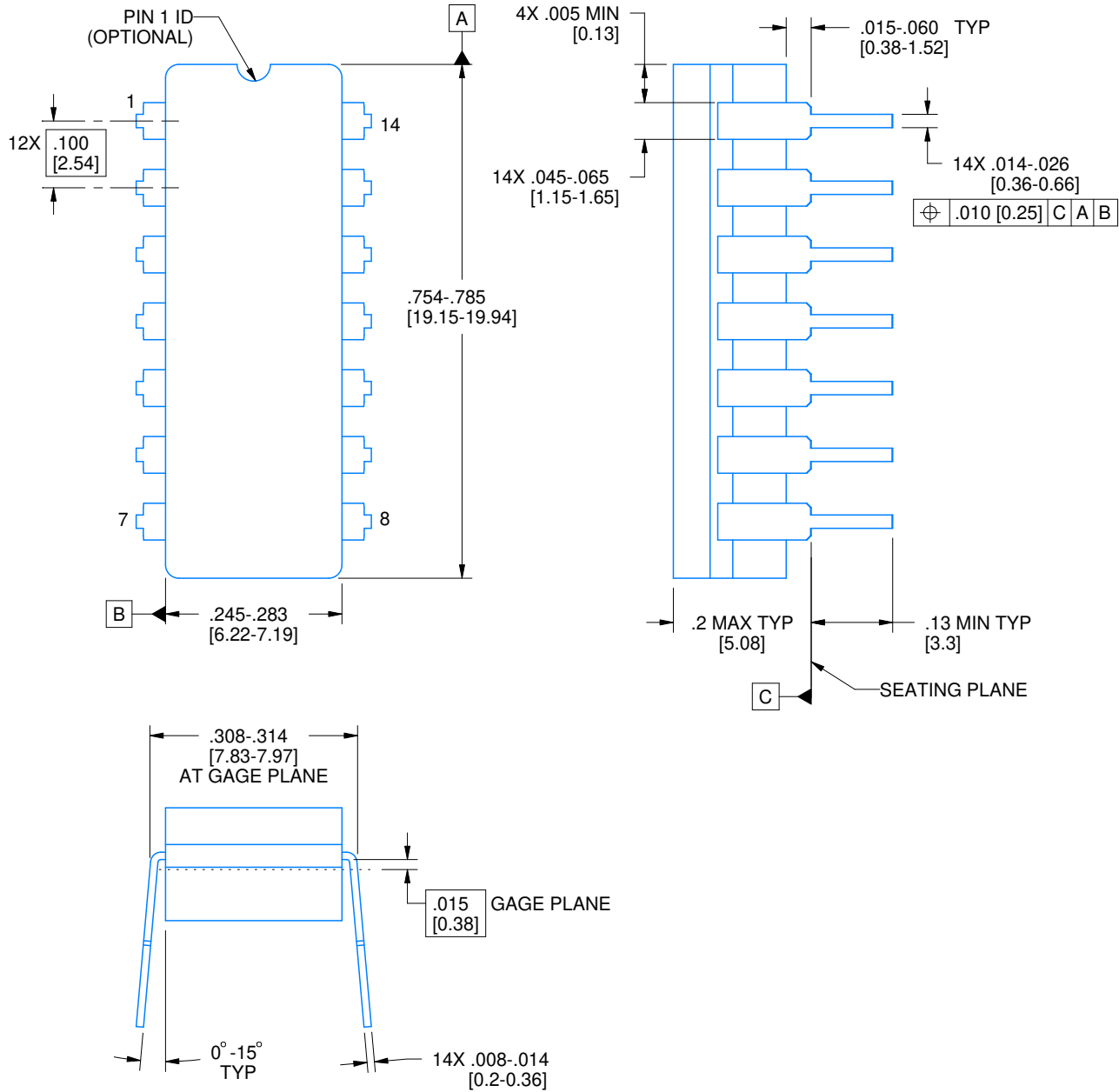


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

**J0014A****PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

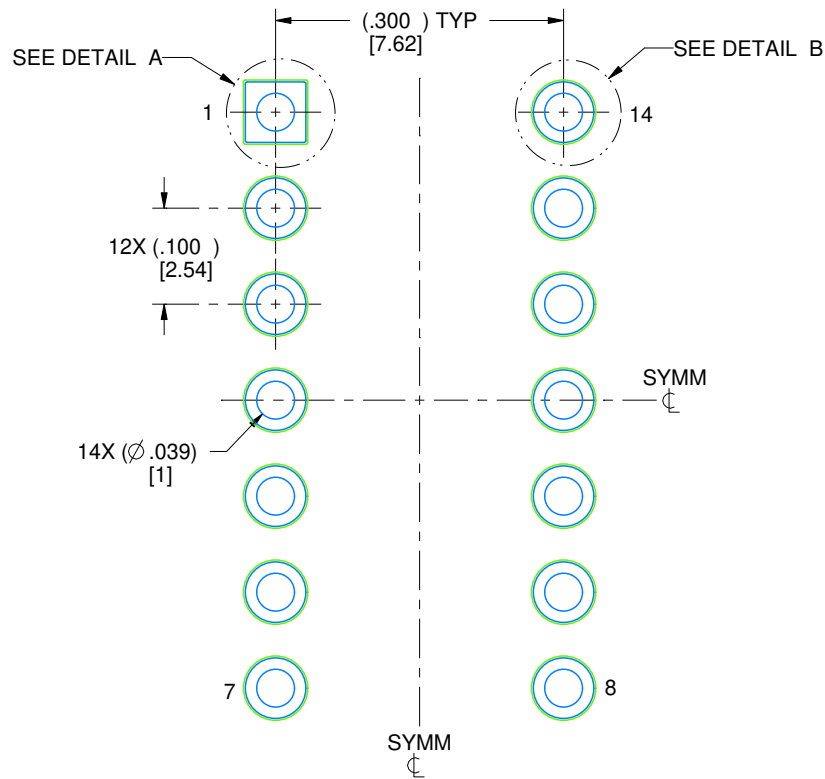
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

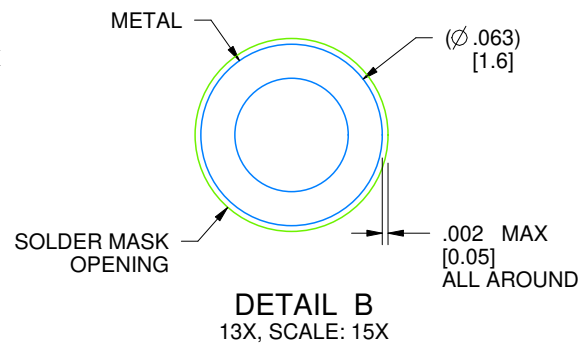
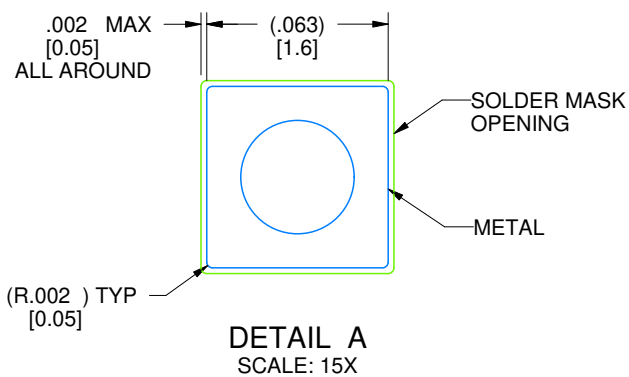
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



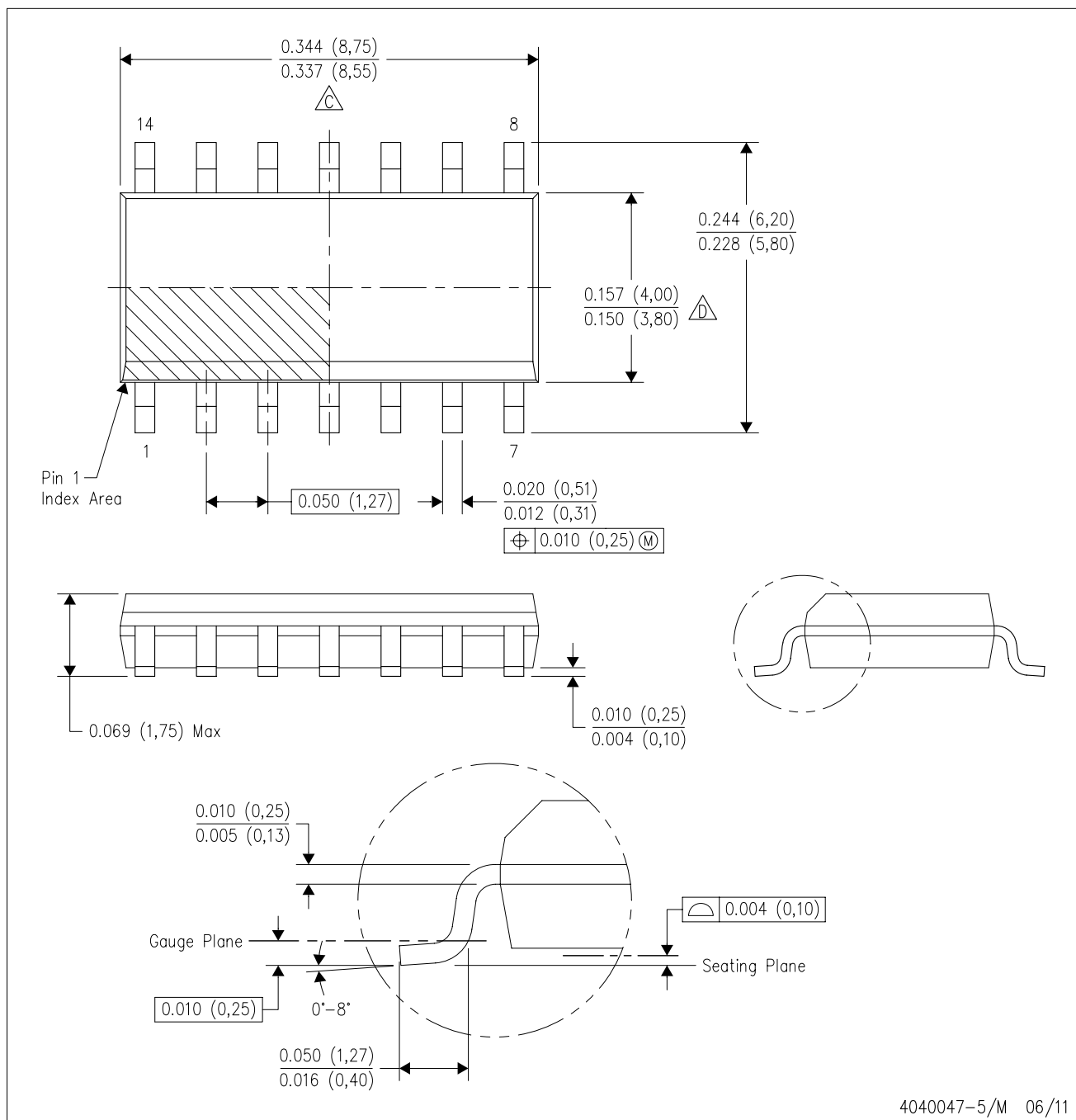
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

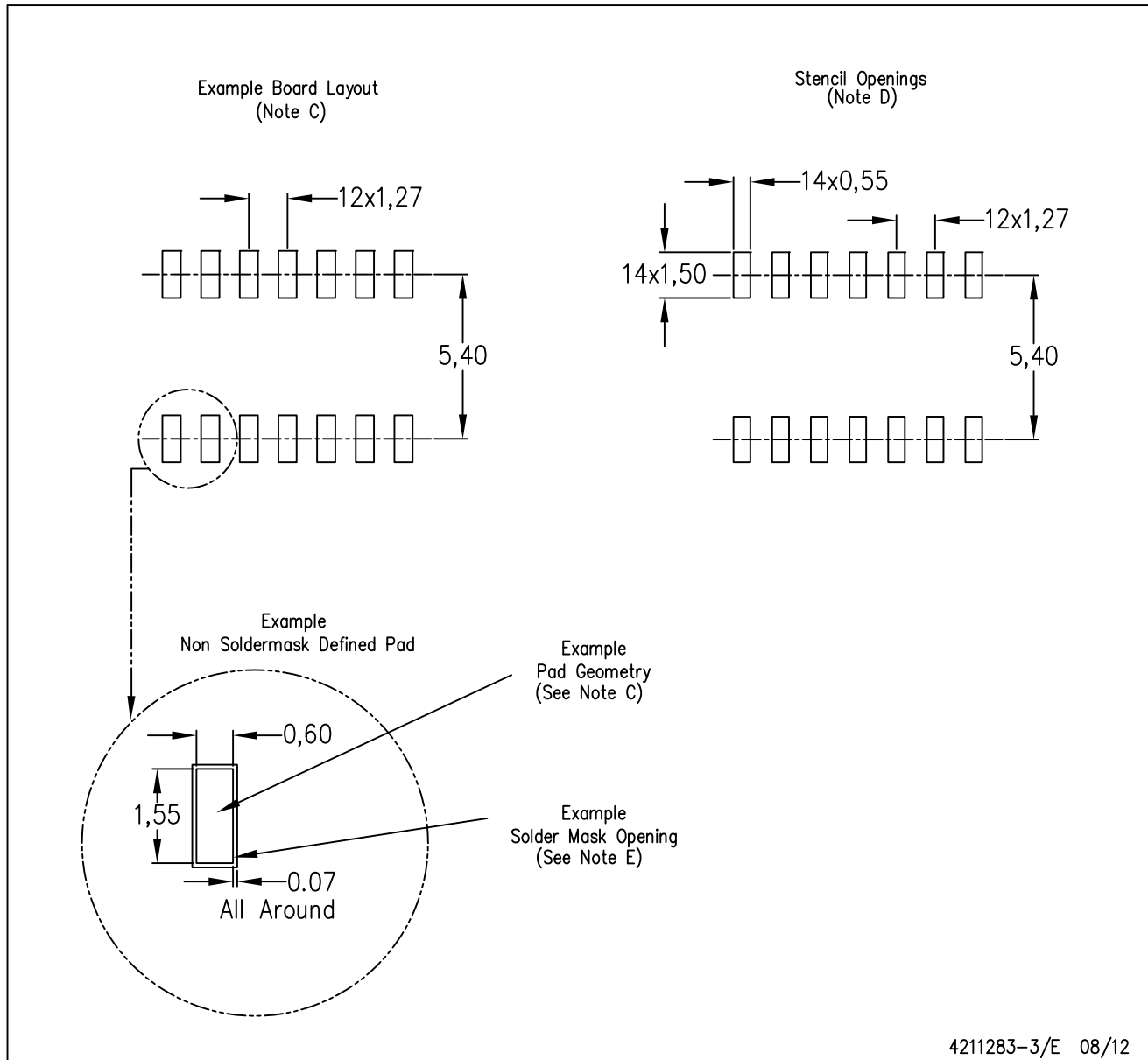
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

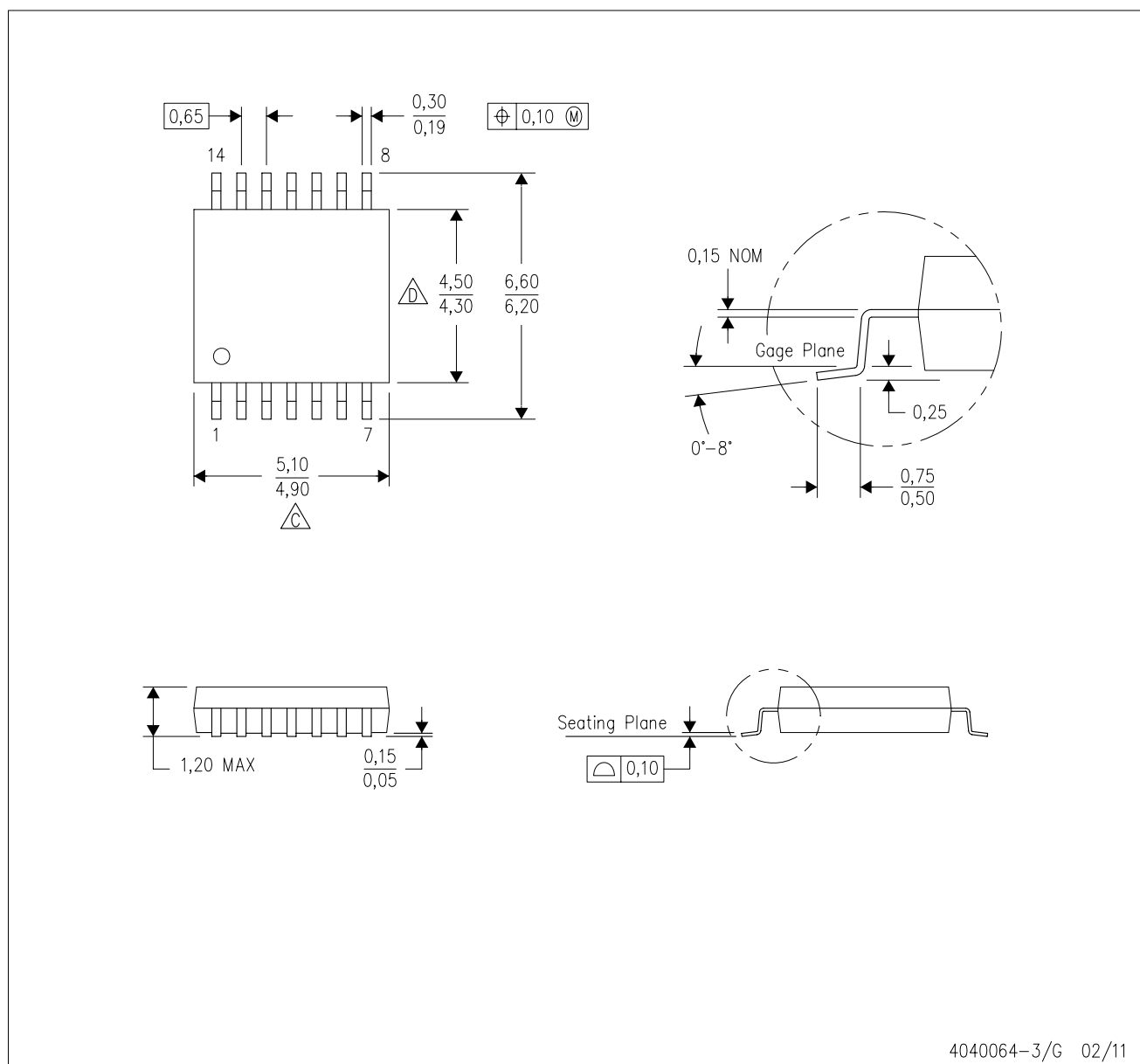
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

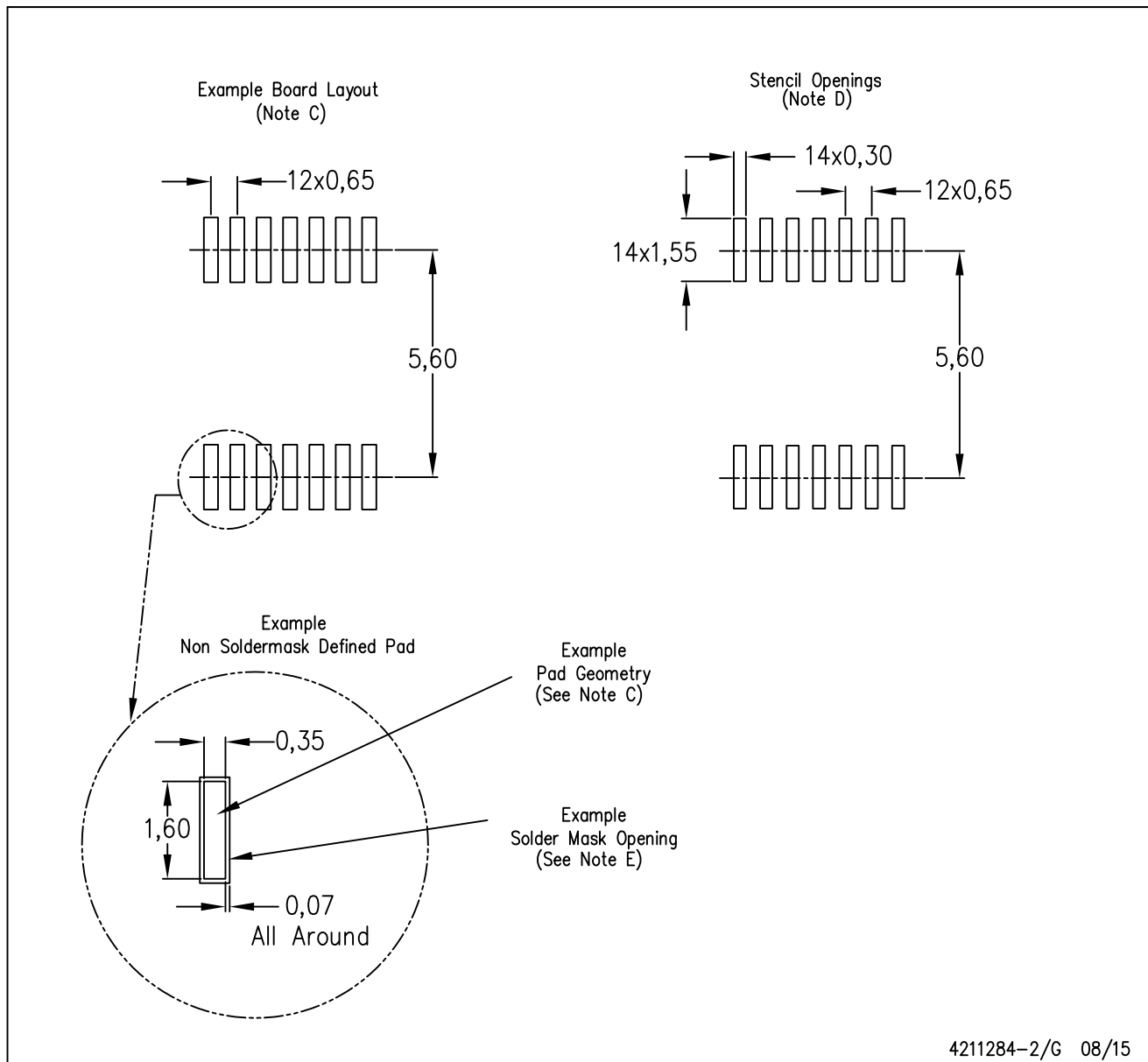
PLASTIC SMALL OUTLINE



4040064-3/G 02/11

PW (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



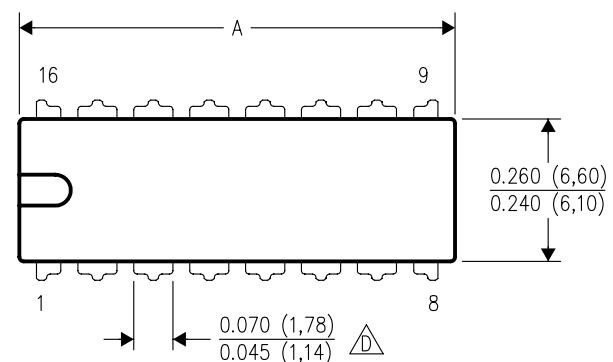
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

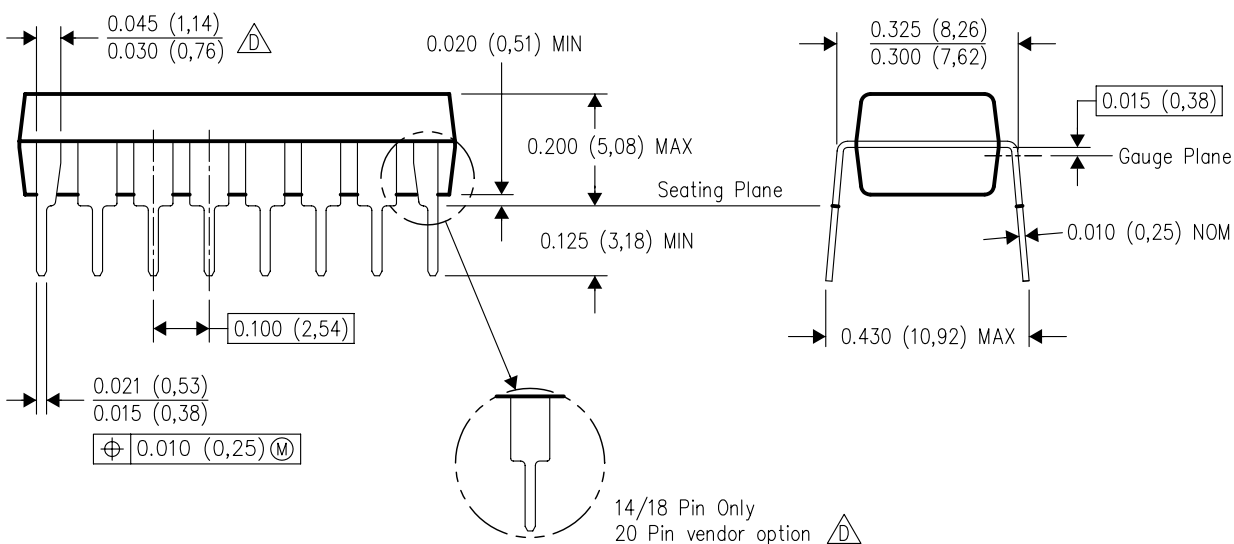
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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