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1 key Touch Pad Detector IC

Outline

- The TTP223E-BA6 TonTouch™ is a touch pad detector IC which offers 1 touch key. Stable sensing method can cover diversity conditions. The touching detection IC is designed for replacing traditional direct button key with diverse pad size. Low power consumption and wide operating voltage are the contact key features for DC or AC application.

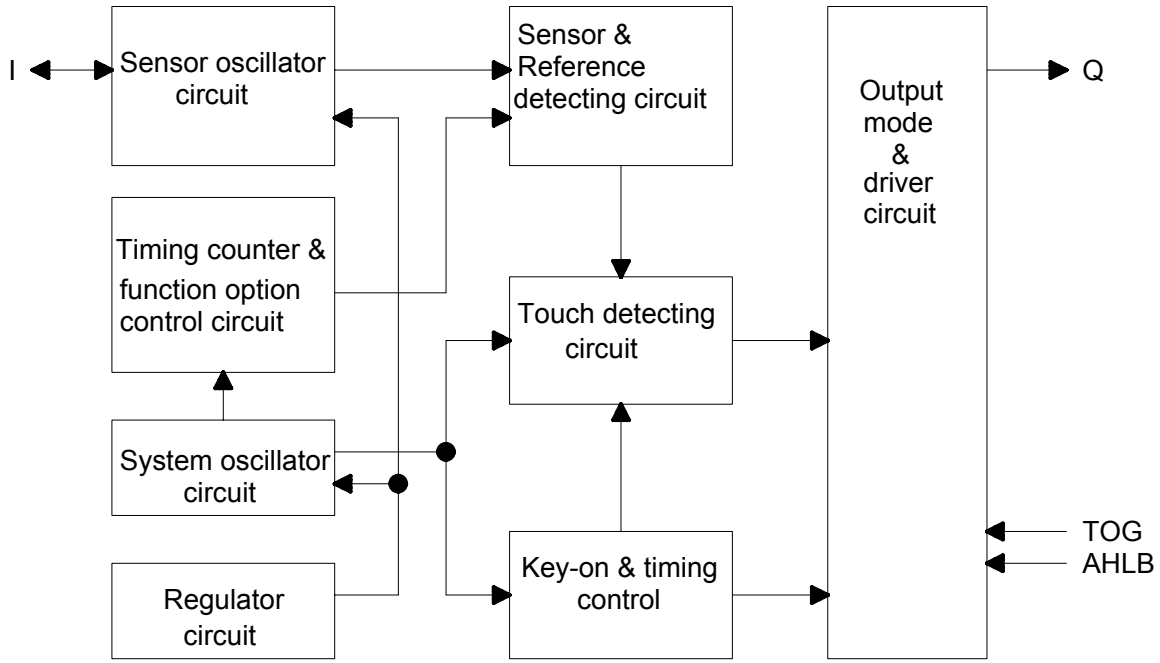
Characteristic

- Operating voltage 2.0V ~ 5.5V
- Operating current, @VDD=3V no load
  At low power mode typical 2.0uA, maximum 4.0uA
- The response time max about 220mS at low power mode @VDD=3V
- Sensitivity can adjust by the capacitance（1~50pF）outside
- Stable touching detection of human body for replacing traditional direct switch key
- Provides Low Power mode
- Provides direct output or toggle output selection by pin option (TOG pin)
- Q pin is CMOS output can be selected active high or active low by pin option (AHLB pin)
- After power-on have about 0.5sec stable-time, during the time do not touch the key pad, and the function is disabled
- Auto calibration for life
  The re-calibration period is about 1 sec within 8 sec after power-on. When key has been touched within 8 sec or key has not been touched more than 8 sec after power-on, then the re-calibration period change to 4 sec

Applications

- Wide consumer products
- Button key replacement

Block diagram



Pin Description

Pin NO	Pin Name	Type	Pin Description
1	Q	O	CMOS output pin
2	VSS	P	Negative power supply, ground
3	I	I/O	Input sensor port
4	AHLB	I-PL	Output Q active high or low selection, 0(Default)=>Active high; 1=>Active low
5	VDD	P	Positive power supply
6	TOG	I-PL	Output type option pin, 0(Default)=>Direct output; 1=>Toggle output

Pin Type

- I CMOS input only
- O CMOS push-pull output
- I／O CMOS I／O
- P Power／Ground
- I-PH CMOS input and pull-high resister
- I-PL CMOS input and pull-low resister
- OD Open drain output, have no Diode protective circuit

Electrical Characteristics

- **Absolute maximum ratings**

Parameter	Symbol	Conditions	Rating	Unit
Operating Temperature	T_{OP}	—	-40～+85	℃
Storage Temperature	T_{STG}	—	-50～+125	℃
Supply Voltage	VDD	Ta=25°C	VSS-0.3～VSS+5.5	V
Input Voltage	V_{IN}	Ta=25°C	VSS-0.3～VDD+0.3	V
Human Body Mode	ESD	—	5	KV
Note：VSS symbolizes for system ground				

- **DC / AC characteristics：（Test condition at room temperature = 25 ℃）**

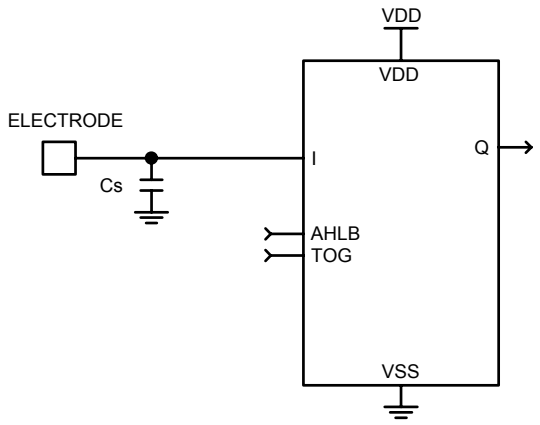
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	VDD		2.0	3	5.5	V
Operating Current	I_{OPL}	VDD=3V, At low power mode		2.0	4.0	uA
	I_{OPF}	VDD=3V, At fast mode		5.0	10.0	uA
Input Ports	V_{IL}	Input Low Voltage	0		0.2	VDD
Input Ports	V_{IH}	Input High Voltage	0.8		1.0	VDD
Output Port Sink Current	I_{OL}	VDD=3V, V_{OL}=0.6V		8		mA
Output Port Source Current	I_{OH}	VDD=3V, V_{OH}=2.4V		-4		mA
Input Pin Pull-low Resistor	R_{PL}	VDD=3V (TOG, AHLB)		25K		ohm
Output Response Time	T_R	VDD=3V、At fast mode			60	mS
		VDD=3V、At low power mode			220	

Function Description

Ⅰ. Sensitivity adjustment

The total loading of electrode size and capacitance of connecting line on PCB can affect the sensitivity. So the sensitivity adjustment must according to the practical application on PCB. The TTP223E-BA6 offers some methods for adjusting the sensitivity outside.

1. by the electrode size
   Under other conditions are fixed. Using a larger electrode size can increase sensitivity. Otherwise it can decrease sensitivity. But the electrode size must use in the effective scope.
2. by the panel thickness
   Under other conditions are fixed. Using a thinner panel can increase sensitivity. Otherwise it can decrease sensitivity. But the panel thickness must be below the maximum value.
3. by the value of Cs（please see the down figure）
   Under other conditions are fixed. When do not use the Cs to VSS, the sensitivity is most sensitive. When adding the value of Cs will reduce sensitivity in the useful range （1≦Cs≦50pF）.



Ⅱ. Output mode（By TOG、AHLB pin option）

TOG pin： Direct output or toggle output selection.

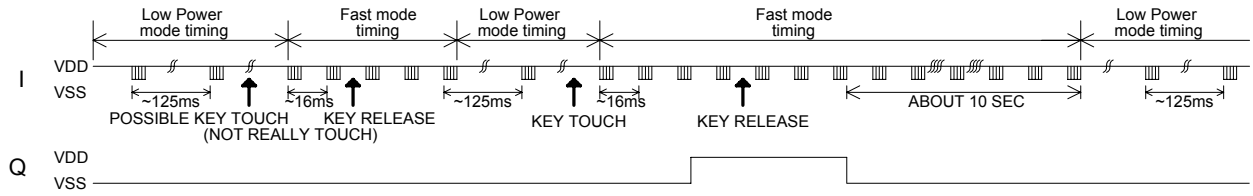
AHLB pin： Output Q active high or active low selection.

Pin Q（CMOS output）option features：

TOG	AHLB	Pin Q option features
0	0	Direct output, CMOS active high
0	1	Direct output, CMOS active low
1	0	Toggle output, power on state = 0
1	1	Toggle output, power on state = 1

Ⅲ. Low power mode

The TTP223E-BA6 is Low Power mode, it will be saving power. When detecting key touch, it will switch to Fast mode. Until the key touch is released and will keep a time about 10 sec. Then it returns to Low Power mode.



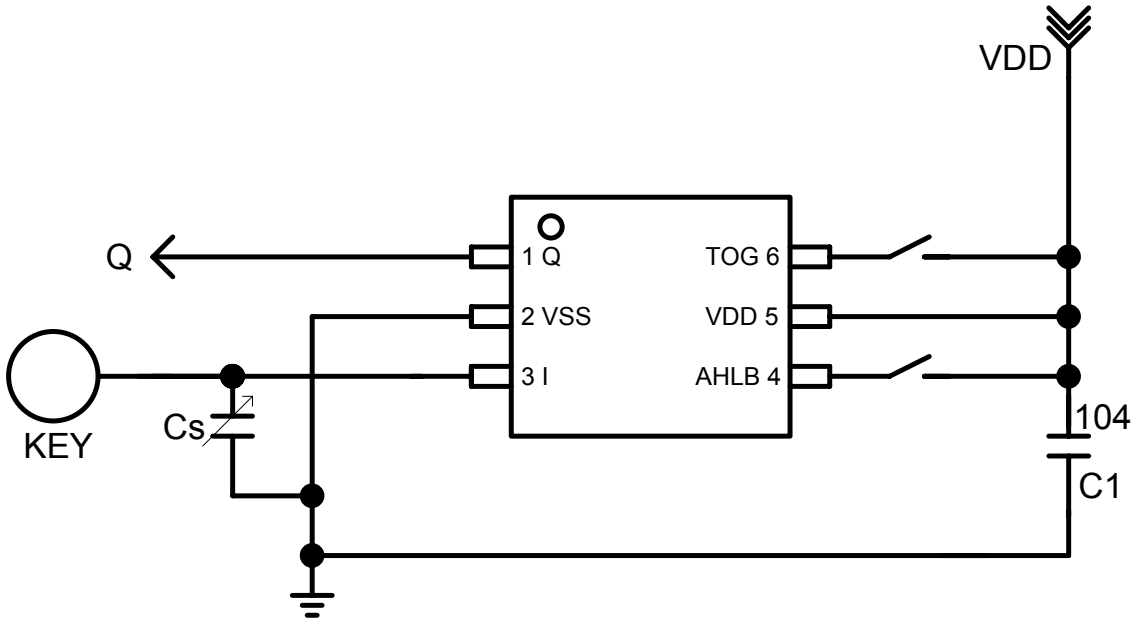
Low Power Mode

Ⅳ. Option pin

For power saving concern and package bonding option consideration, all the feature option pins with latch type design and initial states are 0 or 1 as power on. If those pins are forced to VDD or VSS, the states will be changed to 1 or 0 without any current leakage to conflict the power saving issue.

Feature option pins	Initial state by Power on
AHLB	0
TOG	0

Application circuit

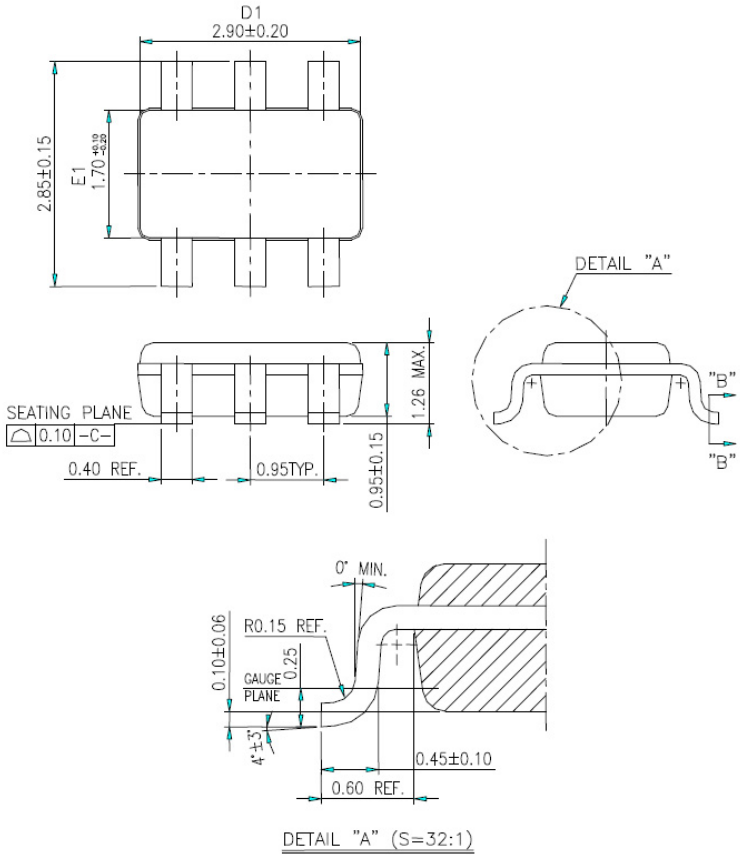


P.S.：

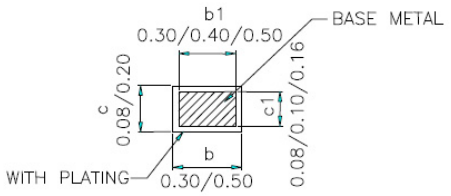
1. On PCB, the length of lines from touch pad to IC pin shorter is better.
   And the lines do not parallel and cross with other lines.
2. The power supply must be stable. If the supply voltage drift or shift quickly, maybe causing sensitivity anomalies or false detections.
3. The material of panel covering on the PCB can not include the metal or the electric element. The paints on the surfaces are the same.
4. The C1 capacitor must be used between VDD and VSS; and should be routed with very short tracks to the device's VDD and VSS pins (TTP223E-BA6).
5. The capacitance Cs can be used to adjust the sensitivity. The value of Cs use smaller, then the sensitivity will be better. The sensitivity adjustment must according to the practical application on PCB. The range of Cs value are 1~50pF.
6. The sensitivity adjustment capacitors（Cs）must use smaller temperature coefficient and more stable capacitors. Such are X7R, NPO for example. So for touch application, recommend to use NPO capacitor, for reducing that the temperature varies to affect sensitivity.

Package outline

Package Type: SOT23-6L



DETAIL "A" (S=32:1)



SECTION "B"–"B"

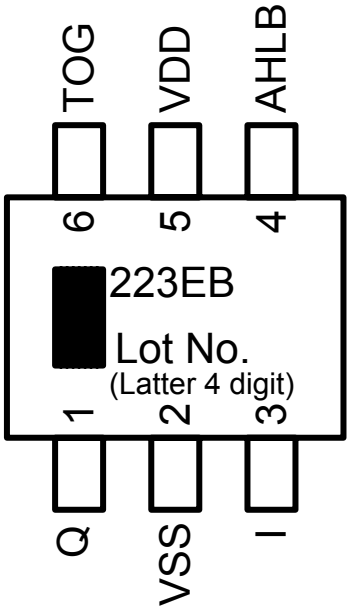
NOTES:

1. DIMENSION D1 & E1 DOES NOT INCLUDE MOLD PROTRUSION.
2. COPLANARITY OF ALL LEADS SHALL BE (BEFORE TEST) 0.1 MAX. FROM THE SEATING PLANE. UNLESS OTHERWISE SPECIFIED.
3. GENERAL PHYSICAL OUTLINE SPEC IS REFER TO TMC'S FINAL VISUAL INSPECTION SPEC UNLESS OTHERWISE SPECIFIED.

Package configuration

TTP223E-BA6

Package Type SOT23-6L



Ordering Information

TTP223E-BA6

Package Type	Chip Type	Wafer Type
TTP223E-BA6	No support	No support

REVISE HISTORY

1. 2016/04/28
   - Original version：V1.0